Recommendations on Standardisation

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Approvals

Name, Organisation	Role	Validation date
Melanie Hentsche, WP5 leader, ICOS	First approver	20 August 2025
Francis Balestra, Grenoble INP & International Cooperation On Semiconductors - ICOS, France	Final Approver	19 September 2025

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Foreword

Semiconductors are at the strategic core of modern technological advancements, serving as the fundamental building blocks for everything from consumer electronics to complex industrial systems. As we stand on the brink of an era defined by artificial intelligence and hyper-connectivity, the role of standardized frameworks in the semiconductor industry becomes critically important. This landscape analysis focuses on almost 5,000 identified semiconductor standards and technical specifications, which are pivotal to driving the industry's ability to meet global challenges. The following listing only covers the most important technical specifications.

Standards and technical specifications in the semiconductor sector support the industry by ensuring interoperability, increasing reliability, and enhancing security across a wide range of applications. They provide the foundation for innovation while maintaining high-quality benchmarks that are essential for safe and efficient technology deployment. In the context of semiconductors, these standards facilitate international collaboration and trade, allowing for components to be seamlessly integrated into complex global supply chains.

Geopolitically, the semiconductor industry is becoming a focal point for discussions on national security and economic independence. As noted in recent workshops, regions like Europe are emphasizing technological sovereignty, especially in the development and deployment of AI chips to secure their digital futures. The concentration of manufacturing capabilities within a few global entities has created unprecedented vulnerabilities, making standardization a tool not only for innovation but also for geopolitical leverage.

In a world where alliances are continually evolving and new security threats are emerging, having control over semiconductor technologies equates to geopolitical influence. The ability to ensure the trustworthiness of semiconductors — where backdoors are eradicated and security is verifiable — is a matter of strategic importance. For instance, semiconductor standards are integral in European efforts to differentiate themselves by providing guarantees of no hidden vulnerabilities, which is an asset in global markets.

Moreover, semiconductor technologies have become critical in national defence systems, energy infrastructures, and telecommunication networks, elevating their importance in international policy discussions. Countries are increasingly cautious of their dependence on foreign semiconductor technologies, with the potential for these components to end up in adversary military applications posing a serious concern. Initiatives such as the US and EU's efforts to reframe technology diffusion policies illustrate the intersection of semiconductor technology and geopolitics, impacting international relations.

This landscape analysis acknowledges the intricate balance needed to maintain a comprehensive array of standards robust enough to support technological growth while

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addressing compliance complexity. Through collaborations and initiatives like the European Union's focus on automotive digitization and secure platforms, and the G7 forums spotlighting semiconductor trustworthiness, there's a recognition of the vital role standards play in navigating these geopolitical challenges.

In conclusion, the evolution and implementation of semiconductor standards are imperative to confronting the multifaceted global challenges we face. This analysis aims to offer a detailed understanding of these standards' roles and encourages ongoing international cooperation and dialogue to ensure that, as the semiconductor industry evolves, it does so within a framework of mutual trust, security, and ethical responsibility.

Thomas Reibe

Senior Expert at European Commission

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Executive Summary

Semiconductors and chips are essentials to digital innovation, enabling advancements across multiple industries, including mobility, energy, digital industry, health, agrifood, and even beyond through AI or cybersecurity technologies.

On 21 September 2023, the European Chips Act [1] entered into force. The aim was to bolster Europe's competitiveness and resilience in semiconductor technologies and applications, and help achieve both the digital and green transition. In 2022, the European Commission highlighted that global semiconductor shortages forced factory closures in a range of sectors, from cars to healthcare devices [2]. In addition, the findings from the chips survey [3], launched by the European Commission, highlighted that the industry expects demand for chips to double by 2030. These reflect the growing importance of semiconductors for European industry and society and show the extreme global dependency of the semiconductor value chain on a very limited number of actors in a complex geopolitical context.

Within that perspective, standardisation activities in this field are critical to ensuring interoperability, resilience, efficiency, and technological leadership. Therefore, through a proactive and clustered effort carried out by three European Commission funded Coordination and Support Action CSA Projects - Horizon Europe & the Digital Europe Programme ICOS [4], in cooperation with StandICT.eu [5] and ALLPROS.eu [6] launched a technical working group on Semiconductor and Chip Standardisation to draw a landscape of existing standards and analyse any potential gap within those standards in connection with semiconductors and chips.

This report provides an overview of the work done by the Technical Working Group (TWG), performed by analysing almost 5,000 global standards in connection with semiconductors and chips technology. The table used for this analysis will be published in 6 months from the publication date of this report.

This report is split in two major parts: a landscape overview, and a gap analysis. It is aimed to be circulated widely among experts and Standard Development Organisations (SDOs) to help share the findings and the analysis of the TWG.

The landscape overview lists some of those major standards relevant to semiconductors and chips. It provides some statistics and numbers linked to some segregating factors set by the TWG to define observable and relevant criteria needed for the gap analysis. The gap analysis highlights opportunities for developing new standards, which can lead to the formation of new working groups to support these innovative standards and activities.

When it comes to the development of standards, SDOs have their own processes and own timeline, nevertheless, this report aims at reducing such a timeframe, facilitating convergence

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with the EU policies and providing incentive for collaboration between different SDOs to create more common standards through collaborative development.

In addition, the report aims at being used and studied by the European Commission and different SDOs. This will contribute among other reports to draw a roadmap for future investments and future standards that will contribute to the European Union economy and foster strategic autonomy, paving the way for stronger partnerships with global stakeholders.

Ryoichi Ishihara, Lead Chair, ICOS member
Salahuddin Nur, Co-Chair, ICOS member
Abhishek Ramanujan, Co-Chair, IEC TC 47/SC47A/WG9 convenor
Karim Tobich, Co-Chair, ISO/IEC JTC1 SC27 & ISO/IEC JTC1 SC41 member.

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Josef Preishuber-Pflügl	Innobir e.u., **Austria**
Thomas Reibe	European Commission, **Belgium**
XiaoRui Zhang	ADAPT Centre - School of Computing, Dublin City University, **Ireland**
Sharon Farrell	ADAPT Centre - School of Computing, Dublin City University, **Ireland**
Harshvardhan Pandit	ADAPT Centre - School of Computing, Dublin City University, **Ireland**
Bárbara Iryde	ADAPT Centre - School of Computing, Dublin City University, **Ireland**
Silvana MacMahon	ADAPT Centre - School of Computing, Dublin City University, **Ireland**
Abhishek Ramanujan	Analog devices, **Ireland**
Gianluca Milano	Istituto Nazionale di Ricerca Metrologica - INRIM, **Italy**
Silvana Muscella	Trust-iT Services, **Italy**
Teresa Ridolfi	Trust-iT Services, **Italy**
Maria Giuffrida	Trust-iT Services, **Italy**
Luigi Colucci	Trust-iT Services, **Italy**

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Patrick Cogez	Aeneas, **France**
Vincent Le Meau	Aeneas, **France**
Thierry Poiroux	Commissariat à l'énergie atomique et aux énergies alternatives - CEA, **France**
Francis Balestra	Grenoble INP & International Cooperation On Semiconductors - ICOS, **France**
Mathilde Berric	International Cooperation On Semiconductors - ICOS, **France**
Ryoichi Ishihara	Department of Quantum & Computing Engineering, Delft University of Technology, **Netherlands**
Salahuddin Nur	Department of Quantum & Computing Engineering, Delft University of Technology, **Netherlands**
Asbjorn Hovsto	Hafenstrom, AS, **Norway**
Amir Sohail Khan	Ajou University, **South Korea**
Iñigo Artundo	VLC photonics - Hitachi Group Company, **Spain**
Karim Tobich	Cybersecurity and technology consultancy, **UK**
Richard Pitwon	Resolute Photonics, **UK**
Pantelitsa Paraskeva Markus	SEMI, **USA**

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1 Landscape of standards

1.1 Methodology

1.1.1 Approach

Semiconductor and chip technologies have been in use for almost a century with constant innovation and evolution. To make sure the landscape analysis is valuable, the technical working group (TWG) identified different standard development organizations (SDOs) and their relevant working groups covering different sectors of applications, and different technologies. This led to the creation of a list, based on the collection of almost 5,000 standards that has been prepared and classified into four main types of categories:

- applications,
- modules, or components,
- process steps, and
- relevance of those standards to the semiconductor and chip technologies.

Finally, from the list of standards and their classifications, a landscape analysis was performed based on statistical and mathematical functions, and a gap was drawn.

1.1.2 SDOs

Table 1 highlights the major SDOs that were considered in the landscape analysis. Each of these SDOs contributes a vital piece to the overall semiconductor standards landscape. International bodies like IEC, ISO, JTC, IEEE provide broad consensus standards and high-level frameworks. Regional and strategic groups like CENELEC, ECS-SRIA ensure alignment with local policies and future needs. Industry-specific SDOs and consortia (SEMI, JEDEC, IPC, Accellera, Si2, SAE, AEC, HSA, etc.) develop detailed technical standards and specifications directly used in manufacturing, design, and qualification of chips. Together, they can address current standardization needs and can collaborate to fill gaps and anticipate challenges. Continued engagement and coordination among these SDOs are essential to foster a robust, interoperable and innovation-friendly semiconductor ecosystem globally.

Table 1 Important Standard development organizations (SDOs)

Standard Development Organization (SDO)	Region/Scope	Focus / Role in Semiconductor Standardization

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IEC – International Electrotechnical Commission	International	Electrotechnical standards (e.g. semiconductor device specifications, testing, safety). Develops global consensus standards (IEC TC 47 - Standardization covers areas from wafer-level reliability to physical environmental testing to device specifications and applications) for chips to ensure interoperability and reliability.
ISO – International Organization for Standardization	International	Broad international standards across industries. In semiconductors: quality management (ISO 9001), environmental/safety (ISO 14001, ISO 26262), and other process-level standards used by chip makers. Also partners with IEC on joint tech standards (e.g. ISO/IEC JTC 1 for IT).
ISO/IEC JTCs – Joint Technical Committees (e.g. JTC 1, JTC 3)	International	Collaborative ISO-IEC committees for emerging tech that impact semiconductors. JTC 1 covers IT (JTC 1's subcommittees have relevance to semiconductors in areas like computer architecture, the Internet of Things (IoT), artificial intelligence, and cybersecurity (all of which depend on semiconductor innovations)), JTC 3 covers quantum technology standards, ensuring unified global standards in new domains (with semiconductor components).
IEEE – Institute of Electrical and Electronics Engineers	USA (global membership)	Global technical professional society and major SDO for electronics/computing. Develops key microelectronics standards: chip design languages (Verilog/VHDL/SystemVerilog), test interfaces (JTAG/1687), semiconductor device measurements, communications interfaces (Ethernet, Wi-Fi) and more. For the semiconductor sector, IEEE standards are deeply influential – often effectively industry norms. Ensures interoperability and common EDA/tool methodologies worldwide.
CENELEC – European Committee for Electrotechnical Standardization	Europe (EU)	Regional (EU) standards body for electrotechnical fields. Adopts IEC semiconductor standards as European Norms and creates EU-specific standards when needed (e.g. **TC 47X for "Semiconductor devices & trusted chips"** to support EU initiatives). Aligns chip

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		standards with European regulatory and market needs (e.g. cybersecurity requirements, **EU Chips Act**).
ECS-SRIA – Electronic Components & Systems Strategic R&I Agenda	Europe (EU)	European industry roadmap (not a formal SDO) highlighting R&D priorities and standardization needs in semiconductors and electronic systems. Emphasizes **standardization & interoperability** as key enablers for emerging tech (AI chips, 6G, quantum, etc.). Guides EU policy and SDOs on addressing **standards gaps** for the European semiconductor ecosystem.
SEMI – Semiconductor Equipment and Materials International	USA (global programs)	Global industry association setting **semiconductor manufacturing standards**. Focus on equipment, materials, process and safety standards in chip fabs (wafer sizes, equipment interfaces like SEMI E-series, material specs, EHS guidelines). Its voluntary consensus standards enable interoperability of tools and materials, reducing cost and complexity in global chip production.
JEDEC – Joint Electron Device Engineering Council	USA (global membership)	Leading **microelectronics standards** body (ANSI-accredited) for semiconductor components. Focus on memory (DRAM, Flash) standards, packaging and component reliability (e.g. JESD22 stress tests), power electronics (GaN/SiC), and more. JEDEC's open standards (developed by ~300 companies) ensure compatibility and quality of semiconductor devices industry-wide.
IPC – Association Connecting Electronics Industries	USA (global offices)	Industry association standardizing **PCB fabrication and electronic assembly**. Publishes widely used standards for soldering and assembly quality (IPC-A-610), PCB design/fabrication, component packaging and handling. These standards are crucial for integrating semiconductor chips onto boards and in end products, ensuring reliability and uniform assembly processes globally. Additionally, IPC works on materials data exchange standards (for supply chain transparency) and recently has engaged with the US

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		government on strategies for advanced packaging standards
Accellera Systems Initiative	USA (global members)	Industry consortium creating **EDA and design** standards for semiconductors. Developed SystemVerilog, UVM, SystemC, IP-XACT, etc. – languages and frameworks now standardized via IEEE. Facilitates faster adoption of new design/verification methodologies by uniting industry on common specifications, which are later ratified as international (IEEE) standards.
Si2 – Silicon Integration Initiative	USA	Industry coalition improving **IC design flow interoperability**. Provides open standards like **OpenAccess** database for EDA tools, standard cell library formats, and models (via Compact Model Coalition). Focuses on the **semiconductor design ecosystem** – ensuring different tools and IP can work together smoothly. Its standards (often developed with broad industry input) enhance productivity and reduce duplication in chip design.
SAE International (Society of Automotive Engineers)	USA (global)	Develops **automotive and aerospace standards**. In semiconductors, SAE's focus is on **automotive electronics reliability and safety**: e.g. standards for qualification of electronic modules (robustness validation), guidelines to avoid counterfeit parts (such as SAE J1211: Handbook for Robustness Validation of Automotive Electrical/Electronic Modules and and SAE J1879: Robustness Validation of Semiconductor Devices), and co-developing vehicle-specific standards (like **ISO/SAE 21434** for cybersecurity). Ensures chips used in vehicles meet strict performance and quality benchmarks for safety-critical use.
AEC – Automotive Electronics Council	USA	Automotive industry council defining **qualification standards for electronic components**. Unlike SAE (a broad professional society), AEC is specifically focused on standardizing reliability tests for electronic components (especially semiconductors) to ensure

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		they can handle the automotive environment without additional OEM-specific testing. It issues the AEC-Q series: **AEC-Q100 (ICs)**, SAE J1211 **(discrete semiconductors)**, **Q200 (passives)** – widely adopted stress test requirements that certify parts as "automotive-grade". AEC standards harmonize how semiconductor suppliers validate reliability for the harsh automotive environment, accepted globally by automakers.
HSA Foundation (Heterogeneous System Architecture Foundation)	USA (global founders)	Industry-led foundation creating **standards for heterogeneous computing**. Develops the HSA spec – open hardware and software standards that allow CPUs, GPUs, DSPs, etc., on a chip to share memory and tasks efficiently. Targets **semiconductor IP interfaces** for unified memory architecture and parallel computation. Helps semiconductor firms design accelerators and processors that adhere to a common programming model for heterogeneous systems.

1.1.3 Classification based on applications

An application-based classification was prepared, grouping use cases into nine categories: automotive, aerospace and defence, consumer, healthcare, industry, security, data center, edge and cloud computing, and a generic or transversal category that spans multiple sectors. This decision was made to try to identify any correlation between the standards that were developed and their major sector of applications.

Europe's major application domains share a common pattern: they each rely on a small set of **international standards** that guarantee safety, security and interoperability, while a wave of **new initiatives** is updating or supplementing those foundations to cope with sovereignty goals. Table 2, shows some examples of those two elements - baseline standards & SDOs and new initiatives.

Table 2 Classifications based on applications

Application domain	Example of baseline standards & SDOs	New initiatives shaping the roadmap

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Automotive	• ISO 26262 (functional-safety) • AEC-Q100/-Q101 (IC & discrete qualification) • ISO/SAE 21434 (cybersecurity) • UNECE WP.29 R155/R156	• AEC-Q Rev J adds EV/ADAS stress profiles • EU-US TTC work-stream on EV & autonomy standards
Aerospace & Defence	• RTCA DO-254 / EUROCAE ED-80 (airborne HW) • MIL-STD-883 (micro-electronic tests) • ECSS-Q-ST-60 (space EEE parts)	• ESA "European Components Initiative" to qualify EU rad-hard chips • NATO/EDA work on secure micro-electronics supply-chain
Consumer	• IEC 62368-1 (product safety) • IEEE 802.11 / Bluetooth SIG (communications) • EN 303 645 (IoT security baseline)	• Matter smart-home spec (CSA) unifying IoT ecosystems • EU Cyber Resilience Act to mandate baseline IoT security
Healthcare	• IEC 60601-1 (medical electrical safety) • ISO 13485 (QMS) • IEEE 11073 (personal-health data)	• EU digital-identity wallet & eHealth data-space require secure medical devices • IEEE 11073 PHD extensions for new wearables
Industry (Automation / IIoT)	• IEC 61508 (functional safety) • IEC 62443 (industrial cyber-security) • OPC UA + IEEE 802.1 TSN (deterministic Ethernet)	• OPC UA FX unifying field-level comms • Industry 4.0 Asset-Administration-Shell digital-twin spec

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Security (Secure HW / Crypto)	• ISO/IEC 15408 (Common Criteria) • ISO/IEC 19790 & 24759 (crypto modules) • GlobalPlatform SE/TEE, TCG TPM 2.0	• Post-Quantum Crypto transition (NIST PQC, ETSI QSC) • EU eIDAS 2.0 digital-wallet hardware profile
Datacenter / HPC	• JEDEC DDR5 & HBM (JESD235) • PCI-SIG PCIe 5/6 • CXL 3.0 (memory pooling)	• Open Compute Project (OCP) open server & NIC 3.0 specs • UCIe chiplet interconnect consortium
Edge & Cloud	• ETSI MEC (GS MEC series) • ISO/IEC 17788 & 17789 (cloud concepts & architecture) • 3GPP R17 edge enablers	• GAIA-X federated cloud/edge infrastructure • LF Edge / CNCF projects for lightweight edge-K8s
Generic / Transversal	• SEMI M1 / E-series (wafer & equip.) • JEDEC JESD22 (reliability tests) • IPC-J-STD-020 (package moisture sens.) • IEC TC47 (semiconductor devices)	• IRDS chip-technology roadmap • SEMI-UCIe & IEEE P1838 work on chiplet/3-D test

1.1.4 Classification based on module, or component technologies

In the classification of modules, or components, important emerging technologies were specifically identified and categorised to help identify any gap in standardization activities related to those emerging technologies. The following categories of module, or component technologies were made:

1. Sub-5nm
2. Photonics
3. Quantum computing
4. Neuromorphic/ReRAM/AI Chip

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5. AI Applications
6. Edge & Cloud computing – Applications
7. Wide Bandgap
8. Flexible hybrid electronics
9. MEMS
10. Generic/Non-specific

The first nine (9) categories were specifically made to identify such emerging technologies, while the last one includes existing modules, or components and standards that are transversal or generic in use.

It is also important to note that emerging technologies such as advanced lithography, chiplets or advanced packaging, and energy efficiency & sustainability were included in the process steps classification.

The decision to focus on those emerging technologies was made based on different studies and reports like the ECS SRIA 2025 [7] with the aim to assess the level of maturity of such emerging technology through standardization development and to provide SDOs and decision makers with a clearer vision for the need for new standards.

1.1.5 Classification based on process steps technologies

Different steps are required to create a semiconductor component or a chip, those usually start from the raw materials to make the wafer, followed by different front-end processes and different steps of back-end activities to reach a component or a chip that can be used in standalone or integrated into PCB to make more complex devices. The following process steps technologies were made:

1. Materials: This covers materials to make semiconductors eg: silicon, germanium, gallium arsenide, etc
2. Equipment Front-End and services: This covers equipment and services related to wafer fabrication, creation of transistors, capacitors, and other basic circuit elements on a silicon wafer. This involves a series of intricate steps like etching, deposition, and doping to create the desired circuit patterns on the wafer. Front-end equipment includes lithography machines, etching tools, and deposition systems. Also, different subcategories were defined in an attempt to provide a better granularity to the analysis:

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(1) Energy efficiency & sustainability: aiming at reducing energy usage during chip manufacturing, using environmentally friendly chemicals, recycling chips and design for sustainability

(2) Advanced Lithography

3. Equipment Back-End and services: This covers equipment and services used in Assembly, packaging, and testing of the integrated circuits (ICs) after they are fabricated on the wafer. This includes dicing the wafer into individual chips, bonding the chips to a substrate, and then packaging them with pins or leads for connection to other components. Back-end equipment includes die-saws, bonding machines, and packaging equipment. Additionally, different subcategories were defined in an attempt to provide better granularity:

   (1) Energy efficiency & sustainability: aiming at reducing energy usage during chip manufacturing, using environmentally friendly chemicals, recycling chips and design for sustainability

   (2) Chiplets or advanced packaging

4. IC Design EDA tools and services: This covers electronic design automation (EDA) tools, VHDL, Verilog, etc

5. IC Design Blocks: This category is specific for IC design blocks: RAM, EEPROM, FLASH, LOGIC. This can be based on multiple dies, or single die with single functionality.

6. IC Design Whole IC: This covers the whole IC, one or more die(s) in the same package, with multiple functionalities. Additionally, different subcategories were defined in an attempt to provide a better granularity to the analysis:

   (1) IC Design Whole IC - Chiplets or advanced packaging (from architecture perspective)

   (2) IC Design Whole IC - Energy efficiency & sustainability: aiming at reducing energy during chip manufacturing, environmentally friendly chemicals, recycling chips and design for sustainability

7. Front-End Fabrication: This covers wafer fabrication, creating the transistors, capacitors, and other basic circuit elements on a silicon wafer. This involves a series of intricate steps like etching, deposition, and doping to create the desired circuit patterns on the wafer. Front-end equipment includes lithography machines, etching tools, and deposition systems. Also, different subcategories were defined in an attempt to provide a better granularity to the analysis:

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(1) Energy efficiency & sustainability: aiming at reducing energy usage during chip manufacturing, using environmentally friendly chemicals, recycling chips and design for sustainability

8. Back-End Fabrication: This covers Assembly, packaging, and testing of the integrated circuits (ICs) after they are fabricated on the wafer. This includes dicing the wafer into individual chips, bonding the chips to a substrate, and then packaging them with pins or leads for connection to other components. Back-end equipment includes die-saws, bonding machines, and packaging equipment. Also, different subcategories were defined in an attempt to provide a better granularity to the analysis:

   (1) Energy efficiency & sustainability: aiming at reducing energy usage during chip manufacturing, using environmentally friendly chemicals, recycling chips and design for sustainability

   (2) Chiplets or advanced packaging

The decision to focus on those process steps aligns with the established stakeholders involved in making semiconductors and chips as all those steps are not always performed by one large organization but also involve different SMEs. The aim through this classification was to provide readers from each of those types of stakeholders and SMEs a window through which they can relate to this report and join different SDOs based on their interests.

1.1.6 Classification based on relevance to the semiconductor and emerging chip technologies

Some standards are indirectly linked to semiconductor and chip technologies, for example ISO 9001 quality management system is a management system standard usually used to improve the organization processes and to reach better yield and better quality. However, these standards neither focus on the technology used nor define such technological requirements. Similarly, ISO/IEC 18033-1:2021 Information security - Encryption algorithms - Part 1: General, introduces the nature of encryption and describes certain general aspects of its use and properties. Despite being used in semiconductors and chips for the design of passports, banking, and telecoms chips, those algorithms are technologically agnostic. Therefore, such standards were classified differently compared to those highly used in semiconductor and chip designs. Similarly, some standards like those linked to photovoltaics were intentionally excluded from our analysis as they constitute a wide domain on their own.

This led to the creation of a five-tier classification based on the relevance of the standard to the scope of this project.

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1. Very High relevance: This covers standards and specifications developed by chip and semiconductor committees directly used in manufacturing, design, and qualification of semiconductors and chips.

2. High relevance: This covers standards and specifications developed by chip and semiconductor committees indirectly used in manufacturing, design, and qualification of semiconductor chips.

3. Medium relevance: This covers standards and specifications developed by other committees which are technology agnostic like security encryption and algorithms used in semiconductors and chips. This also covers standards that are used in manufacturing, design, and qualification of PCBs and devices that rely directly on semiconductors and chips.

4. Low relevance: This covers standards that are withdrawn or inactive. It also covers passive components resistors, capacitors, inductors, etc, and it also covers the transversal standards defining system of systems which are technology agnostic.

5. Very Low relevance: This covers organizational standards that could be applied to semiconductors industry and factories (information security management system, quality management system, medical devices, etc). This also covers standards and specifications that have been excluded as they constitute a wide domain on their own like photovoltaics.

1.2 Example of standards

This section provides an extraction of some of the standards analysed during this project. It represents approximately 0.1% of the total number of standards analysed and is used for illustrative purposes. The selected standards are all classified as very highly relevant to the scope of this project. Therefore, the Classification based on relevance to the semiconductor and chip technologies is omitted.

Organisation: Accellera system initiative

Doc Reference: Verilog-AMS

Title: Verilog-AMS (Analog Mixed-Signal

Abstract: This Verilog-AMS Hardware Description Language (HDL language reference manual defines a behavioral language for analog and mixed-signal systems. Verilog-AMS HDL is derived

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from IEEE Std 1364-2005. Verilog HDL (referred to as IEEE Std 1364 Verilog from this point forward. This document is intended to cover the definition and semantics of Verilog-AMS HDL as proposed by Accellera.

Document Type: Standard_Specification

URL: https://www.accellera.org/downloads/standards/v-ams

Published: Yes

Date of Publication: 2024-02-01

Category of applications: Generic or transversal

Category of module of component: Non-specific

Category of process steps: IC Design EDA tools and services

Organisation: IEEE Nanotechnology Council

Doc Reference: IEEE 62659-2015

Title: IEC/IEEE International Standard - Nanomanufacturing -- Large scale manufacturing for nanoelectronics

Abstract: This International Standard provides a framework for introducing nanoelectronics into large scale, high volume production in semiconductor manufacturing facilities through the incorporation of nanomaterials (e.g. carbon nanotubes, graphene, quantum dots, etc.). Since semiconductor manufacturing facilities need to incorporate practices that maintain high yields, there are very strict requirements for how manufacturing is performed. Nanomaterials represent a potential contaminant in semiconductor manufacturing facilities and need to be introduced in a structured and methodical way. This International Standard provides steps employed to facilitate the introduction of nanomaterials into the semiconductor manufacturing facilities. This sequence is described below under the areas of raw materials acquisition, materials processing, design, IC fabrication, testing, and end-use. These activities represent the major stages of the supply chain in semiconductor manufacturing facilities.

Document Type: Standard_Specification

URL: https://standards.ieee.org/ieee/62659/6049/

Published: Yes

Date of Publication: 2015-09-30

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Category of applications: Generic or transversal

Category of module of component: Sub-5nm

Category of process steps: Materials (Materials to make semiconductors eg: silicon, germanium, gallium arsenide, etc)

Organisation: IEC TC 113 Nanotechnology for electrotechnical products and systems

Doc Reference: ISO TS 23302:2021

Title: Nanotechnologies - Requirements and recommendations for the identification of measurands that characterise nano-objects and materials that contain them

Abstract: ISO TS 23302:2021 This document specifies requirements and recommendations for the identification of measurands to characterize nano-objects and their agglomerates and aggregates, and to assess specific properties relevant to the performance of materials that contain them. It provides recommendations for relevant measurement.

Document Type: Standard_Specification

URL: https://webstore.iec.ch/en/publication/62257

Published: Yes

Date of Publication: 2021-11-30

Category of applications: Generic or transversal

Category of module of component: Sub-5nm

Category of process steps: Front-End Fabrication

Organisation: IEC TC 113 Nanotechnology for electrotechnical products and systems

Doc Reference: ISO TS 80004-12:2016

Title: Nanotechnologies - Vocabulary - Part 12: Quantum phenomena in nanotechnology

Abstract: ISO/TS 80004-12:2016 lists terms and definitions relevant to quantum phenomena in nanotechnologies.

All of these terms are important for nanotechnologies, but it is to be noted that many of them are not exclusively relevant to the nanoscale and can also be used to some extent to refer to

This project has received funding (2023 – 2025) from the European Union's Horizon Europe research and innovation programme under GA No 101092562.

larger scales. The list of terms presented does not claim to provide exhaustive coverage of the whole spectrum of quantum concepts and phenomena in nanotechnology. It covers important phenomena as acknowledged by many stakeholders from academia, industry, etc. ISO/TS 80004-12:2016 is intended to facilitate communication between organisations and individuals in industry and those who interact with them.

Document Type: Standard_Specification

URL: https://webstore.iec.ch/en/publication/34404

Published: Yes

Date of Publication: 2016-03-17

Category of applications: Generic or transversal

Category of module of component: Quantum computing

Category of process steps: Materials (Materials to make semiconductors eg: silicon, germanium, gallium arsenide, etc)

Organisation: IEC TC 47 Semiconductor devices

Doc Reference: IEC 63550-1 ED1

Title: Semiconductor devices - Neuromorphic devices - Part 1: Evaluation method of basic characteristics in memristor devices

Abstract: Not available

Document Type: Standard_Specification

URL:
https://www.iec.ch/dyn/www/f?p=103:38:213007726067219::::FSP_ORG_ID,FSP_APEX_PAGE,FSP_PROJECT_ID:1251,23,119252

Published: No

Date of Publication: 2026-06

Category of applications: Generic or transversal

Category of module of component: Neuromorphic/ReRAM (memristor device for non von Neumann device and computing architecture / architecture)

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Category of process steps: Equipment Back-End and services

2 Gap analysis

2.1 Analysis

2.1.1 Analysis based on applications

A set of application-based categories has been established, revealing several key findings. Figure 1 shows that applications related to Generic/Transversal and Security categories are well covered. In contrast, coverage is limited for Automotive, Aerospace & Defence, Consumer, Healthcare, and Industry sectors, and almost none existent for Data Center, or Edge & cloud applications. This also reflects the way semiconductor components are currently used; in a transversal manner where a microcontroller can be used in a car, a plane, or a laptop. This may change as the industry is shifting into more specialised components that may contain neural processing units (NPUs), for dedicated applications.

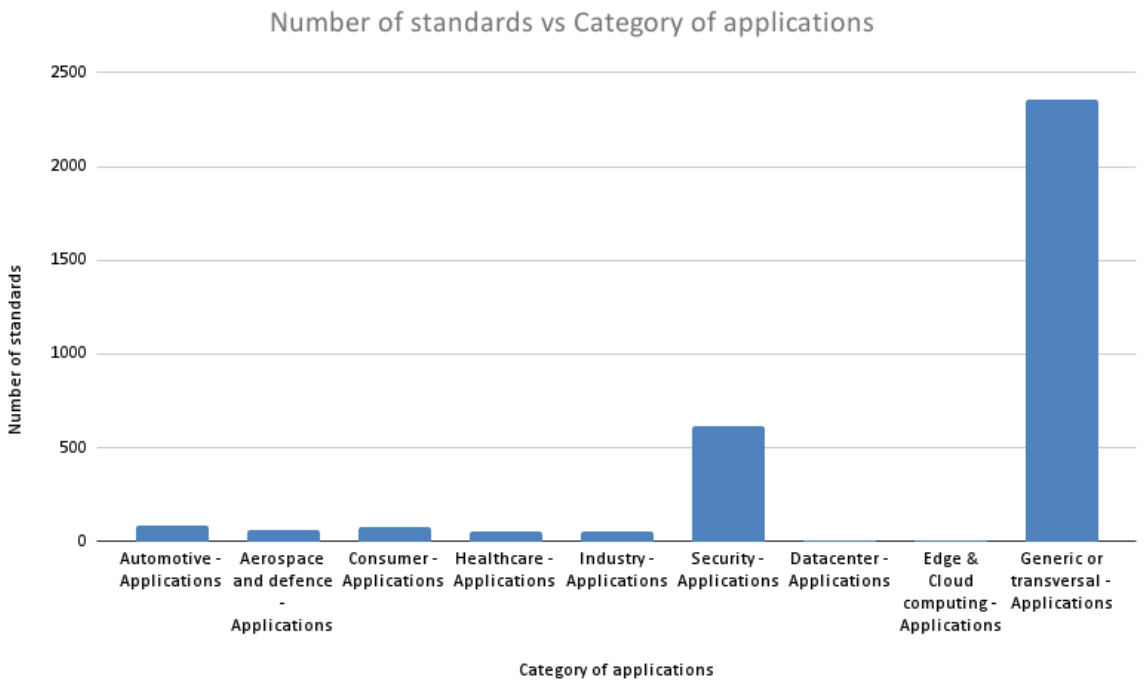

Figure 1: standardizations vs applications – with Generic or transversal applications

Figure 2 provides a zoomed picture by excluding the generic and transversal applications and highlights current trends with regard to the other applications.

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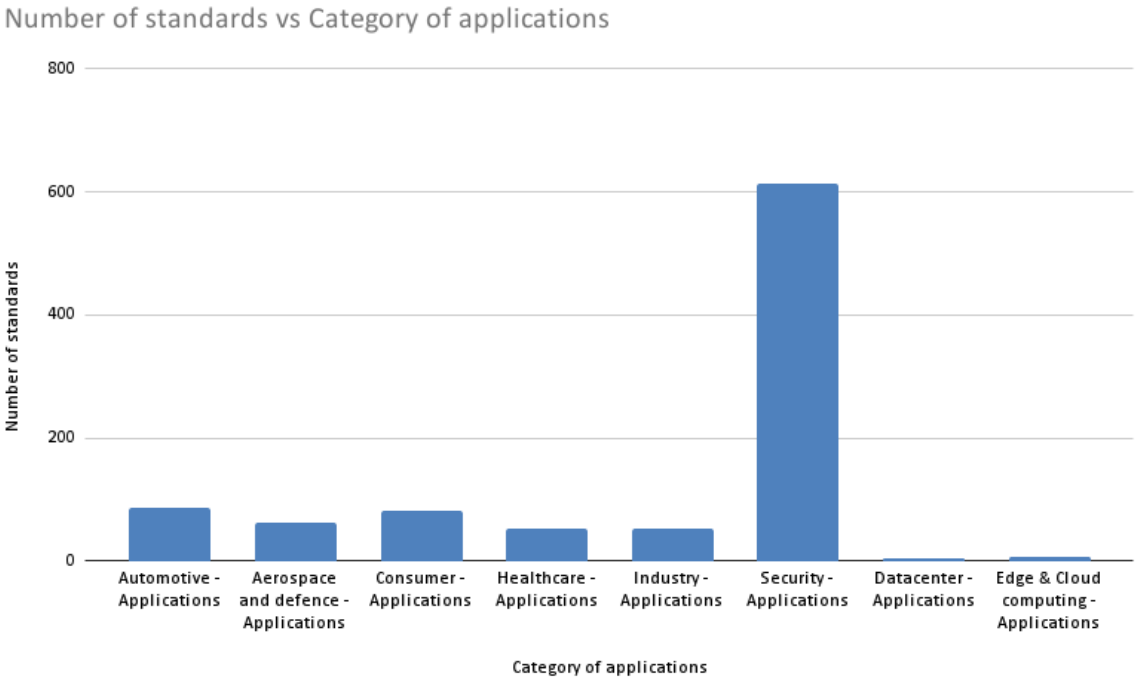

Figure 2: standardizations vs applications – without Generic or transversal applications

2.1.2 Analysis based on module, or component technologies

A classification based on modules or components has been prepared, leading to the following observations. Figure 3 shows that the coverage is found to be low for photonics, AI, wide-bandgap, flexible-hybrid electronics, and MEMS devices. However, as shown in Figure 4, there is a notable lack of coverage for emerging devices such as sub-5nm, quantum, and neuromorphic technologies. Moreover, the classification shows that the different standards fall under the non-specific category. This was expected as most SDOs do use different classifications, and the technical working group selected categories that are related to new emerging technologies and help highlight any gap in standardisation activities.

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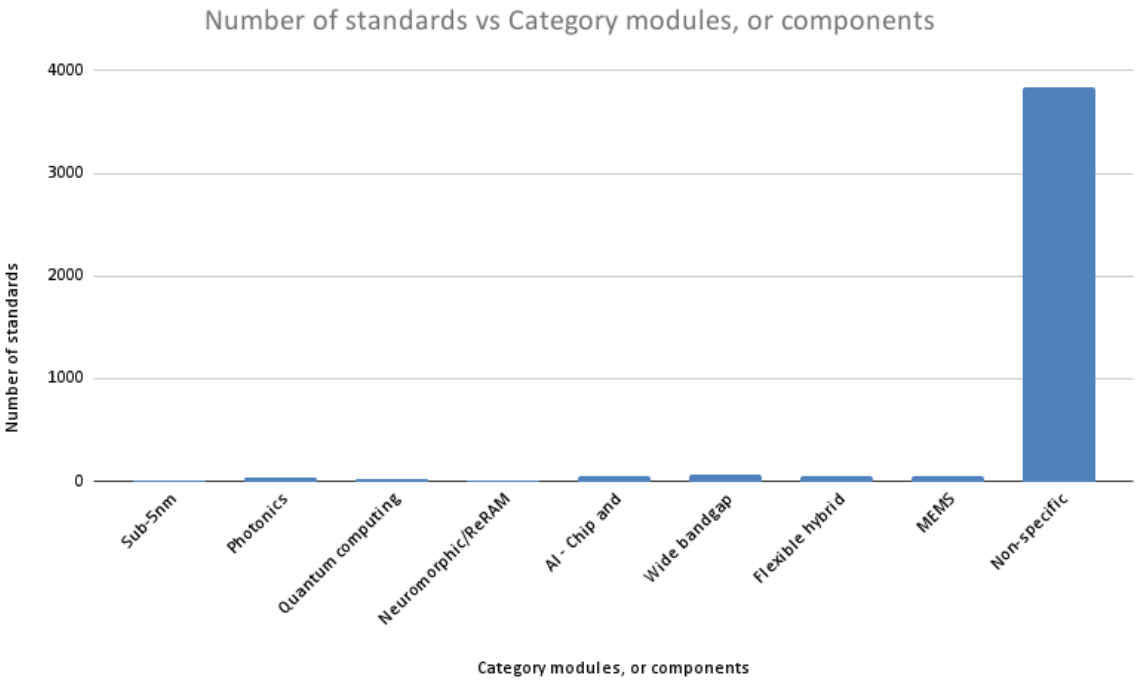

Figure 3: standardizations vs components with non-specific components

Figure 4: standardizations vs modules, or components shows the numbers of standards based on the emerging technologies and by excluding old technologies or non-specific modules or components. We can easily observe that the number of standards related to sub-5nm is still behind other emerging technologies. This can be explained by a need for a heavy investment to develop such technology.

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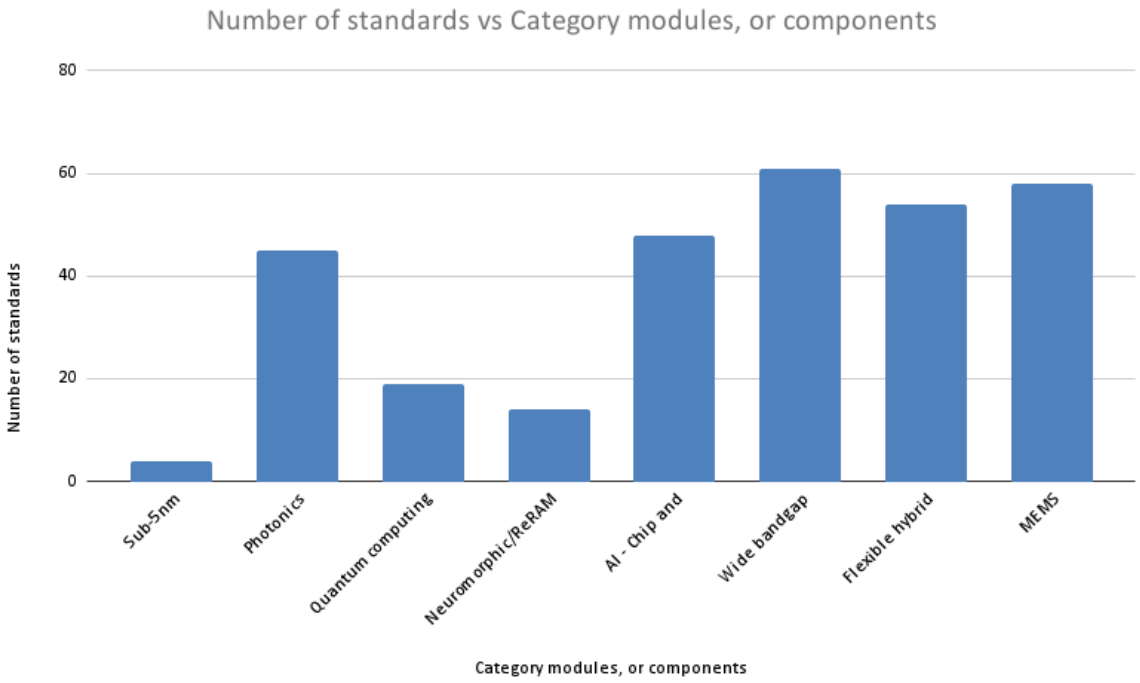

Figure 4: standardizations vs modules, or components

2.1.3 Analysis based on process steps technologies

A classification of standards according to semiconductor process steps was performed, leading to the following observations related to Figure 5. Process steps related to front-end and back-end fabrication are well covered, while coverage for front-end and back-end equipment is somewhat limited. Additionally, distinguishing clearly between equipment and fabrication categories proved challenging. Very few classifications were identified so far for IC design tools and the overall IC design process.

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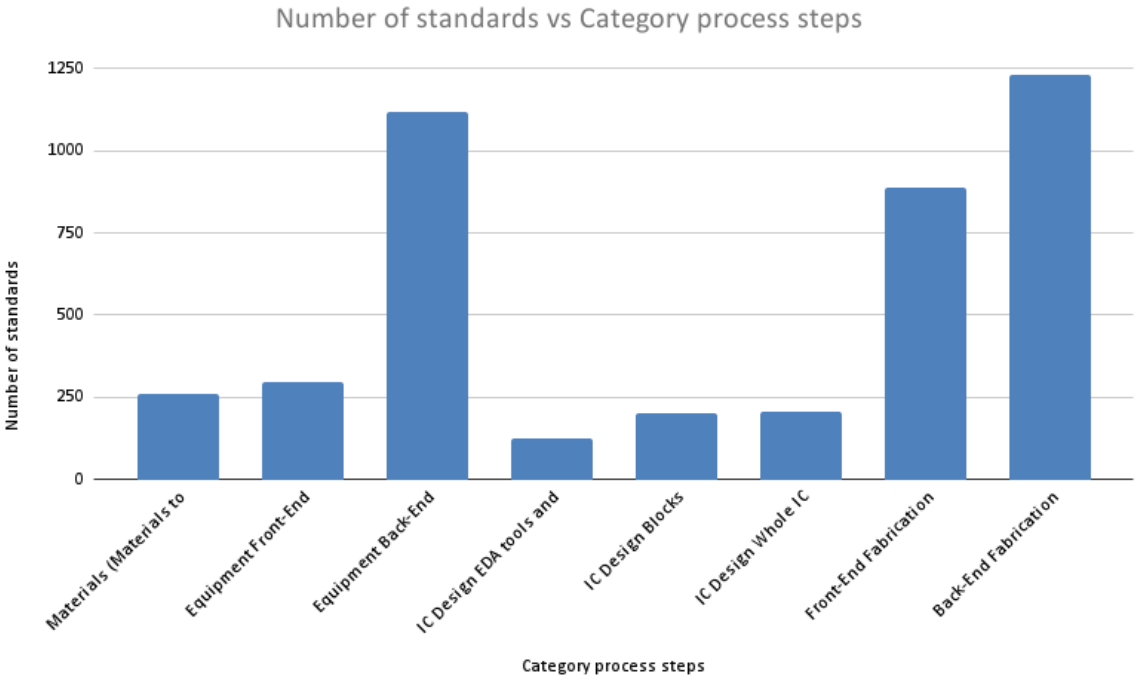

Figure 5: standardizations vs process steps

Figure 6 shows the classifications based on process steps activities related to emerging technologies. The compiled classification of standards by semiconductor process steps and the analysis show that there is a very limited number of standards addressing energy efficiency and sustainability, advanced lithography, and chiplet/advanced packaging. Additionally, certain standardization activities remain obscured within generic process steps, which need clearer differentiation and also indicate potential areas for further investigation and development - all of which highlights a potentially significant gap.

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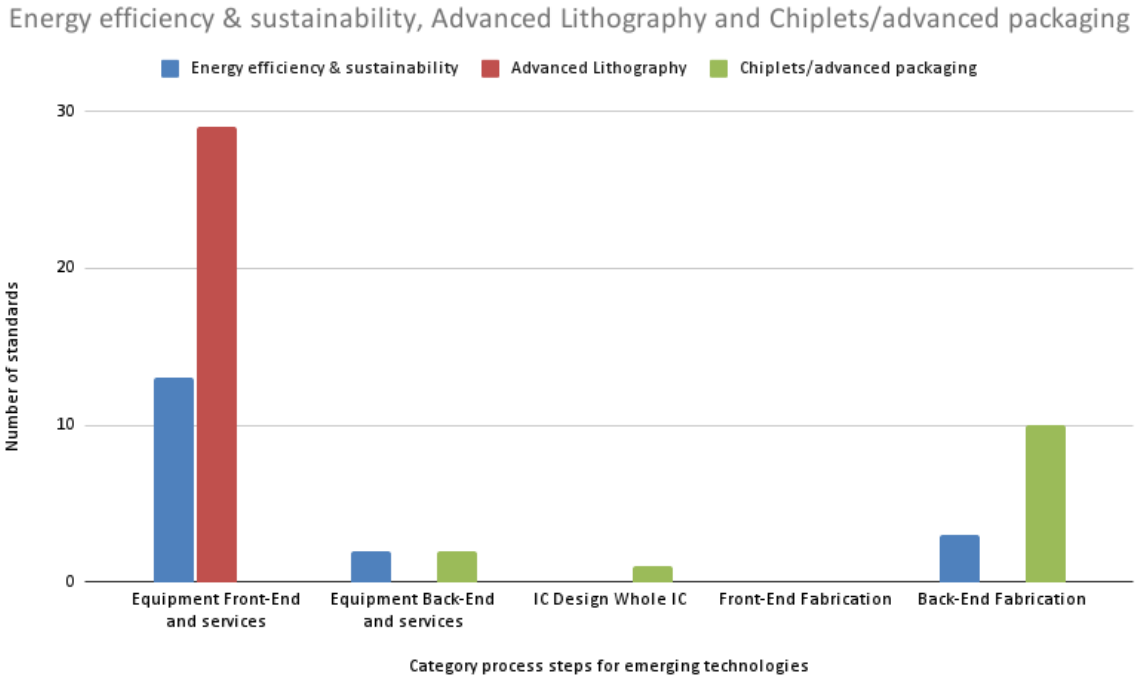

Figure 6: Standardizations vs process steps for emerging technologies

2.1.4 Analysis based on relevance to the semiconductor and chip technologies

A classification of standards according to their relevance to the semiconductor and chip technologies was drawn in Figure 7: Number on standards vs relevance, leading to the following observations. From approximately 5,000 standards analysed, a high number of standards were classified as “low relevant”, followed by a fair number of standards classified as “high relevant” or “very low relevant”. Those classified as “very high relevance” are behind the other categories. This was expected as the “low relevance” category covers standards that are withdrawn or inactive. It also covers passive components resistors, capacitors, inductors, etc, and it also covers the transversal standards defining system of systems, which are technology agnostic. Likewise, the “very low relevance” standards cover organizational standards that could be applied to the semiconductor industry and factories (information security management system, quality management system, medical devices, etc). This also covers standards and specifications that have been excluded, as they constitute a wide domain on their own, like photovoltaics.

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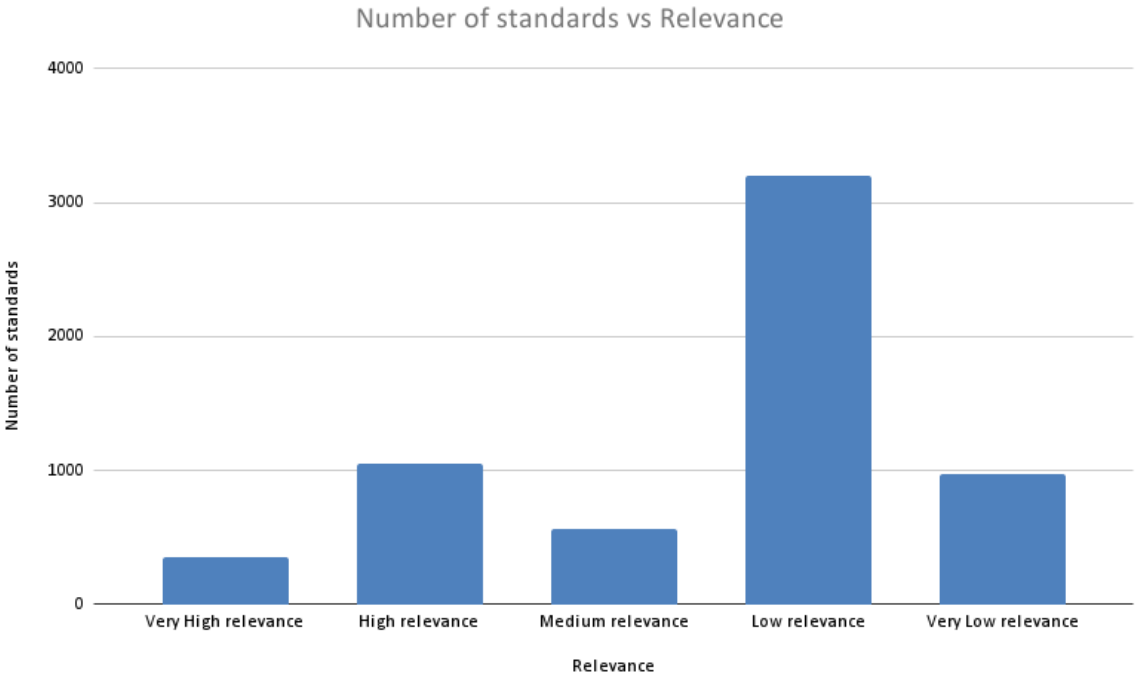

Figure 7: Number on standards vs relevance

Figure 8 shows the Number of standards, Very high relevance, High relevance and Medium relevance per SDO's committee. This shows that the IEEE Power and Energy Society has the highest number of standards but it has one of the lowest relevance among the other SDOs. To provide a better understanding of the landscape, standards from the same SDO were regrouped in Figure 9. This result shows that despite IEEE having the highest number of standards, their relevance to our study was low. Similarly, the IEC number of standards was almost 10 times the number of very high relevant standards.

In Figure 10, the number of standards was excluded to provide a better understanding and better visualisation of the relevancy. We can observe that IEC standards have very high relevant standards to our study, followed by the CENELC TC47x. While SEMI has high relevant standards, JTC 1 has medium relevant standards.

Obviously, these observations are related to our study and our criteria and different criteria may have led to different results and different interpretations.

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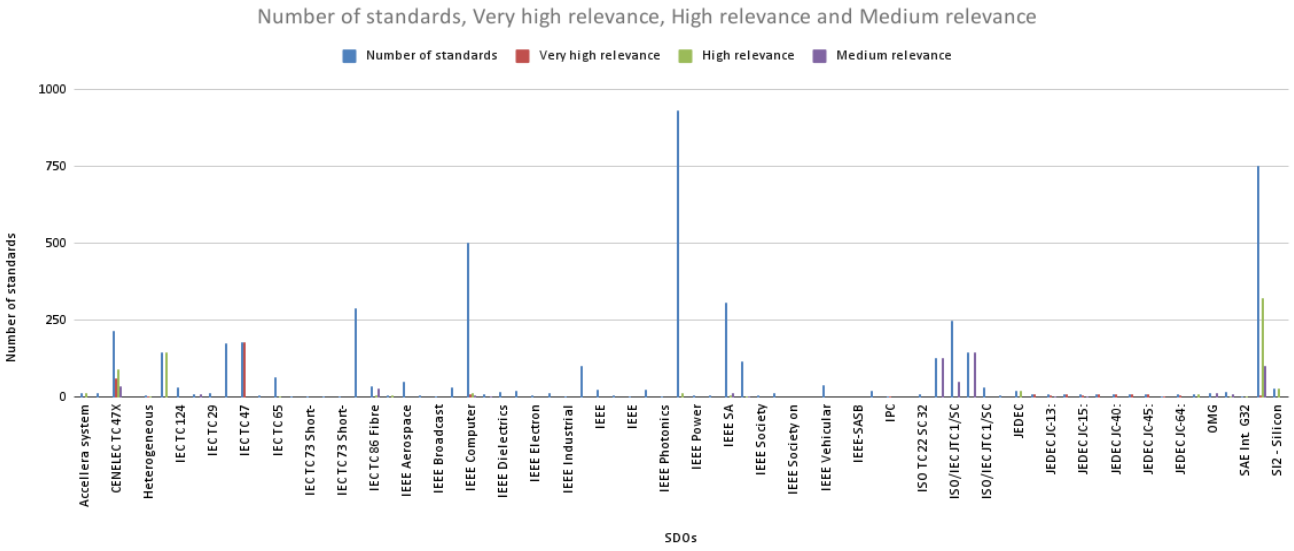

Figure 8: Number of standards, and level of relevance per SDO's committee

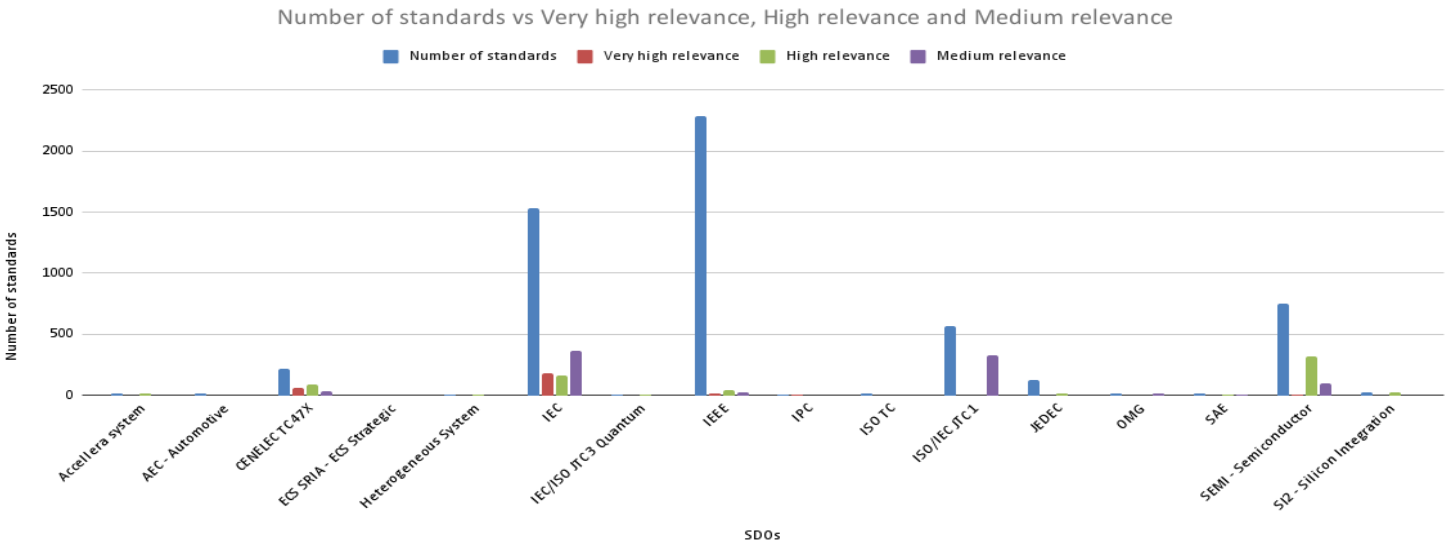

Figure 9: Number of standards, and level of relevance per SDOs

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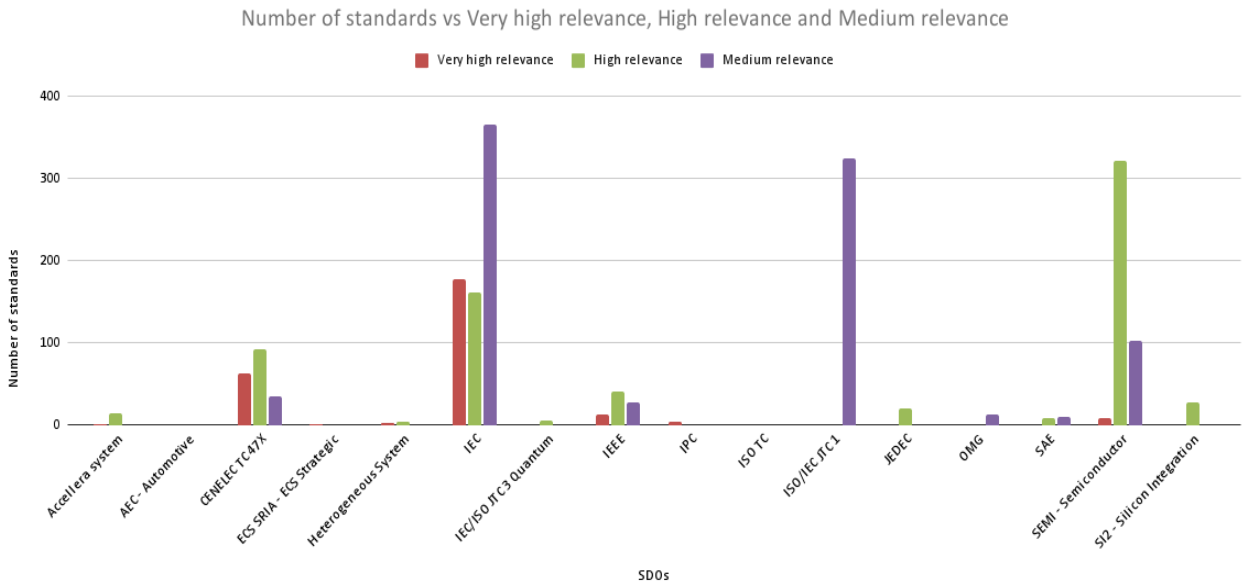

Figure 10: Level of relevance per SDOs

2.2 Gaps

The analysis from the previous section shows different gaps based on the publicly available information on those SDOs websites. Those gaps are consolidated in this section by providing additional resources related to those topics and also recommendations to the European Union as a whole including its institutions, industries and citizens to develop a sustainable semiconductor future.

2.2.1 Datacenter, Edge & Cloud Computing applications

- Gaps: There is no global consensus yet on design rules, interface pin-outs, or test methods for semiconductors and chips used in datacenters, edge, and cloud computing. So far, organisations are relying on the use of multiple chips and multiple systems through multithreading and load balancing techniques to achieve heavy and consuming processing tasks. This is not optimised from energy efficiency and sustainability. Moreover, it does not allow for easy scalability without increasing the number of lands, buildings, and structures to host those expansions.
- Additional resources:

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https://csa.catapult.org.uk/wp-content/uploads/2025/02/Data-centre-report-Feb-2025-final-version.pdf

https://www.weforum.org/stories/2023/11/data-centres-power-semiconductor-technologies-decarbonization/

- **Recommendations for EU:** The EU should help create initiatives to make chips with multicores dedicated to datacenters, edge and cloud computing infrastructures. Such chips would be able to reduce energy consumption and provide better scalability without the need to invest in new datacenters and new locations. Such initiative should be combined with the use of new materials that help increase efficiency and power density like Gallium nitride (GaN) and others.

2.2.2 Sub-5nm Semiconductor Technologies

- **Gaps:** No global consensus on design rules, interface pin-outs, or test methods for beyond-5nm chips. In particular, chiplet and heterogeneous packaging lack uniform bus/interface standards; advanced test metrics (e.g. for quantum effects) are under-defined. Yield and reliability tests for new transistor structures (e.g. gate-all-around) are not fully standardized.

- **Additional resources:**

  https://irds.ieee.org/images/files/pdf/2023/2023IRDS_MET.pdf

  Nearly Invisible: Defect Detection Below 5nm

  CMOS Scaling for the 5 nm Node and Beyond: Device, Process and Technology

  5nm Design Progress

  Development Flows For Chiplets

- **Recommendations for EU:** Support participation of EU experts in SEMI, IEEE/IEC nanoelectronics groups, and JEDEC memory committees to push for open standards. Integrate standardization into Chips Act projects (require pilot lines to publish interface and test specifications). Fund joint metrology and reference-chip initiatives to develop standardized characterization methods for sub-5nm devices. Convene EU-IEEE/IEC working groups to define multi-die packaging standards (building on SEMI and UCIe efforts). Ensure EU fab pilots adopt international frameworks (e.g. ISO/IEC P62659) to “pull” standard adoption and close gaps between research and industry.

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2.2.3 Quantum Computing

- **Gaps:** There are virtually no de-facto interconnect or bus standards for quantum processors. No common API or data formats across platforms. Benchmarking (quantum volume, etc.) is proprietary. Terminology, trustworthiness and certification frameworks are in progress (e.g. by ETSI ISG, not yet finalized).

- **Additional resources:**

  Quantum Technologies (RP2024) | Interoperable Europe Portal

  IEEE SA - IEEE Standards & Projects for Quantum Technologies

  Quantum Technologies - CEN-CENELEC

- **Recommendations for EU:** Align Chips Act and Quantum Flagship programs to fund EU representation in ISO/IEC JTC 3 and IEEE quantum committees. Establish an EU Quantum Standardization Roadmap (building on CEN-CENELEC focus group on Quantum Technology (FGQT)) with concrete milestones. Create liaison channels between EU HPC (EuroHPC) and quantum labs to push for interoperable interfaces (e.g. adopt IEEE P3185 for quantum-classical binding). Support development of European quantum simulators as reference platforms for testing and benchmarking standards. Promote early EU standards (vocabularies, protocols) to set effective/de-facto rules (e.g. EU standard for quantum-safe key exchange, European pilot certification labs for quantum devices).

2.2.4 Neuromorphic/ReRAM/AI Chips

- **Gaps:** No common metrics for neuromorphic performance (e.g. synaptic event rate, power per spike). No agreed modeling language for spiking networks (beyond proprietary frameworks). Memory standards do not yet cover ReRAM cell endurance and variability.

- **Additional resources:**

  Inspired by biological neurons – New VDE SPEC on neuromorphic computing

  The road to commercial success for neuromorphic technologies | Nature Communications

  (5) Neuromorphic Computing: The Next Frontier in Brain-Inspired AI, Scalable Architectures, and Intelligent Systems | LinkedIn

  2022 roadmap on neuromorphic computing and engineering

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- **Recommendations for EU:** Support the VDE and CEN/CLC to evolve neuromorphic SPECs into European standards, say, in partnership with IEEE. Encourage IEEE to launch formal projects (e.g. “P neuron spike interface standard”). Tie EU R&D funding (Chips for Europe) to standardization outcomes: mandate that public neuromorphic testbeds publish interface and test specs. Facilitate liaison between IEC/TC 47 (for device qualification) and neuromorphic chip developers. On ReRAM, push JEDEC/SEMI to create specific committees for memristive memory definitions, leveraging EU expertise from Material Science institutes.

2.2.5 IC design

- **Gaps:** Europe’s chip designers still rely on expensive, proprietary U.S. software tools and foundry files. There is no truly open, EU-controlled design toolkit or shared process kit. Reusable IP blocks and new chiplets follow different, often proprietary, formats, so parts from different vendors do not “click together” easily. Furthermore, when designers use pre-made "building blocks" (IP cores) from different suppliers, there's no standard quality or security label, which creates risk and slows down integration. At the whole-chip level, Europe also lacks common rules for testing, power, security and eco-metrics when many chiplets are stacked into one package. This is inefficient because it's difficult to reuse the tests from the smaller building blocks at the full system level.

- **Additional resources:**

  IC Equipment Communication Standards Struggle As Data Volumes Grow

  Chips Act | Updates, Compliance, Training

  European Chips Act - European Commission

  Chiplets Still A Challenge With UCIe 2.0

  Chiplet IP Standards Are Just The Beginning

  Chips Act

  European Chips Act: The Chips for Europe Initiative | Shaping Europe’s digital future

  European Chiplet Innovation: APECS Pilot Line starts Operation in the Framework of the EU Chips Act

  Closing The Test And Metrology Gap In 3D-IC Packages

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Design Meets EDA: Gaps And Countermeasures In Analog/Mixed-Signal IC Design

Setting Ground Rules For 3D-IC Designs

- **Recommendation:** The EU should help create a common and open "rulebook" for chip design. This means actively funding projects that use and develop open standards, so tools and design parts from different companies can work together smoothly. Speed up the Chips-Act design cloud and ensure it includes free, open-source EDA tools plus at least one open PDK per node. Ask all EU-funded projects to package IP in standard, public formats (IP-XACT, UCIe, etc.). The EU should fund training and projects that use the latest, most efficient testing methods to ensure chip designs are correct before they are manufactured, saving time and money; and support European labs that test and certify chiplets and IP for security and interoperability. Give SMEs easy, low-cost access to the design cloud, pilot fabs and training, and place EU experts in global bodies (IEEE, JEDEC, UCIe, RISC-V) so Europe helps write the next wave of chip standards.

2.2.6 Energy efficiency and sustainability

- **Gaps:** Standards related to energy efficiency and sustainability are not well developed and are not spread among the process steps to make semiconductors or chips. Ecological friendly processes should be encouraged to be integrated within all the steps and not limited to equipment front-end and services. Some initiatives, like standards for concrete, similar to BS EN 206 and BS 8500-2, address the use of recycled aggregates. However, such initiatives are limited and should be expanded.
- **Additional resources:**

  https://knowledge.bsigroup.com/products/concrete-complementary-british-standard-to-bs-en-206-specification-for-constituent-materials-and-concrete-1

- **Recommendation:** The EU should help create a common and open rule to recycle semiconductors and chips in Europe.

2.2.7 Standards development and content harmonisation

- **Gaps:** Through our analysis we noticed a gap in the way SDOs are developing their standards. This is also the case for committees within the same SDOs. For example, some SDOs are providing only high-level abstract descriptions of their standards while

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others are providing scopes and in some cases both. Similarly, some SDOs are providing keywords helping to link such standards with other topics, while others SDOs don't. In addition, some standards are mixing requirements and guidance without a clear language distinguisher. Such discrepancies make any data analysis lengthy and limit the scope and forecast for future standards development.

- Additional resources:

  https://www.iso.org/files/live/sites/isoorg/files/developing_standards/docs/en/how-to-write-standards.pdf

  https://www.etsi.org/images/files/Brochures/AGuideToWritingWorldClassStandards.pdf

  https://www.iso.org/sites/directives/current/part2/index.xhtml

- Recommendation: The EU and mainly SDOs should help create a common and open rule to harmonise standard development and mainly harmonise the contents through the identification of predefined fields that can be common to all SDOs. For example, providing information about the primary sectors or applications that will be directly impacted by such a standard and the sectors or applications that might be related to such a standard will be helpful to the standards' buyers. Similarly, some keywords or acronyms can be used to help readers to identify straightaway the type and importance of a standard based on their needs. The following list is not exhaustive and is provided for illustrative purpose, so standards developers can select one or multiple keywords:

- DEF (Terms and Definition)
- ARC (Reference Architecture)
- USC (Use Cases)
- TAX (Taxonomy & Ontology)
- PER (Performance)
- USB (Usability)
- IOB (Interoperability)
- SAF (Safety)
- SEC (Security and Privacy)
- REG (Regulation, Requirement and Policy)

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- GID (Guidance, Guideline)

3 Horizon for SDOs

3.1 Standardisation of Research and Development

Developing new standards is an exciting opportunity that brings together the efforts and support of various experts and organisations. For example, standardization activities related to manufacturing are supported by the European Metrology Networks (EMNs). The European Metrology Network for Advanced Manufacturing aims to help European industries to meet high-precision requirements in quality assurance along the entire manufacturing chain from advanced materials, smart manufacturing systems, to components and products [8]. The European Metrology Network (EMN) for Quantum Technologies provides active coordination of European measurement science research to maintain competitiveness in the field of quantum technologies [9]. Among on-going and past metrological research projects, we can mention on-wafer microwave metrology for future industrial applications [10], application of digital-metrological twins for emerging measurement technology in advanced manufacturing [11], RF key quantities for 6G development [12], fundamental principles of sensor_network metrology [13], self-calibration photodiodes for UV and exploitation of induced junction technology [14], memristive devices as quantum standard for nanometrology [15], digitalisation route for dimensional nanometrology [16]. The EURAMET research programs can be found in [17].

It is also recognised that research and development activities highly contribute to the development of new standards. For example, standardisation activities on quantum technologies (QT) are at an initial stage, as an example IEC/ISO JTC3 Quantum technologies [18] and CEN-CENELEC [19] show a reduced number of published standards. This is understandable as the technology is still at its early stages. This phase is characterised by different R&D activities where partnership between academic and industry are at the core of those activities before reaching wide consensus and full standardization. For example, in Europe, Fujitsu and TUDelft, Netherlands are collaborating on modular quantum computing based on spins in diamond [20]. Moreover, the extreme diversity of quantum hardware (diamond, superconducting, ion-trap, photonic qubits) makes a single architecture specification very difficult. Thus, standards can be developed for specific platforms from relevant academic or academia-industry research collaboration. The Fujitsu-TUDelft collaboration would allow the development of standards for many components and techniques for diamond and/or solid-state quantum systems, such as material processing, quantum techniques/operations, cryogenics, control electronics, packaging/integration, on-chip system,

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scalability, error correction, software and middleware stacks etc., which fall outside the available standard categories.

Beyond this, there are several academic and collaborative projects ongoing in Europe which have high potential to influence and establish quantum technology standards. For example, the Quantum Flagship (FQ) [21, 22] is one of the most ambitious long-term research and innovation initiatives of the European Commission. It consists of a coherent set of research and innovation projects selected through a thorough peer-review process. To support and coordinate the activities of standardisation in QT, the QF has a dedicated work group on Standardisation [23].

Similarly, the Quantum Internet initiative from the Quantum Internet Alliance [24], a team of Europe's world-leading quantum research institutes and industry actors in nine countries, complements by preparing the future generation of quantum networks. It lays the foundation for distributed quantum computing and sensing, and ultra-secure data sharing. This will also help position the EU at the forefront of international standardisation in this area. To support technical interoperability and new standards for quantum industrialisation, the EU aims to publish a European Quantum Standards Roadmap in 2026 to update and complement any other initiative set by researchers [25] or institutions like CEN-CENELEC [26, 27] and ETSI [28].

We can also mention, Qu-Pilot (Quantum Pilot Lines), a Horizon Europe project, that connects and upgrades existing European pilot-fabrication facilities to create the first European production capabilities for quantum hardware. With 21 partners from 9 countries (mostly research institutes), Qu-Pilot aims to build a "one-stop-shop" network of pilot lines covering superconducting qubits, photonics, semiconductor quantum dots, and diamond platforms. This can lay the groundwork for manufacturing standards of quantum chips (e.g. compatible process flows for photonic and superconducting devices) and a more integrated supply chain [29, 30].

As technologies become more advanced, CO2 emissions associated with the manufacturing of ICs have increased. Not only CO2, emission of other gas, such as fluorine-containing etching gas should also be reduced. IC production should also minimize waste resulting from the manufacturing. Different projects like Sustainable Semiconductor Technology and Systems Program (SSTS) at imec [31] or the EU funded project GENESIS [32] could initiate standards on reducing environmental impact from electronics manufacturing. As the amount of e-waste increases and the consumers become increasingly environmentally conscious, the demand for sustainable and eco-friendly products are emerging. There is a need for recyclable electronics and biodegradable electronics that need to be overcome by the industry. The challenge for biodegradable electronics lies in addressing regulatory and standard issues, as there is currently a lack of standardisation in this area.

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Those Research and Development activities are at a level of maturity where standardisation activities can be initiated. In most cases, innovative activities start in laboratories at universities for concept validation. The most promising move into an industrial partnership for assessment and implementation at higher scale, before reaching full industrialisation and international standardisation. Supporting such activities through the full cycle requires long term vision and strategic thinking that should be coordinated at a higher level.

3.2 Intra and Extra SDOs Collaboration

Semiconductors are the foundational components for nearly all modern electronics, including smartphones, computers, and cars. The semiconductor industry is a crucial part of the broader electronics and technology sectors, driving advancements across multiple industries, including mobility, energy, digital industry, health, agrifood, and even beyond through AI or cybersecurity technologies. It is also a major contributor to the industrial internet of things (IIoT) and smart factories which relies heavily on semiconductor chips for automation and data analysis.

Within that context, different sector specific SDOs have been working on increasing collaboration through the use of roles like liaison officers (LO) and joint working group (JWG) within the same SDOs or among different SDOs with the aim to reduce friction and repetition of some existing standards. Such initiatives should be encouraged, praised, and even enforced in some cases to make sure all SDOs have other SDOs as liaison members to create more meaningful standards.

As an example, IEC TC 47 Semiconductor devices have different liaisons [33] with IEC, ISO, and other organisations. However, it does not have liaisons with any of the ISO/IEC JTC 1 committees [34], SEMI [35], JEDEC [36], SAE [37], SI2 [38], and IEEE [39]. The same can be observed among other SDOs as they are still not widely collaborating together to reach a wider international consensus to build a better initiative and develop new standards.

It is also important to notice that the European Commission has a liaison with ISO/IEC JTC 1/SC 27 [40], and therefore can follow and influence the standards developed by SC 27. This initiative is more than welcome and should be encouraged to cover not only SC 27 but also other committees like IEC TC 47 when it comes to semiconductors.

It is generally recognised that the semiconductor industry is characterized by high capital expenditure for manufacturing facilities (fabs) and a constant need for innovation and R&D. According to Intel [41], building a new semiconductor fabrication plant (fab) can cost between $10-15 billion. This makes collaboration and early initiative to standardize new technology a

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good way to reduce financial, technological, and operational risks to the industry, the investors, and the tax payers in times where uncertainties are high and resources are limited.

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4 Conclusion

In this report, an extensive database comprising approximately 5,000 standards was collected. Based on the database, a comprehensive gap analysis was performed, focusing primarily on the emerging technologies related to semiconductors and chips. The analysis reveals different major gaps, mainly in the areas of Datacenter Edge & Cloud, Sub-5nm semiconductor technologies, Quantum Computing, Neuromorphic/ReRAM/AI Chips, IC Design, and Energy Efficiency and Sustainability.

These gaps pose risks to European innovators and European industries if not addressed promptly. The rapid advancement of global technology ecosystems should be assessed and embraced at an early stage to avoid fragmenting Europe's market through different outsourced suppliers, making it vulnerable to environmental and political changes.

To address these risks, targeted recommendations have been put forward to strengthen Europe's strategic position by actively shaping and adopting unified standards in these technology domains. The key objectives have been aligned with the EU Chips Act and Europe's broader Digital Decade ambitions.

Europe can strengthen its semiconductor sovereignty and establish a global benchmark for responsible high-tech development by championing open, secure, and sustainable standard

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