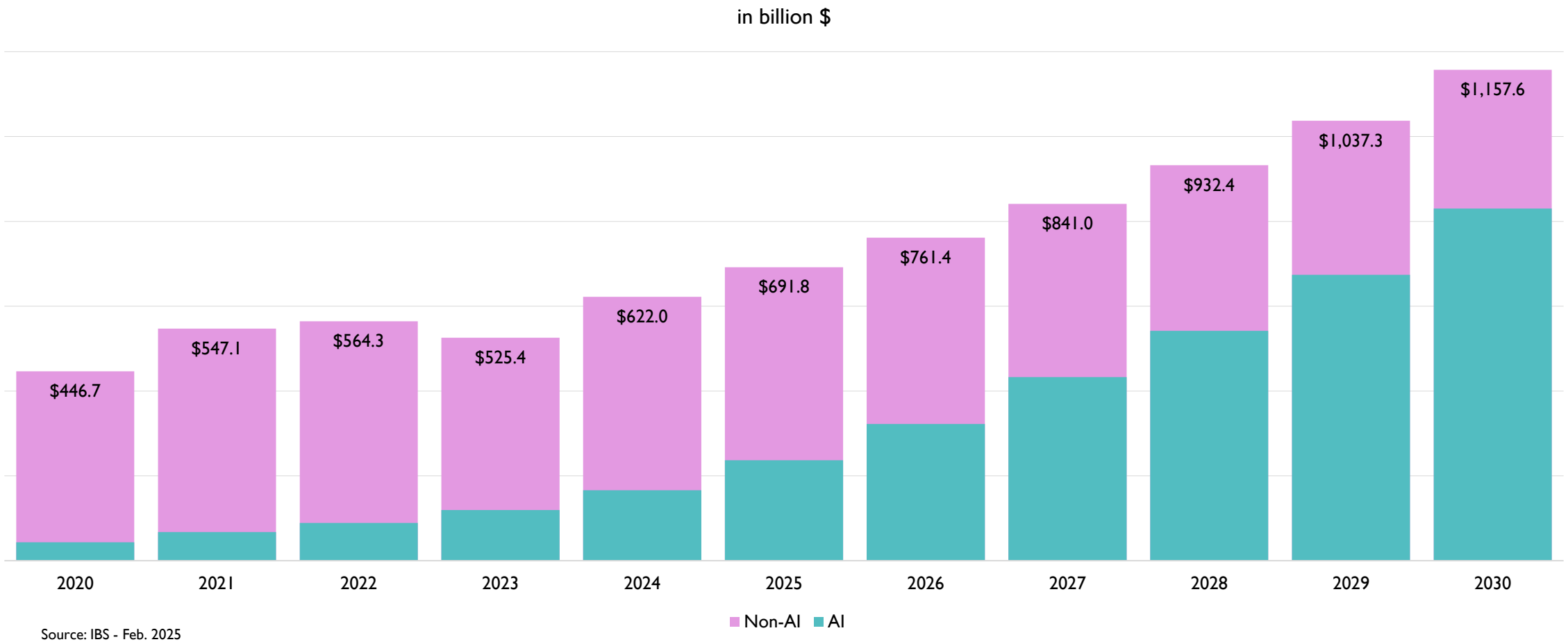
New device architectures for Advanced Computation

Nadine Collaert

imec

The AI market is ~~expected~~ to drive the semiconductor ecosystem is driving



Source: IBS - Feb. 2025

Diversified applications drive different system solutions

Hyperscale datacenters

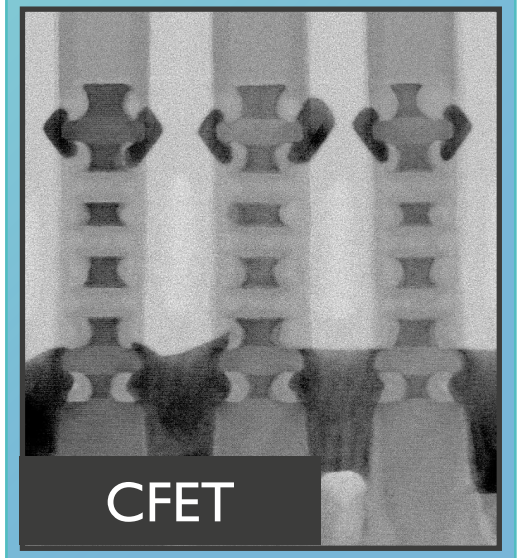
Edge & Cloud datacenters

Autonomous and mobile applications

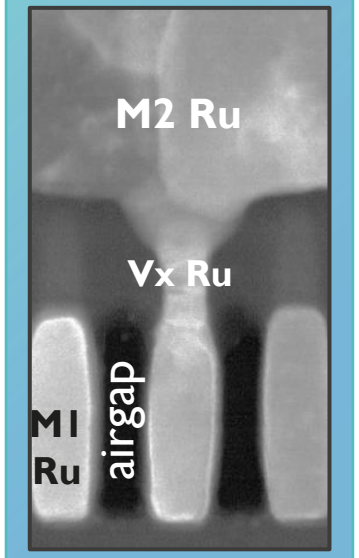
Performance ⟷ **Latency & power**

Technology solutions becoming more sophisticated to support dimensional scaling

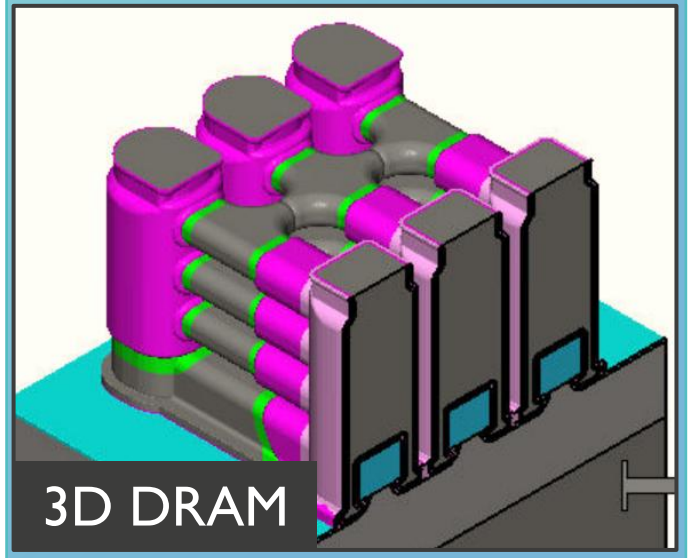
New device architectures



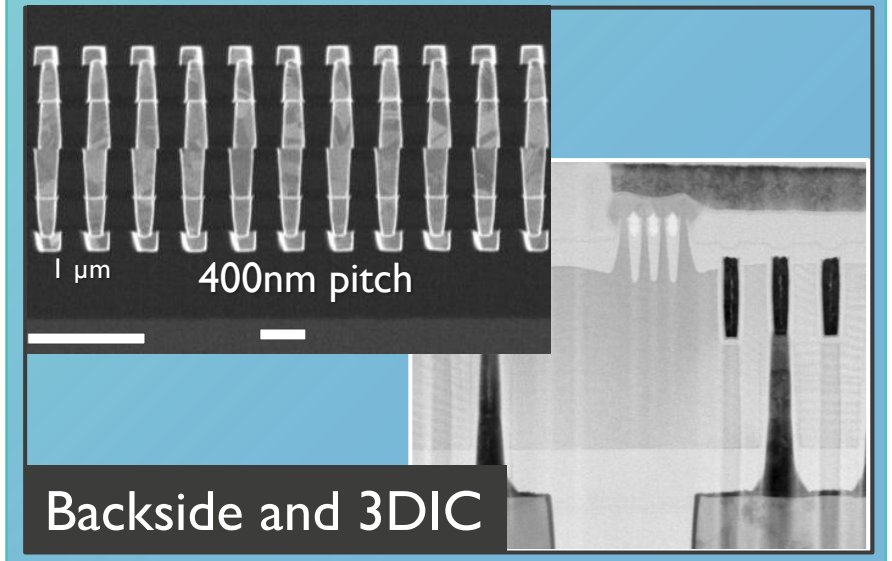
RC boosted interconnect



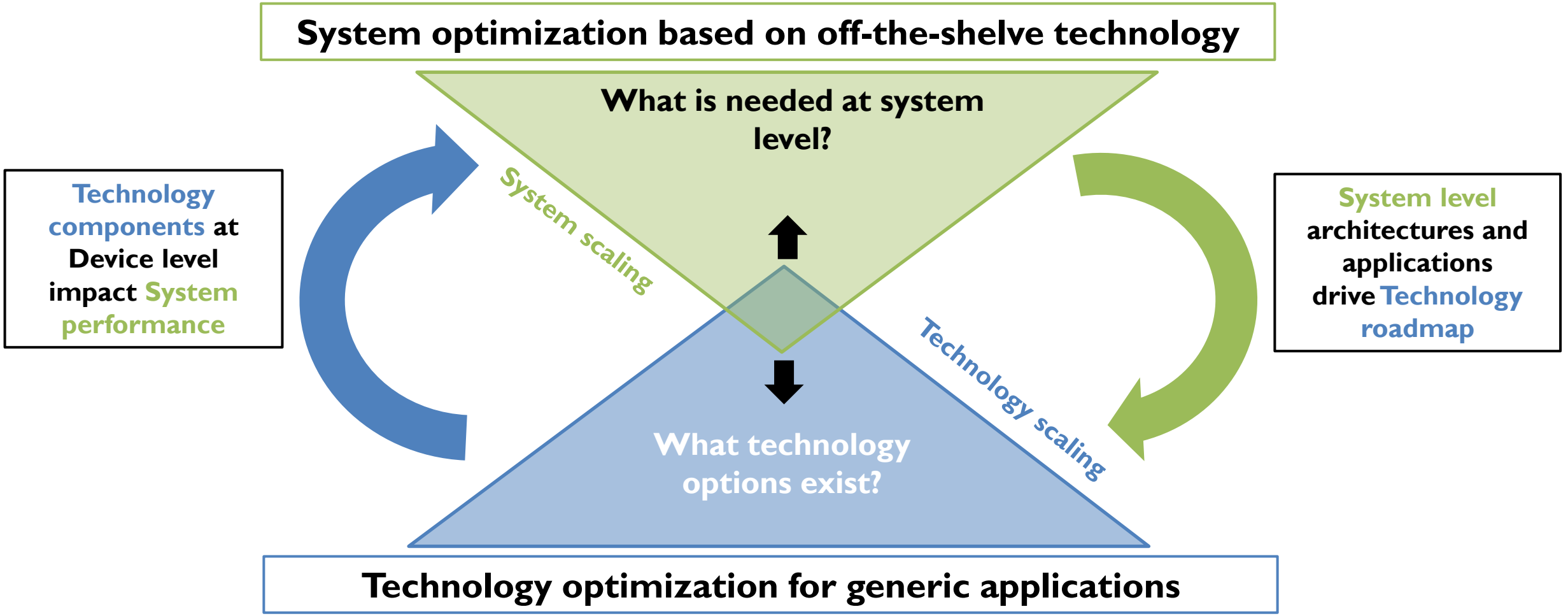
3D-integrated DRAM



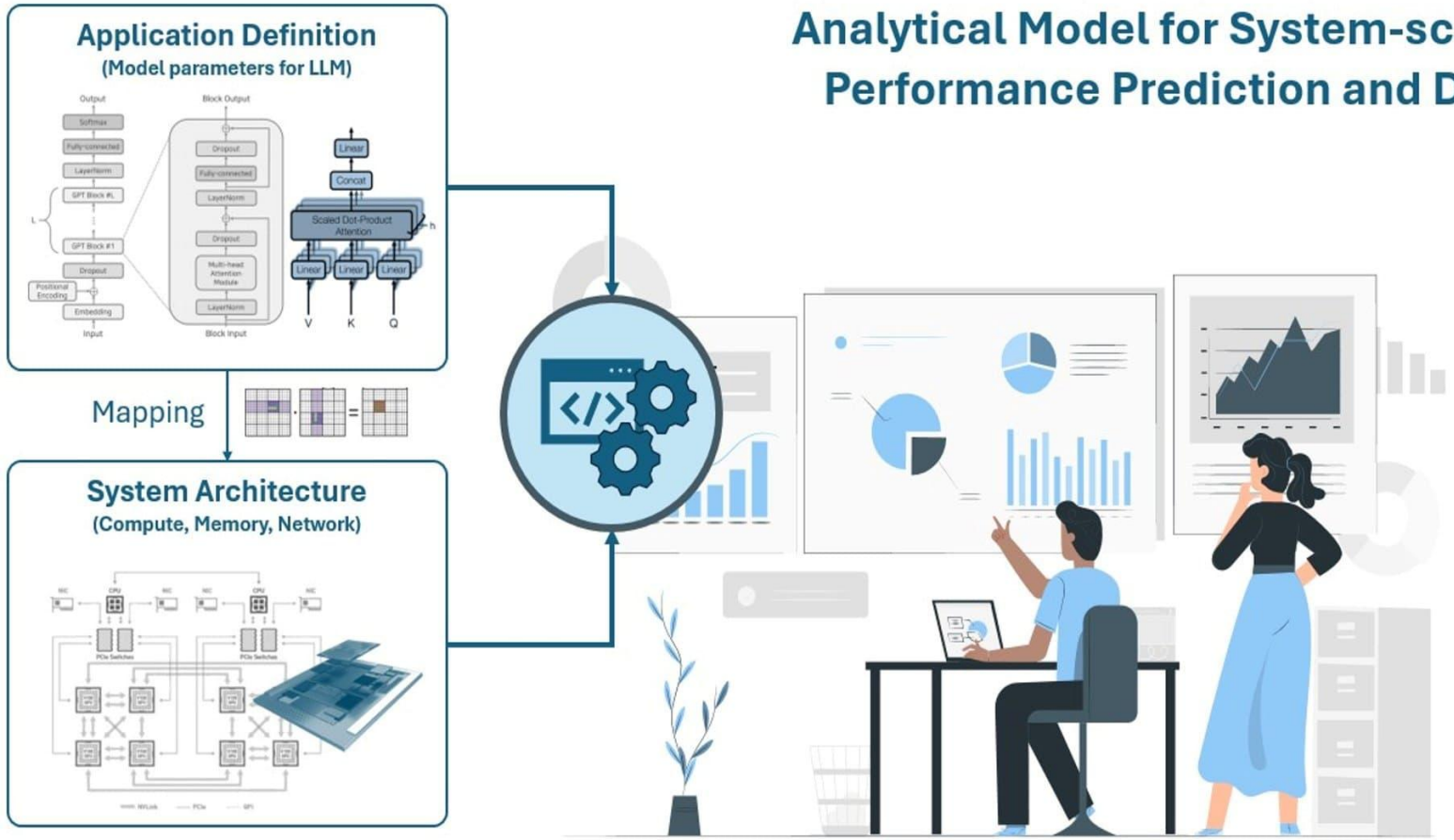
Novel Global interconnect solutions



Solution needs to come from system-level scaling



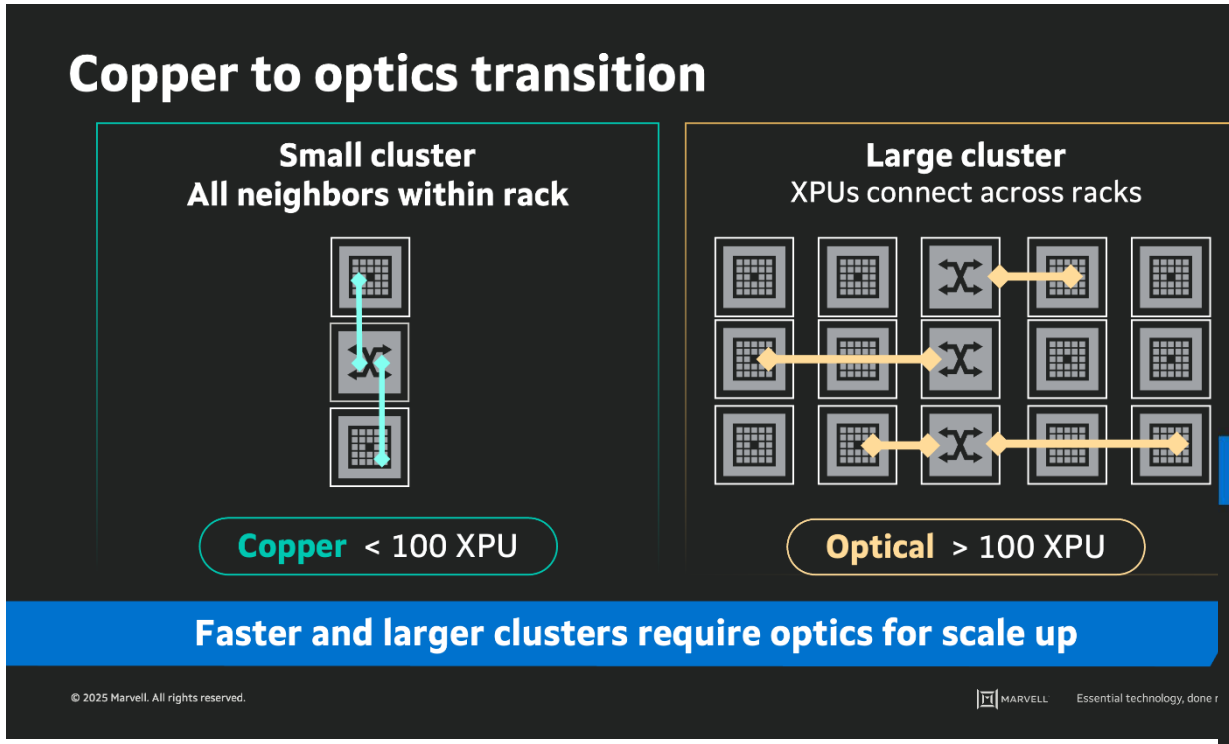
Hardware-software-technology codesign approach



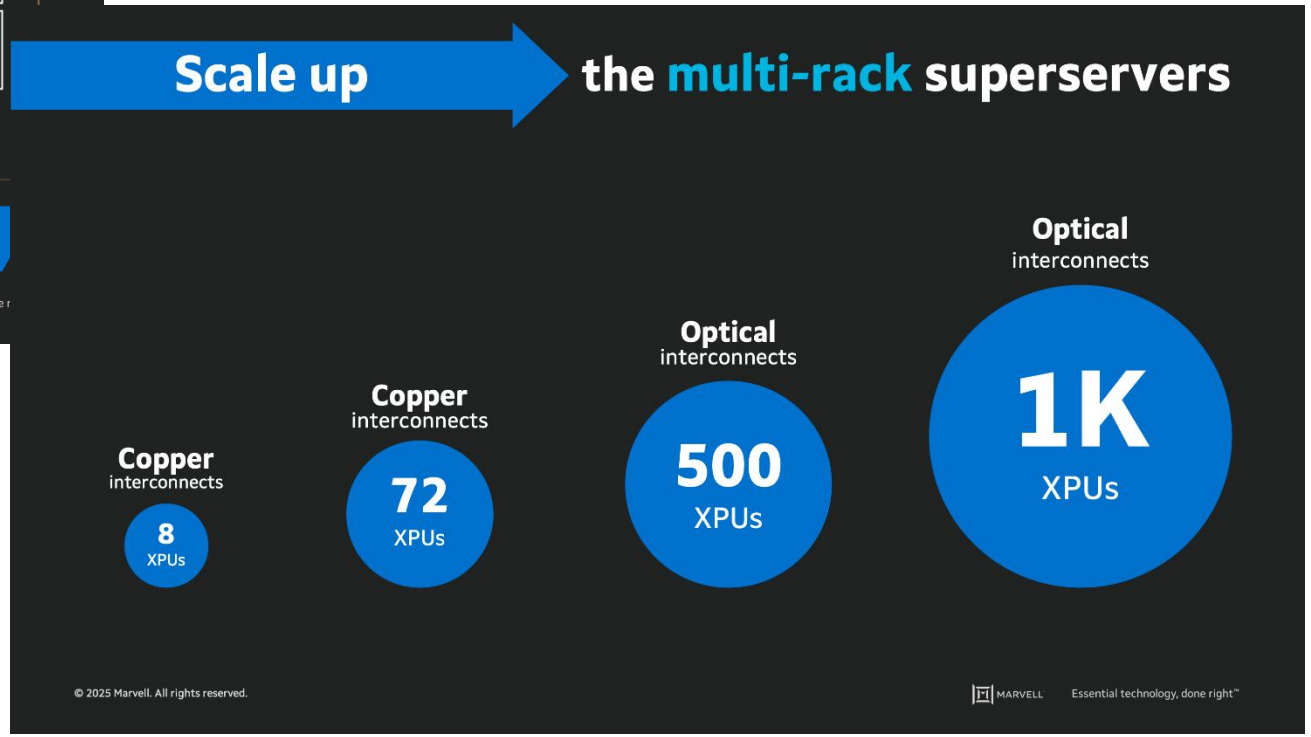
https://www.imec-int.com/en/expertise/compute-system-architecture/imeckelis

Compute is nothing without connectivity

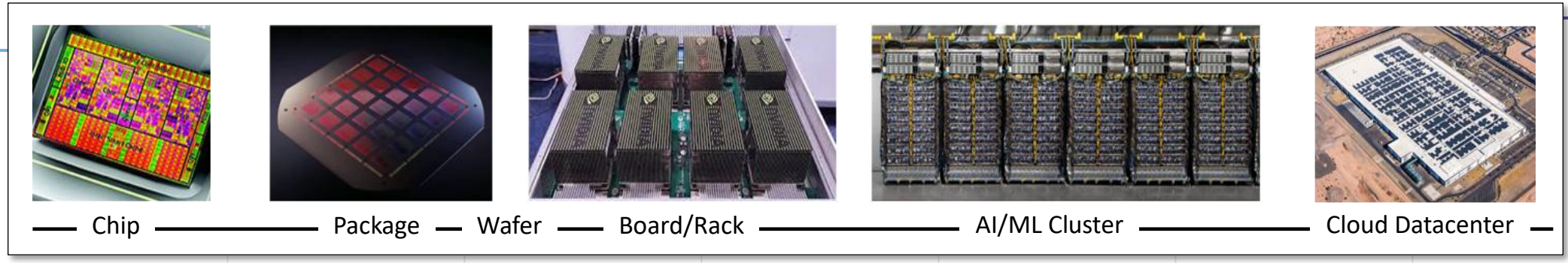
Increasing pressure on connectivity in AI

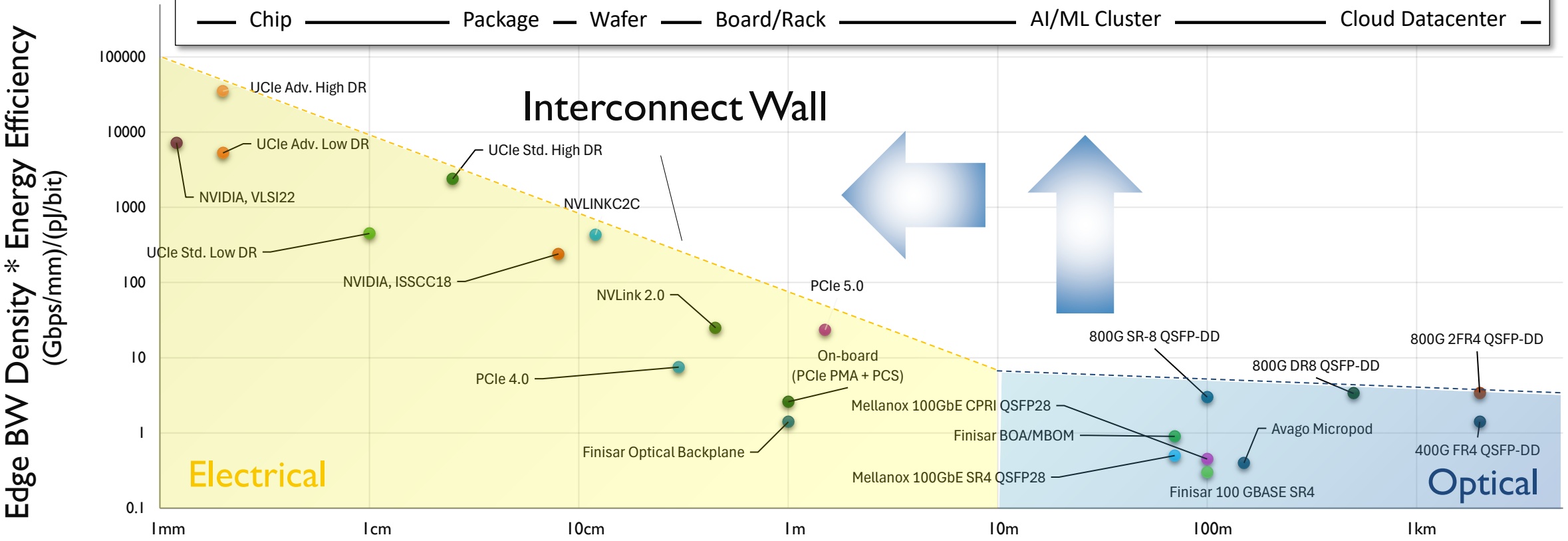


https://www.marvell.com/blogs/the-evolution-of-ai-interconnects.html



The interconnect landscape

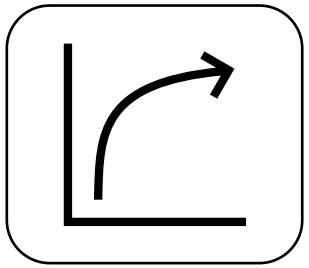
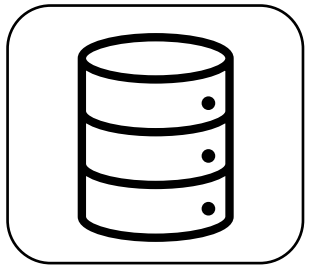
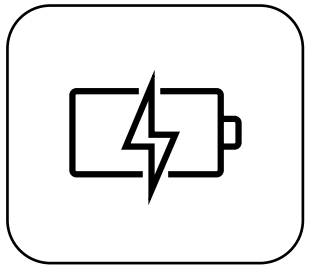
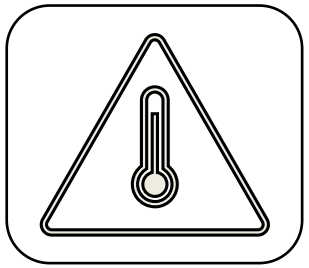
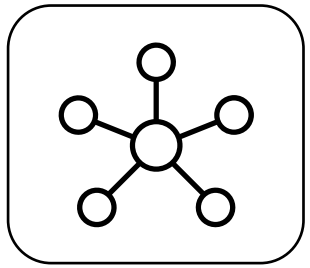
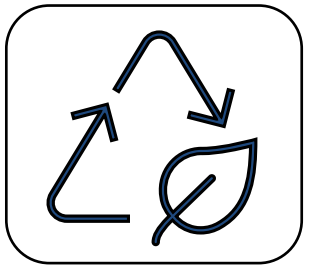




Inspired by Gordon Keeler, ex-DARPA

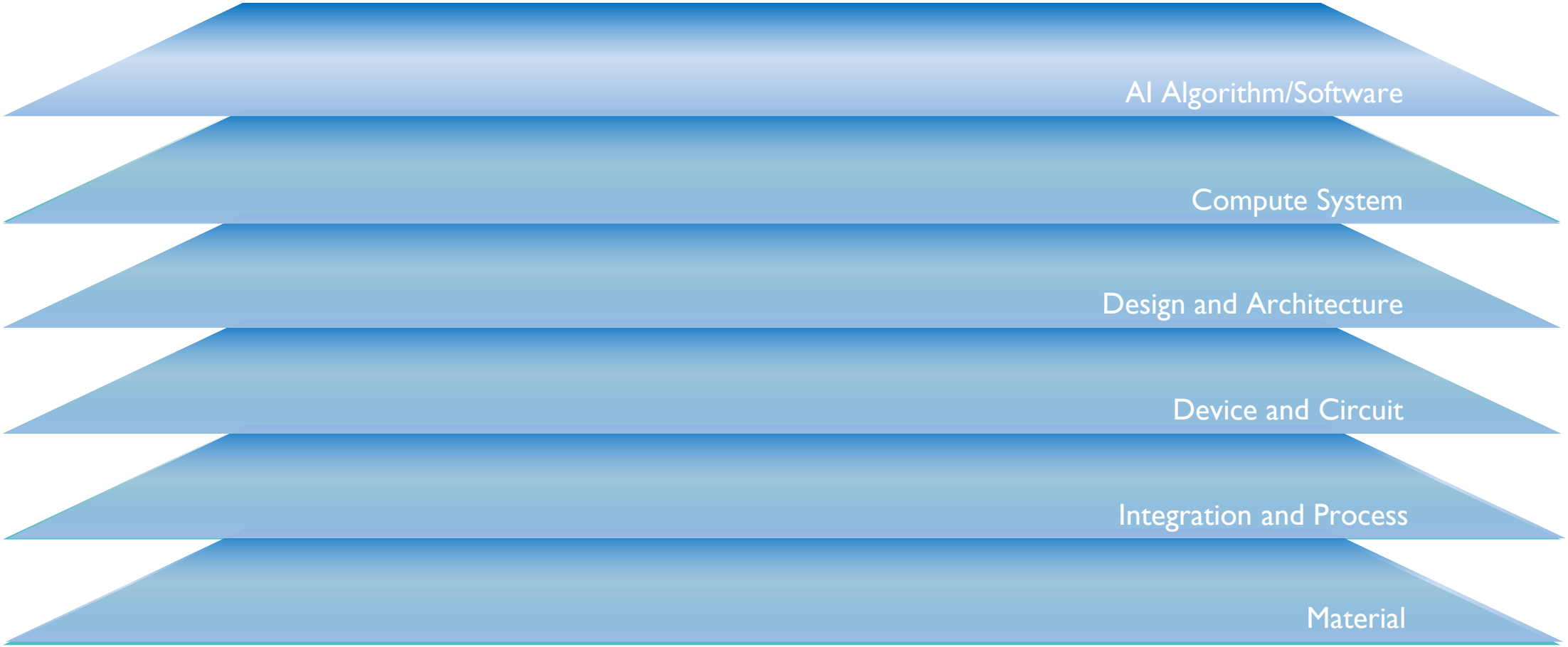
Addressing the system scaling needs

Challenges for future systems

Compute	Memory	Power	Thermal	Connectivity	Sustainable Manufacturing

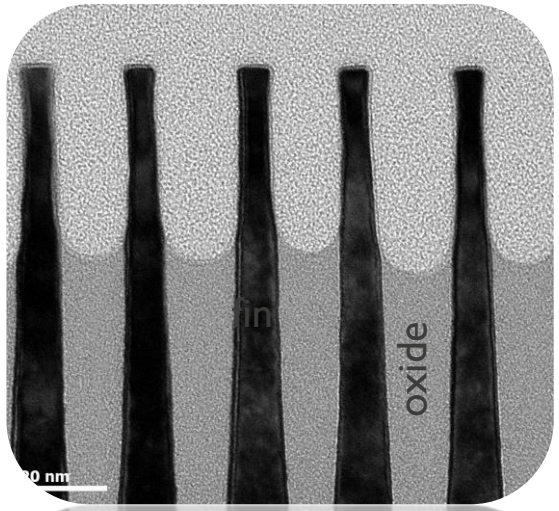
System scaling



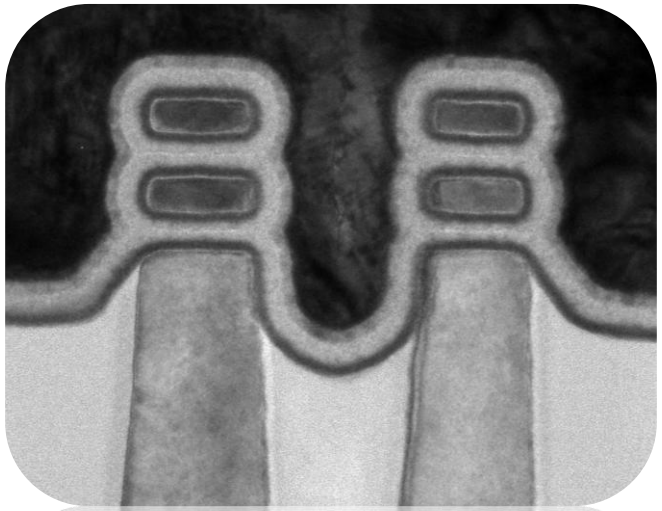
From FinFETs to nanosheets to CFET

14-3nm | 2nm-10Å | 7-2Å

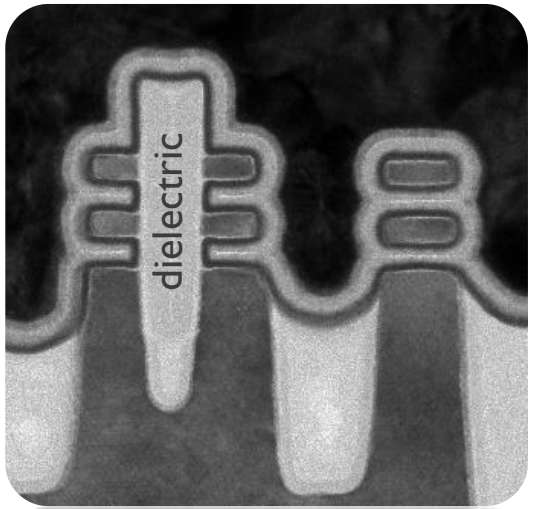
FinFET



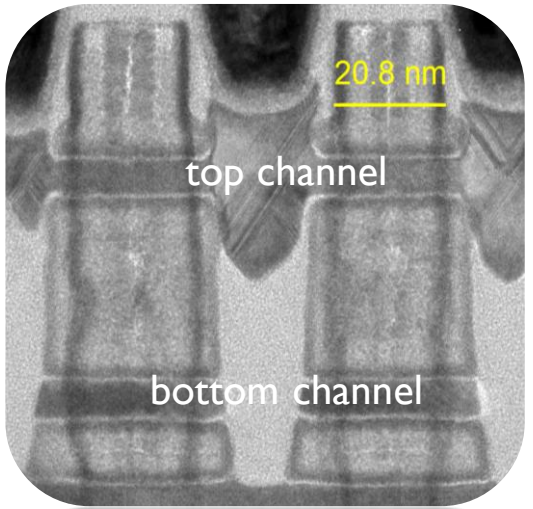
Nanosheets



Forksheets



CFET



N. Collaert, "Advancements in IC Technologies: A look toward the future," in IEEE Solid-State Circuits Magazine, vol. 15, no. 3, pp. 80-86, 2023.

Possible roadmap

2018	2020	2023	2025	2027	2029	2031	2033	2035	2037	2039
N7	N5	N3	N2	A14	A10	A7	A5	A3	A2	sub-A2

DEVICE AND MATERIAL INNOVATIONS

FinFET → **NanoSheet** → **CFET** → **2DFET, ?, …**

	Introduction	Scaled	Extended	Introduction	Scaled	Extended	Introduction	Scaled	Extended	Introduction	Scaled
Metal Tracks	6	6	6	5	5	5	4	<4	<4	<4	<4

CONTINUED DIMENSIONAL SCALING

0.33NA EUV → 0.55NA EUV → 0.75NA EUV ?

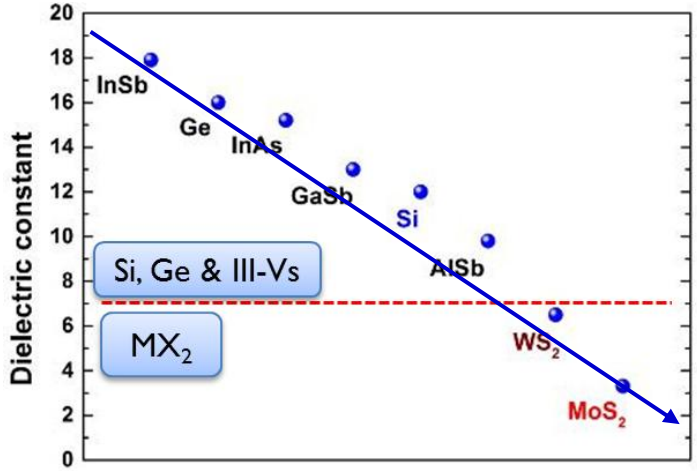
Metal Pitch [nm]	40	28	23	22	21	18	18-16	18-14	16-12	16-12	14-10

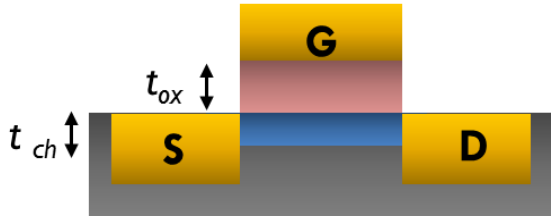
CHIP INTERCONNECT ARCHITECTURE

Back-side Power - Global interconnects → Back-side Power - Local signal lines

Back-side Metal Pitch estimate [nm]	-	-	160-65	115-45	90-42	40-34	40-28	tbd	tbd	…

2D Materials



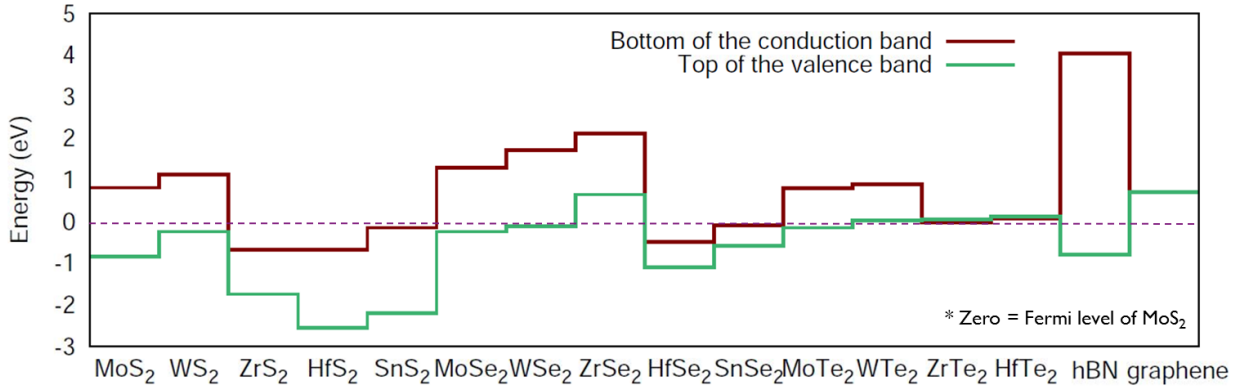


Characteristic length of short channel FETs:

$$\lambda = \sqrt{\frac{\epsilon_{ch}}{\epsilon_{ox}} t_{ch}.tox}$$

Expect reduced short channel effects in planar devices

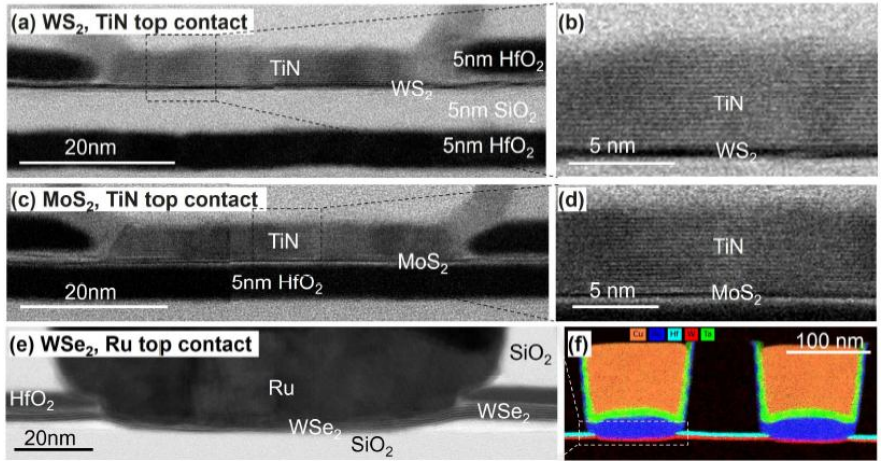
Ultra-thin materials



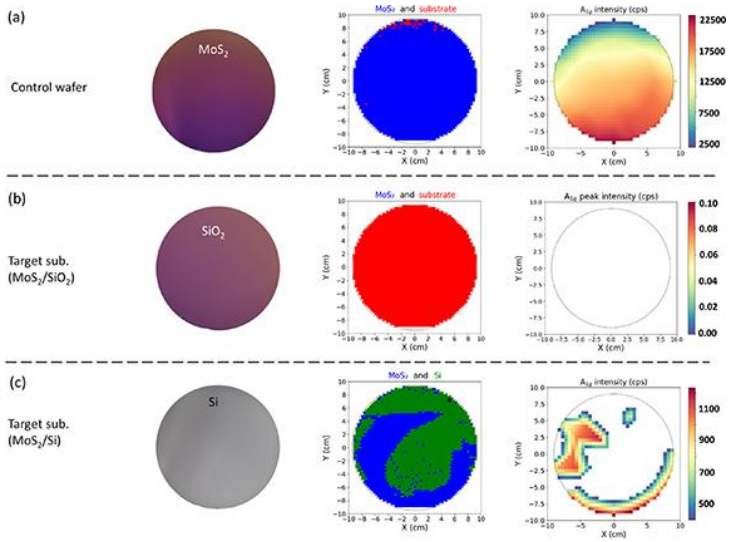
Choice of bandgaps and band alignment

No/few dangling bonds at interfaces

Progress in 2D materials

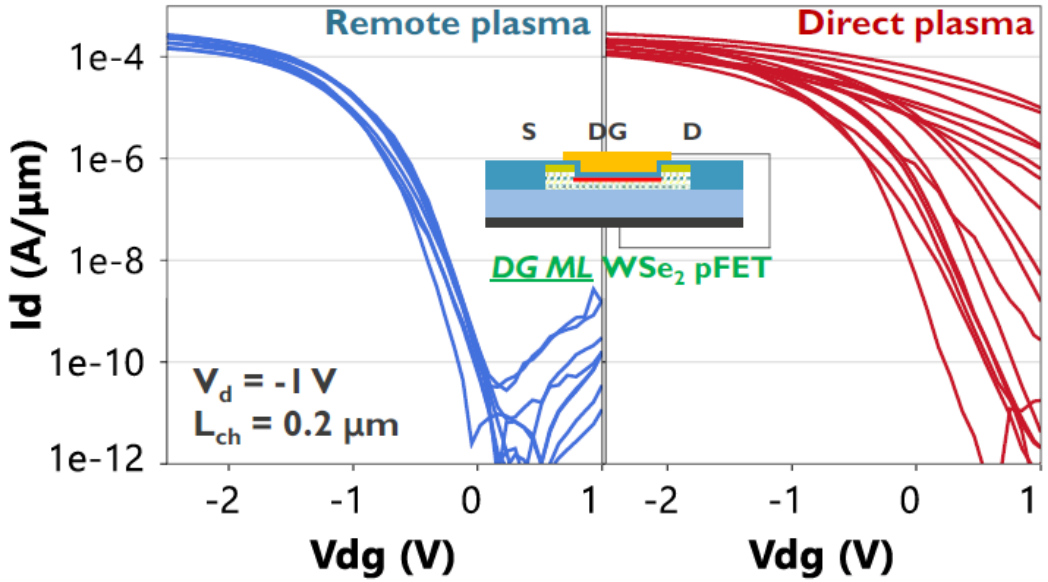


Q. Smets et al., IEDM 2025.



Paul Brunet *et al* 2025 *2D Mater.* **12** 035013

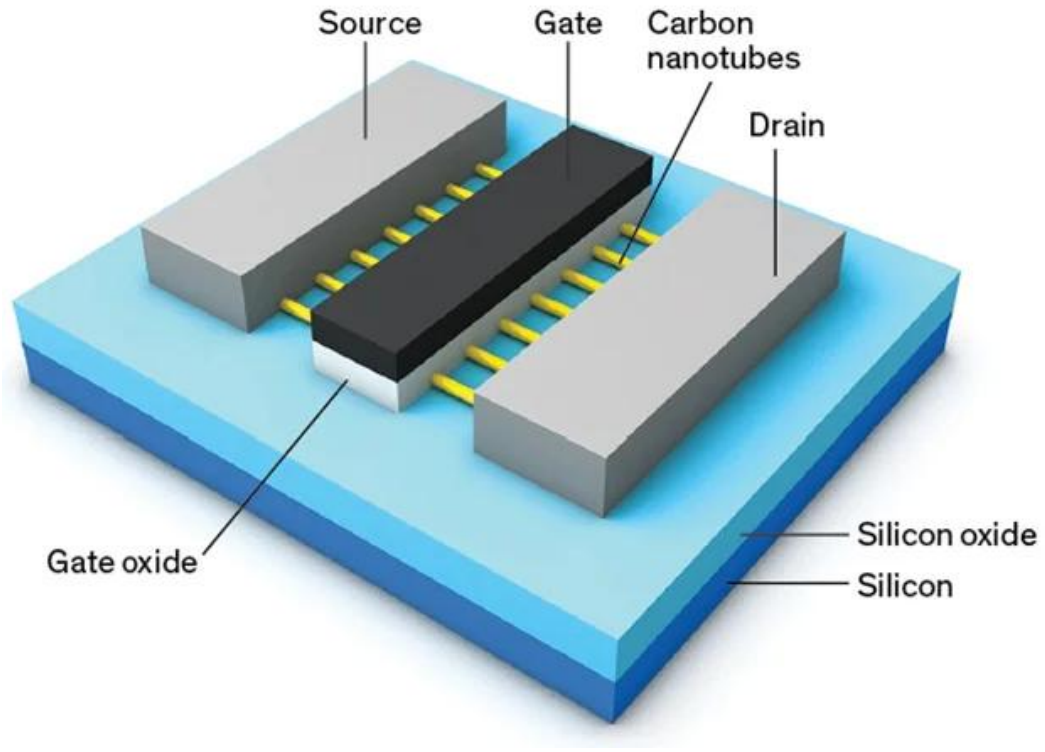
T.D. Ngo et al., IEDM 2025.



- Progress in key device modules: gate stack, contacts, layer transfer
- Progress in enabling high-performant pFET

New materials to fuel the roadmap

Carbon nanotubes



https://spectrum.ieee.org/how-well-put-a-carbon-nanotube-computer-in-your-hand (2016)

Advantages:

- High mobility
- Reduced power consumption
- Scalability
- Thermal stability
- Diversity of applications

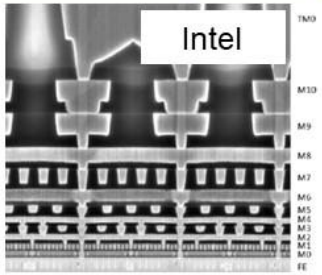
Challenges:

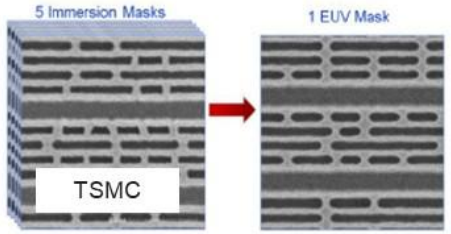
- Purity and uniformity
- Large scale cost-effective production
- Co-integration with existing technology
- Contact resistance
- Environmental stability

Industry BEOL trends

~36-40nm BEOL pitch

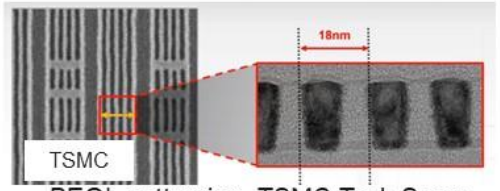
10nm technology, C. Auth et al. IEDM 2017





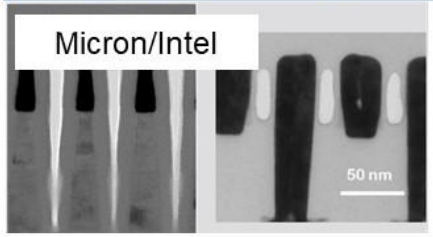
5nm CMOS, G. Yeap et al. IEDM2019

<20nm pitch

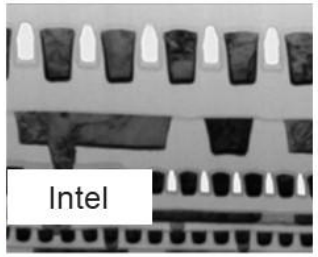


BEOL patterning, TSMC Tech Symp. 2020

AGs in memory & logic

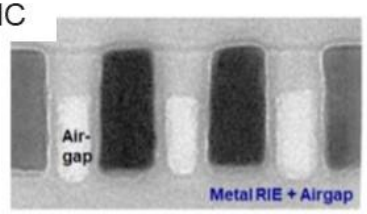


25nm NAND using air gaps K. Prall/K. Parat IEDM2010



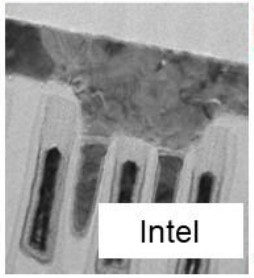
K. Fisher et al., 14nm, IITC2015

TSMC

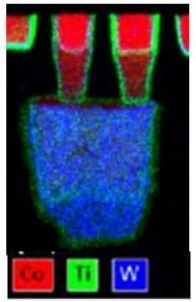


Y.J. Mii et al. Keynote, VLS022

Co interconnects



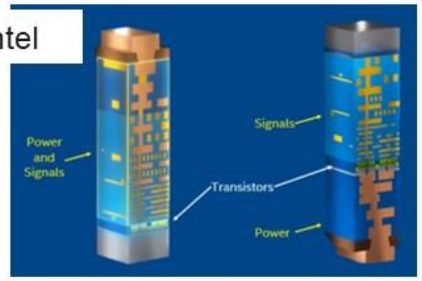
Self- aligned contact, C. Auth et al. IEDM 2017



Reliability of Co, F. Griggo et al. IRPS 2018

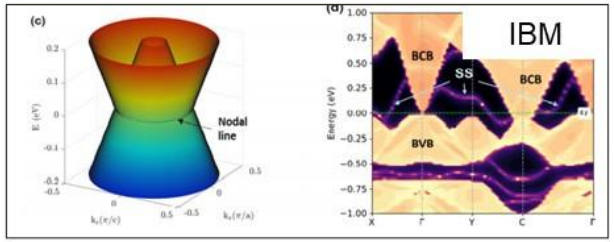
Backside Power Delivery

Intel

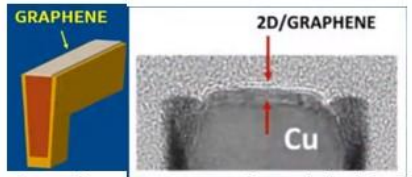


M.C. Mayberry, Keynote IITC 2020

New materials on the horizon

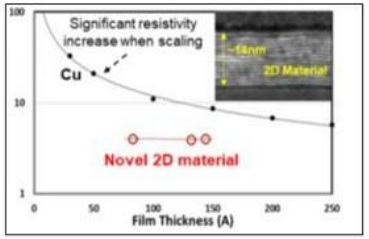


Topological semi-metal, C.T. Chen et al. IEDM2020



Intel

Graphene capped metal, R. Chau et al. Keynote IEDM2019



TSMC

New conductor, Y.J Mii Keynote VLSI2022

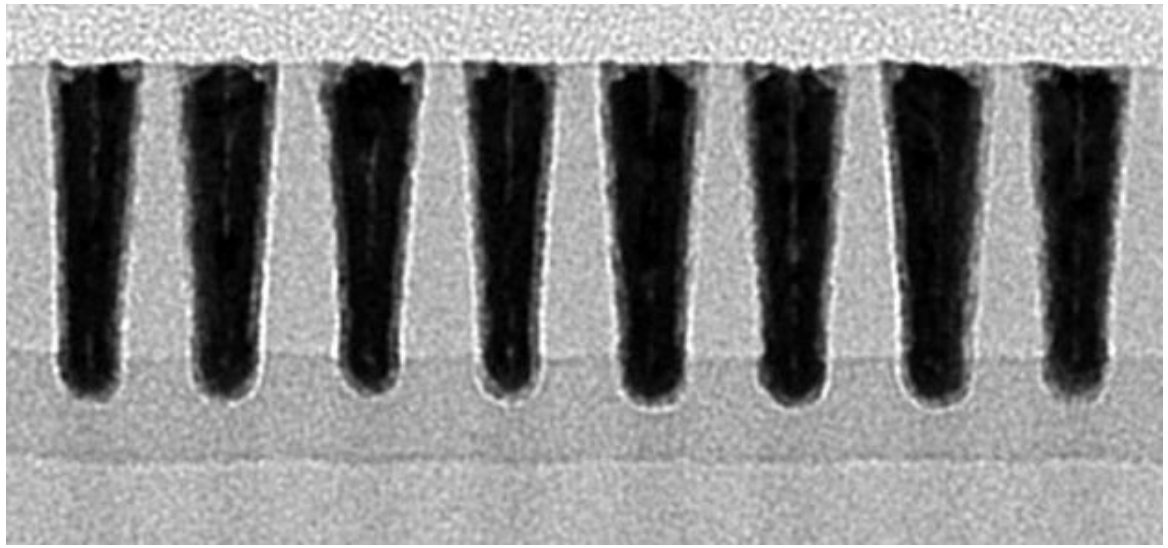
Pitch scaling, airgaps both in memory and logic, new materials

Courtesy: Z. Tokei (imec)

Lithography still key enabler

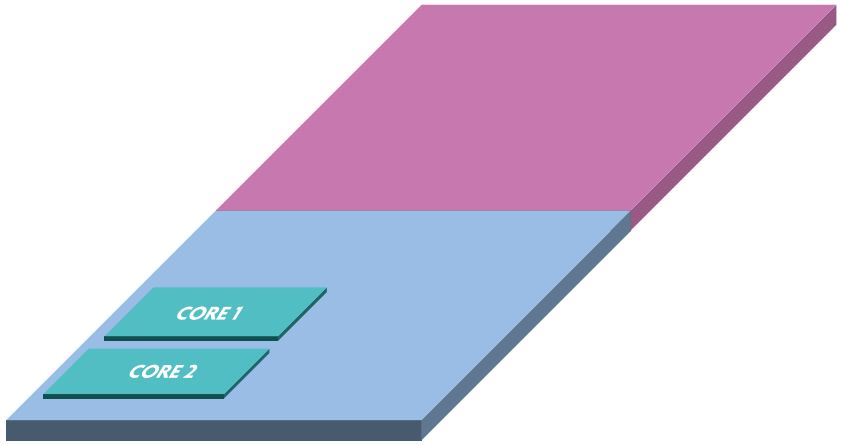
Courtesy of ASML

20nm

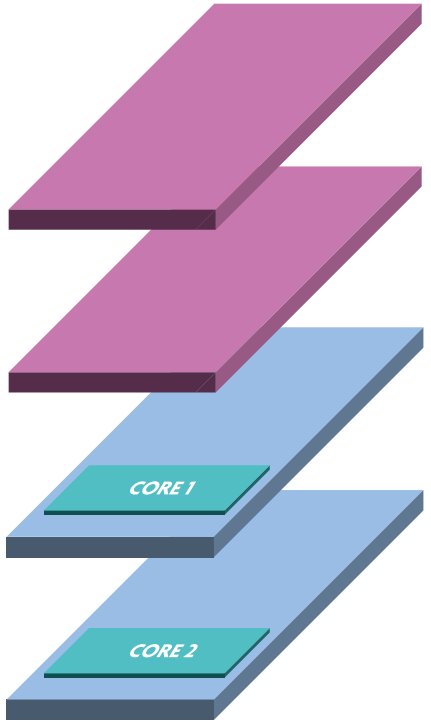


https://www.imec-int.com/en/press/imec-demonstrates-electrical-yield-20nm-pitch-metal-lines-obtained-high-na-euv-single

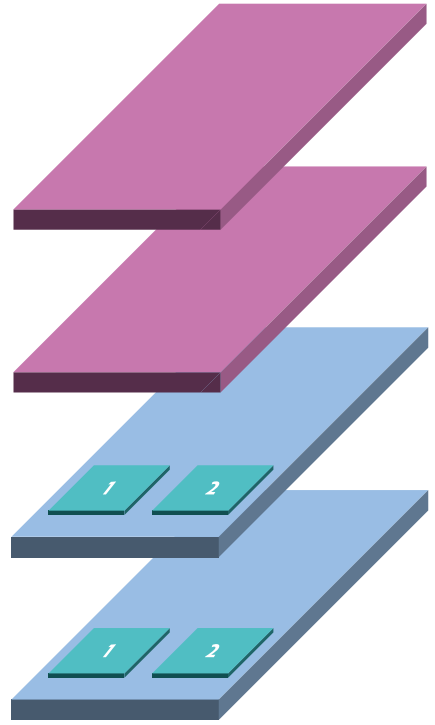
Taking 3D to the next level



2D
(or 2.5D chiplet)

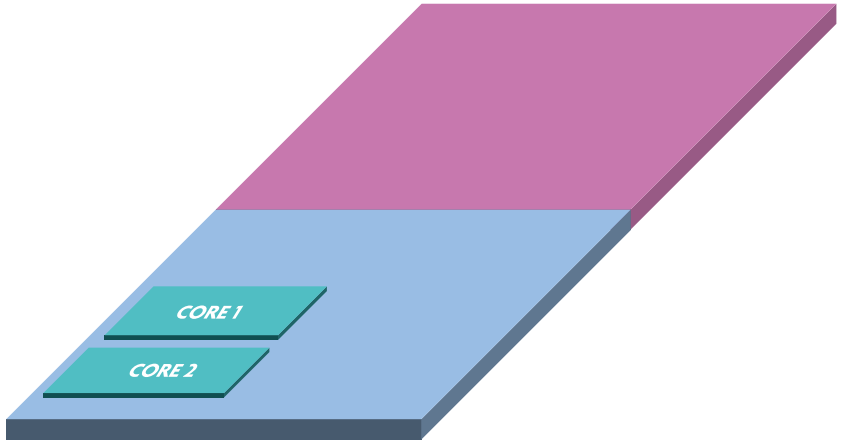


3D stacked system

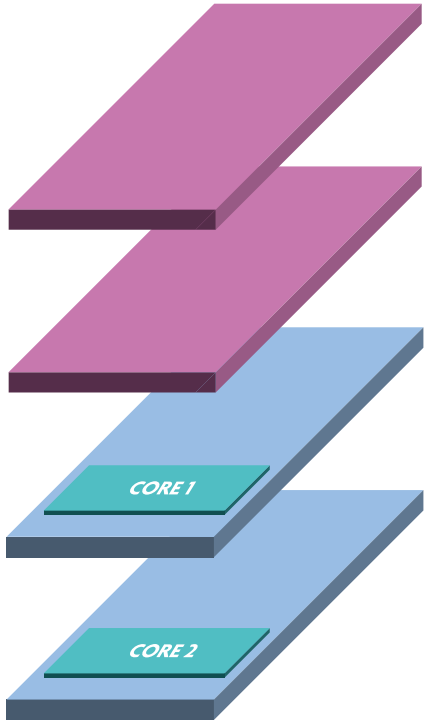


CMOS 2.0 Compute system

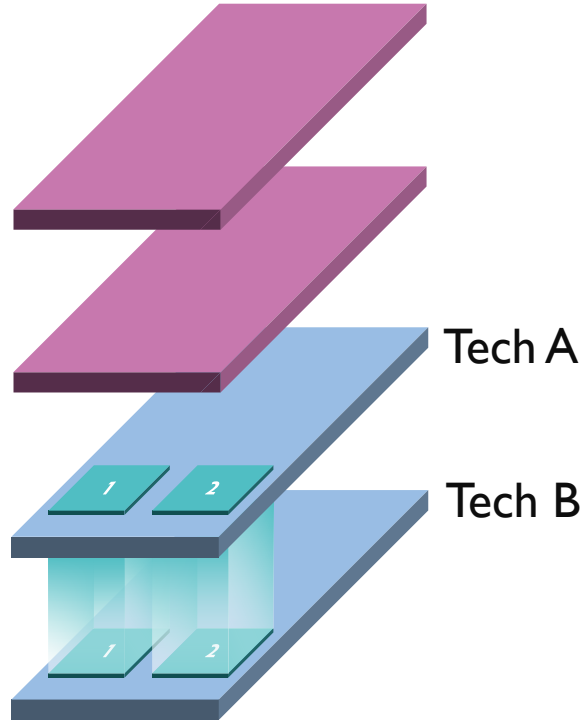
CMOS 2.0 uses functional specialization per tier



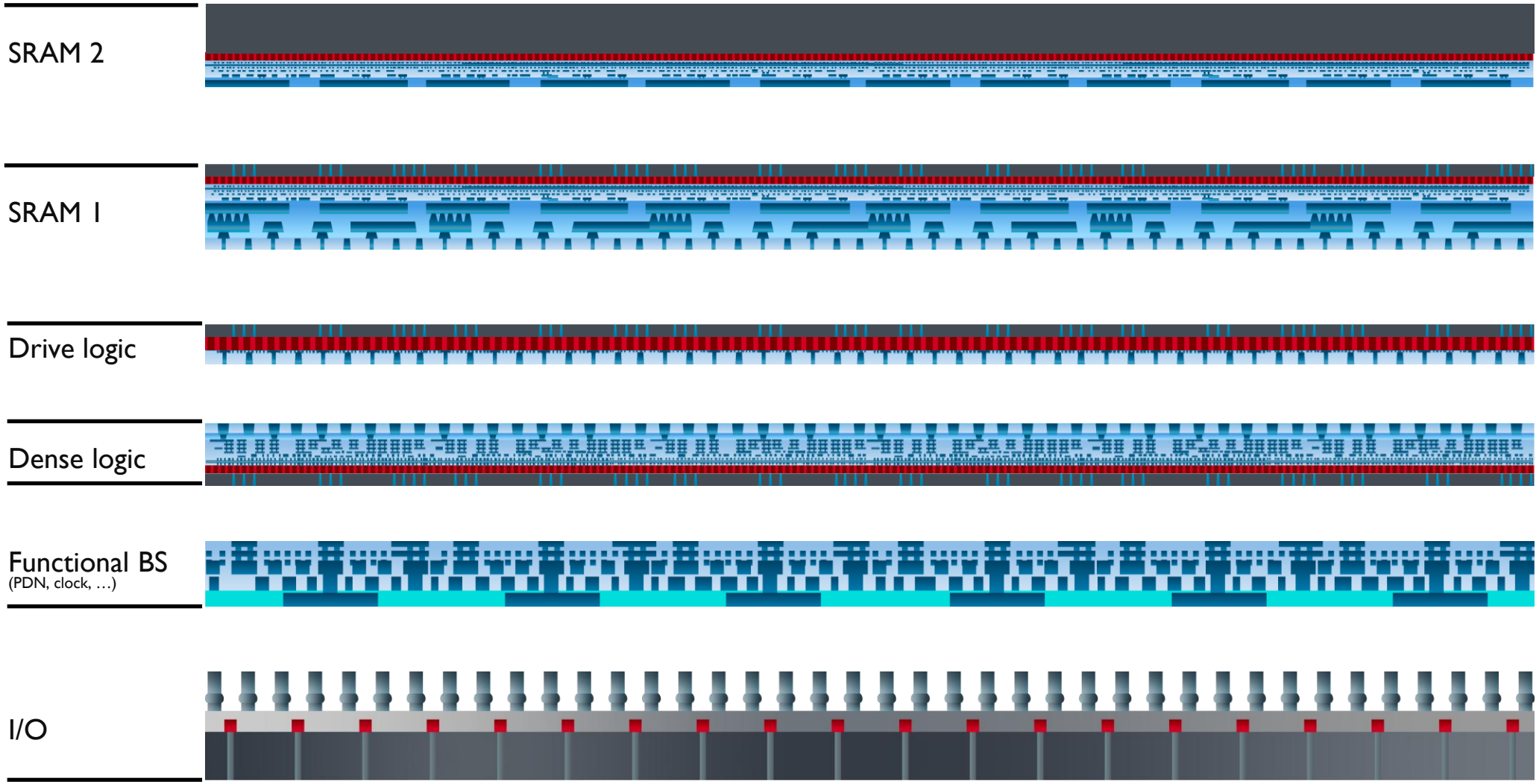
2D
(or 2.5D chiplet)

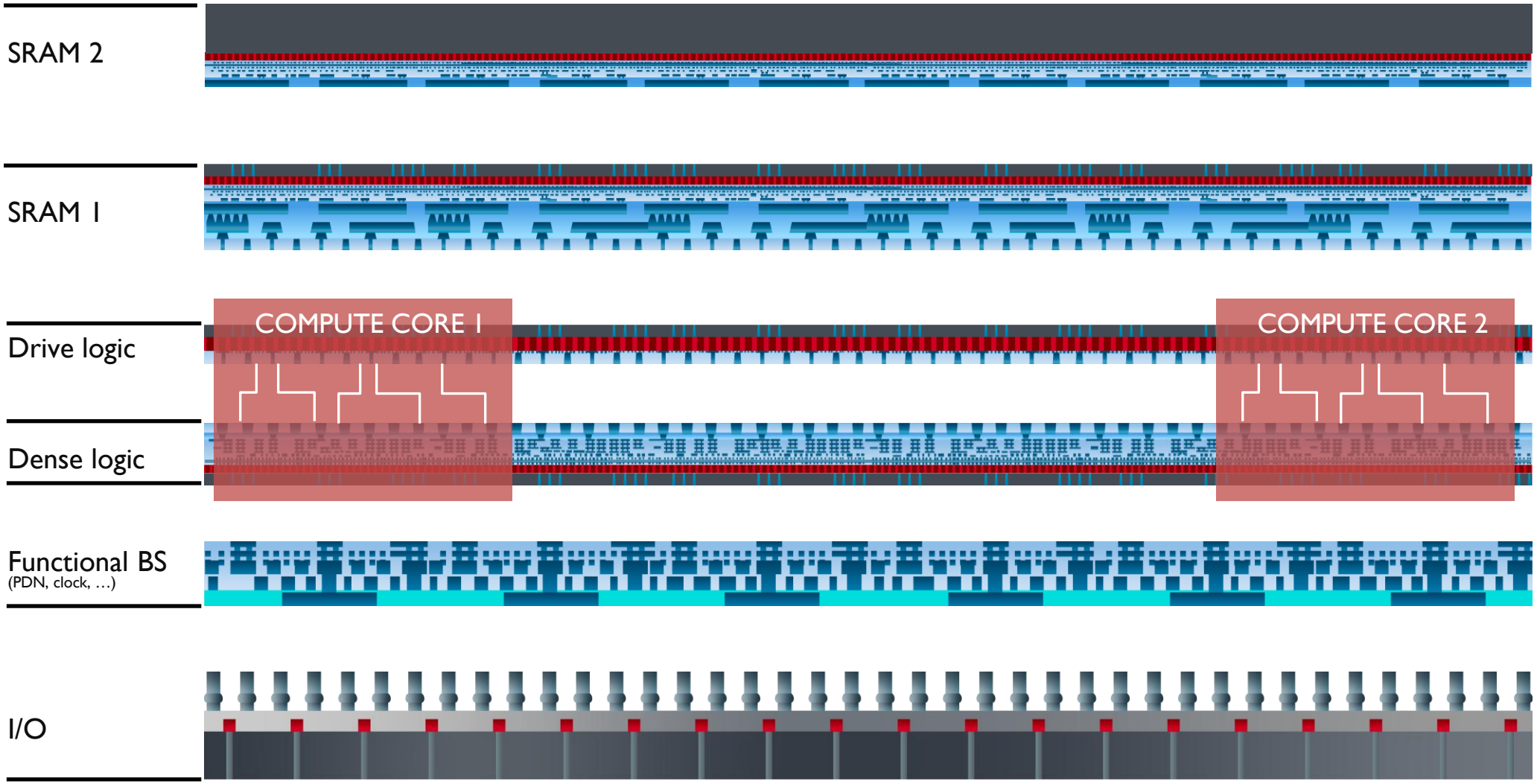


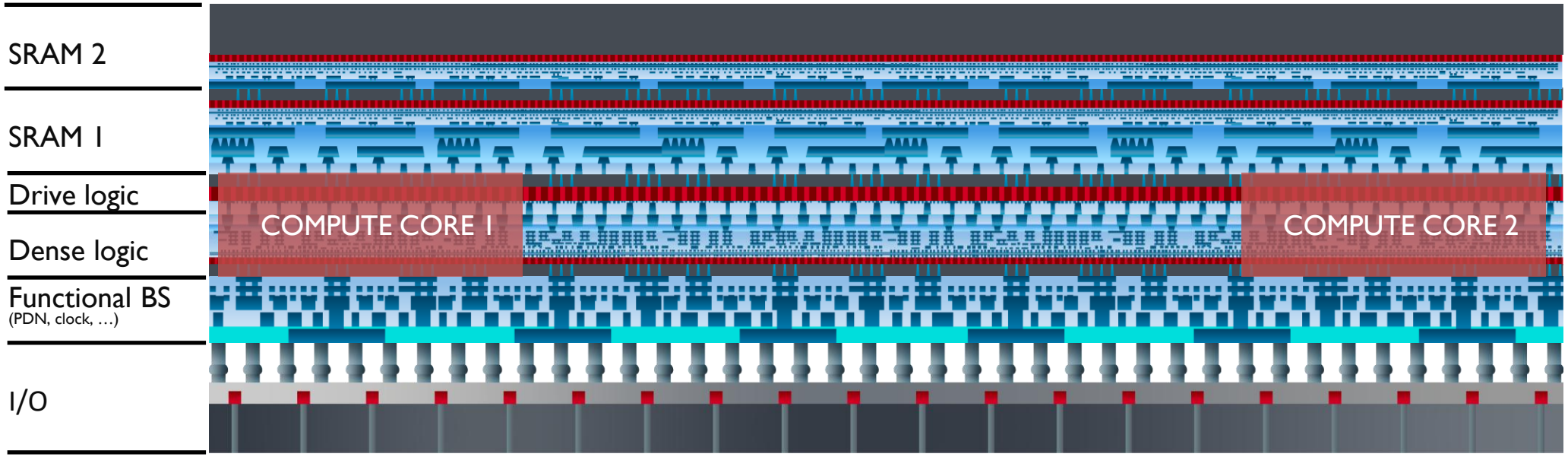
3D stacked system



CMOS 2.0 Compute system

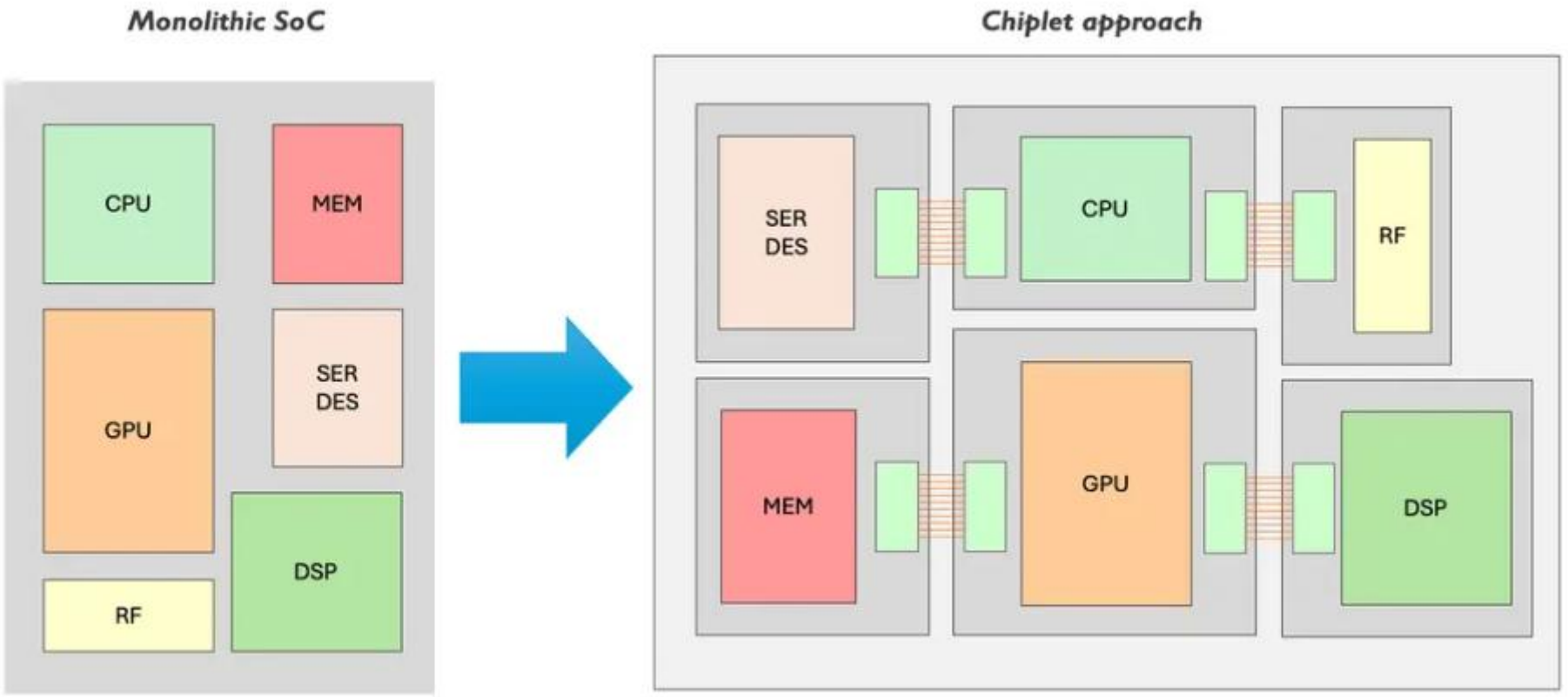

SRAM 2
SRAM 1
Drive logic
Dense logic
Functional BS
(PDN, clock, …)
I/O


SRAM 2
SRAM 1
Drive logic
Dense logic
COMPUTE CORE 1
COMPUTE CORE 2
Functional BS
(PDN, clock, …)
I/O


SRAM 2
SRAM 1
Drive logic
Dense logic
Functional BS
(PDN, clock, …)
I/O
COMPUTE CORE 1
COMPUTE CORE 2

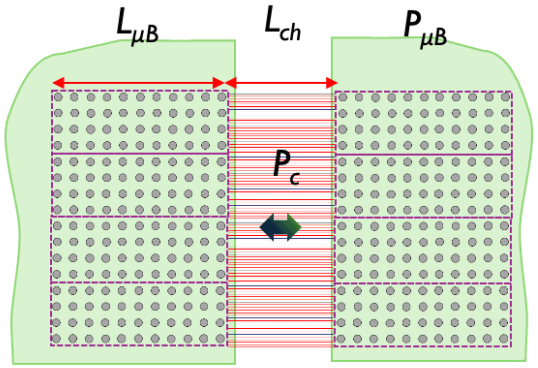
Heterogeneous integration as key enabler

Chiplets offer a modular system

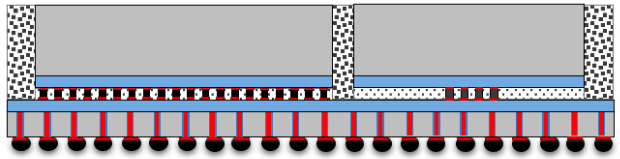


https://www.imec-int.com/en/articles/chiplets-piecing-together-next-generation-chips-part-i

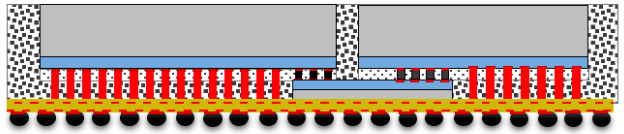
2.5D interposers

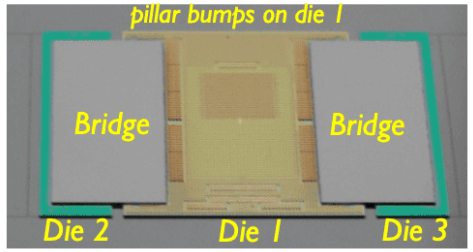


2.5D Si interposer

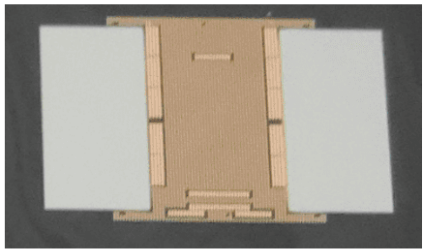


Fan-out WLP with embedded Si-bridge interposer

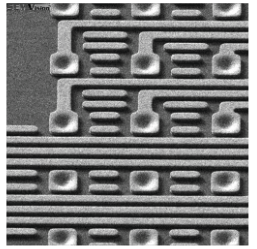




Die placement and bridge bonding

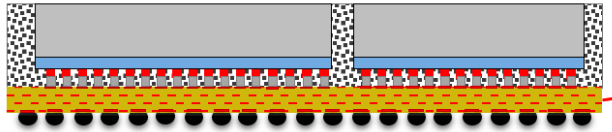


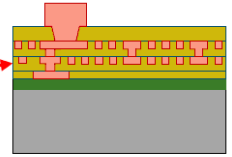
Post molding and back grinding



2 µm Line/Space
Semi-additive RDL

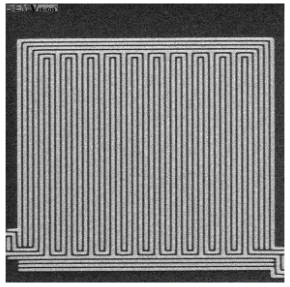
Fine pitch Cu/polymer RDL-first FOWLP



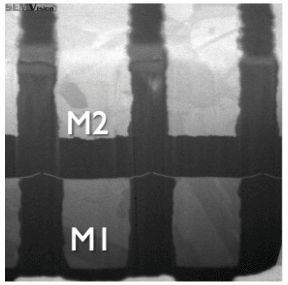


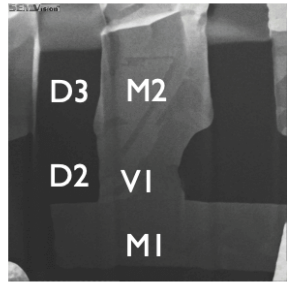
"Damascene"
RDL-first
on carrier wafer

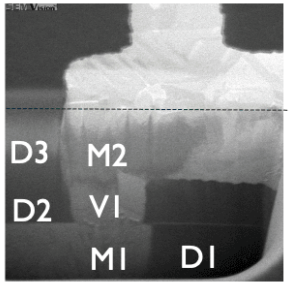
Line/Space scaling: 2 ⇒ 1 µm ⇒ 0.5µm



1µm Line/Space





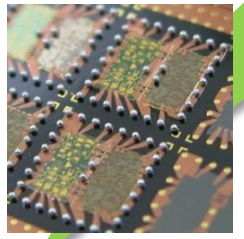


Multilayer Single and Dual Damascene metal integration

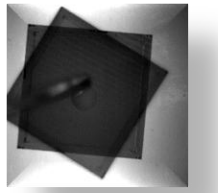
3D: from packaging to monolithic

TSV + µBump[1]
Pitch : 20 µm

~10³ 3DC/mm²
=> Entire core

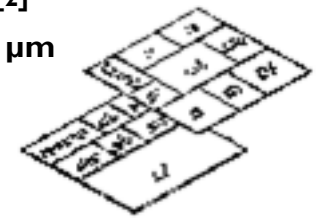


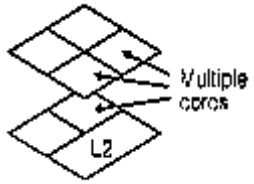
Self Assembly
Pitch : 1-5 µm



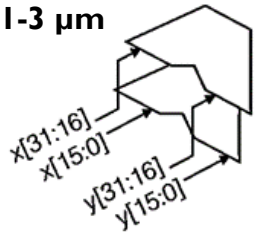
~10⁵ 3DC/mm²
⇒ Logic Blocs
⇒ Logic Gates

Cu/Cu [2]
Pitch : 2-5 µm



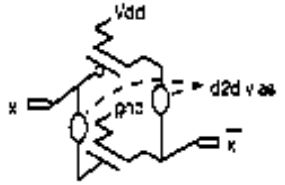


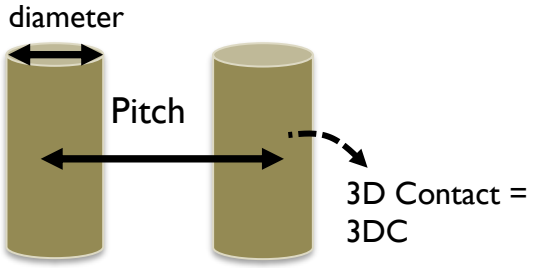
HD-TSV [2]
Pitch : 1-3 µm



M3D (CoolCube™) [3]
Pitch : 0.05-0.1 µm

10⁸ 3DC/mm²
=> Transistor level



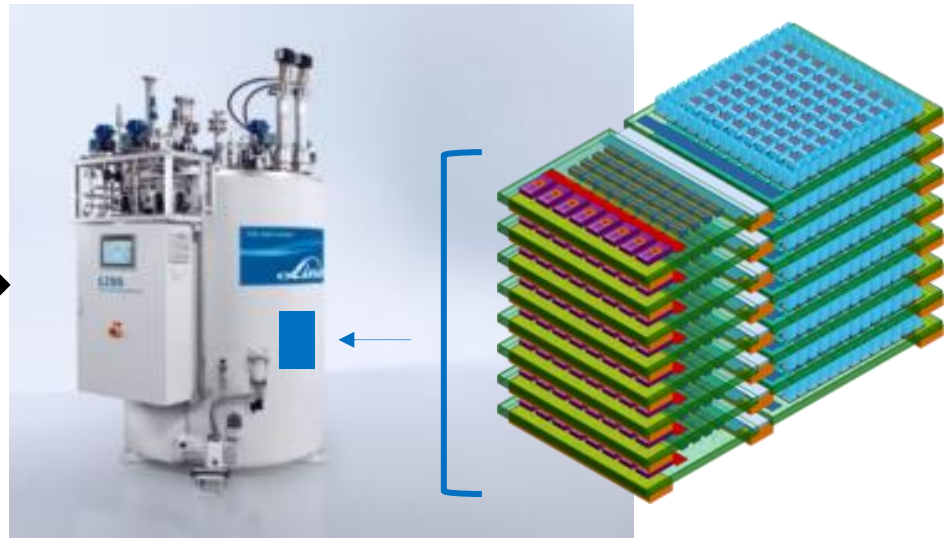


[1] Cheramy, S., et al. "Advanced Silicon Interposer", C2MI Workshop, 2015
[2] Patti, B., "Implementing 2.5D and 3D Devices", In AIDA workshop in Roma, 2013
[3] Batude, P., et al. "3DVLSI with CoolCube process: An alternative path to scaling ." VLSI technology symposium 2015

Making faster machines

Data center in a shoebox…

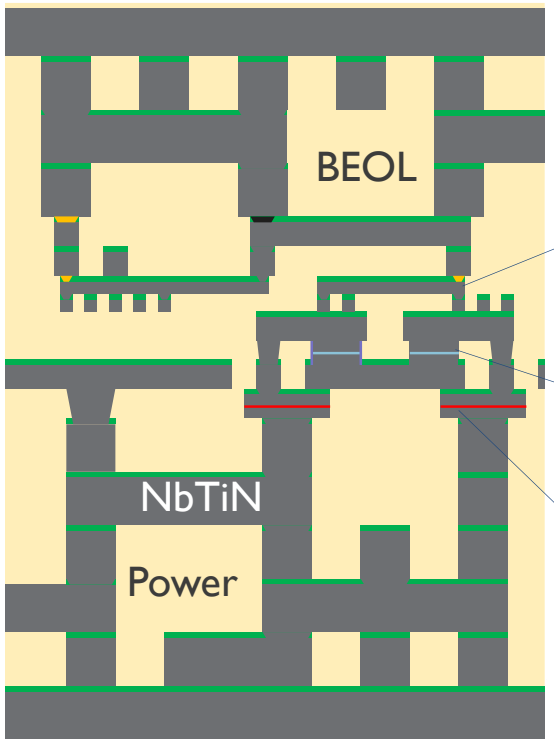
The same performance as NVIDIA EOS: 79.32 ExaFLOPS



18 Trillion devices 150 x 320 x 100 mm

Superconducting digital technology

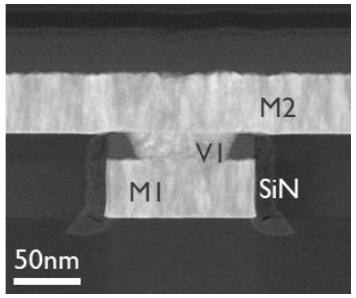
Production process vision



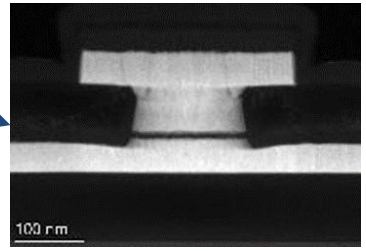
400 MJJ/cm^2 @ 30 GHz

16 Metal layers

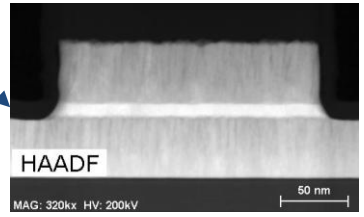
NbTiN wires & vias



NbTiN/aSi JJ



NbTiN/HZO/NbTiN cap



Imec 28 nm 300 mm SCD process

Only one new material, NbTiN

Fully compatible with CMOS process

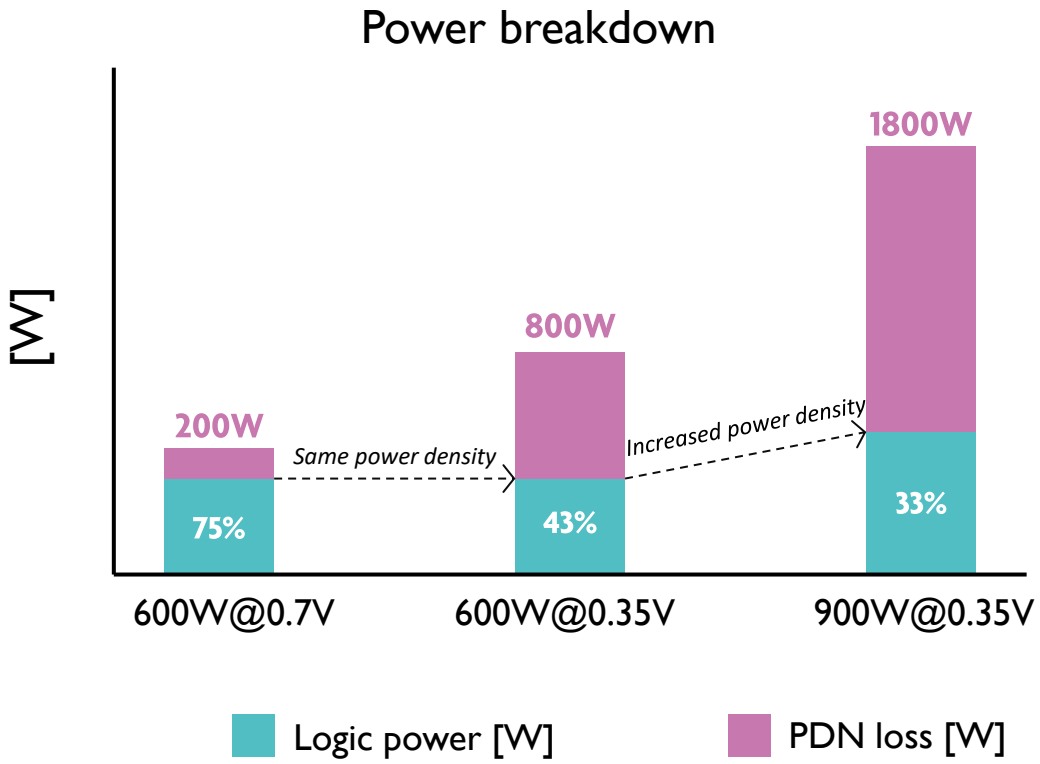
Computational density the same as 7nm CMOS

Compatible with Place & Route

A. Pohkrel et al., IEDM 2024 & 2025.

The power wall

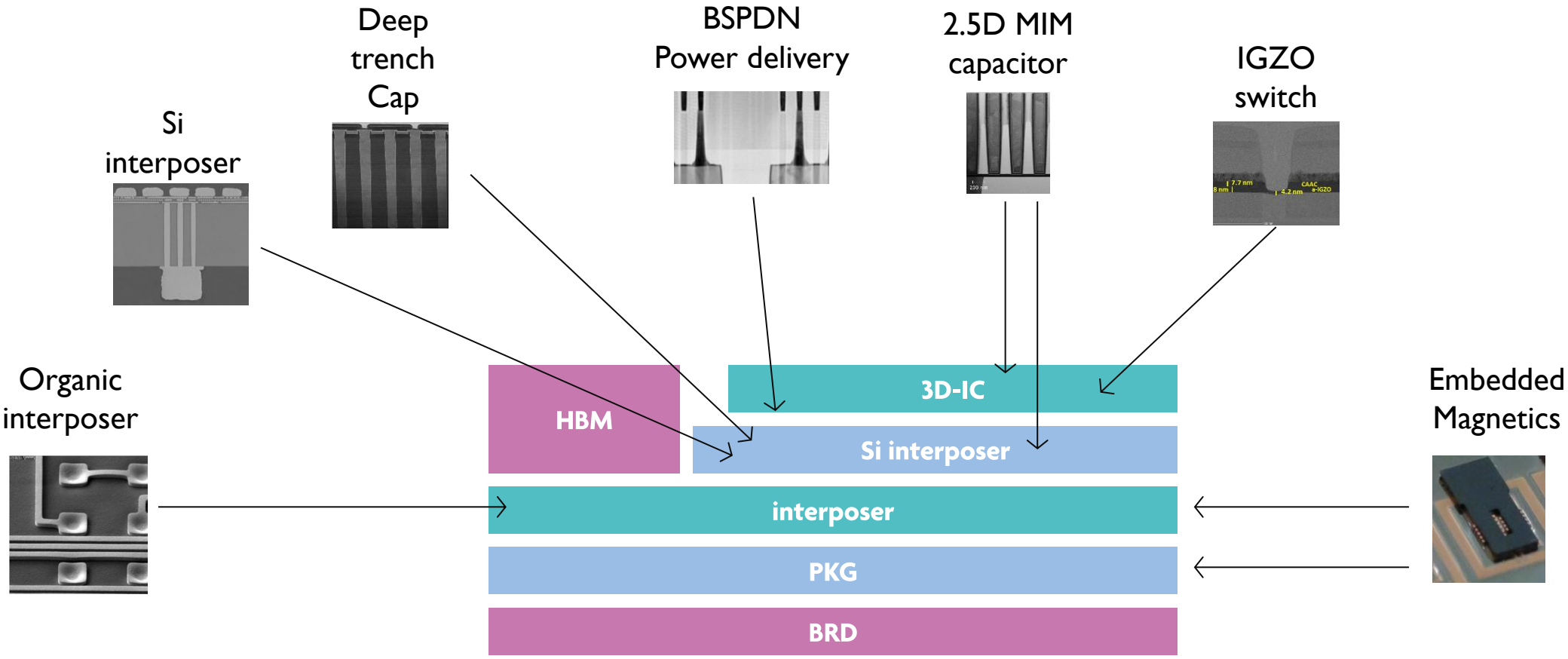
Power loss in PDN kills power efficiency of the system



[assumptions: 75% efficiency for reference PDN, halving Vdd & increasing power by 50% on same PDN]

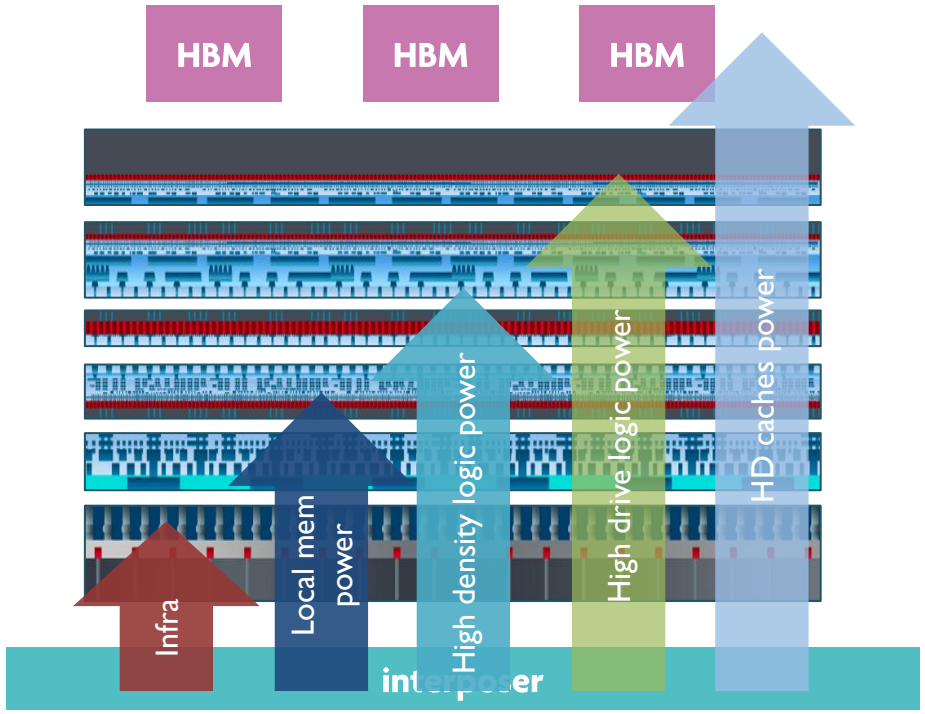
With the same power delivery network performance
the **Power Delivery Network (PDN) losses** will dominate when reducing V_{DD} and increasing Power

Technology for power delivery improvement

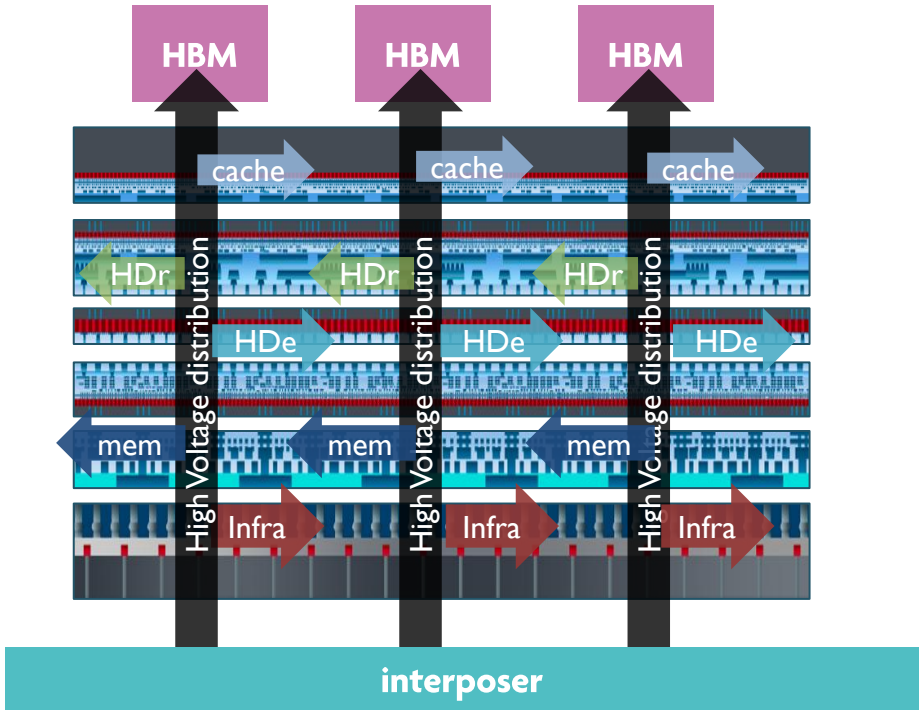


BSPDN=backside power delivery network

Bringing power conversion closer



Bring in voltage for each function from outside

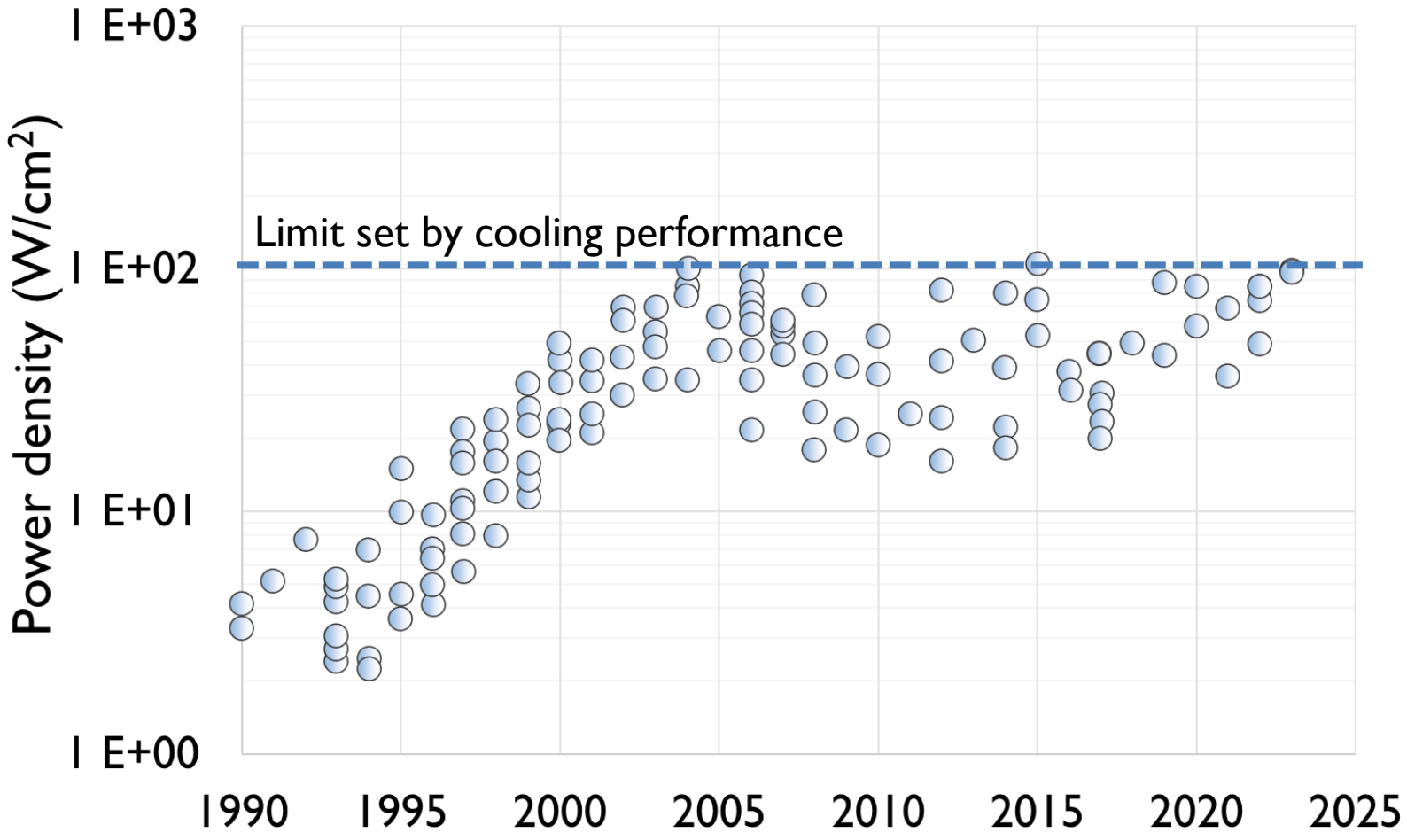


Locally generate voltage from HV distribution

Local down-conversion from main power could become more efficient

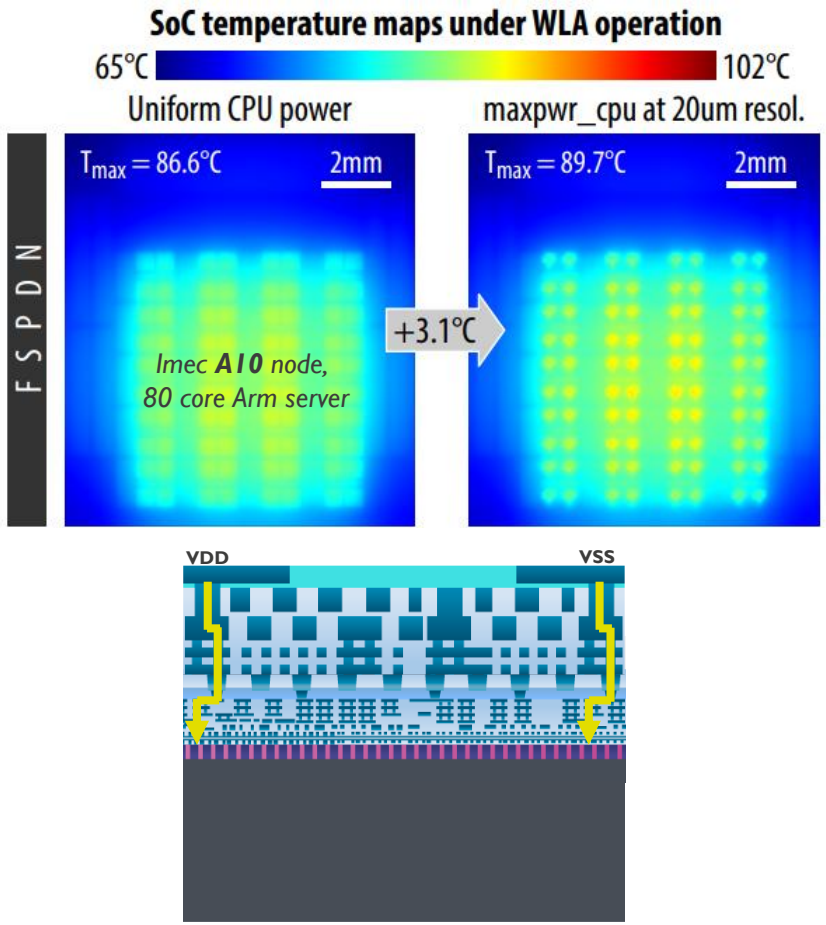
Thermal

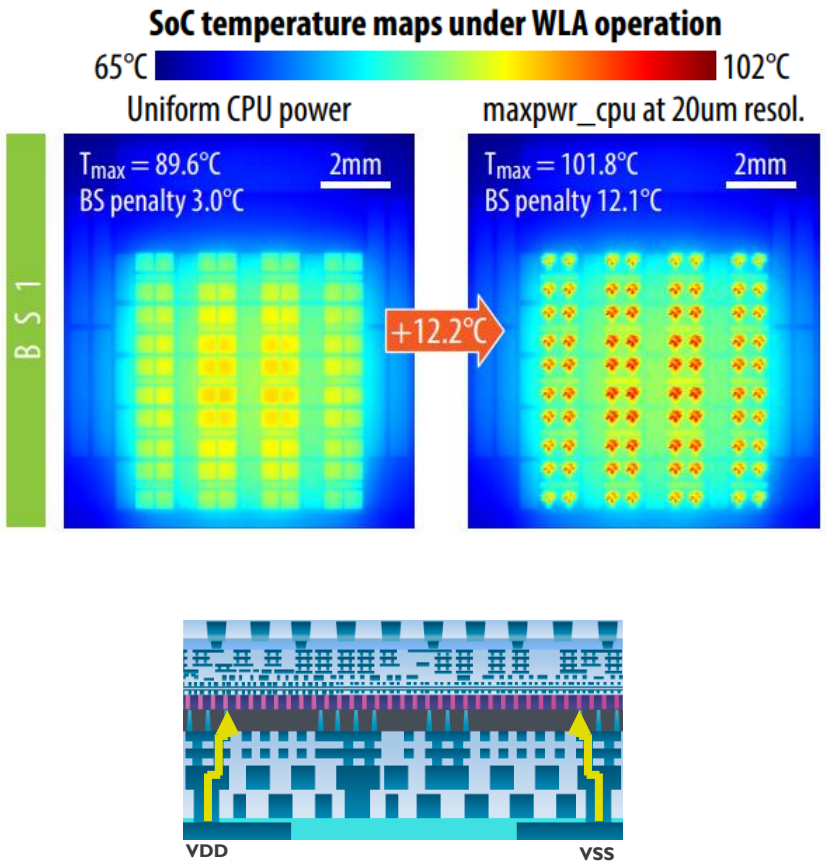
Cooling and Power Delivery Limit Chip Performance



Source: Michael L. Rieger, J. Micro/Nanolith. MEMSMOEMS18(4), (2019) and https://www.techpowerup.com/

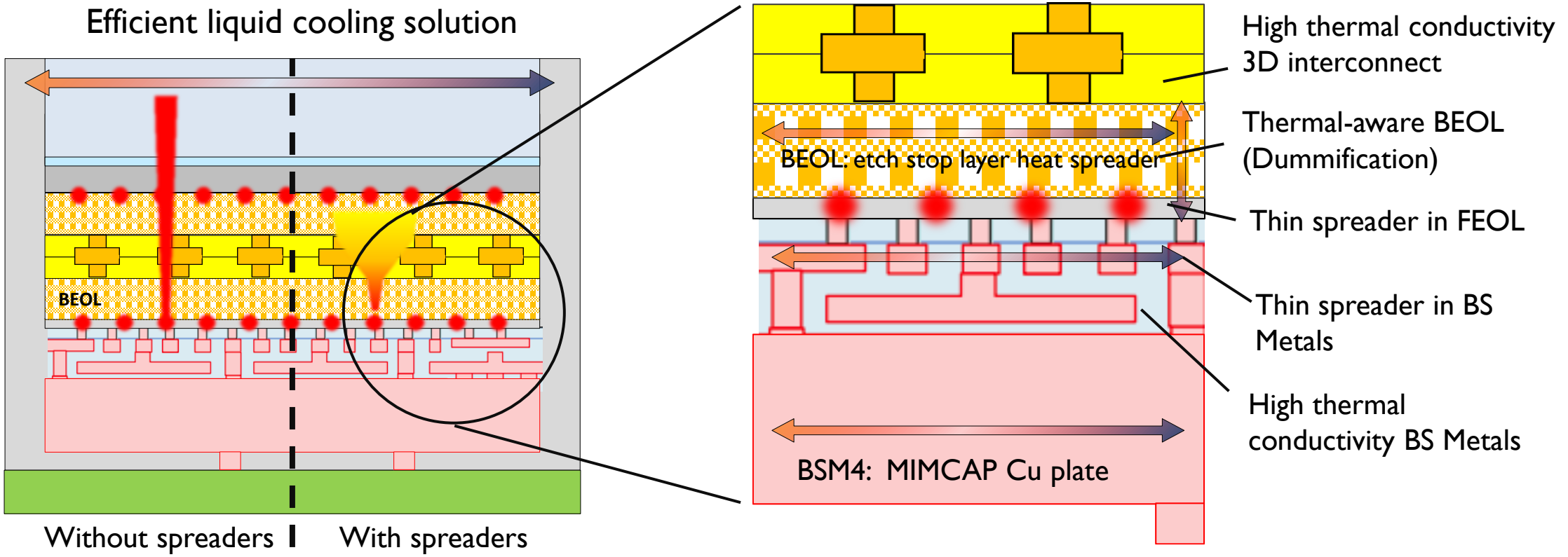
With BSPDN, hotspot size shrinks





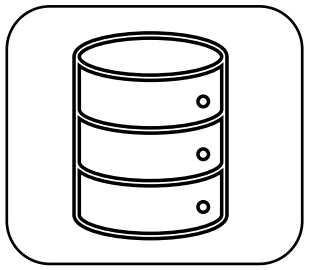
BSPDN increases lateral resistance, denser logic concentrates the power

Spreading the heat in 3D is key

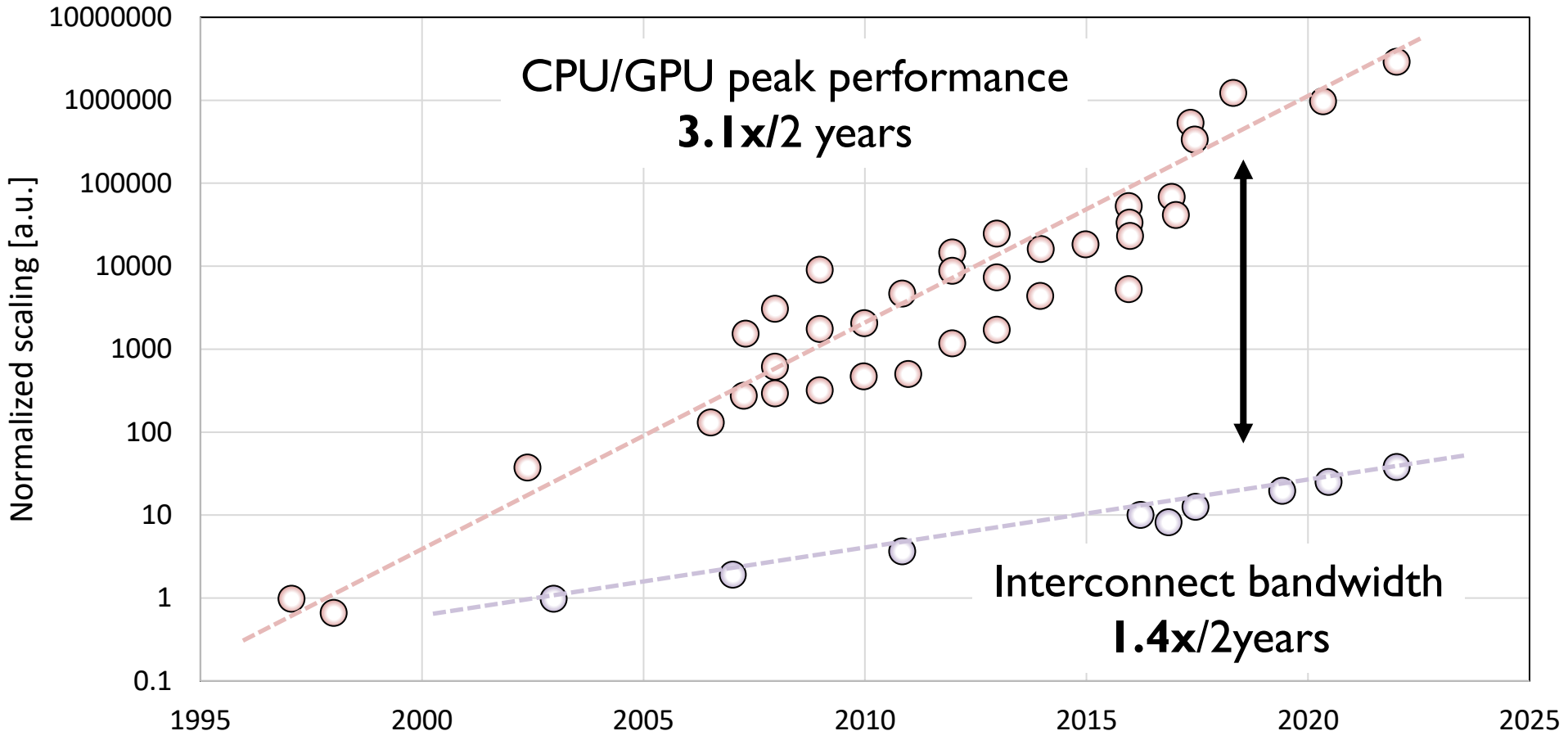


Memory

Compute performance increasing faster than memory interconnect bandwidth

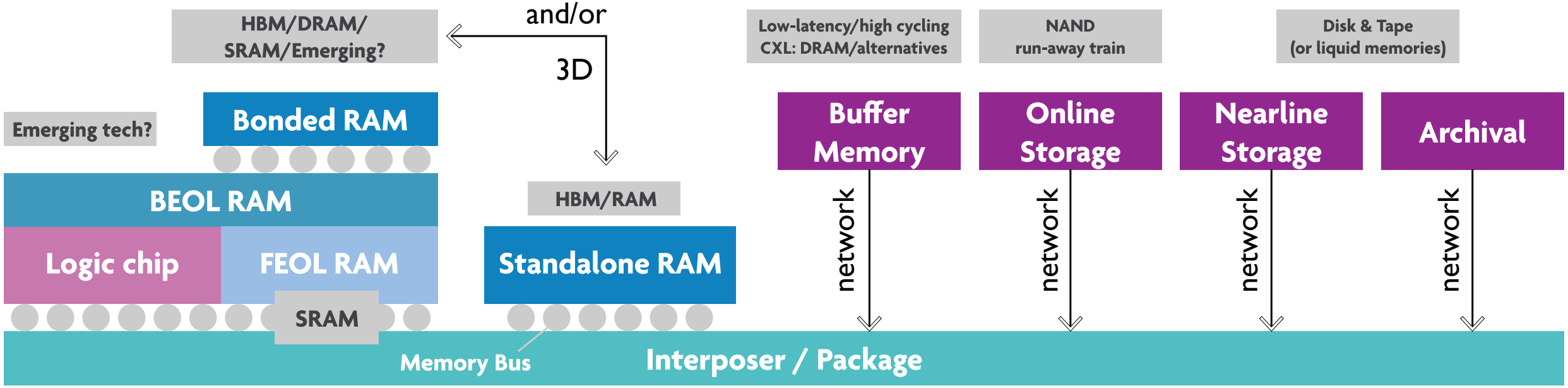


Memory wall



Amir Gholami, et. Al. "AI and Memory Wall", https://medium.com/riselab/ai-and-memory-wall-2cb4265cb0b8

System memory is a complex ecosystem

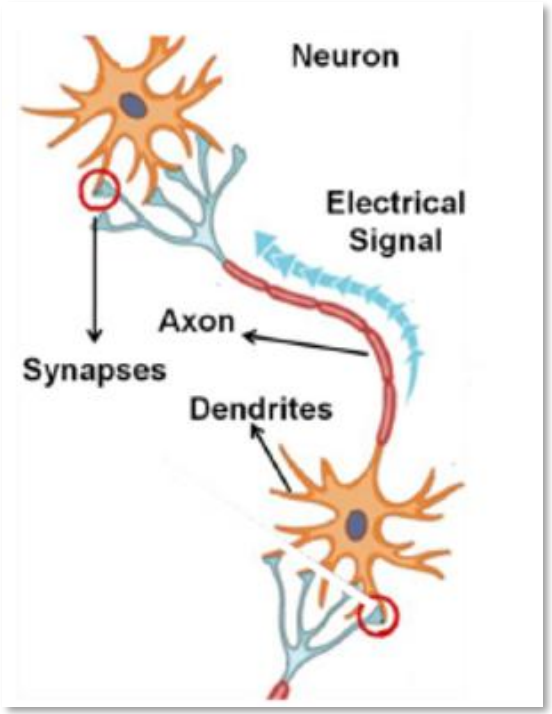


- AI is driving the HBM/DRAM growth.
- High-density, low-cost, non-volatile memory solution for both embedded (LLC) and stand alone are needed to keep the cost and power under control.

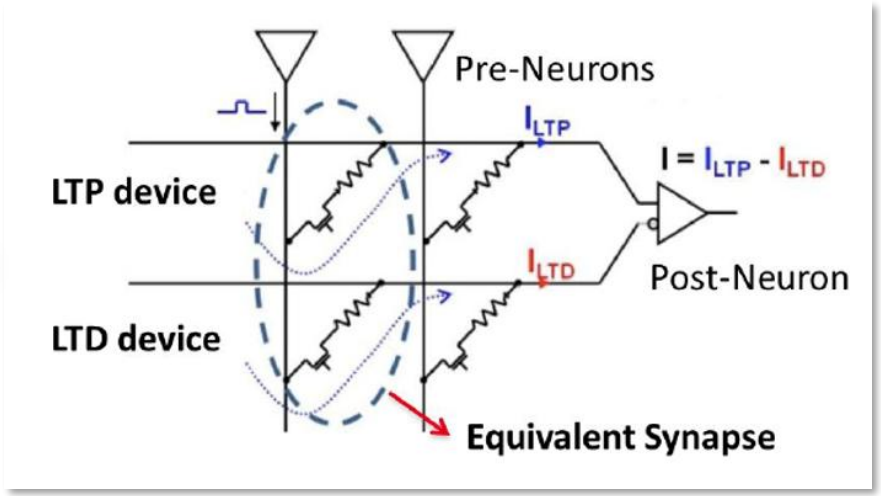
Beyond Von Neumann computing

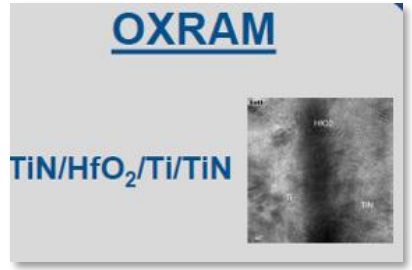
Neuromorphic based RRAM circuit

M. Suri et al, IEDM 2011.

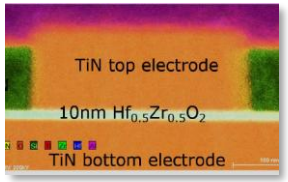


2 PCRAM Example:





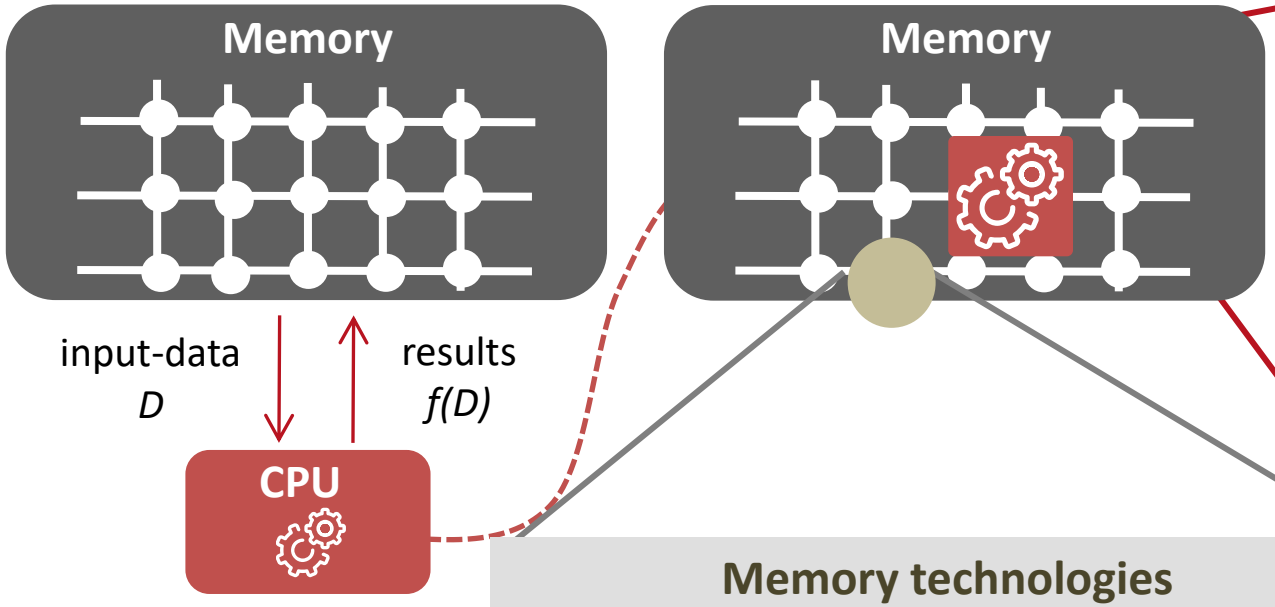
FeRAM

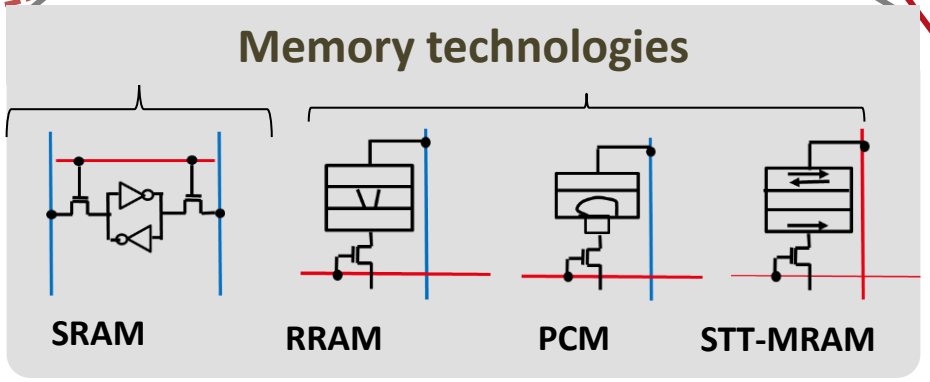


In memory computing

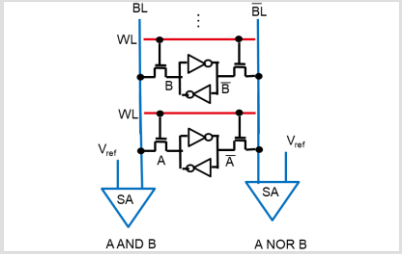
Von Neumann computing

In-memory computing

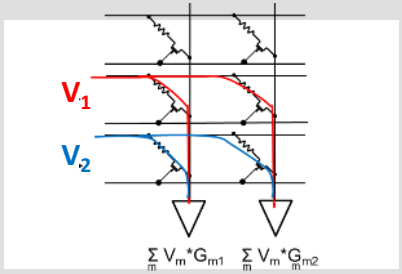




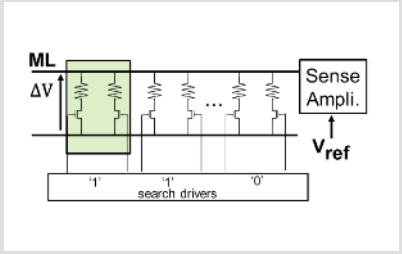
Logic and arithmetic operations



Digital operations using SRAM

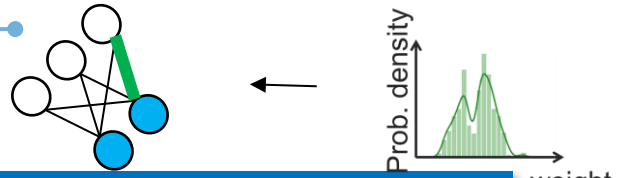


Analog: multiply and accumulate

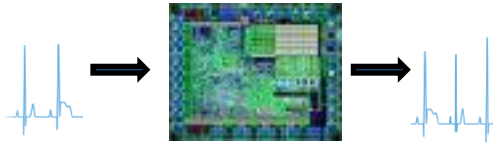


Searching / matching (CAM)

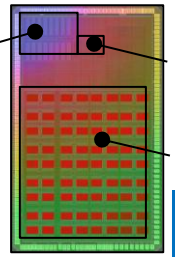
Near- & in-memory computing



Bayesian Neural Networks

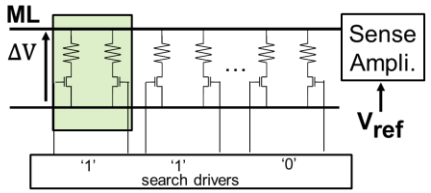


Spiking Neural Network



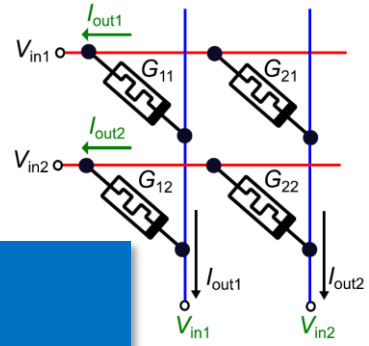
Energy-efficient NN accelerator

RRAM for near- and in-memory computing

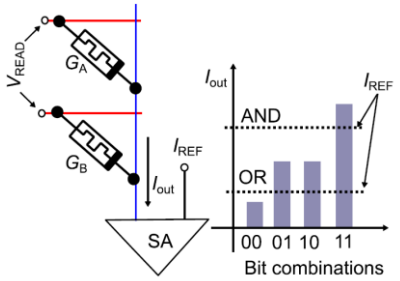


Search/match operations (CAM)

$$\begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} = \begin{bmatrix} b_1 \\ b_2 \end{bmatrix}$$

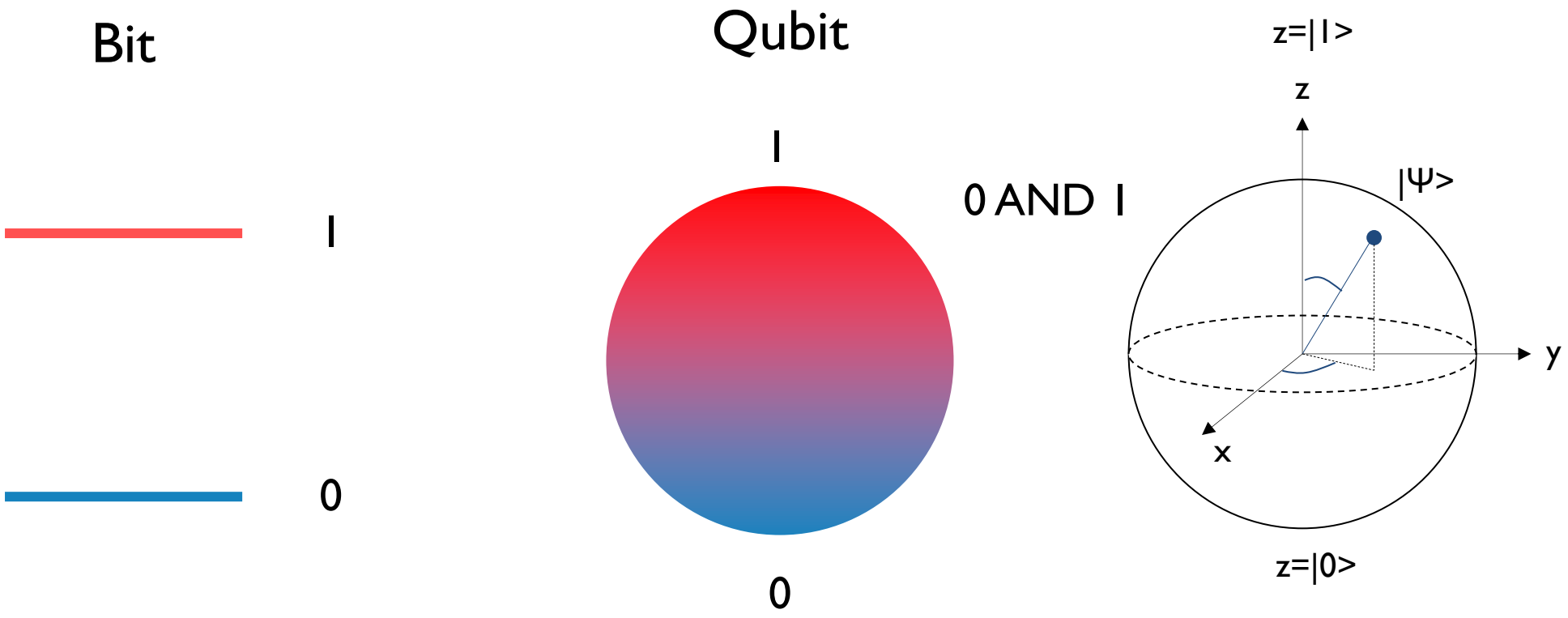


Deep learning, matrix-vector multiply

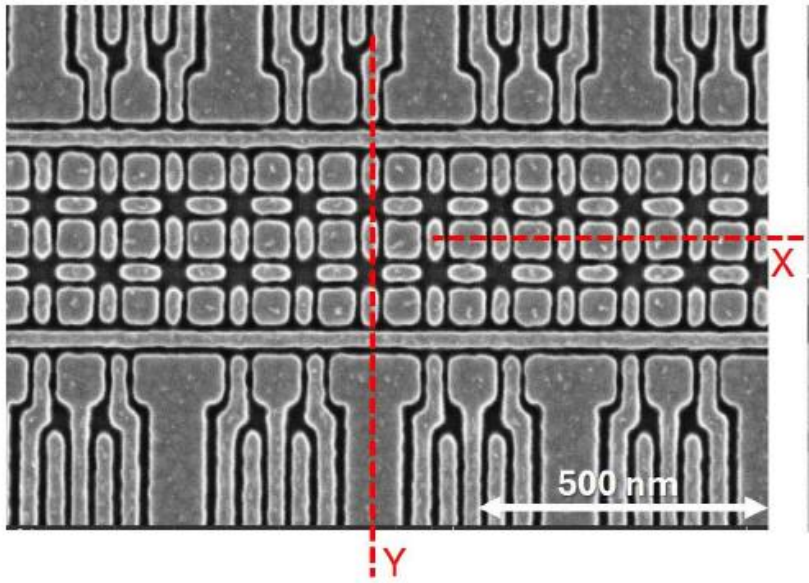


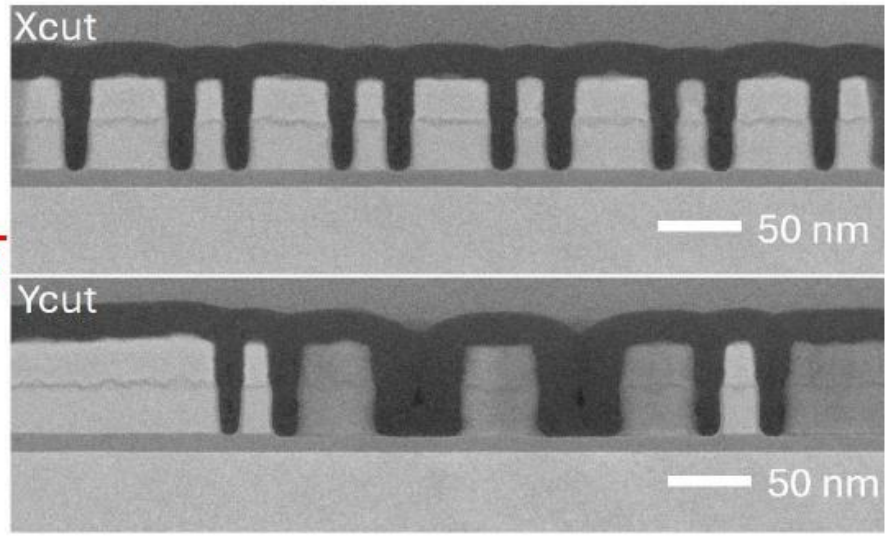
In-memory logic

From bits to qubits

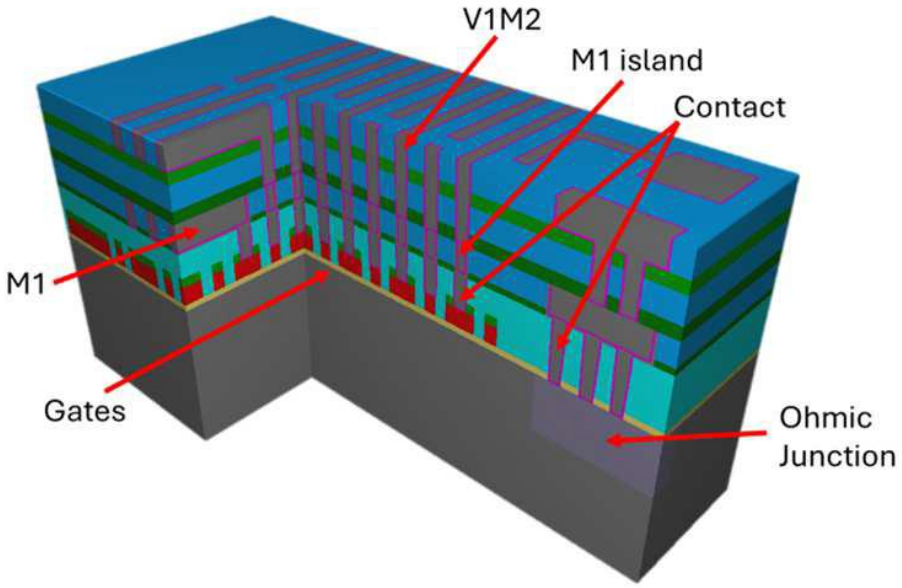


Quantum computing





S. Beyne et al., IEDM 2025.



300mm wafer fabrication of silicon spin qubit arrays using 0.33NA EUV lithography

Take-aways

Key take-aways

- AI-driven compute explosion is reshaping semiconductor priorities
- Heterogeneous integration and chiplet-based design are now essential for scaling performance and energy efficiency beyond monolithic approaches
- Advanced packaging technologies are no longer back-end processes but strategic enablers for advanced computation (as well as advanced functionalization)

Key take-aways

- Memory bandwidth and data movement bottlenecks are critical constraints; research into near-memory compute and processing-in-memory should be accelerated
- Energy and thermal management are decisive for future systems; advanced cooling and energy-aware design must be integrated early in system architecture
- Quantum technologies remain highly exploratory but still hold a lot of promise

Landscape mapping

Global landscape

- United States: CMOS scaling, semiconductor equipment, and compute architectures (Near-/In-memory computing); strongest coordination between industry and academia
- Taiwan: the global anchor for leading-edge foundry technology, chiplet manufacturing, and 2.5D/3D packaging
- South Korea & Japan: dominant in memory (HBM, MRAM), materials engineering, and back-end integration
- Europe: global leader in scientific excellence and pathfinding research (Advanced CMOS, BEOL innovation, 2D materials) but lacks high-volume industrial deployment and system integration

Recommendations

Country/Region	Ecosystem strengths	Potential partnership topics	Key benefits for the EU
United States	• Dominant in EDA, design & IP • CMOS scaling, MRAM, NMC/IMC • Strong equipment base	• Advanced packaging • Chiplet standards (UCIe) • AI-enhanced design • Collaboration with fabless	• Close tech gaps • Strengthen next-gen compute • Reduce dependency on East Asia

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Canada	• Leadership in quantum & photonics • Advanced packaging • Compound semiconductor R&D	• Quantum hardware • Photonics • Chiplet/UCIe • Logic-memory integration • Novel AI compute architectures	• Strengthen EU quantum & photonics • Improve packaging • Accelerate HPC

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Taiwan	• Global leader in advanced manufacturing • Full value chain • CoWoS/3D packaging	• Access to leading-edge nodes • 3D integration • Packaging & heterogeneous integration	• Close advanced-node gap • Speed up packaging innovation • Strengthen supply chain

Recommendations

Country/Region	Ecosystem strengths	Potential partnership topics	Key benefits for the EU
Japan	• Leadership in equipment & materials • MRAM, SiC/GaN, chiplets	• Materials (resists, interconnects, ferroelectrics) • Advanced memory • Heterogeneous integration	• Improve system integration • Close memory/material gaps • Strengthen resilience

Recommendations

Country/Region	Ecosystem strengths	Potential partnership topics	Key benefits for the EU
Japan	• Leadership in equipment & materials • MRAM, SiC/GaN, chiplets	• Materials (resists, interconnects, ferroelectrics) • Advanced memory • Heterogeneous integration	• Improve system integration • Close memory/material gaps • Strengthen resilience
Republic of Korea	• Leadership in DRAM, NAND, MRAM • 3D & panel-level packaging	• HBM • Near/in-memory • Neuromorphic & AI-EDA • Backend packaging	• Address memory weakness • Improve packaging • Support AI/HPC integration

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India	• Strong semiconductor design capacity • Large workforce • Growing packaging and manufacturing capabilities	• Chip design & verification • AI/ML optimization • Power electronics	• Accelerate design cycles • Expand talent pipeline • Improve resilience

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Singapore	• Advanced manufacturing and packaging capabilities • Diverse and mature industry cluster • Strong R&D and workforce excellence	• Advanced packaging & heterogeneous integration • Quantum technologies • AI-driven compute and edge architectures • Silicon photonics and optical interconnects	• Access to cutting-edge packaging and photonics technologies • Accelerate AI and quantum integration into advanced compute systems • Enhance energy efficiency and security in HPC and edge

THANK YOU

ICOS International Cooperation On Semiconductors

European Commission

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