Updated Technology Scanning and Foresight

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Executive Summary

This deliverable provides an updated, forward-looking view of future and emerging technologies across advanced computation and advanced functionality, building on D3.1–D3.3. It synthesizes recent roadmaps and expert inputs to reassess technological maturity, strategic relevance, and Europe's positioning. The analysis combines desk research on international and European sources with consortium expertise to ensure alignment with the latest trends and priorities.

Key messages for advanced computation: AI workloads are reshaping system design; performance is now limited by memory bandwidth, data movement, and energy/thermal constraints more than transistor density. The industry momentum is toward chiplet-based architectures, 2.5D/3D stacking, hybrid bonding, near/processing-in-memory, and optical interconnects/CPO. Device scaling continues (e.g., CFET, backside power delivery), but system-level co-optimization of compute, memory, interconnect, power, and cooling is becoming key. Quantum technologies remain exploratory.

For advanced functionality, innovation is strong in sensors (heterogeneous integration and in-sensor AI), energy harvesting & storage (sustainability, flexible integration, micro-power management), power electronics (WBG/UWBG with heterogeneous integration and pilot-line scale-up), wireless (incremental FR3 evolution, NTN/TN convergence), and photonics (silicon photonics scaling for datacenter interconnect).

Across all domains, both compute as well as functionalization, advanced 3D/packaging emerges as a strategic enabler bridging devices to systems and accelerating modular ecosystems.

Finally, a consolidated landscape mapping highlights Europe's strong research position but also persistent gaps in advanced manufacturing, packaging, and design capabilities. By comparing strengths across major global regions, the analysis identifies where targeted international cooperation, especially in advanced packaging, memory-centric compute, photonics, and More-than-Moore functionalities, can most effectively accelerate Europe's technological and industrial competitiveness.

1 Overview

1.1 Introduction

The purpose of this deliverable is to provide an updated overview of future and emerging technologies, with a particular focus on newly emerged paradigms across Advanced Computation and Advanced Functionality. Building on the analysis presented in the previous deliverables (D3.1, D3.2, D3.3), this report reviews and updates relevant international and European roadmaps, catalogues next-generation and emerging technologies, and refines the assessment of their expected impact. The deliverable further complements the previous quantitative and qualitative evaluations of European and non-European strengths and

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weaknesses, offering an updated perspective on technological progress, strategic positioning, and potential opportunities for Europe in key areas of advanced technology development.

1.2 Evaluation methodology

The methodology applied in this deliverable builds upon the structured analytical framework established in the previous deliverables. It combines systematic desk research, comparative analysis of international and European strategic roadmaps, and expert input from the consortium and its partner network.

The process began with the identification and review of updated and newly published roadmaps, reports, and strategic documents covering Advanced Computation and Advanced Functionality domains. These sources include major international initiatives, industrial alliances, and research roadmaps (e.g., IRDS, ECS-SRIA, and domain-specific CSAs), which were analysed to identify emerging technological paradigms and evolving priorities.

To complement the desk research, expert consultations and internal brainstorming sessions were conducted to validate findings, ensure consistency with ongoing technological trends, and capture new developments not yet reflected in formal publications. Quantitative and qualitative assessments were then updated to reflect changes in technological maturity, industrial relevance, and strategic importance, with particular attention to Europe's positioning relative to other global regions.

The resulting synthesis provides a coherent and forward-looking view of emerging technologies and their expected impact, supporting strategic recommendations for research and innovation in the coming years.

2 Future technologies for Advanced Computation

2.1 Trends

Since their industrialisation six decades ago, semiconductors have transformed society at a pace few technologies can match. Without semiconductor chips, modern consumer electronics, transport systems, energy grids, health-care infrastructure and the financial sector simply couldn't operate. What may look like "business as usual" today is in fact underpinned by a relentless cycle of advanced research and innovation in device, circuit, system and packaging technologies.

In the first two decades of the 21st century the dominant drivers of semiconductor innovation were laptops, desktops, datacentre servers, mobile and entertainment devices. But now we are entering a markedly different era: one defined by digital-physical convergence (Industry 4.0), ubiquitous sensors and connectivity (IoT), autonomous systems, and above all by the pervasive role of artificial intelligence (AI) and machine learning (ML). Semiconductors are foundational to these emerging innovations.

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Below we highlight major trends shaping the advanced-computation domain, with particular relevance to AI-driven compute, scaling, energy and memory/thermal constraints.

The AI driving compute explosion

- AI and ML workloads have triggered a surge in compute demand: training and inference of deep neural networks now dominate many advanced-computation systems.
- The scale of the models is growing rapidly (e.g., models with over a trillion parameters), meaning that compute requirements are rising by orders of magnitude compared to conventional workloads.
- This shift places distinct demands on architectures: massive throughput for parallel operations (e.g., matrix multiplications, tensor operations), high-efficiency accelerators (ASICs, FPGAs, neuromorphic), and system-level orchestration across many compute units.

The need for increasing compute, scaling and heterogeneous integration

- The end of "free" transistor scaling and barrier of Dennard scaling has shifted the emphasis from pure transistor density to heterogeneous architectures, multi-chip assemblies, chiplets, and advanced packaging.
- 3D heterogeneous integration, where logic and memory or multiple die types are stacked and interconnected, is emerging as a key enabler of performance and energy gains by shortening interconnects, improving bandwidth and reducing latency [1].
- To meet the ever-higher compute demands (driven by AI), scaling must be achieved not just in individual chips, but in system architecture: integrating CPUs, GPUs, accelerators, memory subsystems, interconnects and co-packaged fabric in a modular and heterogeneous fashion [2].
- Heterogeneous integration also supports functional diversification: different kinds of processing blocks (general-purpose, vector, tensor, neuromorphic) can co-exist, increasing flexibility and efficiency.

Energy efficiency, thermal and power constraints

- As compute grows, energy and thermal limits become key constraints. Scaling simply by adding more chips or circuits is no longer viable if the power or cooling demands are prohibitive.
- Energy consumption of memory and data movement is increasingly dominating the system power budgets. For example, in AI-centred systems the cost of moving data between memory and compute can exceed the cost of the computation itself [3].

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- Thermal issues further complicate packaging and integration: stacked architectures and high-density systems must manage heat effectively. Otherwise, thermal throttling, reliability or yield issues may arise.
- Efficiency trends (such as described by Koomey's law) have slowed, meaning that energy per computation is harder to reduce at the same rate as earlier generations.
- Hence, energy-aware architectural decisions (such as near-memory compute, low-power accelerators, dynamic power/voltage scaling) are critical.

Memory bandwidth and data movement bottleneck

- One of the most acute bottlenecks in advanced computation is memory bandwidth and the cost of moving data. As compute capacity grows dramatically, memory and interconnect systems struggle to keep pace [3].
- The so-called "memory wall" or "Sun-Ni law" describes how memory access speeds and bandwidth increasingly limit system performance when compute grows.
- Emerging workloads, especially AI/ML, demand very high memory bandwidth and very low latency, both within the chip/package and across the system. The power cost of DRAM access, refresh and data movement is substantial [4].
- To address this, approaches such as processing-in-memory (PIM), near-memory compute, and architectural re-balancing of memory/computation hierarchy are gaining traction [5].
- In the context of heterogeneous integration, stacking memory and logic (3D memory stacks, HBM, logic on interposer) shortens the data path and increases usable bandwidth per watt [5].

System-level scaling and architecture

- As compute, memory and data-movement demands are increasing, systems are evolving beyond monolithic chips to modular building blocks: chiplets, disaggregated resources, fabric interconnects, and heterogeneous nodes.
- CPUs, GPUs, DPUs (data-processing units), specialized AI accelerators, memory modules, and interconnect fabrics all might be co-packaged or networked in a flexible architecture [6].
- The design of interconnects (on-chip, package, board, datacenter) becomes critical: bandwidth, latency, coherency, power and thermal coupling all need to be managed. Moving from copper-based interconnects to optical interconnects, even at short distances, is a trend that likely will continue and accelerate.

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- Data movement is increasingly the design limiter rather than raw compute: one recent commentary states that “data movement, not compute, has become the limiting factor for performance and energy efficiency in complex SoCs” as already mentioned before.
- Modular ecosystems enable easier upgrade, heterogeneity, and optimisation of each block for its role (e.g., inference accelerators vs training accelerators vs general compute). This allows better match between workload and hardware, improving efficiency and cost-effectiveness.

In summary, AI-driven computation is pushing the limits of existing semiconductor architectures, challenging long-standing design paradigms and exposing fundamental bottlenecks. To sustain progress in performance and efficiency, innovation must increasingly focus on heterogeneous integration, advanced packaging, and the scaling of memory and bandwidth capabilities. Minimising data movement and adopting energy-aware design principles are becoming central to achieving balanced system performance. Today, memory and interconnect limitations represent some of the most critical constraints, surpassing transistor density as the dominant factor shaping overall computational efficiency. The future of advanced computation therefore depends on the synergy between all elements of system architecture: compute, memory, interconnect, power, and thermal management must be co-optimised rather than treated in isolation. For Europe, as for other global regions, maintaining competitiveness will require a comprehensive full-stack approach encompassing devices, chips, packaging, systems, interconnects, and software, particularly in light of the escalating demands imposed by AI-centric and high-performance computing workloads.

2.2 Challenges and innovations

As mentioned in the previous sections, Advanced computation is now constrained not by any single device metric but by a set of interdependent system-level limits. As AI workloads scale, the industry faces four tightly coupled challenges, compute density, memory density and bandwidth, thermal and power management, and fabric/connectivity, each of which is already the subject of intense academic and industrial research.

First, compute density continues to rise as AI training and inference drive ever larger models and higher throughput. However, simply increasing the number of processing elements per unit area is no longer viable: limits in power delivery, heat removal, yield, and interconnect overheads make further monolithic scaling inefficient and costly. To overcome these barriers, the industry is shifting toward heterogeneous, modular architectures, combining chiplets, disaggregated dies, and 2.5D/3D stacking, that allow each function to be independently optimised while achieving high overall system density.

This paradigm shift, often referred to as *CMOS 2.0* [7] Figure 1, extends beyond traditional system-on-chip concepts by embedding heterogeneity directly into the CMOS platform. Through advanced 3D interconnects, backside technologies, and layered logic, CMOS 2.0 aims to enhance system-level performance rather than merely increasing transistor counts. A key

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enabler of this evolution is the backside power delivery network (BSPDN), which relocates power rails to the wafer's backside [8]. This approach reduces IR drop, frees routing resources on the frontside, and decouples power from signal distribution, critical benefits for dense stacked logic and multi-tier systems. BSPDN will be introduced at the first nanosheet technology nodes and is expected to play a central role in sustaining compute utilisation in future chiplet-based designs.

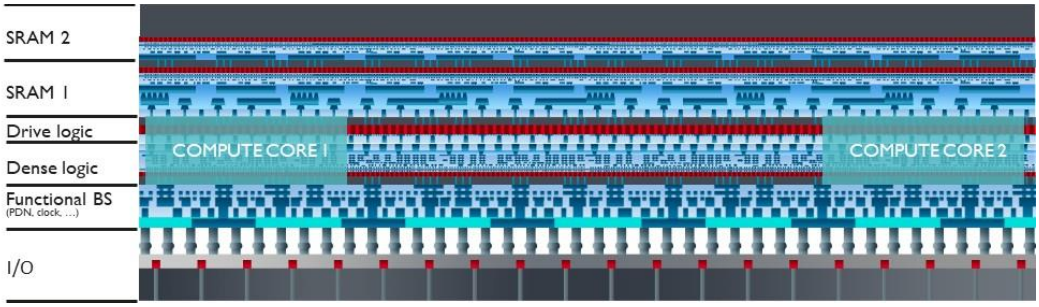

Figure 1 : Schematic presentation of CMOS 2.0, functionalities are partitioned over different tiers at a much finer granularity than typical 3D integration.

At the packaging level, fine-pitch hybrid bonding and chiplet ecosystems are rapidly maturing into mainstream solutions. Hybrid bonding enables true 3D stacking with much finer interconnect pitch and lower parasitics than micro-bumps, delivering higher bandwidth, lower energy per bit, and improved yield. In parallel, the modularisation of chiplets, supported by emerging interface standards, is being advanced by major industrial players and consortia as a means to integrate best-in-class IP blocks, reduce time-to-market, and tailor architectures for specific workloads such as AI training or inference.

In parallel, the concept of *software-defined silicon* is gaining traction. Here, hardware resources, such as chiplets, accelerators, and memory tiles, are dynamically composed and managed by software. This approach enables workloads to be allocated to the most energy- and performance-efficient hardware resources, making the software stack an integral part of hardware efficiency. Hardware–software co-design is thus becoming essential to fully exploit the benefits of heterogeneous systems.

While integration and packaging dominate current innovation, transistor scaling continues at the device level. Complementary FETs (CFETs), which vertically stack n- and p-type transistors within a single cell, represent a promising path for continued logic density scaling beyond nanosheet nodes (Figure 2). Early research indicates that CFETs could significantly reduce standard cell height and logic area, though they introduce new challenges in thermal management, back-end integration, and via formation.

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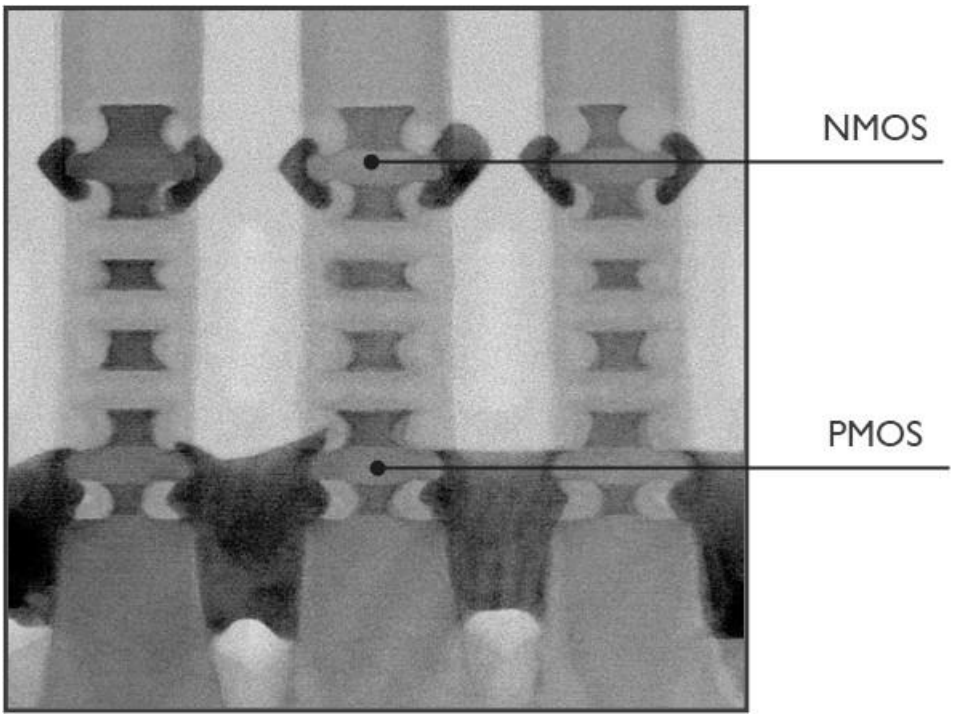

Figure 2: TEM picture of a CFET device, stacking pMOS and nMOS on top of each other.

Second, memory density and, crucially, memory bandwidth are major bottlenecks for AI. Modern accelerators can execute huge numbers of operations per second, but performance and energy efficiency are increasingly limited by the rate at which weights and activations can be supplied to the compute units. This "memory wall" has elevated data movement into the critical path: moving data between DRAM and accelerators, and across chips and racks, often costs more energy and time than the arithmetic itself. To address this, several research and commercial streams are gaining traction, including wide-interface high-bandwidth memories (HBM), near-memory and processing-in-memory (PIM) approaches that perform computation where the data reside, and re-architected memory hierarchies tailored to tensor workloads. These techniques aim to shrink the energy and latency cost of data movement and to rebalance system performance around bandwidth per watt rather than raw FLOPS alone.

Third, thermal and power constraints are a decisive limiter on practical scaling. Dense compute and stacked integration concentrate heat and create hotspots that degrade performance, reliability and lifetime. At datacenter scale, the total energy draw of AI workloads creates sustainability and cost pressures. This has pushed the rapid development of thermal management technologies and system-level power strategies like direct liquid cooling and immersion techniques for racks and modules, microfluidic cooling integrated at the die or package level, dynamic power management and volt-frequency control, and architectural approaches that reduce the energy cost of data movement. Research into optimized cooling media, microchannel geometries and AI-driven thermal control is ongoing because improved cooling enables higher sustained utilization of dense systems and therefore better energy efficiency per unit of useful work.

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Fourth, the fabric that connects compute and memory, on-chip networks, package interposers, board traces and data-center fabrics, must scale in bandwidth, latency and energy efficiency. Traditional copper links and electrical I/Os are increasingly strained at the densities and distances required by modern AI clusters; as a result, co-packaged optics, silicon photonics and other advanced interconnect paradigms are being explored to deliver orders-of-magnitude higher aggregate bandwidth with lower energy per bit. At the same time, new coherence and memory-sharing protocols (e.g., CXL and future fabric standards), as well as data-processing units (DPUs) and smart NICs that offload data-movement tasks, are being deployed to reduce the burden on host processors and simplify system orchestration. These fabric innovations are essential because even the most advanced compute and memory blocks cannot perform if the interconnect cannot feed them data at sufficient rate and latency [9].

Taken together, these challenges form a tightly coupled optimisation problem. Improving compute density without commensurate gains in memory bandwidth or cooling simply shifts the bottleneck; boosting interconnect bandwidth without addressing energy per bit or memory organisation can expose limits elsewhere. Consequently, research and industrial efforts are converging on full-stack solutions: co-design of algorithms, system architectures, packaging and cooling; adoption of modular heterogeneous building blocks that can be reconfigured for training versus inference; and exploration of new device and interconnect technologies that change the trade-space for data movement and energy. The most promising advances, from PIM and HBM to chiplets, co-packaged optics and advanced cooling are all driven by the recognition that system-level co-optimisation is the only viable path to meet the scaling, energy and latency demands of modern AI workloads.

2.3 New compute paradigms: Quantum technology

Quantum technologies are also seen as the next wave to renew the computation approach. Various technologies are investigated today, as illustrated in the Figure 3 below. Each of the technologies have advantages and drawbacks, but it is clear that all of them need to be scaled up in order to be able to achieve a computational power compatible with the demand (few millions of Qbits). Today superconducting Qbit is the technology that enables the first quantum computers, but silicon-based Qbits and photonic Qbits could become the successful technologies as they could provide the right compromise between scalability, performance and manufacturability. While progress has been made, today the choice is still open and many research entities are working towards the technological challenges.

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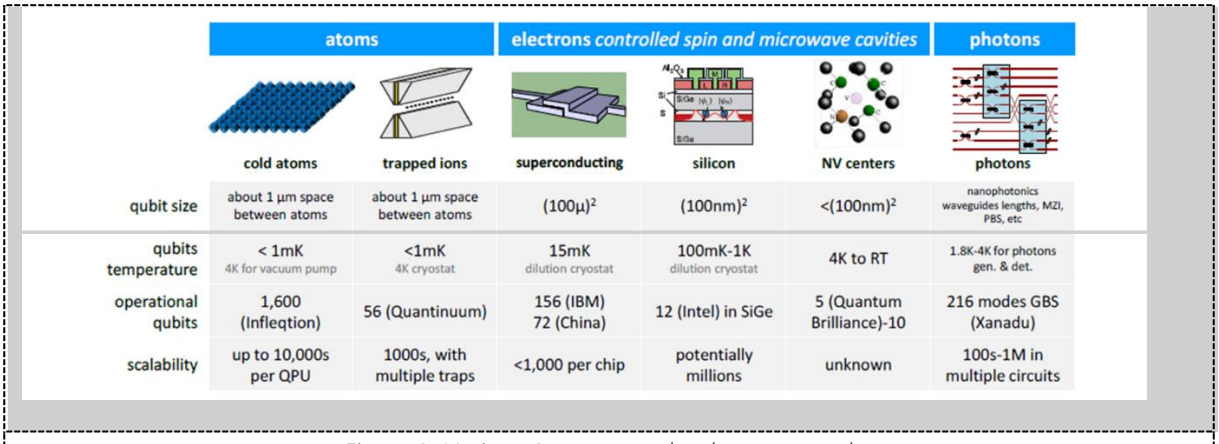

Figure 3: Various Quantum technology approaches

3 Future technologies for Advanced Functionality

3.1 Introduction

In this section, we will cover the emerging trends, challenges and innovations across following advanced functionality tracks:

- Sensor technologies
- Energy harvesting
- Power devices
- Wireless communications
- Photonics

3.2 Trends, challenges and innovations across the different tracks of advanced functionalities

3.2.1 Sensor technologies

By integrating various components at the package level, HI reduces the overall footprint and improves system reliability and efficiency. In particular, it allows designers to optimise each component using the most suitable fabrication technology, achieving higher performance metrics compared to traditional approaches. An interesting analysis is done in [10] [11], where the advantage of integrating Artificial Intelligence (AI) into vision pipelines can be an important improvement for applications ranging from autonomous vehicles to mobile devices, where leveraging HI technologies [12] it is possible to address the bottleneck between image capture and CNN processing. In [12] is described how photodetectors, pixel front-end circuits, analog mixed-signal and digital processors, and memories can be integrated more efficiently, as shown in Figure 4, where the image sensor architectures will further evolve in the future to expand the functionalities through device stacking technology.

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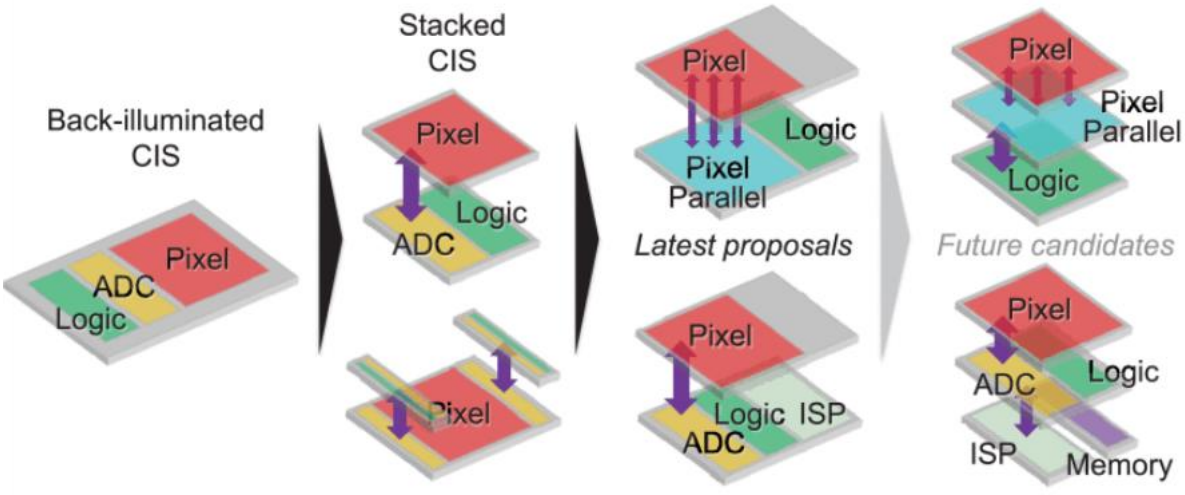

Figure 4: Prospects of the evolution of stacked CMOS image sensors, from [12].

One of the most significant advantages of HI applied to sensing systems is its ability to enhance sensor signal quality. By placing signal processing elements closer to the sensing components, the system can reduce noise and achieve better data accuracy. Furthermore, this approach facilitates the development of multifunctional sensor systems capable of simultaneously detecting multiple parameters, such as temperature, pressure, and humidity. Such integrated systems are particularly valuable in IoT applications where space and power efficiency are critical [13]. HI is nowadays leveraging what is defined as In-Sensor-AI-Computing (ISAIC). This emerging field, as described in [14], can combine real-time data acquisition and processing that can be achieved as soon as data are acquired, within the same package, thus reducing latency and minimising the need for extensive data transmission to cloud systems.

Concerning chemical and biochemical sensors the following future challenges are:

- Materials and process compatibility: different materials (2D TMDs, perovskites, MOFs, polymers, CMOS metals) often require incompatible thermal budgets, solvents and surface chemistries, complicating wafer-scale integration and backend processing. Process needs to be developed and optimised for large scale integration
- Interface stability and reliability: long-term chemical/biological exposure, moisture, and electrochemical reactions cause delamination, corrosion, or drift at heterogeneous interfaces (metal/organic/2D/bio). Suitable packaging approaches will be necessary.
- Biofouling and functionalization durability: maintaining selective biological recognition (antibodies, aptamers, enzymes, molecularly imprinted polymers) while preventing nonspecific adsorption and ensuring shelf-life is difficult for integrated devices. Work is required to extend shelf life and operational lifetime particularly during deployment in harsh environments.
- Signal transduction limits and noise: integrating ultra-sensitive transducers (FETs graphene/TMDs, electrochemical electrodes, plasmonic, SERS) with CMOS readout requires low-noise, low-leakage interfaces and possibly shielding to preserve SNR at small footprints. During deployment, particular emphasis must be placed on the

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interface between the sensor and analogue front end to prevent ingress of sample and retaining digital integrity.

- Packaging, microfluidics and sample handling: creating hermetic, biocompatible packaging that integrates microfluidic sample prep (filtration, preconcentration) without degrading sensor performance or adding prohibitive cost is a major systems challenge.
- Scaling, yield and testability: heterogeneous stacks and late-stage materials functionalisation reduce manufacturing yield and complicate wafer-level testing, calibration, and standardisation needed for high-volume deployment.
- Interconnects and 3D assembly challenges: high-density electrical, optical and fluidic interconnects (through-silicon vias, edge connectors, optical coupling, microfluidic vias) must be aligned and reliable across dissimilar materials and chiplets.
- Regulatory, reproducibility and standardization barriers: variable biofunctional chemistries, lack of standardized qualification protocols for hybrid materials (MOFs, COFs, MXenes, organics) hinder clinical/field adoption and certification.

Trends and innovations (materials, architectures and methods)

- Wafer-level heterogeneous/3D integration and chiplet architectures: fan-out packaging, embedded die and hybrid 3D stacking enabling co-integration of CMOS readout, photonics, MEMS. Electrochemical chemical and biosensor layers at scale.
- Methods for development and deposition of 2D materials and heterostructures for ultra-sensitive transduction: graphene, nanomaterials MoS_2, WSe_2 and van der Waals heterostructures used in field-effect biosensors and photodetectors for single-molecule/low-ppb detection with CMOS interfaces.
- Selectivity of sensors for target analytes, particularly at ultralow concentrations (ng/L) will rely on integration of novel and emerging materials including: MXenes and conductive nanocarbon composites for electrochemical sensing: Ti3C2Tx MXenes, doped graphene and carbon nanotube composites offer high conductivity, tuneable surface chemistry and fast kinetics for integrated electrodes. Metal and covalent organic frameworks (MOFs/COFs) and selective porous layers for on-chip preconcentration and selectivity and nanoporous polymers integrated as sieving/capture layers to enhance selectivity and lower limits of detection but wafer scale integration challenges remain.
- Plasmonics and nanophotonic integration for label-free enhancement: on-chip plasmonic metasurfaces, SERS substrates and silicon photonics coupling to integrated light sources/detectors for high-sensitivity optical chemical readout.
- Perovskite and hybrid optoelectronic materials for compact photodetectors: halide perovskites and organic–inorganic hybrids enabling low-voltage, high-responsivity photodetection for optical biosensing when integrated with CMOS.

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- Advanced surface chemistries and biofunctionalization strategies: click chemistry, peptide/aptamer engineering, etc. for tailored for robust, CMOS-compatible immobilization and longevity.
- Integrated microfluidics and sample-to-answer modules: 3D-printed and wafer-level microfluidic integration, on-chip filtration, (di)electrophoretic preconcentration and electrochemical pumps combined with sensor arrays for multiplexed, automated assays.
- Edge AI and on-chip signal processing: low-power neuromorphic or ML accelerators co-packaged with sensor arrays for anomaly detection, calibration and drift compensation, multiplex deconvolution and calibration at the edge.
- Additive manufacturing and heterogeneous printed electronics: inkjet/roll-to-roll printing of functional inks (conductive, semiconducting, biological) enabling flexible, wearable and disposable sensor integration with traditional silicon electronics.

In summary, HI will evolve from a packaging strategy into a holistic enabler of smart, multifunctional, and AI-native sensors, paving the way for compact, high-performance systems that support real-time analytics and adaptive functionality across automotive, healthcare, sustainable agriculture and food, industrial, and consumer domains.

3.2.2 Energy harvesting

In the context of the emergent market of connected devices (IoT), healthcare and wearables, one important aspect is the need for energy supply. In the case of small objects consuming a small amount of power (in the range of micro-watts to milliwatts) batteries are the typical solution. In some applications, because of cost, complexity or environmental constraints (for instance reducing the use of non-rechargeable batteries and the impact of battery technology in our environment), providing energy autonomy to the connected devices is the best solution. Energy autonomy will also allow the development of maintenance-free and easily reconfigurable sensors networks [15].

Different ambient energy sources can be exploited and converted into electricity: sun or artificial light, heat, RF power (which can be harvested from radiating devices or intentionally transfered), mechanical movements and vibrations among others. The converted energy needs to be used and transferred wisely to sensors, microcontrollers or other electronic components included in the system. Thus, power management circuits and energy storage devices are also an essential element.

Different technologies [16], [17], [18] have been investigated to develop energy harvesters (EH), some of them are commercialized. The most known technologies and principles are: i) mechanical EH, using typically three principles – electrostatic, piezoelectric and electromagnetic -,ii) Thermal EH using typically the Seebeck effect, iii) light EH using the photovoltaic effect and iv) RF EH using structures (e.g. antennas, coils, metallic plates, etc.) to radiate and receive RF power.

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Energy storage solutions for EH devices are typically solid-state micro-batteries (maintaining device operation over long periods) and supercapacitors (used for shorter timeframes or when large energy pulses are required). Both are required ideally to maintain average power consumption and high levels of pulsed power [19].

Micro power management consist of circuits to take maximum advantage of energy transducers (i.e. harvesters), converting and storing the available energy and distribute it efficiently, providing a continuous source of power.

Challenges:

The main challenge in EH technologies [15], [19] is the reduction of fabrication cost, increasing efficiency without using toxic or rare materials. Materials should be from sustainable sources and be easy to recycle, re-use, compost, etc. Wearables applications also demand flexibility and/or transparency. Compatibility with Silicon is also important.

Concerning specific EH technologies:

Mechanical EH rely typically on input vibrations, and the main challenges are the compatibility with low frequency vibration sources (<100 Hz), wider operational frequency bandwidth and higher sensitivity to small vibrations.

Thermal EH requires materials with high electrical conductivity, and low thermal conductivity. Achieving both is challenging.

Photovoltaic (light EH) technology is mature for both outdoor and indoor applications. New materials being flexible and with low weight (thin films) at reduced cost and high efficiency are promising for emerging applications.

RF EH suffers of low power densities because of RF regulations. RF power transfer "on demand" solutions are currently preferred and are exploited (e.g. RFID, wearable or implantable devices using eco-compatible materials).

Thin film solid-state batteries require more energy density and higher power options at lower cost. *Supercapacitors* on the other hand have a large series resistance limiting their charge/discharge efficiency, reducing this resistance at a lower cost is a challenge.

The main challenges associated to *power management circuits* are related to the miniaturization of the system embedding micro-magnetic components or power converters, the reduction of overall leakage enabling low power consumption, and the development of energy-aware circuit design techniques for achieving operation in ultra-low power regimes.

Another big challenge resides in designing EH systems comprehensively, combining all aspects of the fabrication process, harvesting structure, power conversion circuits and storage. This will lead to an overall higher power generation efficiency.

Trends and innovation:

There are many trends and innovations in the different technologies (and principles) related to EH, energy storage and micro-power management circuits, we can mention a few [15]:

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Mechanical EH: In general, the exploitation of non-linear mechanical systems for larger frequency bandwidth and the use of frequency-up converting. Concerning the different principles: i) Piezoelectricity: porous materials [20] and nanostructured materials, such as ZnO nanowires among others [21] are currently investigated as a solution to enhance performance. Ii) Electrostatic: The use of new materials like Fluorin polymers, the use of surface texturation in relation to triboelectricity and the improvement of the performance of electret materials [22] iii) Electromagnetic: The use of thick, polymer bonded powdered permanent magnets or nano-structured, patterned magnet development for the development of CMOS compatible, high-performance micro/nano-magnets for MEMS/NEMS-scale integration.

Thermal EH: Emerging trends involve using silicon and silicon-germanium thin films as environmentally friendly alternatives to toxic materials like Bi_2Te_3, thus ensuring compatibility with CMOS technology [23]. Emerging spintronics via novel mechanisms such as the anomalous Nernst effect and magnon drag [24] are studied to improve the efficiency of energy conversion.

Light EH: The development of thin-film PV cells (III-V, organic, DSSC…) for flexible, transparent [25] and low-cost applications. The performance improvement of outdoor (using Organic, DSSC, semiconductors compounds like III-V or CdTe, a-Si, Perovskite) and indoor (using Si cells, tandem cells on Si, semiconductors compounds like CdTe or CIGS, DSSC, Organic) PV cells. One emerging technology consists in harvesting infrared heat by optical rectennas [26].

RF EH: Current trends exploits real-time beamforming, coupled with localization capabilities, and novel signal format excitations to support Electromagnetic harsh and dense indoor environments [27]. Another important field of development is to enable rectifiers with augmented capabilities in keeping the highest RF-to-DC conversion efficiency for wider range of RF power [28].

Solid state batteries: Initial prospects to increase energy density and higher power may involve multilayer options and the use of thicker electrodes. New materials for both electrodes and electrolyte with increased conductivities, nano structuring and new printing capabilities [29] will also be beneficial. Low-temperature fabrication techniques allowing the integration of batteries into flexible substrates are being explored as well to improve energy density and power while reducing costs [30].

Supercapacitors: Current trends include working on more efficient electrodes (carbon and pseudocapacitive materials) and electrolytes (liquids and gels), and “smart supercapacitors” adding characteristics as mechanical flexibility, self-healing, and being biodegradable and biocompatible [31].

Micro-power management circuits: Some of the main directions characterizing the evolution of this technology are [15]: (i) reducing cold start thresholds (minimum required input power and/or voltage); (ii) management of heterogeneous and/or multiple input energy transducers; (iii) integration of complex load management functions into the same silicon (e.g. generation

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of multiple regulated voltages, management of primary batteries and supercapacitors, etc.) (iv) integration of digital interfacing; (v) include very efficient ultra-low power modes to be activated in sleep modes of low duty-cycle devices; (vi) provide energy measurement circuitry to estimate the remaining battery life or the currently available power from the source.

3.2.3 Power electronics

Power devices govern a substantial fraction of global electricity flows, making them a critical lever for systemic efficiency improvements and CO_2 reduction. The transition from silicon to wide-bandgap (WBG) semiconductors—primarily silicon carbide (SiC) and gallium nitride (GaN)—and the emergence of ultra-wide-bandgap (UWBG) materials such as gallium oxide (Ga_2O_3) and aluminum nitride (AlN) represent a fundamental shift in power conversion technology. These materials offer higher critical electric fields, superior thermal conductivity (notably SiC), and wider bandgaps, enabling higher breakdown voltages and elevated junction temperatures compared to silicon. This translates into system-level efficiency gains of up to 10% in many applications, improved partial-load behavior, and reduced converter size, cooling requirements, and total cost of ownership across automotive traction inverters, renewable energy systems, industrial drives, and increasingly data center power supplies.

A key trend accelerating SiC adoption is the sharp decline in substrate costs, driven by the transition from 6-inch to 8-inch wafers. Moving to larger diameters reduces cost per device by up to 50%, with further reductions expected as 8-inch wafers gain traction in high-volume production. Next to that, especially Chinese players are flooding the market with cheap SiC substrates. This cost evolution is shifting the industry's center of gravity toward SiC for high-voltage applications such as 800 V EV architectures and industrial power conversion.

GaN, traditionally dominant in low- to mid-voltage fast-switching applications, is now penetrating data center architectures, where high-frequency operation and compact form factors are essential for AI-driven workloads. GaN-based converters enable high-efficiency power delivery in emerging 800 V DC distribution systems, reducing copper usage and improving rack-level power density. At the same time, GaN is pushing toward 1200 V voltage classes, targeting automotive and industrial sectors, though it faces strong competition from SiC in these domains due to SiC's maturity and thermal robustness.

On the device and process side, the primary technical objectives remain reducing on-state resistance (RDS_{on}) and improving channel mobility while maintaining robust gate and surface reliability. Advanced trench-gate and planar architectures for SiC MOSFETs target channel mobility improvement by mitigating interface trap densities at the SiC/oxide interface, while GaN HEMT and GaN-on-Si approaches pursue low RDS_{on} and high frequency capability with attention to buffer leakage and substrate thermal path. UWBG candidates promise even higher breakdown fields and potentially lower conduction losses, but they introduce new materials challenges: achieving low defect density bulk crystals, engineered doping and contacts, and thermomechanical compatibility with substrate and package materials are unresolved technical tasks.

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Heterogeneous integration is a defining enabler of the WBG/UWBG era and a necessary system engineering step to realize full performance benefits. Co-integration of power dies with silicon CMOS drivers, control ICs, sensors and passive components reduces parasitic inductance and resistance, enabling higher permissible switching frequencies and faster gate drive transitions that improve converter efficiency and power density. Integration modalities span 2.5D interposer solutions, 3D stacked assemblies, embedded-die substrates and co-packaged driver/logic die. Each approach entails trade-offs: interposers and high-density Cu interconnects can lower parasitics but complicate thermal paths; embedded dies reduce loop inductance but increase thermal and mechanical stress coupling; 3D stacks maximize functional density but require stringent yield and thermal-management strategies. Multi-physics co-design—encompassing electrical switching dynamics, thermal transport, mechanical stress and electromagnetic compatibility—is essential to manage high dV/dt and di/dt events, mitigate EMI, and ensure long-term reliability of mixed-material modules.

We are now in a pilot-line era where industry investment and roadmaps are converging on WBG/UWBG technologies, and end-to-end pilot facilities—covering scalable high-quality crystal growth and large-diameter substrates, reproducible front-end epitaxy and device processing, and advanced back-end packaging and system-level test—are central to de-risking scale-up; these pilot lines accelerate UWBG maturation, validate SiC/GaN process flows at production-relevant geometries, enable harmonized electrical and reliability qualification (including standardized, accelerated tests for high-field, high-temperature and fast-switching stresses), and focus technical priorities on bulk crystal yield, interface-trap reduction, low-inductance high-density interconnects and thermal packaging, standardized lifetime models for multi-die heterogeneous modules, and advanced multi-physics co-design tools, all requiring coordinated action across material suppliers, fabs, packaging houses and OEM integrators to translate pilot successes into volume production.

In outlook, the era of WBG and UWBG power electronics will be defined by integrated subsystems where advanced materials, optimized device architectures and sophisticated heterogeneous integration converge. Achieving this era will enable higher efficiency, greater power density and broader industrial adoption, unlocking system-level benefits across electrification, renewable integration and high-performance computing power infrastructures.

3.2.4 Wireless communication

Wireless communication continues to represent one of the largest segments in the semiconductor and systems market, yet its growth trajectory is relatively modest compared to other high-tech domains. While data traffic volumes are rising, the industry remains conservative in its approach to spectrum evolution. The much-discussed FR3 band (7–24 GHz) is positioned as a bridge between sub-6 GHz and mmWave, but progress is incremental: initial deployments are expected around 7–8 GHz, while the bulk of commercial activity still concentrates on 3.5 GHz, reflecting the preference of operators for proven coverage and cost efficiency [32].

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Heterogeneous integration is relevant in this domain, yet the concept is not new: advanced packaging has long been part of RF front-end design. Current innovations focus on antenna-in-package (AiP) and system-in-package (SiP) solutions to minimize signal loss and enable compact phased-array architectures for 5G and future 6G systems. These approaches integrate RF, analog, and digital components within a single module, but the emphasis remains on traditional advanced packaging techniques such as flip-chip, fan-out wafer-level packaging, and 2.5D interposers rather than disruptive new paradigms [33].

On the materials front, GaN-Si is gaining traction for infrastructure power amplifiers thanks to its high efficiency and scalability, offering a cost-effective alternative to GaN-on-SiC for mid-band radios. However, its adoption in user equipment (UE) is less certain, as it faces strong competition from GaAs HBT and RF-SOI, which remain dominant for handset power amplifiers due to their maturity and cost advantages [34].

Another notable trend is the expansion of wireless technologies into defense and aerospace applications. Military systems increasingly leverage 5G (and eventually 6G) for secure, low-latency connectivity, autonomous platforms, and integrated sensing capabilities. Concepts such as Joint Communications and Sensing (JCAS) and Integrated Sensing and Communication (ISAC) are emerging as strategic enablers for situational awareness and drone detection, reinforcing the dual-use nature of next-generation wireless technologies [35].

Non-Terrestrial Networks (NTN) are emerging as a critical component of future wireless ecosystems, complementing terrestrial networks (TN) to deliver truly global coverage. NTN leverages satellite constellations, both GEO and LEO, as well as high-altitude platforms to extend connectivity to remote regions, maritime routes, and disaster zones where traditional infrastructure is impractical. This capability is particularly relevant for IoT deployments, emergency communications, and defense applications, where resilience and ubiquity are paramount.

The strategic direction is toward seamless integration between NTN and TN [36], enabling devices to switch transparently between satellite and terrestrial links without service interruption. This convergence requires harmonized spectrum usage, unified protocols, and advanced beamforming techniques to manage handovers efficiently. Standards bodies such as 3GPP have already incorporated NTN into the 5G architecture, paving the way for hybrid networks that combine terrestrial low-latency performance with satellite reach. In the longer term, NTN will play a foundational role in 6G, supporting ultra-reliable connectivity for autonomous systems, global sensing, and secure communications.

But beyond these developments, the market faces structural constraints: spectrum scarcity, high infrastructure costs, and regulatory complexity slow down radical shifts. While research explores terahertz bands and non-terrestrial networks, commercial deployments will prioritize incremental improvements in coverage, energy efficiency, and cost optimization rather than dramatic frequency leaps. In short, wireless communication is evolving, but cautiously balancing innovation with the realities of global deployment economics.

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3.2.5 Photonics

Semiconductor photonics is a broad field encompassing many different technologies for many different markets. It covers high volume markets such as silicon CMOS imagers, III-V semiconductor LEDs – from UV to infrared – for lighting and for displays, III-V laser diodes for optical communication, for metrology and for laser projection in cinemas, III-V VCSEL-arrays for face recognition etc. In most cases the chips for all these applications are manufactured in dedicated fabs.

One of the main areas of rapid and strategic innovation is the area of optical interconnect in datacenters. Driven by the needs of AI there is a strong push for solutions with higher bandwidth, higher interconnect density, lower power consumption and closer integration with CPUs, GPUs and switches.

Today, the market of datacenter interconnect is dominated by three technologies: 850nm GaAs VCSELs with multimode fiber, silicon photonics with single mode fiber and InP electro-absorption modulators (EAMs), also with single mode fiber. The latter two solutions typically operate in the O-band (1310nm). While the VCSEL/MM solution dominates for short-reach interconnect (<100m), the fastest growth and strategic momentum is happening in silicon photonics, especially since this technology is expected to scale best towards higher performance. Therefore, we focus on silicon photonics in the remainder of this section.

Today, the wafer demand in silicon photonics is largely dominated by the pluggable optical transceiver market, mostly for data center interconnect. State of the art commercial transceivers operate at symbol rates of 25-50GBaud and can handle aggregate data rates of between 100 and 800Gbps. While precise figures are difficult to find, it is estimated that the annual sales of pluggable transceivers based on silicon photonics are in the tens of millions. There are approximately 10 industrial fabs/foundries around the world that manufacture silicon photonics wafers, mostly in the United States and Asia. Most of these fabs/foundries are trailing node CMOS fabs (typically 65 or 45 nm) operating on 300 or 200mm wafers. In Europe there are early initiatives to build industrial manufacturing capacity. Next to the industrial fabs/foundries, there are another ten or so semi-industrial fabrication facilities for R&D, prototyping and low-volume manufacturing around the world, of which several in Europe.

Most silicon photonics chips for pluggable transceivers combine passive optical functions (e.g. filters, (de)multiplexers) with high-speed modulation and high-speed detection monolithically. It is common to include micro-Joule-heaters to tune spectrally selective functions. In most products the light source - the laser diode – is not integrated onto the chip but is fiber connected to the silicon photonics chip, so as to ease repairability. Also, in most products the electronic drivers for the modulators and the receivers are not monolithically co-integrated, even if close assembly with the silicon photonics chip is imperative especially at high symbol rate. Nevertheless, at least two silicon photonics fabs offer process flows with monolithic integration of photonics with electronics.

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There is a strong push towards higher interconnect performance in connection to the growth of AI capability. Key metrics include bandwidth per lane, spatial or spectral density of lanes, power dissipation, latency, range, and more. Conventional silicon photonics solutions cannot keep up with this trend. This is now leading to a race towards new solutions. On one hand the system architecture is changing from pluggable solutions to board-integrated solutions (Co-packaged Optics – CPO), so as to shorten the electrical interconnect between the CPU, GPU or switch and the transceiver. Also, while some high-end transceivers contain digital signal processors (DSPs) for (de)modulation, mitigation of fiber-induced impairments, clock recovery, error correction, adaptive control of link parameters etc., there is a trend towards DSP-less transceivers (Linear Pluggable Optics or LPO) so as to avoid the power consumption and the latency associated with the DSP.

On the silicon photonics chip technology side there is a strong interest in modulators with better performance than what silicon carrier depletion can offer. Therefore, one envisages to integrate electro-optic Pockels materials onto the silicon photonics chip. There is a whole range of new materials considered for this task. These include thin-film lithium niobate (TFLN or LNOI), lithium tantalate, barium titanate (BTO), organic electro-optical materials, 2D materials, and more. Integrating such materials at frontend (FEOL) level is often difficult. Therefore, most work focuses on heterogeneous integration of thin films or chiplets onto the silicon photonics wafer. A variety of heterogeneous integration methods is used in this context: wafer-level flip-chip mounting, die-to-wafer and wafer-to-wafer-bonding, micro-transfer printing, …). The industrial supply chain for such solutions is still embryonic but is developing fast, with relevant actors in Europe, the US and Asia. Heterogeneous integration of laser diodes and SOAs is also gaining traction in the same context.

Apart from the interconnect market, silicon photonics is also deployed for a very broad variety of other applications and markets, some of which have a potential for high volume. These include compute functions in the optical domain, analog signal processing and microwave photonics, quantum computing/sensing/communication and, last but not least, sensing. The sensing area itself is very diverse and spans markets such as 3D imaging (LIDAR, OCT,…), gyroscopes, structural health monitoring, medical devices, chemical and biochemical sensing (in particular for diagnostic assays), and more. A relatively large number of young companies (of which a good fraction in Europe) are active in this huge space, but the commercial traction and growth is still relatively slow. The diversity of applications also leads to diversity in underlying technologies and new flavors of silicon photonics. A major factor leading to diversity is the fact that many of these new applications require operation away from the O- and C-band, either towards shorter wavelength (all the way to the UV) or towards longer wavelengths (mid-infrared). The conventional usage of silicon as a waveguide core material in silicon photonics is now being complemented by other core materials, such as silicon nitride, aluminum oxide, TFLN, and more.

There is considerable dynamics in the silicon photonics wafer manufacturing business. Mostly driven by the demand of AI, there are rather many initiatives to establish new fabs for silicon

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photonics (or at least for integrated photonics on silicon wafers), also in Europe. There are also early examples of consolidation.

4 Advanced 3D/Packaging technologies as key enabler for advanced computation and functionality

Heterogeneous integration has become the cornerstone for enabling both high-performance computation and diversified functionalities. As outlined in Sections 2 and 3, the scaling limits of traditional monolithic approaches and the growing complexity of heterogeneous systems demand solutions that go beyond device-level innovation. 2.5D and 3D integration, chiplet architectures, and hybrid bonding techniques provide the structural foundation to combine logic, memory, photonics, power devices, and sensors within a single compact system. These technologies not only address critical bottlenecks such as bandwidth, latency, and energy efficiency but also unlock new design paradigms where functionality and performance can be co-optimized at the system level. In this context, advanced packaging is no longer a back-end process. It is a strategic enabler that bridges diverse technology domains, accelerates modularity, and supports Europe's ambition to lead in next-generation semiconductor ecosystems.

Rather than relying on large monolithic dies, which suffer from yield limitations and increased parasitics due to long interconnect distances between logic and memory, the industry is moving toward a chiplet-based approach. In this paradigm, a large integrated circuit is disaggregated into smaller, function-specific dies that can be individually optimized and then reassembled into a single system using advanced packaging techniques (see Figure 5). This modular architecture significantly enhances flexibility, scalability, and overall system performance.

The chiplet concept is enabled by a suite of advanced 3D integration technologies, including high-density through-silicon vias (TSVs), wafer-to-wafer and die-to-wafer hybrid bonding, and sequential 3D stacking (illustrated in Figure 6). These techniques differ in achievable interconnect density and complexity, but among them, hybrid bonding, based on Cu/SiO_2 structures, stands out as the most promising. It offers ultra-fine interconnection pitches in the 1–2 µm range, a critical capability for next-generation high-performance systems.

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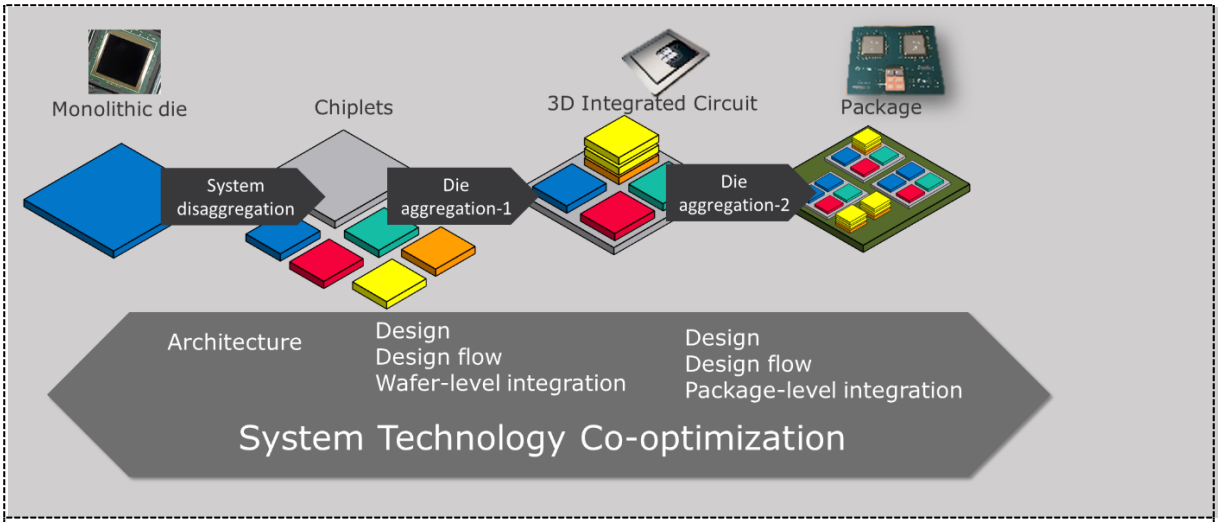

Figure 5: Disaggregation of a monolithic chip into several chiplets, re-aggregated together using 3D integration.

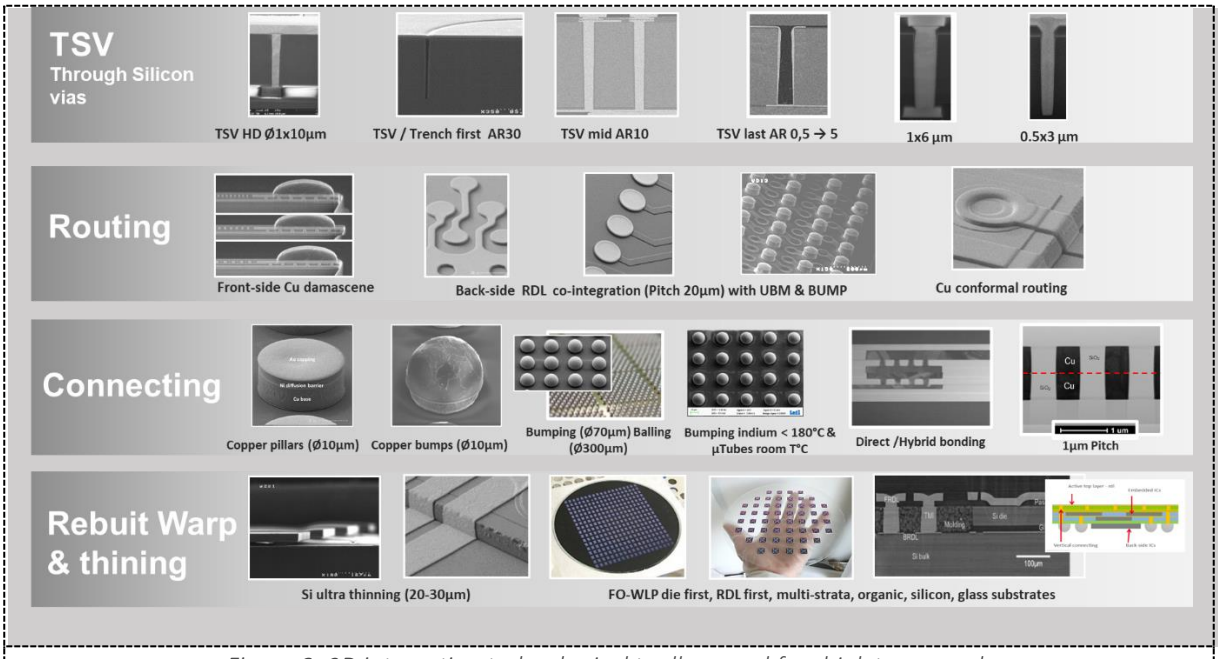

Figure 6: 3D integration technological toolbox used for chiplet approach.

5 Landscape mapping and recommendations

Based on deliverables D3.1-D3.3, D4.2, D4.3, and a survey that was conducted covering the different fields in both advanced functionality as well as advanced computation, this section aims to offer a coherent picture of Europe's current positioning, the strengths and gaps observed in global semiconductor ecosystems, and the most promising areas where international cooperation can meaningfully accelerate Europe's technological and industrial ambitions.

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Across both domains, advanced computation and functionality, Europe stands out as a global leader in scientific excellence. This is particularly visible in areas such as advanced CMOS research, BEOL innovation, heterogeneous integration, 2D materials, sensor and MEMS development, wide-bandgap power electronics, and integrated photonics. European RTOs and universities consistently contribute to pathfinding research and early-stage technology breakthroughs. Europe's sustainability priorities further foster leadership in materials, energy efficiency, and "More-than-Moore" domains, where functional diversification plays a crucial role. Yet, despite these strengths, a recurrent challenge emerges: Europe lacks the same depth in high-volume manufacturing, packaging, and system-integration capabilities as its global competitors. These gaps structurally shape Europe's dependence on foreign ecosystems and underscore the strategic importance of well-aligned international cooperation.

In the field of advanced computation, the global landscape is dominated by non-European actors who combine extensive industrial scale with dense research–industry integration. The United States maintains leadership across CMOS scaling, semiconductor equipment, memory and compute architectures (including near- and in-memory computing), and quantum technologies. Its advantage rests not only on corporate capabilities but also on powerful coordination mechanisms such as industry–academia consortia and sizeable federal investments. South Korea and Japan hold leading positions in memory, MRAM, materials engineering, and back-end integration. Taiwan remains the global anchor for leading-edge foundry technology, chiplet manufacturing, 3D stacking, and related packaging ecosystems. In this global configuration, Europe's strength lies primarily in research and exploratory development rather than in high-volume industrial deployment. Cooperation in computation technologies therefore needs to focus on areas where Europe's pathfinding research can accelerate and can be accelerated by access to industrial-scale infrastructure namely advanced packaging, chiplet ecosystems, memory/logic co-design platforms, and quantum-classical integration.

The mapping of advanced functionality presents a similarly mixed picture for Europe. In domains such as sensors and MEMS, energy harvesting, integrated photonics, and wide-bandgap power electronics, the EU has considerable industrial capabilities and research networks. However, structural gaps persist. Sensor and energy-harvesting innovation is slowed by fragmented markets, high development costs, packaging limitations, and the lack of dedicated multi-physics design tools. Power electronics, while strong, suffers from a shortage of OSAT capacity and integrated module-level manufacturing in Europe, especially as demand for GaN, SiC, and emerging UWBG materials increases. Integrated photonics constitutes a particularly important case: Europe excels in design and R&D but is still building up large-scale foundry capacity and specialised PIC-packaging infrastructures. As data-centric and AI applications now push optical interconnects to the centre of high-performance computing, these gaps take on increased strategic significance. Cooperation in functionality domains must therefore prioritise access to specialised packaging environments, heterogeneous integration pilots, and global ecosystems capable of supporting high-volume or high-complexity functional modules.

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The United States, Japan, and Taiwan clearly emerge as the most desirable partners for R&D collaboration. More-than-Moore technologies, heterogeneous integration, and advanced packaging are identified as priority cooperation topics. Interest in accessing research infrastructures also follows a similar trend, with the US and Japan perceived as offering the strongest technology-development capabilities. Taiwan stands out specifically for packaging and chiplet-centric cooperation, reflecting its leading global role in 2.5D and 3D integration. South Korea and Canada occupy intermediate positions, valued respectively for memory/power electronics and photonics/quantum expertise. While Singapore and India appear less frequently as preferred partners, their ecosystems nevertheless offer targeted strengths: Singapore in advanced packaging pilot lines and India in semiconductor design skills and workforce scaling.

Taken together, the mapping of global strengths and European gaps suggests a focused international cooperation strategy centred around a limited set of high-impact domains. These include advanced packaging and heterogeneous integration; memory-centric compute architectures (HBM, PIM, in-/near-memory computing); co-packaged optics and integrated photonics; wide-bandgap power electronics (including emerging UWBG materials); and quantum-classical hybrid systems. These domains lie at the intersection of Europe's research strengths and industrial vulnerabilities, and they are crucial to emerging computing, communication, and sensing paradigms. By collaborating with global leaders—such as the US for EDA, quantum, and chiplet standards; Japan for materials and MRAM; South Korea for HBM and backend innovation; Taiwan for foundry, chiplets, and 3D stacking; Singapore for packaging R&D; and Canada and Australia for photonics and quantum, Europe can accelerate technology translation while building resilience in areas where domestic capacity remains underdeveloped.

The proposals for collaboration are shown in Table 1 and 2 below:

Country/Region	Ecosystem Strengths	Potential Partnership Topics	Key Benefits for the EU
United States	Dominant in EDA, design & IP; leadership in CMOS scaling, MRAM, NMC/IMC; strong equipment base	Advanced packaging; chiplet standards (UCIe); AI-enhanced design; collaboration with fabless	Close tech gaps; strengthen next-gen compute; reduce dependency on East Asia
Canada	Leadership in quantum & photonics; advanced packaging; compound semiconductor R&D	Quantum hardware; photonics; chiplet/UCIe; logic-memory integration; novel AI compute architectures	Strengthen EU quantum & photonics; improve packaging; accelerate HPC

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Taiwan	Global leader in advanced manufacturing; full value chain; CoWoS/3D packaging	Access to leading-edge nodes; 3D integration; packaging & HI	Close advanced-node gap; speed up packaging innovation; strengthen supply chain
Japan	Leadership in equipment & materials; MRAM; SiC/GaN; chiplets	Materials (resists, interconnects, ferroelectrics); advanced memory; HI	Improve system integration; close memory/material gaps; strengthen resilience
Republic of Korea	Leadership in DRAM, NAND, MRAM; 3D & panel-level packaging	HBM; near/in-memory; neuromorphic & AI-EDA; backend packaging	Address memory weakness; improve packaging; support AI/HPC integration
India	Strong semiconductor design capacity; large workforce; growing packaging and manufacturing capabilities	Chip design & verification; AI/ML optimization; power electronics	Accelerate design cycles; expand talent pipeline; improve resilience

Table 1: Proposed collaborations for advanced computation.

Country/Region	Ecosystem Strengths (Functionalities)	Potential Partnership Topics	Key Benefits for the EU
United States	Strong in sensing platforms, MEMS R&D, RF power electronics, integrated photonics, packaging	Integrated photonics, MEMS & sensors, RF power electronics, AI-enhanced EDA for sensing	Accelerate PIC packaging; strengthen sensing performance; access large-scale photonics ecosystem
Japan	Strong in sensors & MEMS, photonic integration, advanced materials, SiC/GaN power electronics	High-sensitivity sensors, micro-packaging, SiC/GaN devices, photonics–electronics co-integration	Improve sensing accuracy; develop WBG systems; access advanced packaging for MEMS/MOEMS
Republic of Korea	Strength in MEMS, RF passives, flexible electronics, energy-	Flexible MEMS, RF MEMS, microfluidic sensors, EH materials, SiP for sensing/power	Boost microsystem integration; enhance low-power sensing; supply chain resilience

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	harvesting materials, WBG devices		
Taiwan	Manufacturing excellence in MEMS & sensors; PIC capability; CMOS-compatible sensing	MEMS manufacturing, sensor miniaturisation, SiP, sensing+ASIC co-fabrication, PIC prototyping	High-volume MEMS access; reduced prototyping cost; manufacturability of sensing & photonics
China	Large sensor ecosystem; strong chemical/biological sensing; packaging capability	Chemical/biochemical sensing, wearable sensors, low-cost packaging, flexible devices	Pre-competitive collaboration; access cost-efficient packaging; scale-up potential
India	Strong in design, embedded systems, IoT platforms; emerging MEMS research; EH R&D	Sensor system design, firmware, EH modelling, low-power circuits, IoT sensor networks	Expand design workforce; accelerate embedded sensing; cost-efficient integration
Singapore	Advanced packaging (A*STAR IME), photonics & MEMS prototyping, micro-batteries, microfluidics	MEMS packaging, photonic sensors, EH solutions, micro-battery integration, HI testbeds	Access packaging pilot lines; faster prototype-to-product; strengthen photonics & sensing

Table 2: Proposed collaborations for advanced functionality.

An important cross-cutting theme is the transformative impact of artificial intelligence on the entire semiconductor sector. AI not only drives the explosion in compute demand shaping semiconductor roadmaps, it also changes how semiconductor technologies are conceived, designed, and validated. The rise of AI-driven design automation, combined with growing system complexity, is shifting the required skills profile dramatically. Future engineers must increasingly master data science, algorithmic optimisation, system modelling, and software–hardware co-design, in addition to traditional device and process expertise. The growing use of AI-EDA tools, essential for sensor co-design, multi-physics simulation, chiplet partitioning, and advanced packaging, makes these competencies indispensable. Strengthened cooperation on skills, design tools, shared testbeds, and mobility programs should therefore be seen as core enablers of Europe's semiconductor strategy, not peripheral additions. The industry impact is equally significant: AI allows faster design iteration, supports more complex optimisation tasks, and lowers entry barriers for system-level innovation, but it also intensifies competition by favouring actors with strong computational and data infrastructures. Europe must respond by ensuring that its next generation of engineers, researchers, and tool developers are prepared for AI-accelerated semiconductor development.

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Overall, this landscape mapping underscores that international cooperation should not be viewed merely as a mechanism to fill short-term technological gaps. Rather, it is a strategic lever for transforming Europe's strong research base into industrial leadership. Cooperation should be focused, mutually beneficial, and anchored in areas where complementary global strengths can help Europe overcome structural obstacles, particularly in advanced packaging, high-volume integration, memory technologies, and AI-enabled design. At the same time, Europe must reinforce its internal capabilities through coordinated pilot-line efforts, improved access to design and modelling infrastructure, and targeted skills development.

6 Conclusions

- AI-driven compute explosion is reshaping semiconductor priorities; Europe must invest in heterogeneous architectures, optical interconnects, and advanced packaging to remain competitive.
- Heterogeneous integration and chiplet-based design are now essential for scaling performance and energy efficiency beyond monolithic approaches.
- Memory bandwidth and data movement bottlenecks are critical constraints; research into near-memory compute and processing-in-memory should be accelerated.
- Energy and thermal management are decisive for future systems; advanced cooling and energy-aware design must be integrated early in system architecture.
- Quantum technologies remain highly exploratory; Europe should maintain a diversified research portfolio across superconducting, silicon-based, and photonic qubits.
- Advanced functionality domains (sensors, energy harvesting, power electronics, photonics, wireless communication) show strong innovation potential; heterogeneous integration is a common enabler across these tracks.
- Energy harvesting and storage solutions need cost reduction, sustainability, and compatibility with flexible substrates; this is key for IoT and wearable markets.
- Wide-bandgap and ultra-wide-bandgap power electronics are strategic for electrification and AI datacenter efficiency; pilot lines and supply chain coordination are critical.
- Photonics (optical interconnects) is becoming indispensable for AI-driven datacenter scaling. Europe should strengthen its silicon photonics manufacturing capacity.
- Advanced packaging technologies (e.g., hybrid bonding, TSVs) are no longer back-end processes but strategic enablers for both advanced computation as well as advanced functionalization. Europe must develop full-stack capabilities from devices to systems.

In general, Europe must pair domestic pilot-line development with strategic international cooperation, aimed at bridging gaps in packaging, memory, chiplets, photonics, and advanced manufacturing.

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