NANYANG TECHNOLOGICAL UNIVERSITY SINGAPORE

Functional Diversification via Heterogeneous Integration Methods

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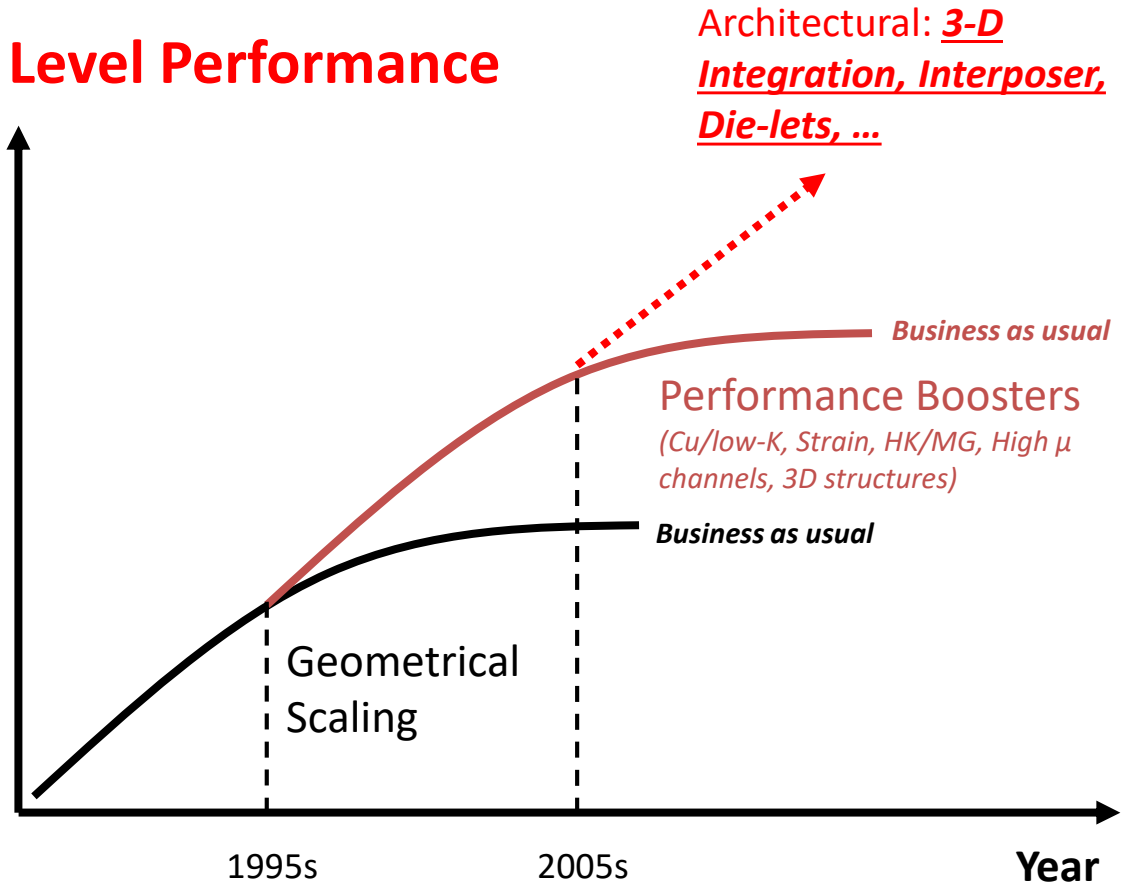
Abstract:

Increasingly, enhancements in system-level performance are being complemented by functional diversification. In this talk, we present our recent work on engineered substrates (X-OI) and advanced packaging techniques—including through-silicon vias (TSVs) and wafer bonding—to advance this dual objective. We will highlight several key demonstrators, such as GaN-LED integration on silicon CMOS, ion-trap architectures on silicon interposers, and our latest proposal involving triple integration of optics, III-V optoelectronics, and silicon technologies.

Heterogeneous Integration

System Level Performance



(Tan *et al*, 2008)

- **Performance, Power, Area, Cost, Time-to-Market (PPACt®)**
- **Functional diversification**

https://paintingvalley.com/

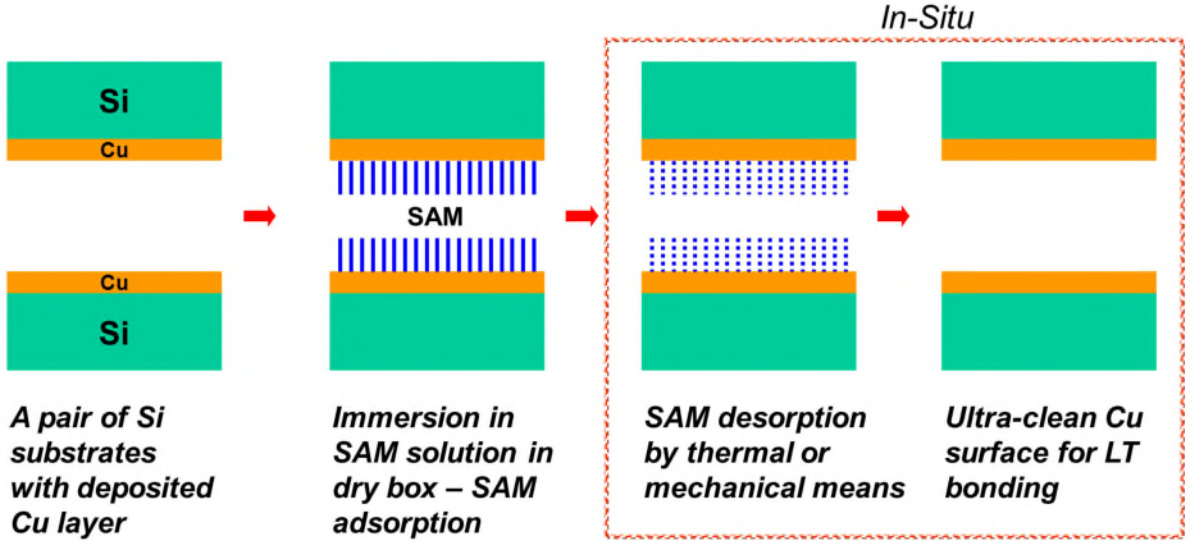
Interconnect and Packaging Bottleneck

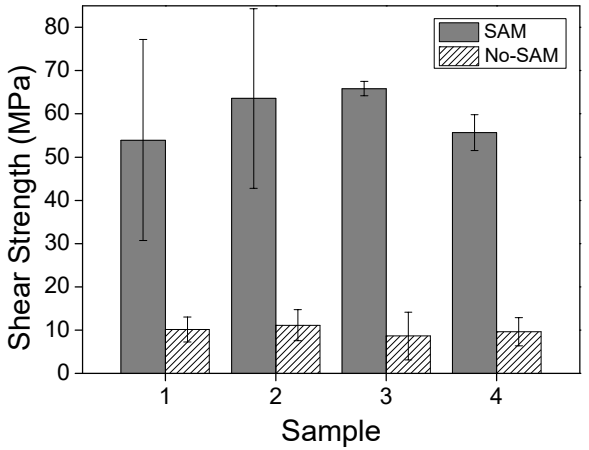
Discussion Points

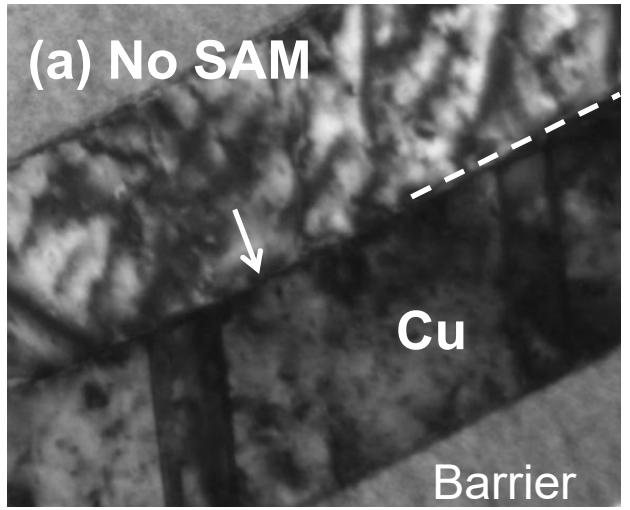
- Enablers for Advanced Packaging
  - Cu-Cu bonding
  - Nano-TSV
  - ML/AI-assisted design optimization (SI, PI)
  - Use-case: Integrated Ion-trap
- Engineered Substrates
  - X-OI
  - GaN-LED + CMOS
- Introducing WISDOM and NCAIP

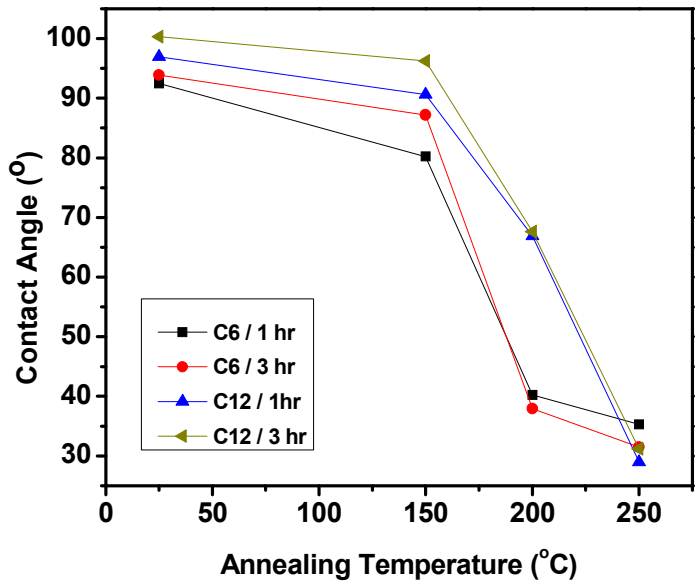
SAM (Alkanethiol) Passivation and Cu Bonding

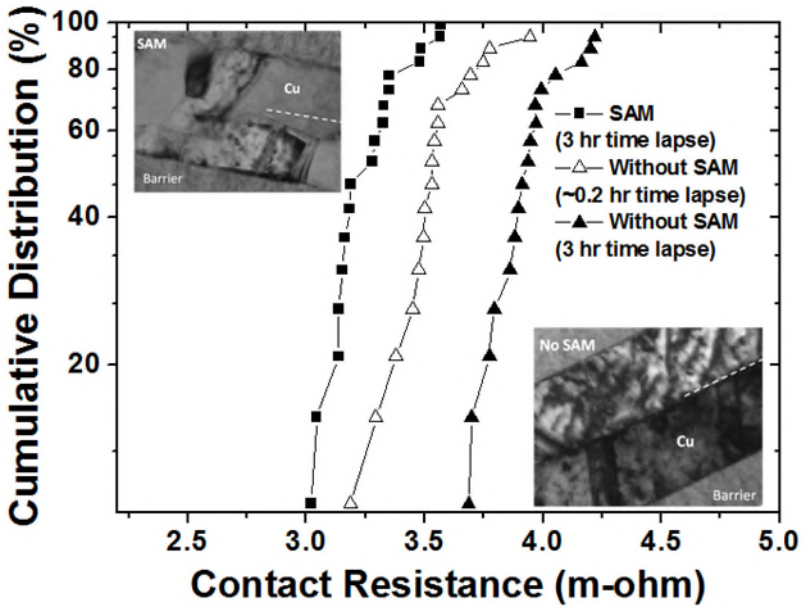
Funded by SRC

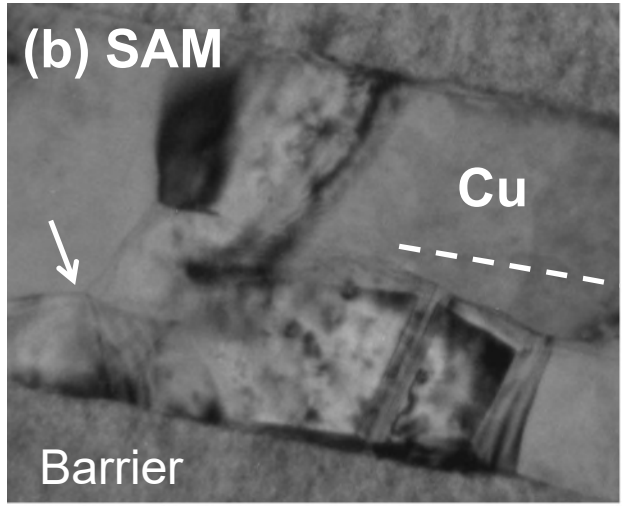








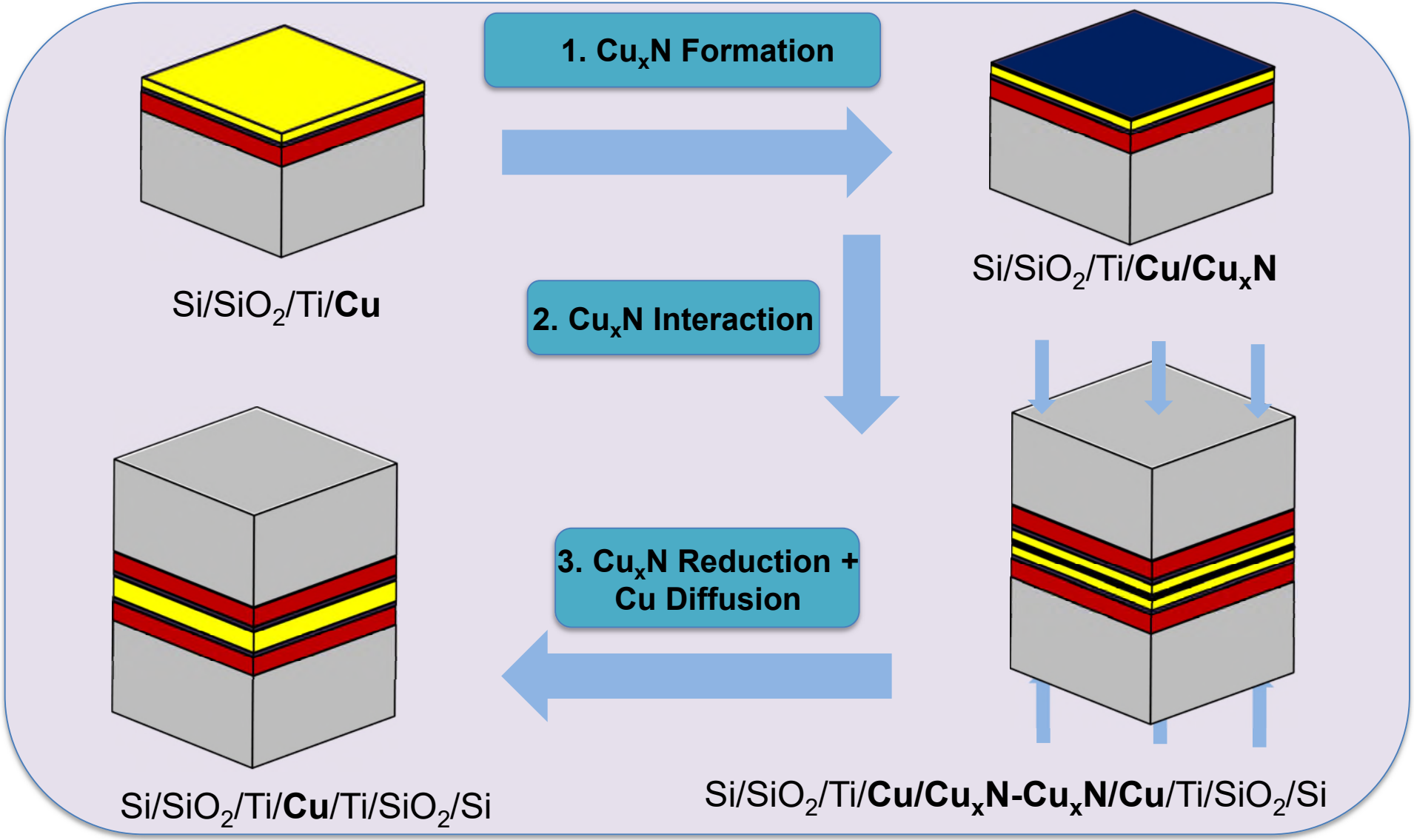




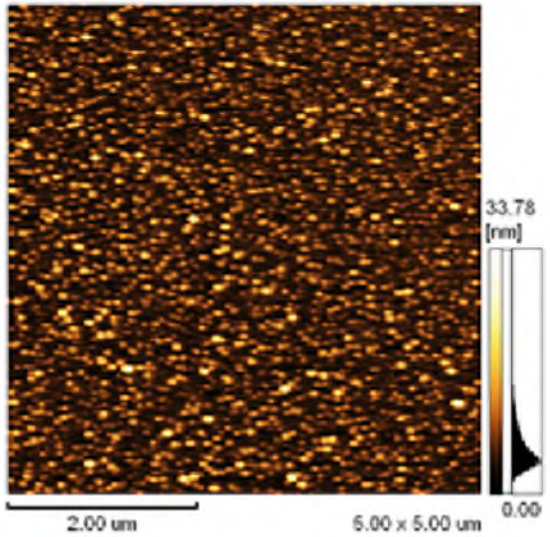
$SH-(CH2)_n-CH3$

Ar/N_2 Plasma-Assisted Cu-Cu Bonding Mechanism

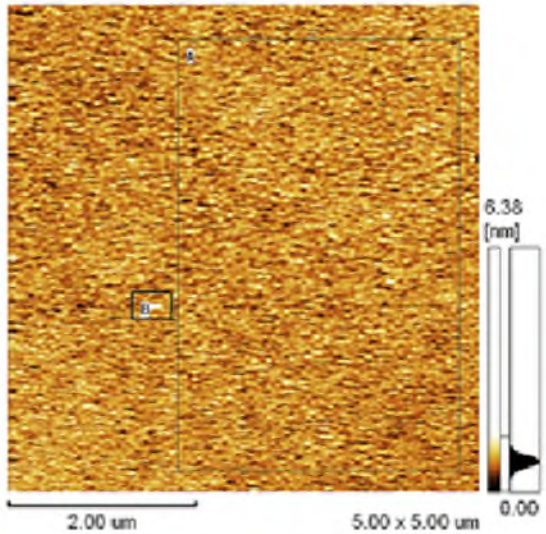
Funded by A*STAR and LAM Research



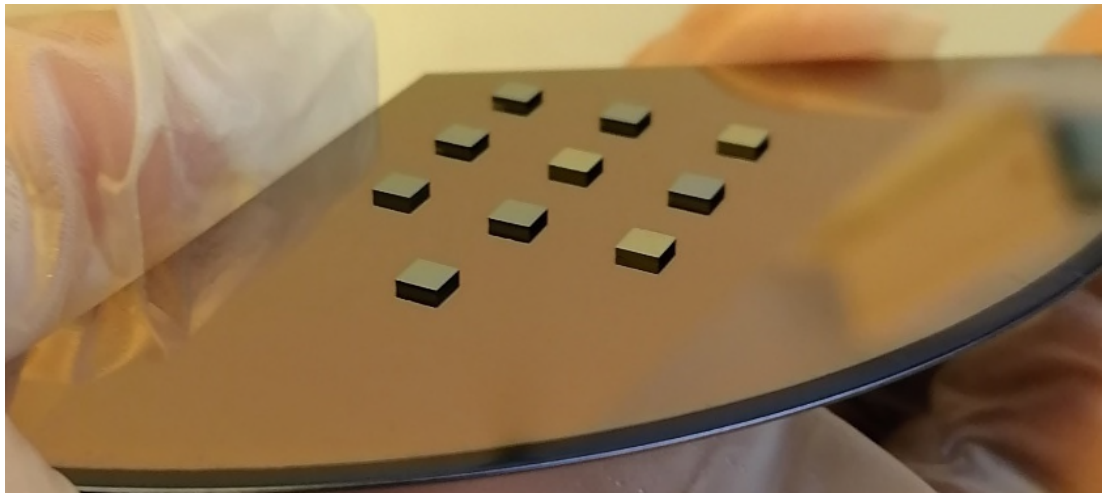
Ar/N_2 Plasma-Assisted Cu-Cu Bonding Mechanism

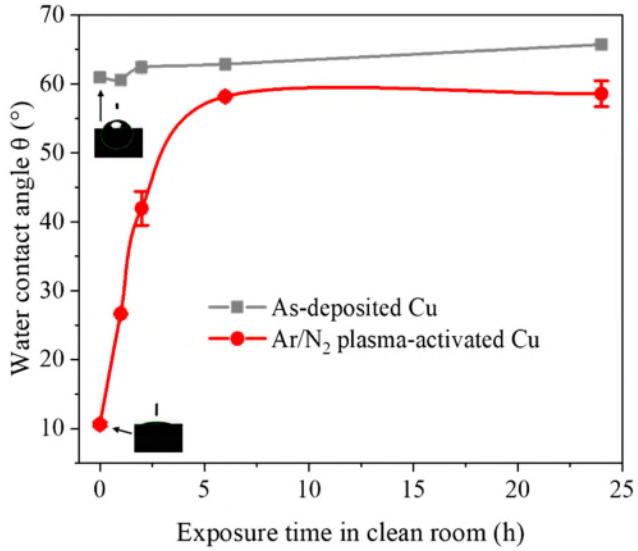


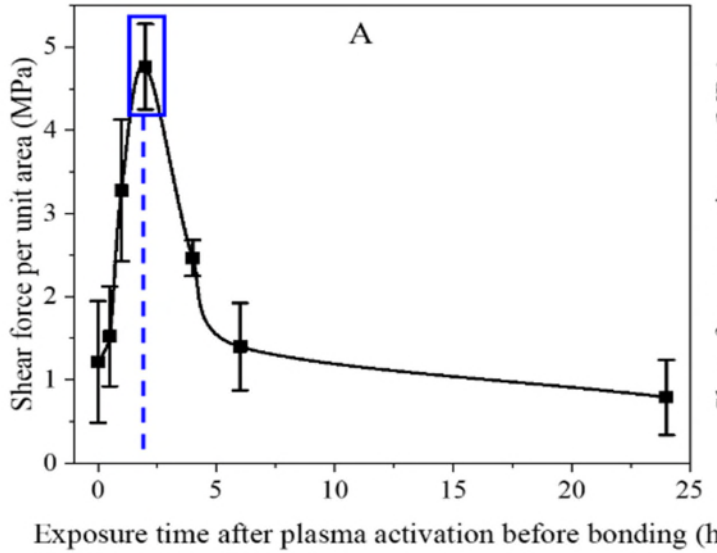
Control sample (2.35nm)

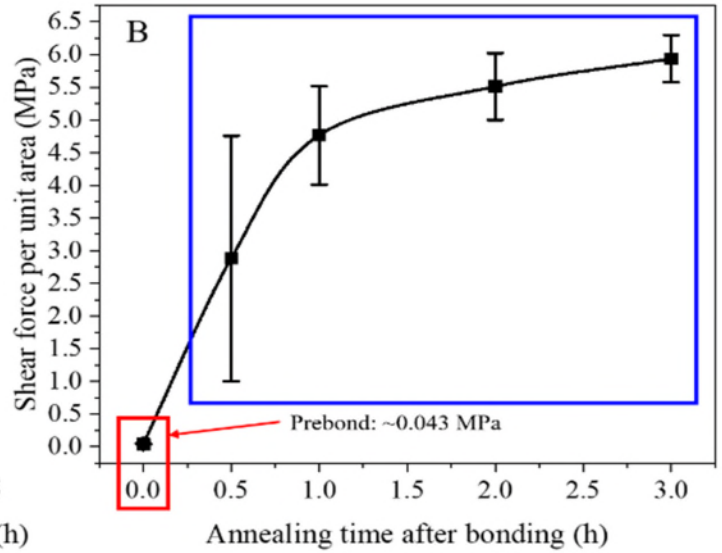


Plasma-exposed sample (0.60nm)

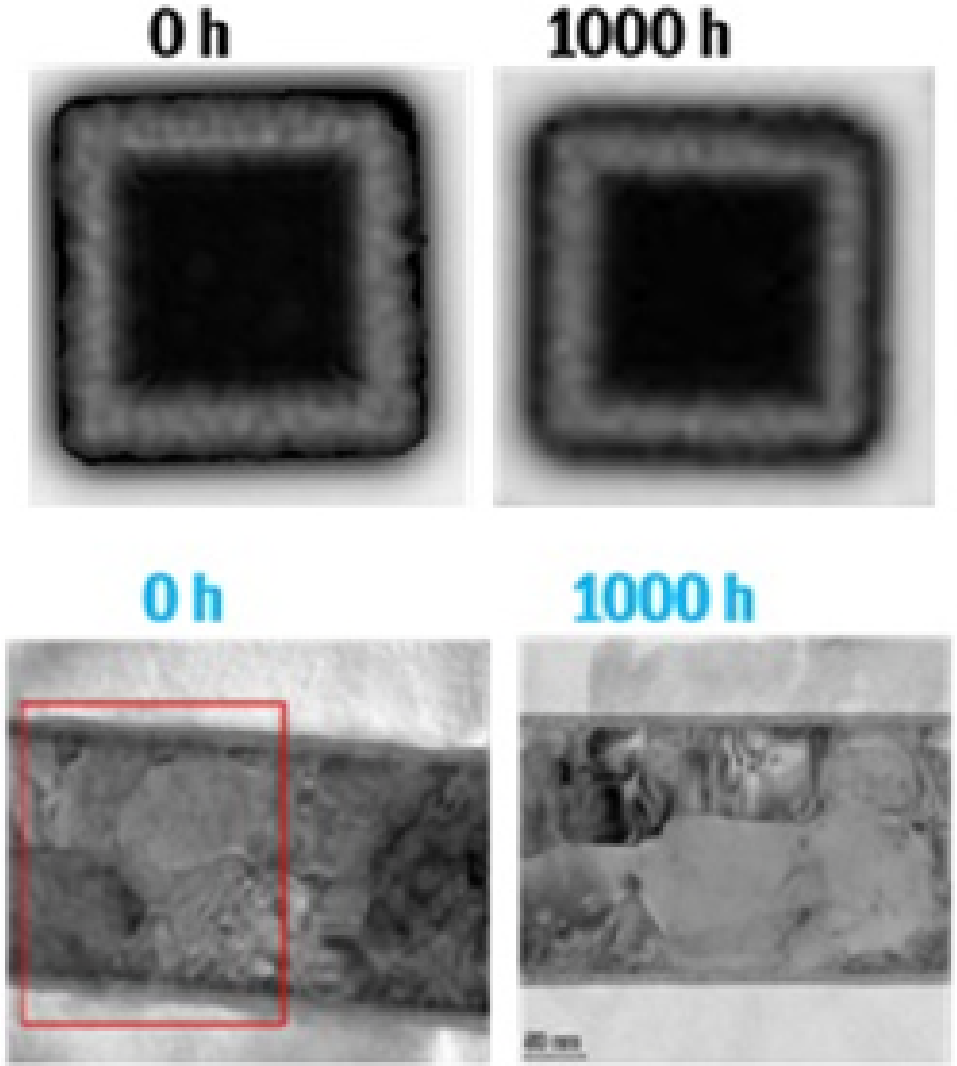




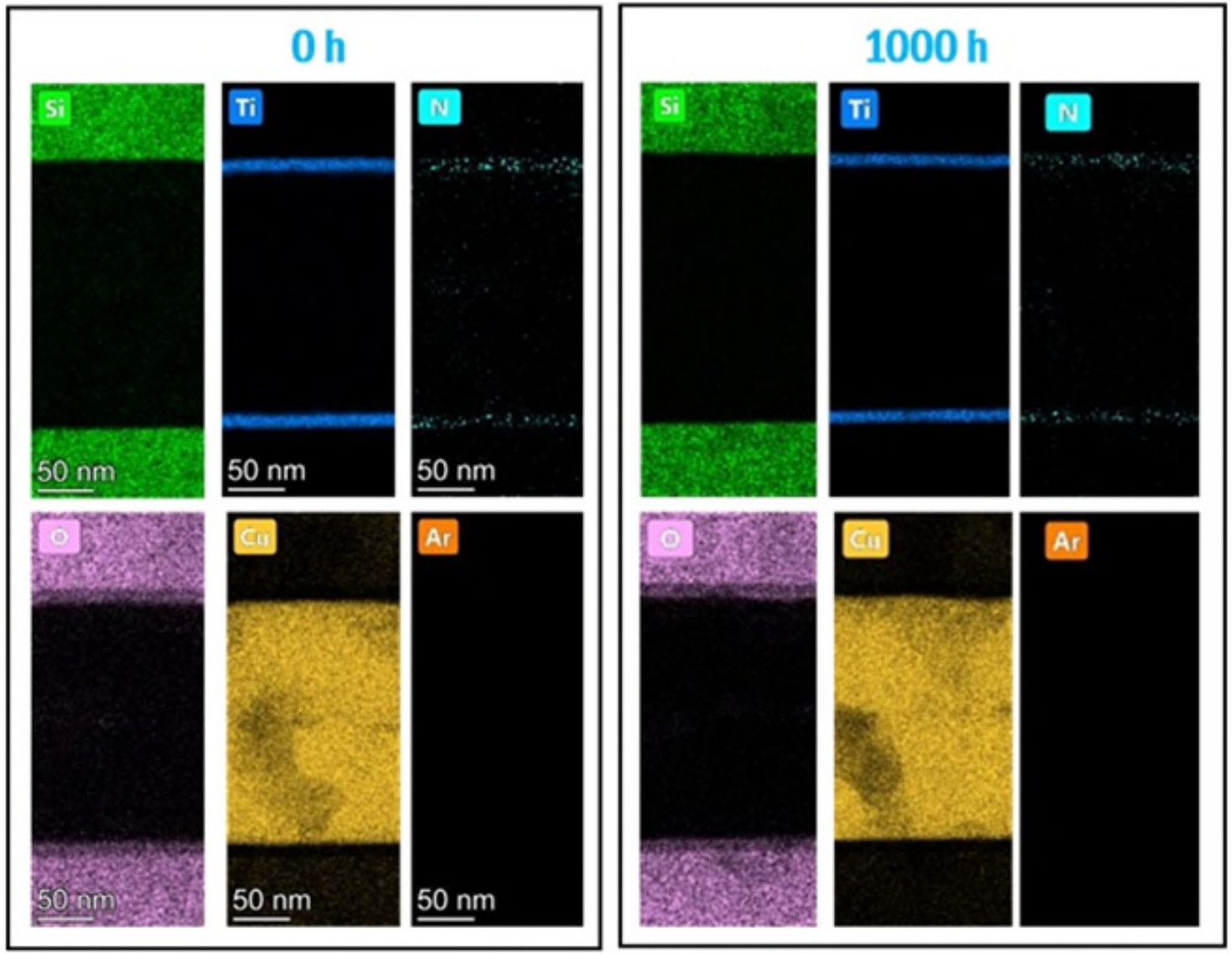




Ar/N_2 Plasma-Assisted Cu-Cu Bonding Mechanism

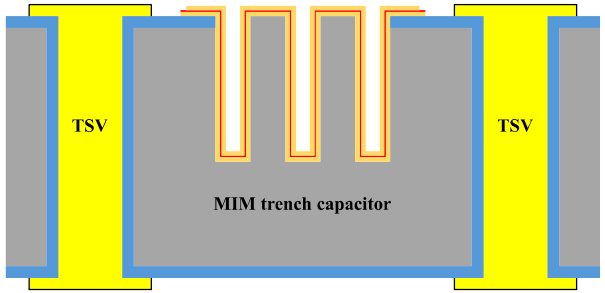


HAST-1000 Hours

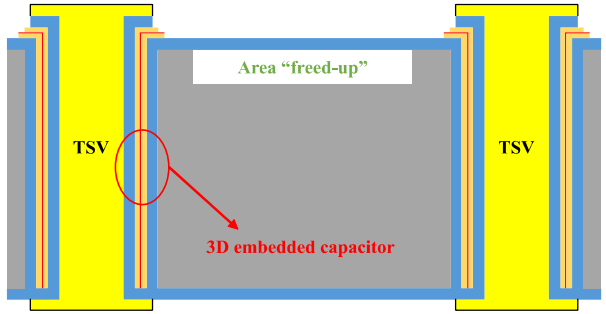


3D MIM Capacitor Embedded in TSV

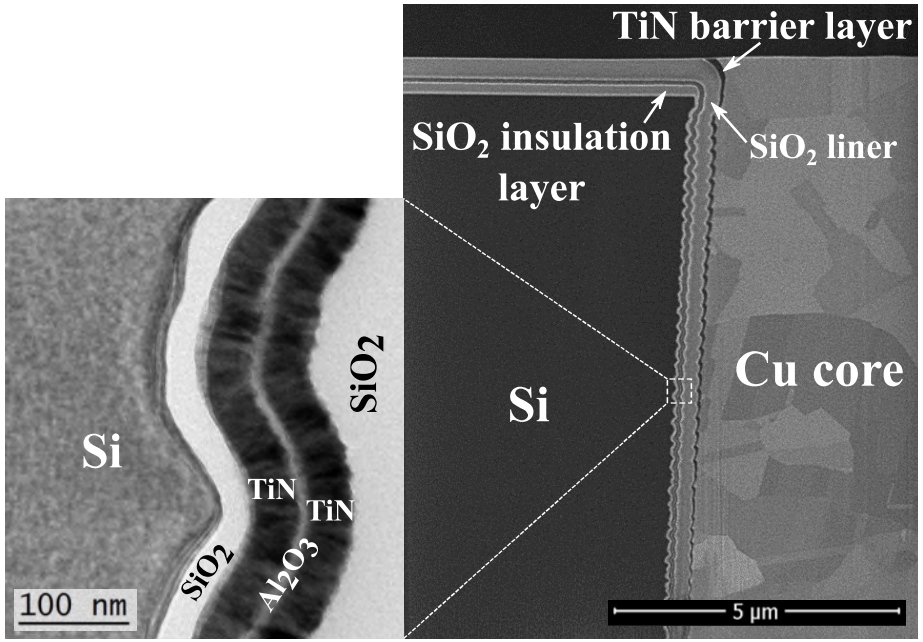
3D capacitors embedded in TSVs
(5,622 nF/mm²)



Stand-alone MIM trench capacitors with TSVs



3D embedded capacitors with TSVs

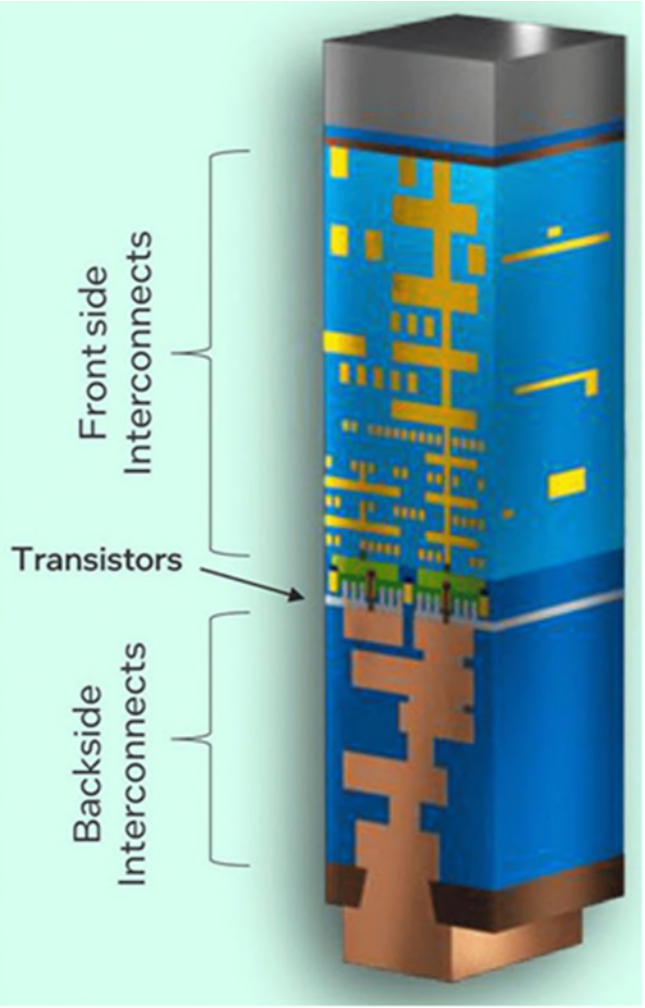


(With IME, Funded by A*STAR IRG, 2017-2020)

US Patent No. 10,950,689B2 (March 16, 2021

Comparison between SiGe Etch Stop Layer (ESL) and BOX of SOI ESL in BSPDN Process Flow			
Term		**Si1-xGex ESL (imec)**	**BOX of SOI ESL (This work)**
Etching	**Si Etching Method to stop at ESL**	Wet Etching (Alkaline chemistries) [1]	DRIE
	ESL Removal Method	Wet Etching (Acidic chemistries) [2]	DRIE
Process Integration	**Integration Method**	RP(Reduced Pressure)-CVD [3]	Use of manufactured SOI wafer
	Flexibility	High (integrate where/when needed)	Lower (fixed structure)
	Complexity	Higher (adds epi steps, requires tight process control)	Lower (simplifies flow, uses standard wafer handling)
	Uniformity Control	Challenging (requires optimized epi process) [3]	Excellent (esp. Smart Cut™ for thin device layers)
	Defect Control	SiGe Layer should be very thin to control defects (10 nm [4])	High quality
	Selectivity Robustness	Chemistry-dependent, may require careful tuning/passivation	High and Robust
	Throughput/Cost Factor	Lower throughput (low-T epi) but processing cost low	Higher wafer cost

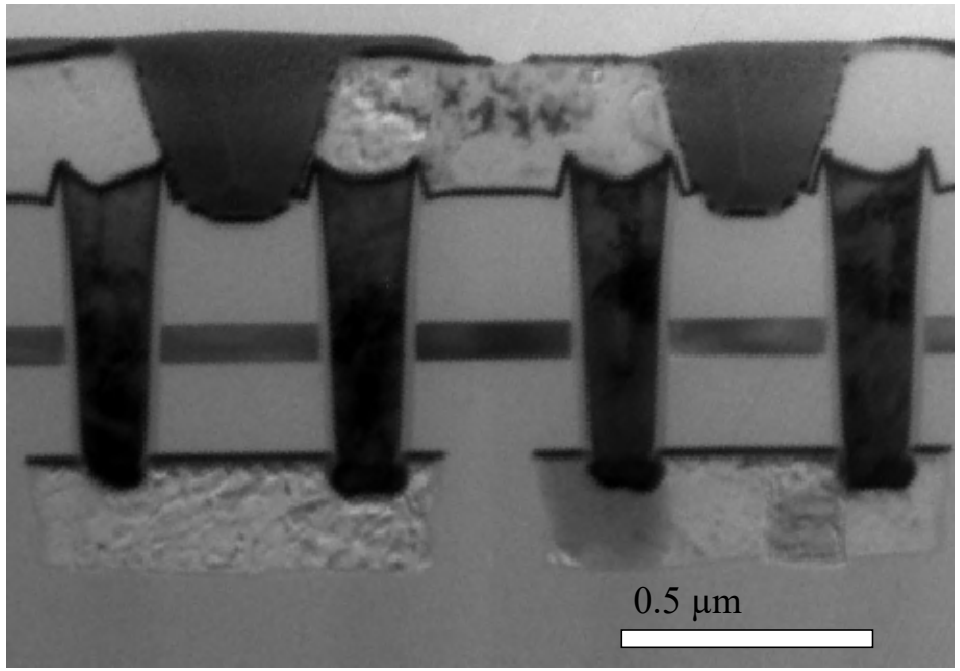
Nano-TSV

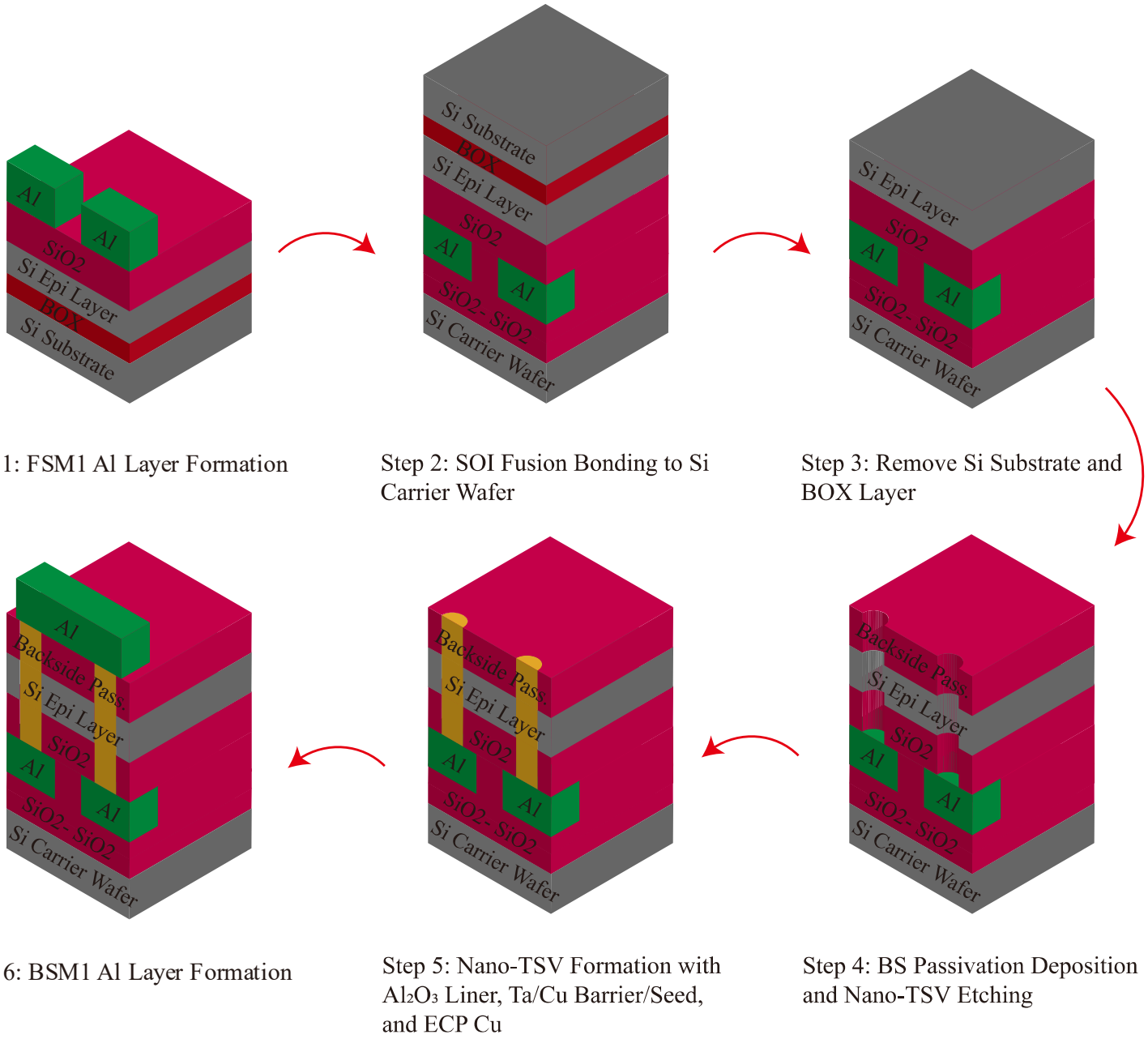


(Intel)

Process Flow

DC, Kelvin, Leakage





Step 1: FSM1 Al Layer Formation

Step 2: SOI Fusion Bonding to Si Carrier Wafer

Step 3: Remove Si Substrate and BOX Layer

Step 4: BS Passivation Deposition and Nano-TSV Etching

Step 5: Nano-TSV Formation with Al_2O_3 Liner, Ta/Cu Barrier/Seed, and ECP Cu

Step 6: BSM1 Al Layer Formation

Supported by A*STAR/IME

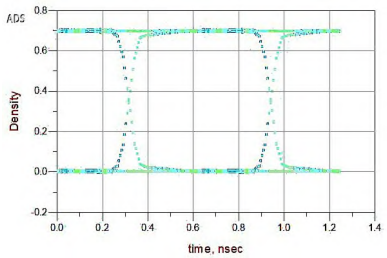
Defect Detection for Signal Integrity (EPTC 2022)

Collaborated with:

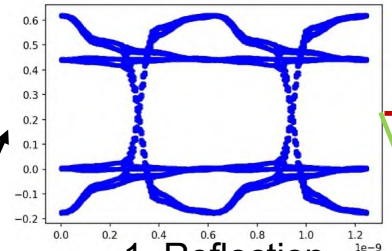
Agency for Science, Technology and Research SINGAPORE

1. Eye diagram analysis with convolutional neural network (CNN)

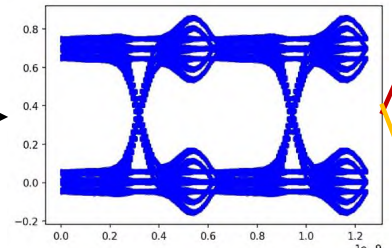
Seven types of signal impairments



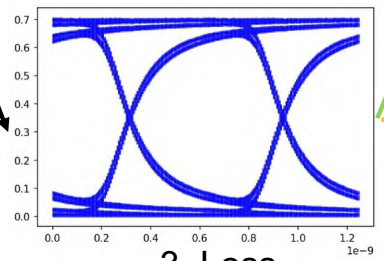
Baseline



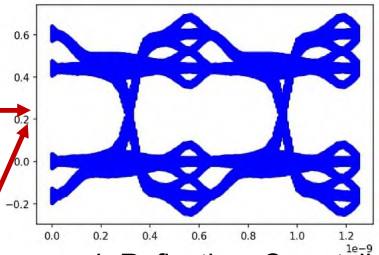
1. Reflection



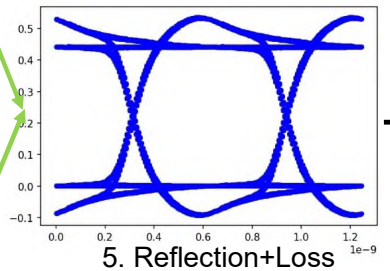
2. Crosstalk



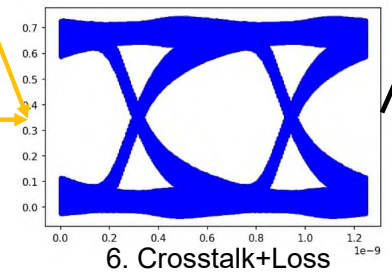
3. Loss



4. Reflection+Crosstalk



5. Reflection+Loss

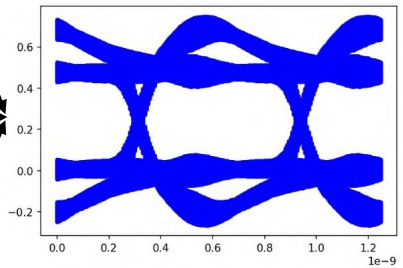


6. Crosstalk+Loss

Reflection: Change impedance of transmission line and receiver

Crosstalk: Add coupled line to transmission line as noise source

Loss: Increase dielectric loss of substrate



7. Reflection+Loss+Crosstalk

Highlights:

- Achieve 100% classification accuracy.
- Enable faster troubleshooting for channel design.
- Reduce design time and cost for high-speed circuits.

Innovation:

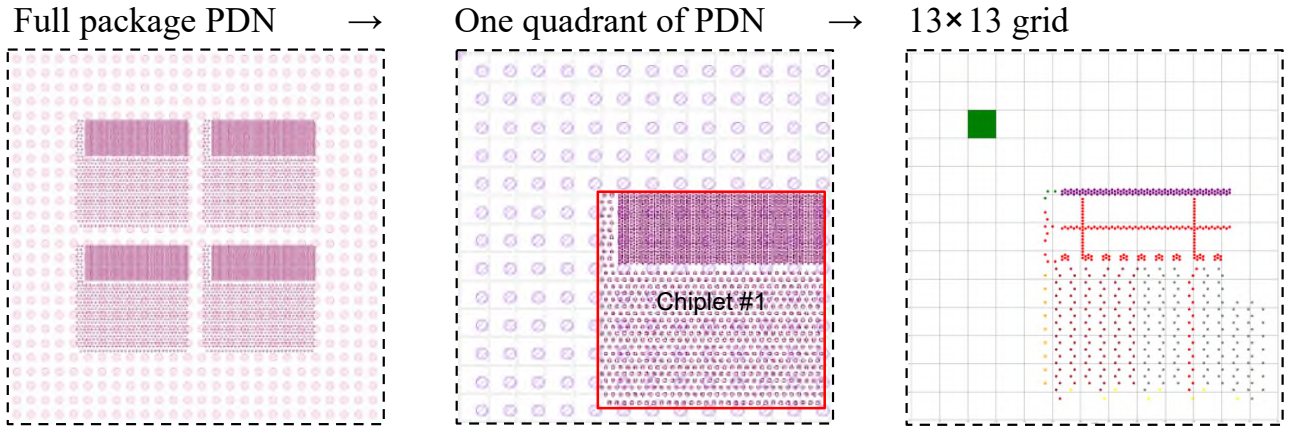
- A convolutional neural network (CNN) is trained to identify and classify signal impairments, and find the locations of impairments in the interconnect channel using the eye diagram.

Design Automation for Power Integrity (ECTC 2024)

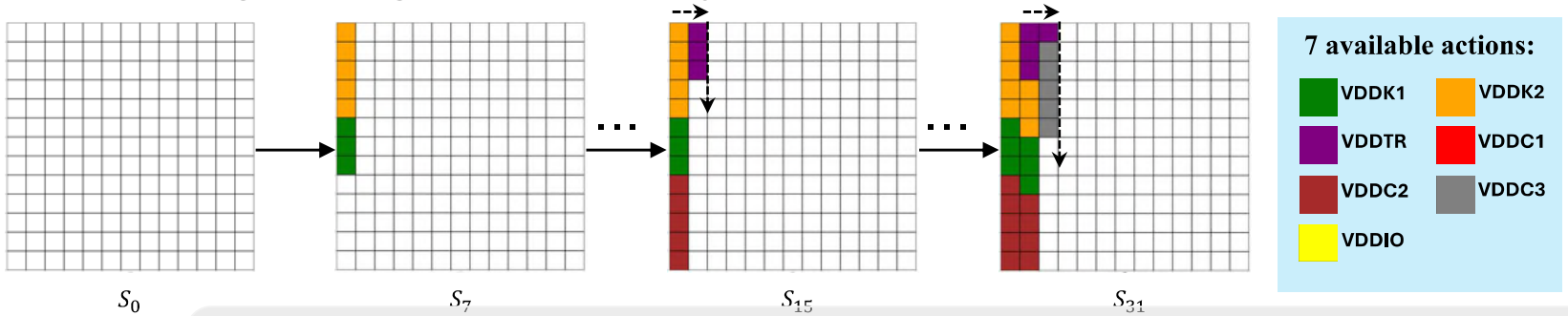
Collaborated with: Agency for Science, Technology and Research SINGAPORE

2. Power distribution network (PDN) design with reinforcement learning (RL)

- **Design environment**



- **The RL agent designs the PDN cell by cell.**



Highlights:

- Reduce PDN design time from 3 months (manual) to 6 CPU hours.
- Lower impedance by up to 82.9% at key frequencies.
- Enables faster, cost-effective and automated PDN design for advanced packaging.
- IEEE 74th ECTC Texas Instruments Outstanding Student Interactive Presentation Award

Innovation:

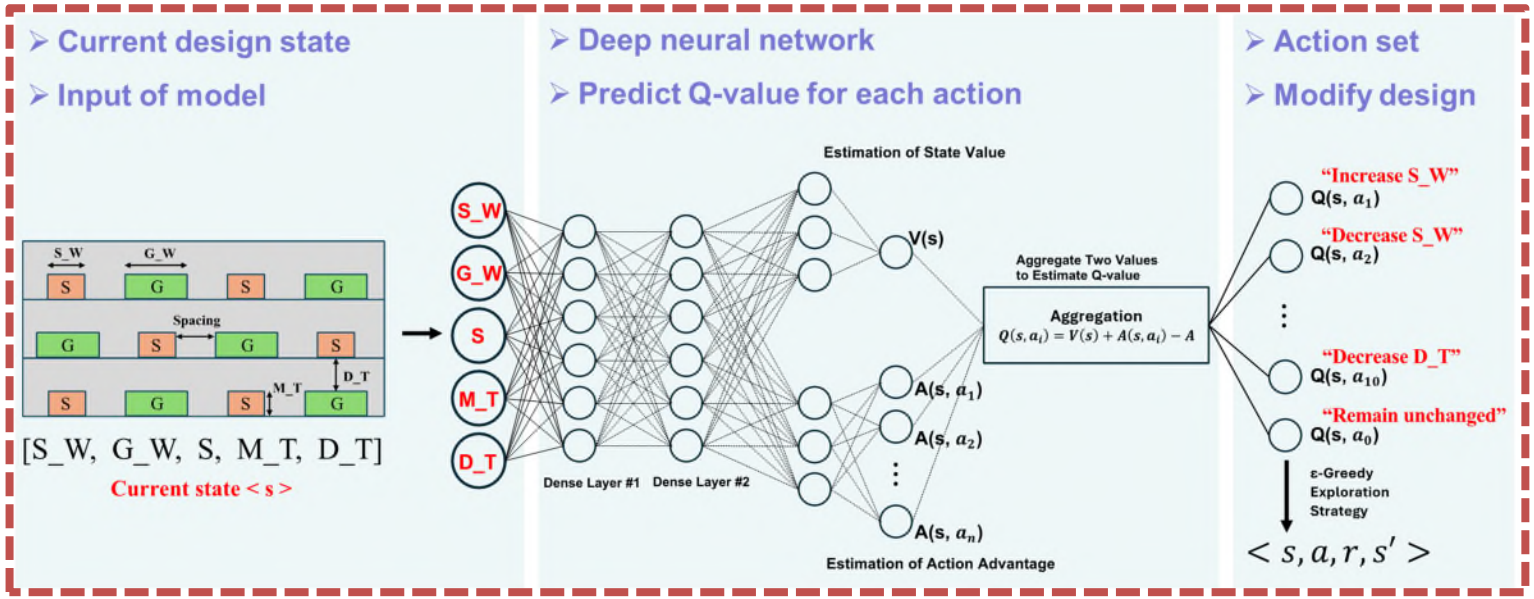
- A reinforcement learning model is trained to automatically design the package-level power distribution network with 28 power domains to supply power for a multi-chiplet system.

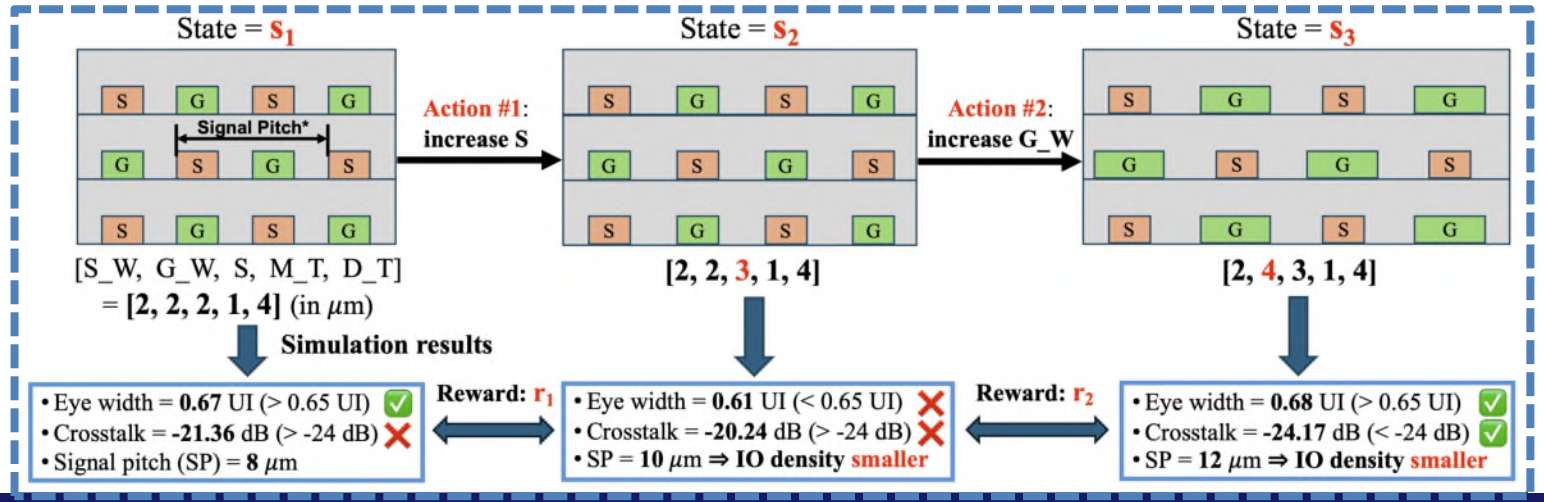
Collaborated with:

Agency for Science, Technology and Research SINGAPORE

Design Optimization for Signal Integrity (ESTC 2024)

3. CoWoS chiplet interconnection optimization with reinforcement learning





Innovation:

- A RL-based framework is proposed to automatically optimize S/G line arrangements in CoWoS interconnects.

Highlights:

- Optimize SI for high-speed data rates (up to 32 GT/s), achieving up to 24.67% improvement in eye width and 22.3 dB reduction in crosstalk.
- Reduce design time, enhances signal quality, and enables higher interconnect density, paving the way for more efficient chiplet-based systems.
- 2024 IEEE ESTC Student Travel Award

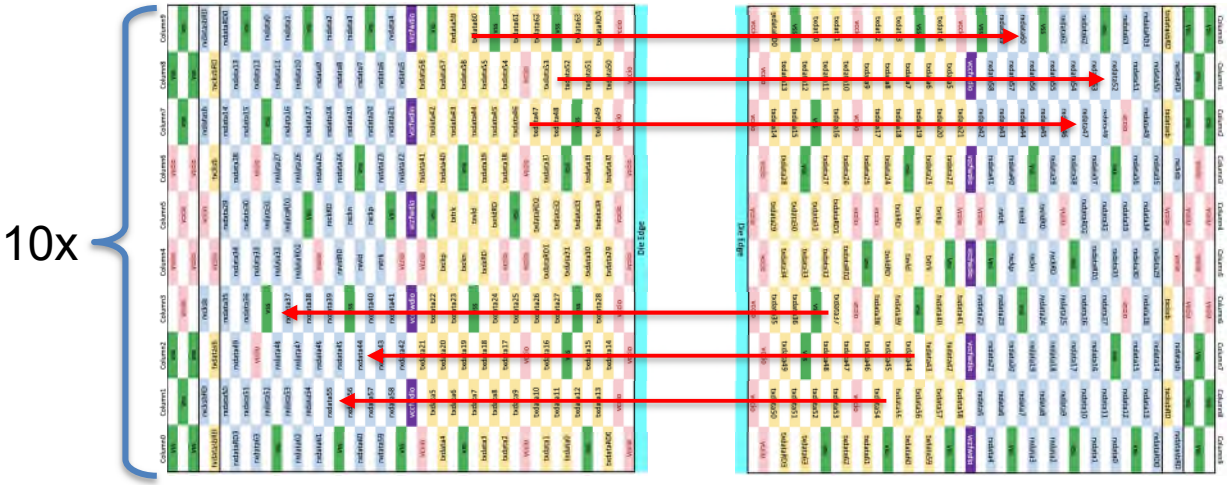
Collaborated with:

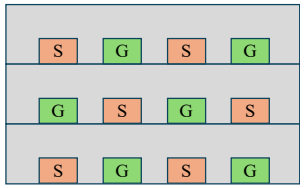
Agency for Science, Technology and Research SINGAPORE

Design Automation for Signal Integrity (ECTC 2025)

4. Automatic signal routing for UCIe bridge with reinforcement learning

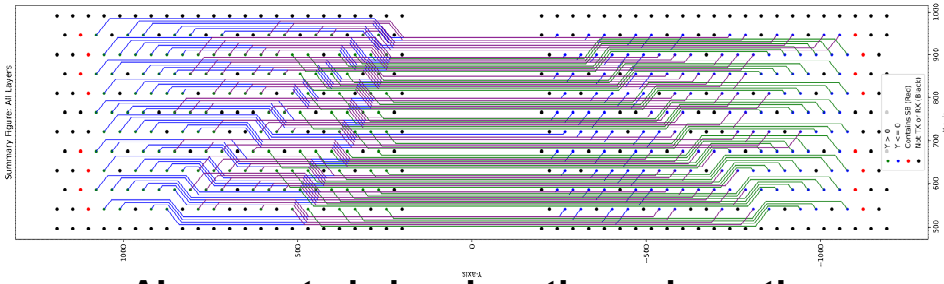
- **Design environment and constraints**



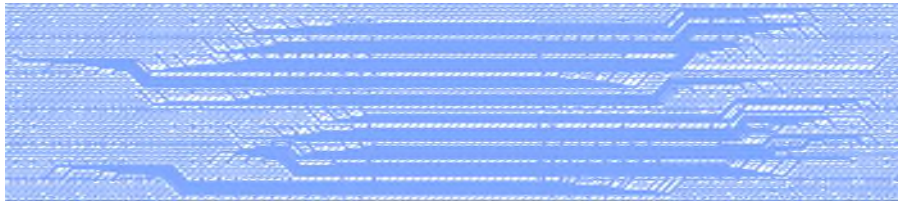


- 8/10/16-column, bump pitch 25/45/55 um.
- Signal line must be width/space = 2/1 um.
- Follow G-S-G staggered structure.

- **Design results from AI model**



AI-generated signal routing schematic



Convert to layout design (GDS file)

Innovation:

- AI-driven automatic routing framework to optimize UCIe bridges between chiplets with varying bump map configurations.

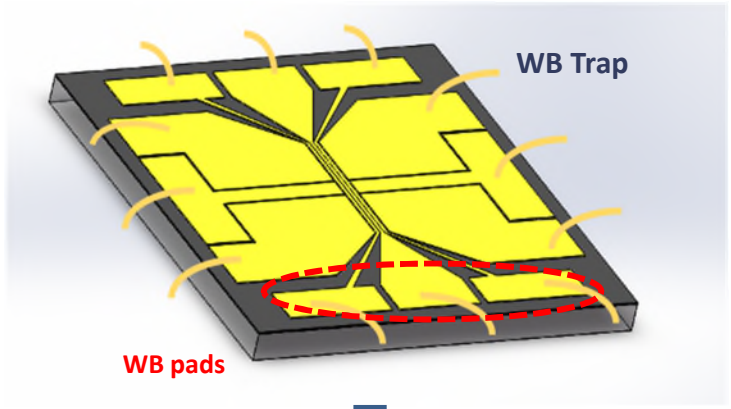
Highlights:

- Generate valid routing designs in a few minutes, meeting UCIe specs and design rule check while reducing manual effort and avoiding detours/extra-vias common in manual designs.
- Scale for heterogeneous chiplet integration, accelerates design cycles, and ensures high-performance chiplet interconnects.

Liner ion trap with TSV integration

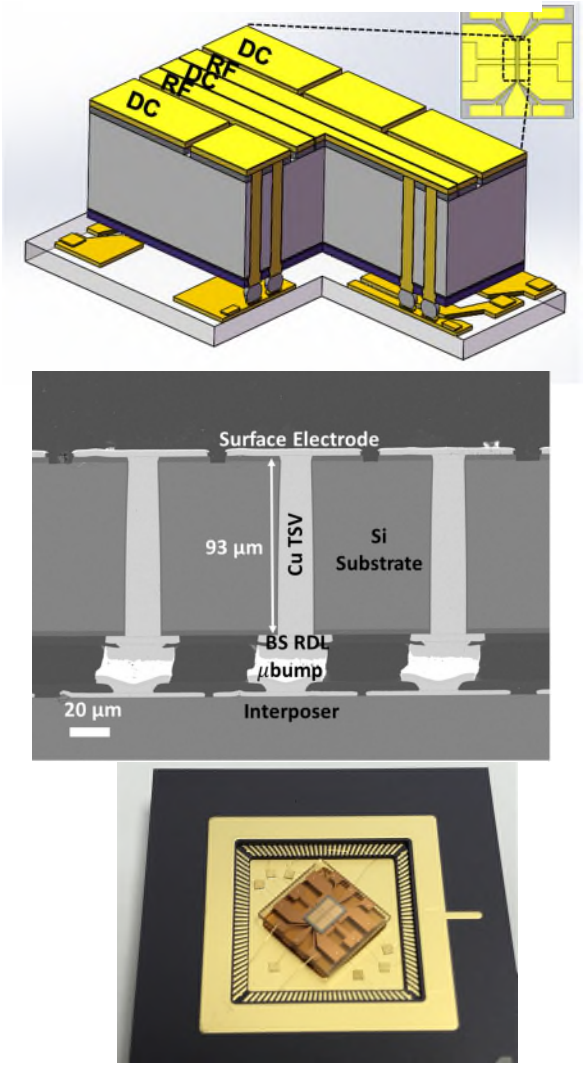
Funded by A*STAR / QTE

Trap W/WO TSV integration

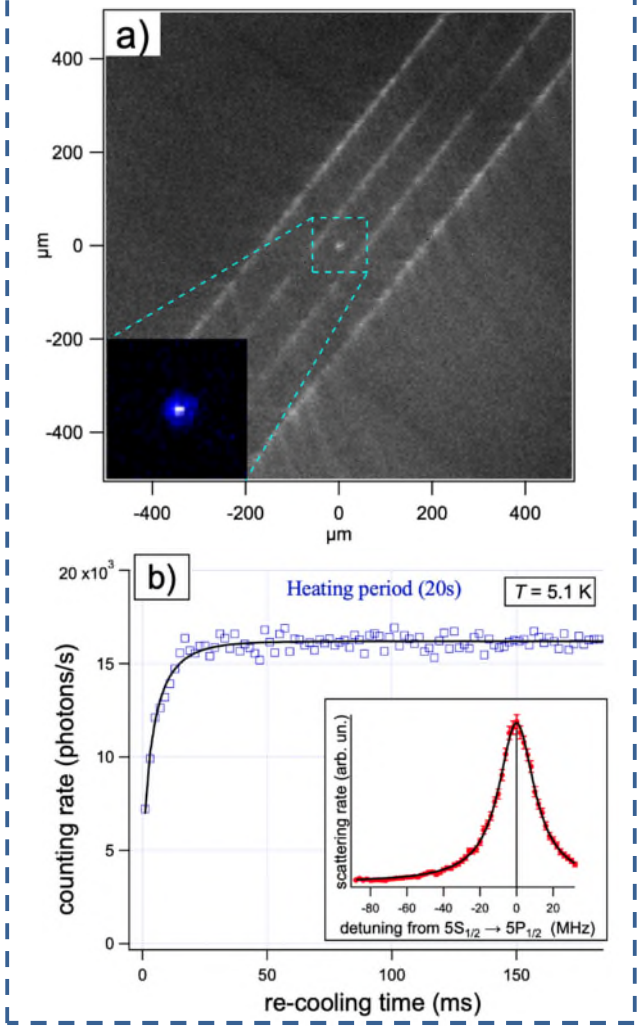


- High flexibility for electrodes design (RDL, TSV and micro bump)
- Clear laser path
- Comparable heating rate and lifetime

TSV Integrated liner trap

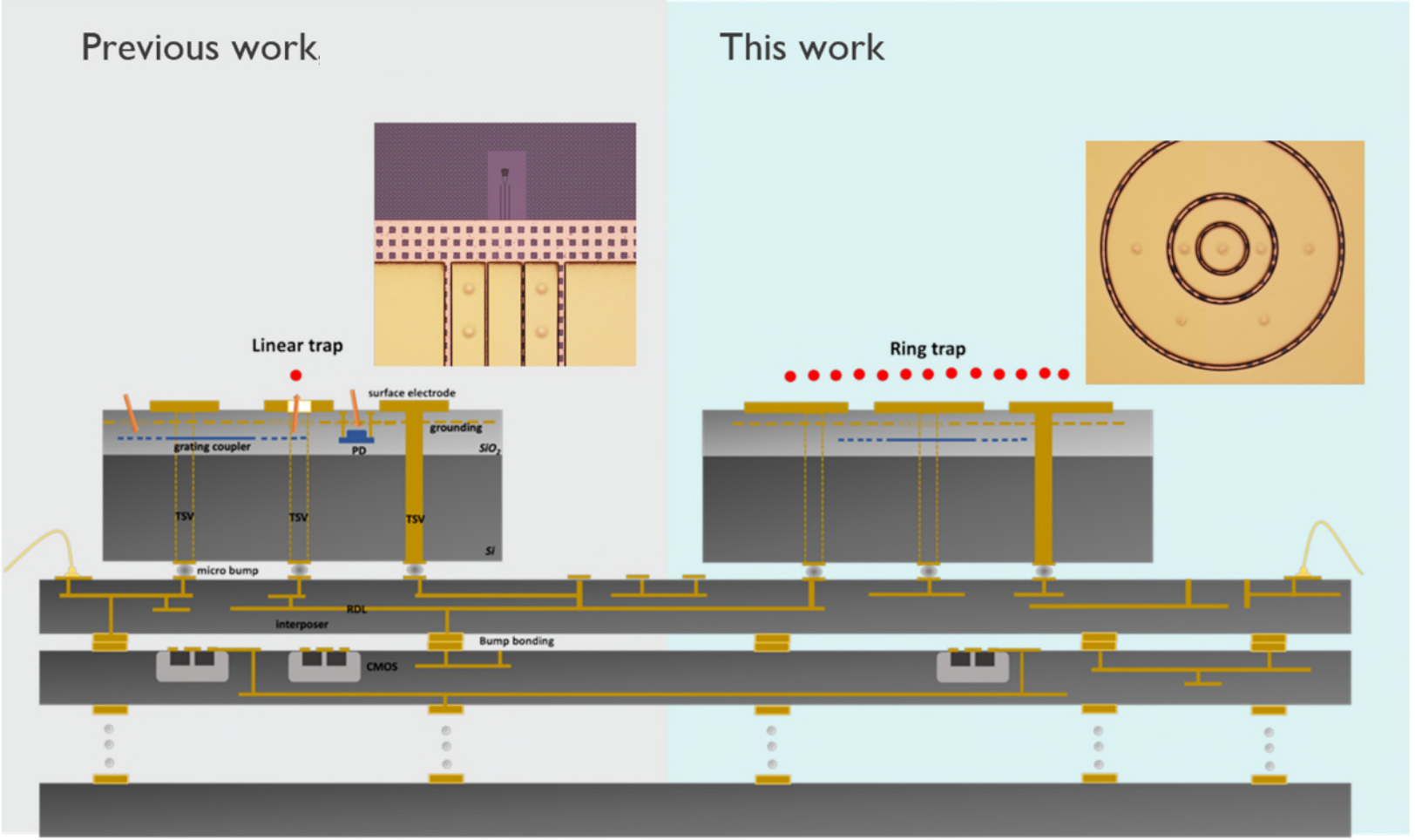


TSV Integrated liner trap- ion Trapping performance



Zhao, Peng, et al. *Applied Physics Letters* 118.12 (2021).

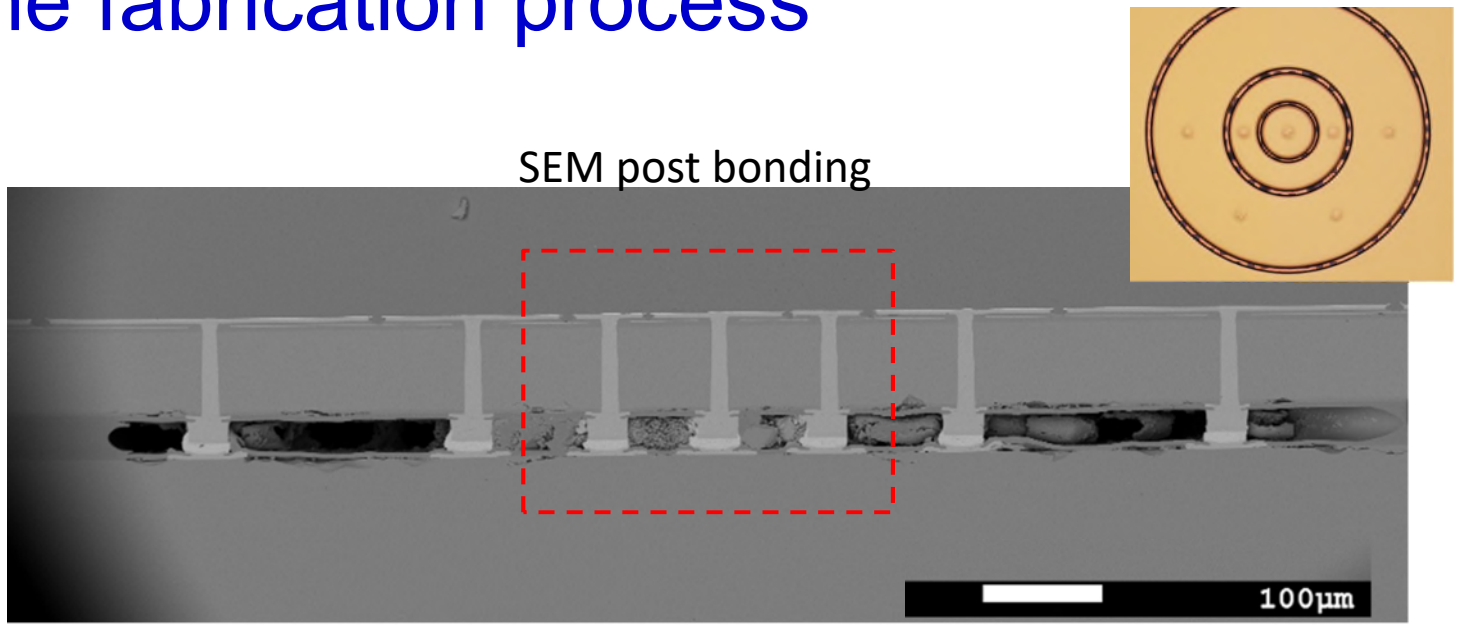
Ring and liner trap - the big picture



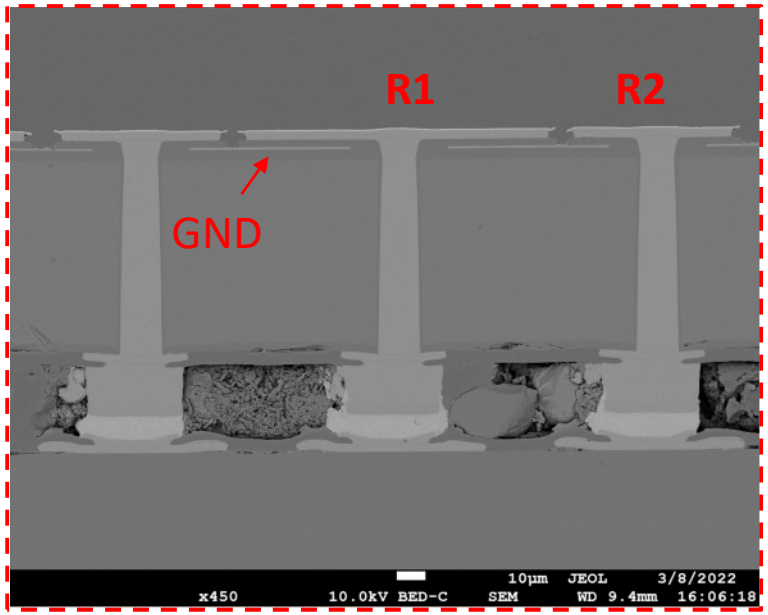
- **Liner trap for logic operation**
- **Ring trap for storage + optical communication (if needed)**
- **Photonics integrated in Si substrates**
- **RDL routing in interposer**
- Interposer functionality to be boosted by W2W bonding
- **<u>3D + Quantum</u>**

The fabrication process

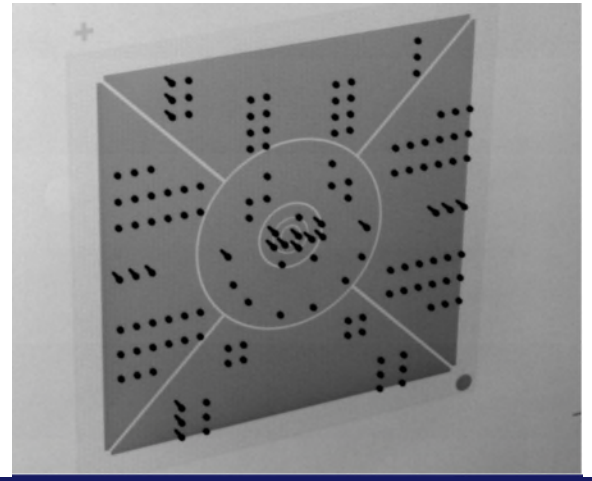
SEM post bonding



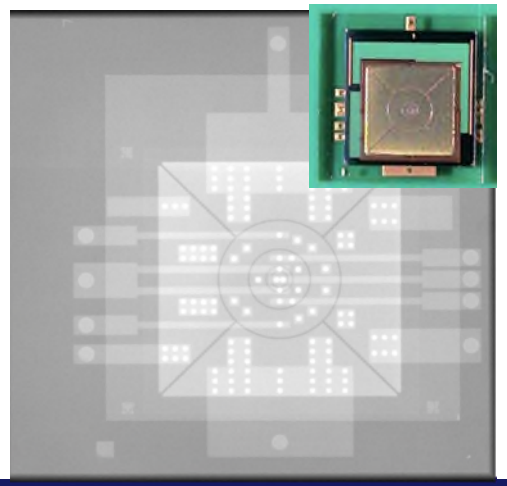
SEM post bonding



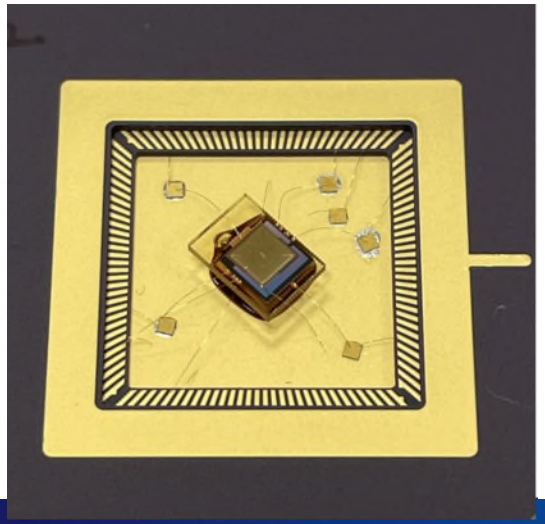
X-ray image of Si die



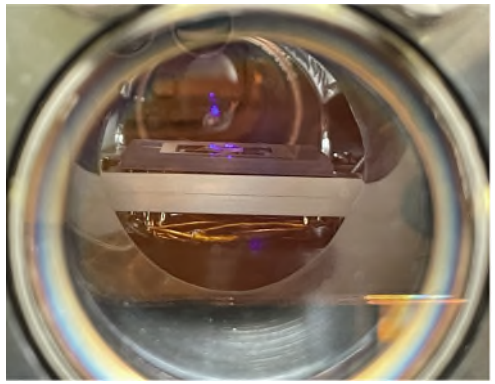
X-ray image post bonding



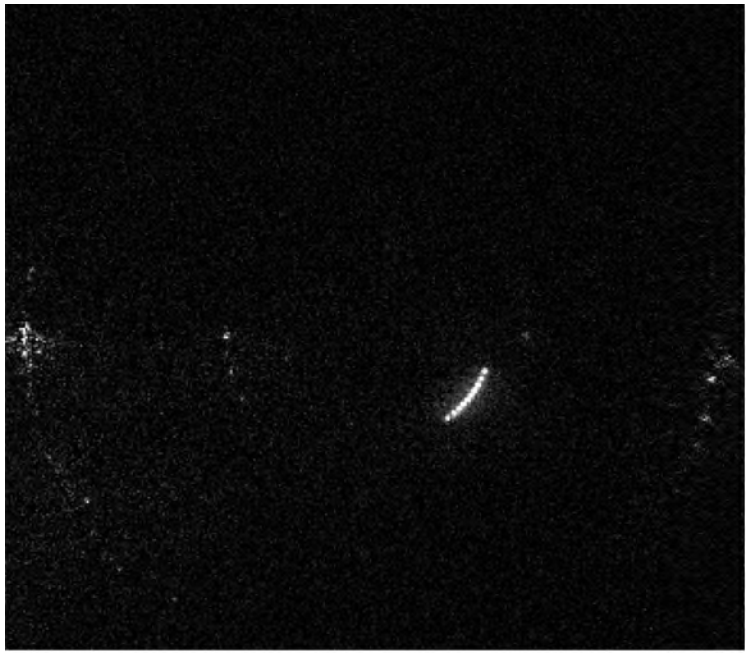
Post assembling into CPGA



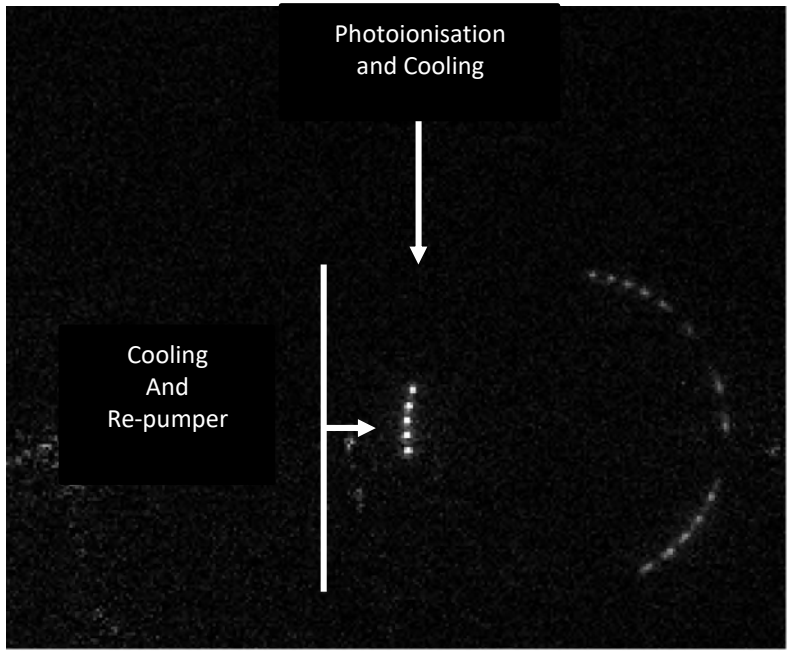
Ion trapping experiment



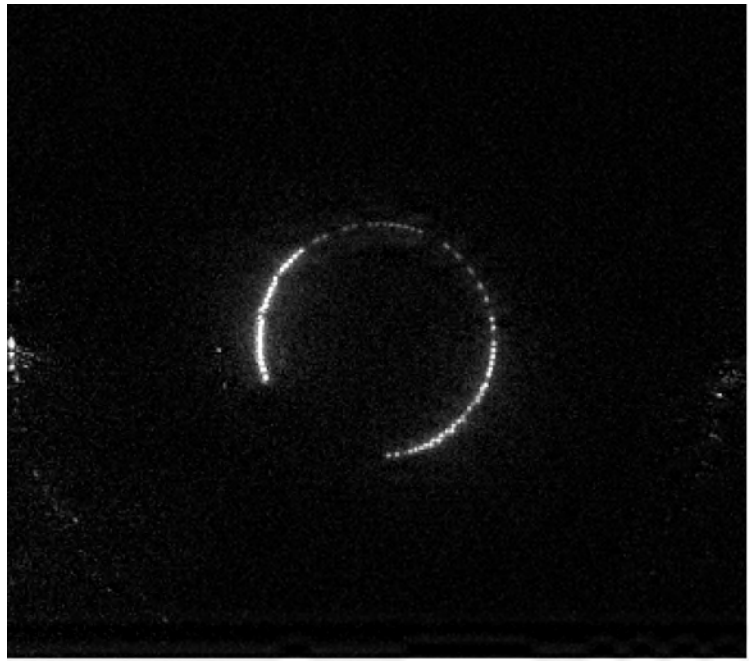
Localized ions



Add more ions

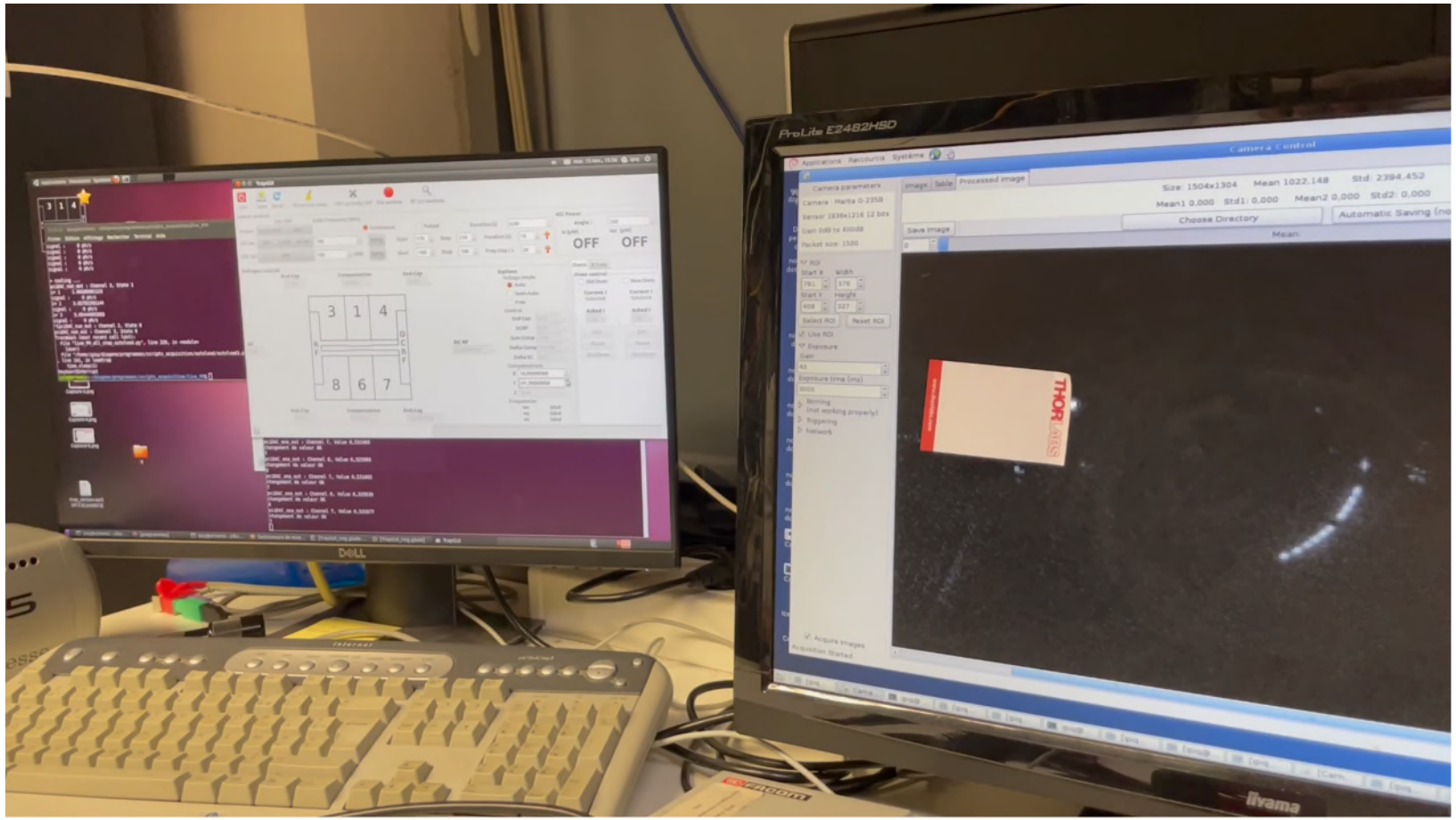


Spreading out ion ring



- Two laser cooling directions perpendicular to each other
- The ions are created and initially trapped in the zone where the photoionization beams are focused and are then free to move along the ring

Ring manipulation demonstration

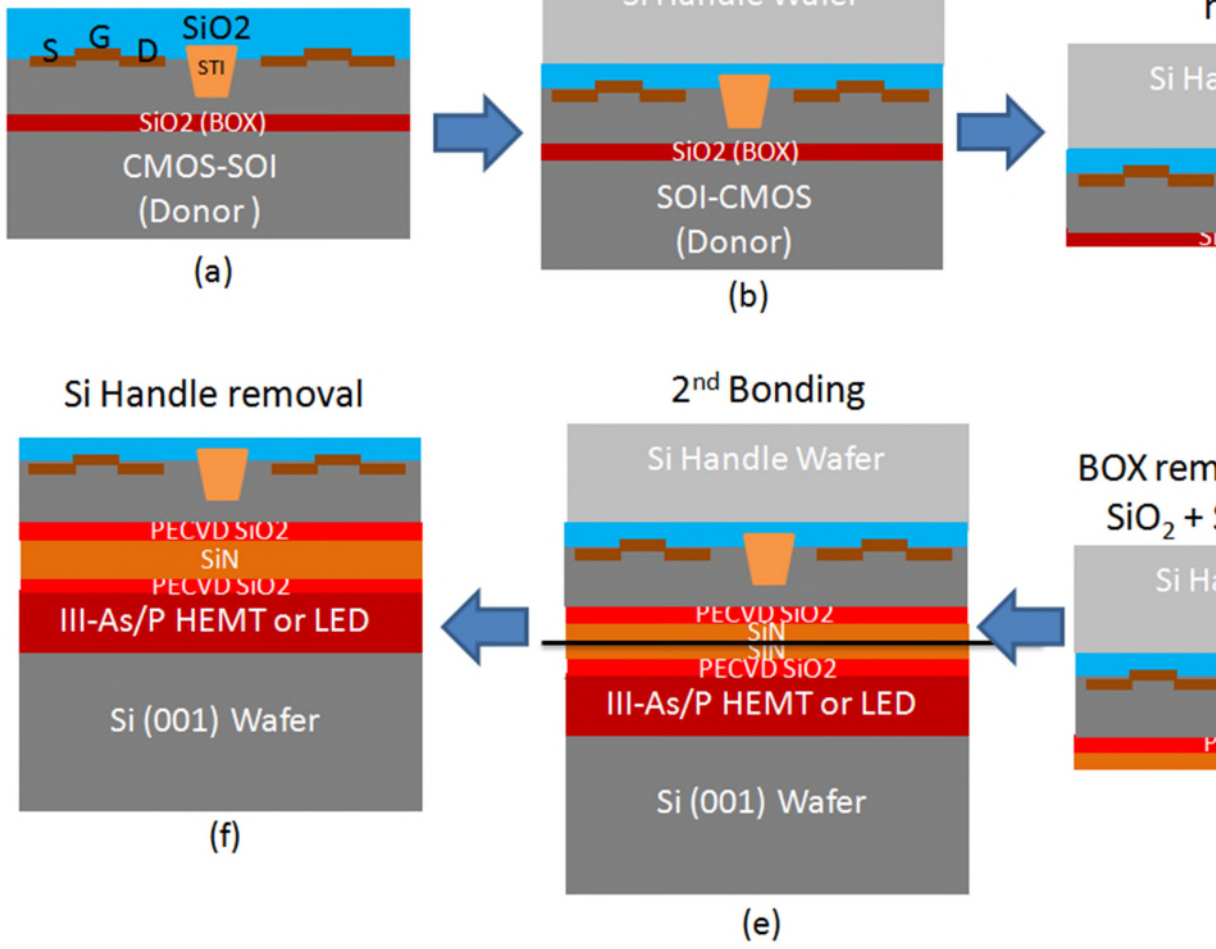


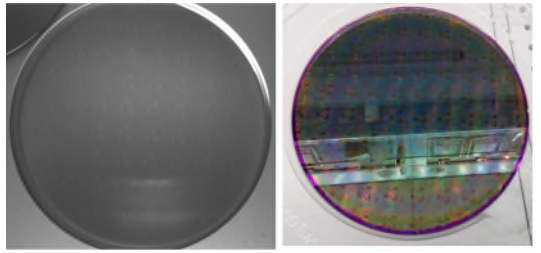
- Ring manipulation between free-rotation and ‘localized stabilization’

Discussion Points

- Enablers for Advanced Packaging
  - Cu-Cu bonding
  - Nano-TSV
  - ML/AI-assisted design optimization (SI, PI)
  - Use-case: Integrated Ion-trap
- Engineered Substrates
  - X-OI
  - GaN-LED + CMOS
- Introducing WISDOM and NCAIP

Bonding approach for Si-CMOS + III-As/P HEMT





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Discussion Points

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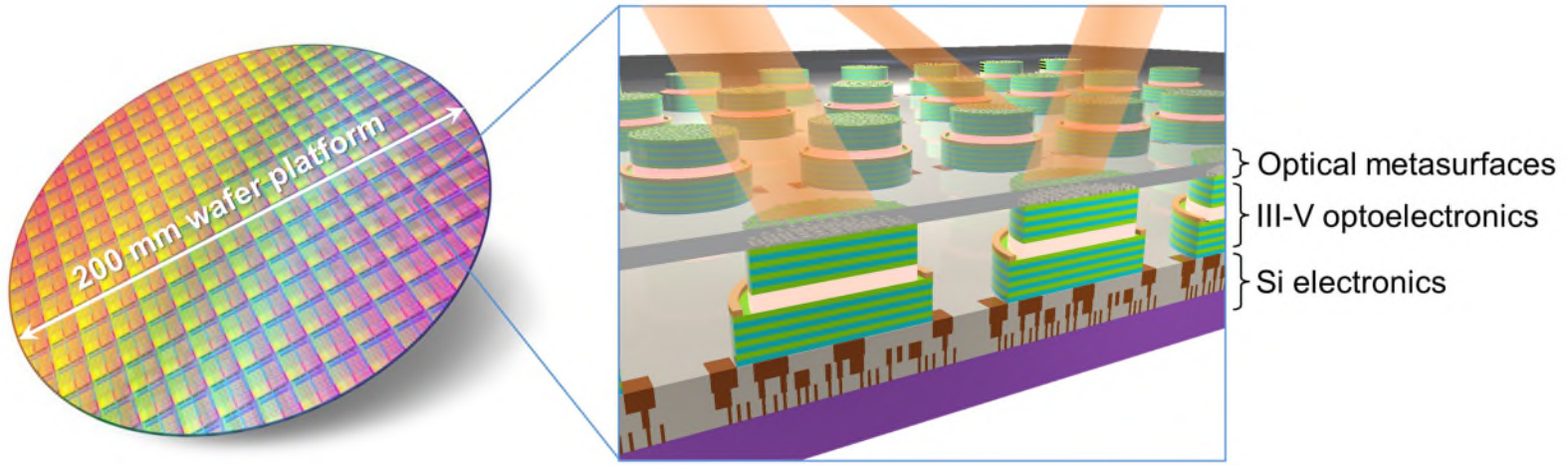
New Program: Wafer-scale triple integration

WISDOM

Wafer-scale Integrated Sensing Devices based on Optoelectronic Metasurfaces



- **Optoelectronics:** surface-emitting lasers, micro-LEDs
- **Electronics:** Si CMOS backplane for control, light detection, and signal processing
- **Optical metasurface:** manipulates emission direction, spectrum, polarization, etc.

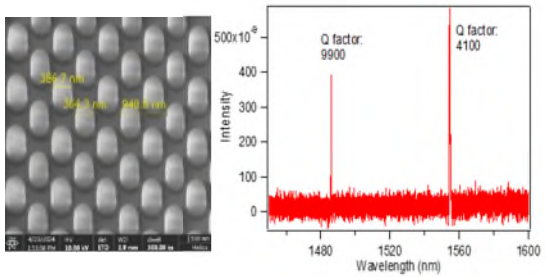
Funded by NRF at SMART

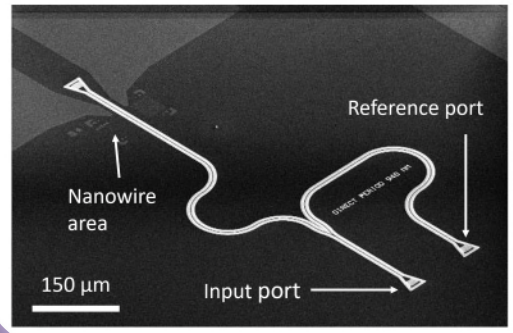
National Centre for Advanced Integrated Photonics (NCAIP)

NCAIP Vis … m and topological photonics, … roundbreaking technologi…

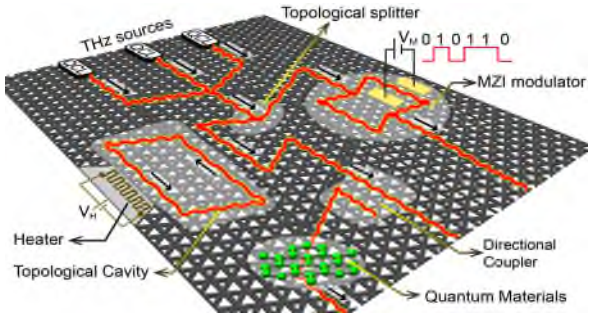
Advanced Materials for Heterogeneous Integration

Materials Screening and CMOS-Compatible Integration





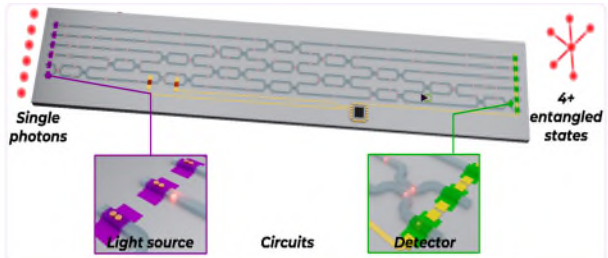
Integrated Topological Devices



(0.1-60 THz) for 6G and sensing

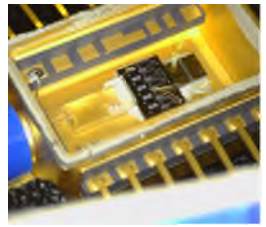
Integrated Quantum Devices

>4 on-chip entangled photonic

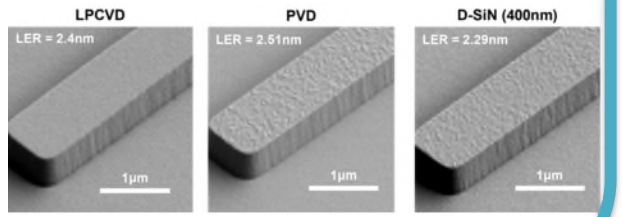


Reduce fibre-to-chip coupling loss to improve photon generation rate.

Advanced Silicon Photonics Platforms



CMOS-Compatible Si-laser, GeSn PD, AlN, SiN TFLN WGs. Scale to 8- or 12-inch wafers.



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Co-Director, National Center for Advanced Integrated Photonics (NCAIP)

Principal Scientist (Joint Appointment), A*STAR Institute of Microelectronics

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Biography:

Chuan Seng Tan is a Professor of Electronic Engineering at the School of Electrical and Electronic Engineering at Nanyang Technological University, Singapore. He received his PhD from MIT in 2006. Currently, he is working on process technology of three-dimensional integrated circuits (3-D ICs), as well as engineered substrate (Si/Ge/Sn) for group-IV photonics. He has numerous publications (journal and conference) and IPs on 3-D technology and engineered substrates. Nine of his inventions have since been licensed to a spin-off company. He co-edited/co-authored five books on 3D packaging technology.

He is a Fellow of IEEE (Class of 2022) and a recipient of the Exceptional Technical Achievement Award from the IEEE Electronics Packaging Society (EPS) in 2019. He was a Distinguished Lecturer with IEEE-EPS from 2019-2023. He is a Fellow of the International Microelectronics Assembly and Packaging Society (IMAPS) since 2019 and a recipient of the William D. Ashman - John A. Wagnon Technical Achievement Award in 2020.

He was the Chair of the Interconnections Sub-Committee for ECTC'2021. He was the General Chair of the 2020 IEEE Electronics Packaging Technology Conference (EPTC). He is currently an Associate Editor of IEEE Transactions on Components, Packaging and Manufacturing Technology, and received the Best AE Award in 2021. He is a member of the Technical Working Group of the Heterogeneous Integration Roadmap (HIR) on wafer-level packaging. He serves as an elected Member-at-Large to the IEEE EPS Board of Governors from 2022-2024.