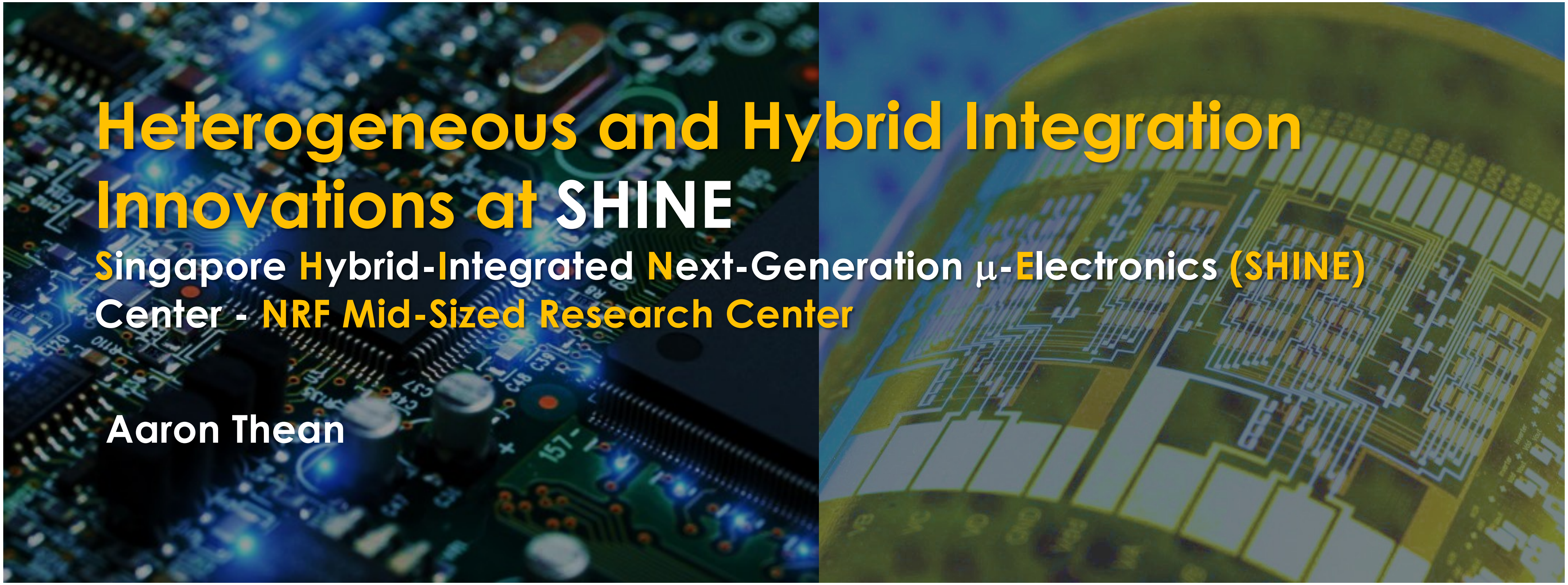
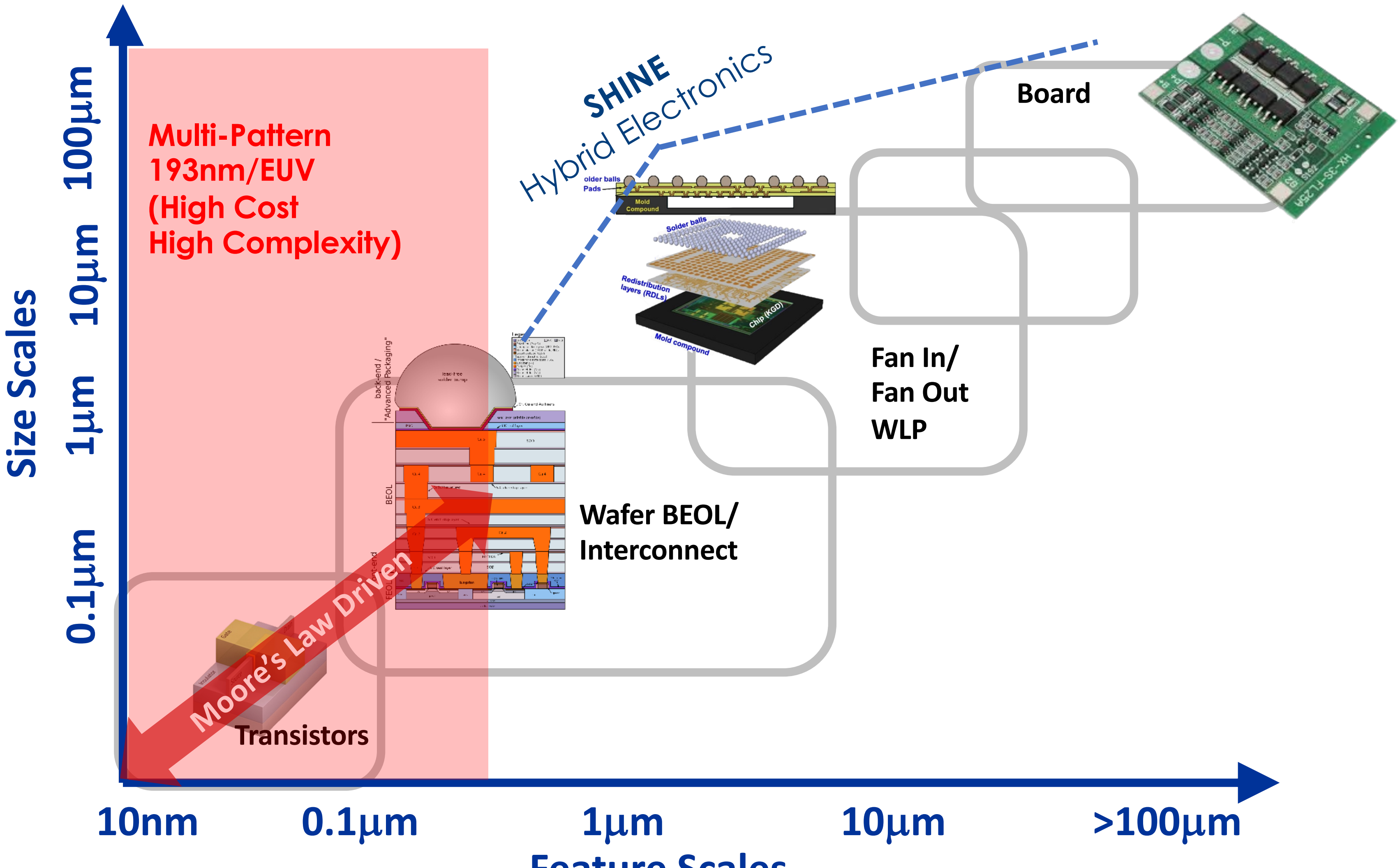


Heterogeneous and Hybrid Integration Innovations at SHINE

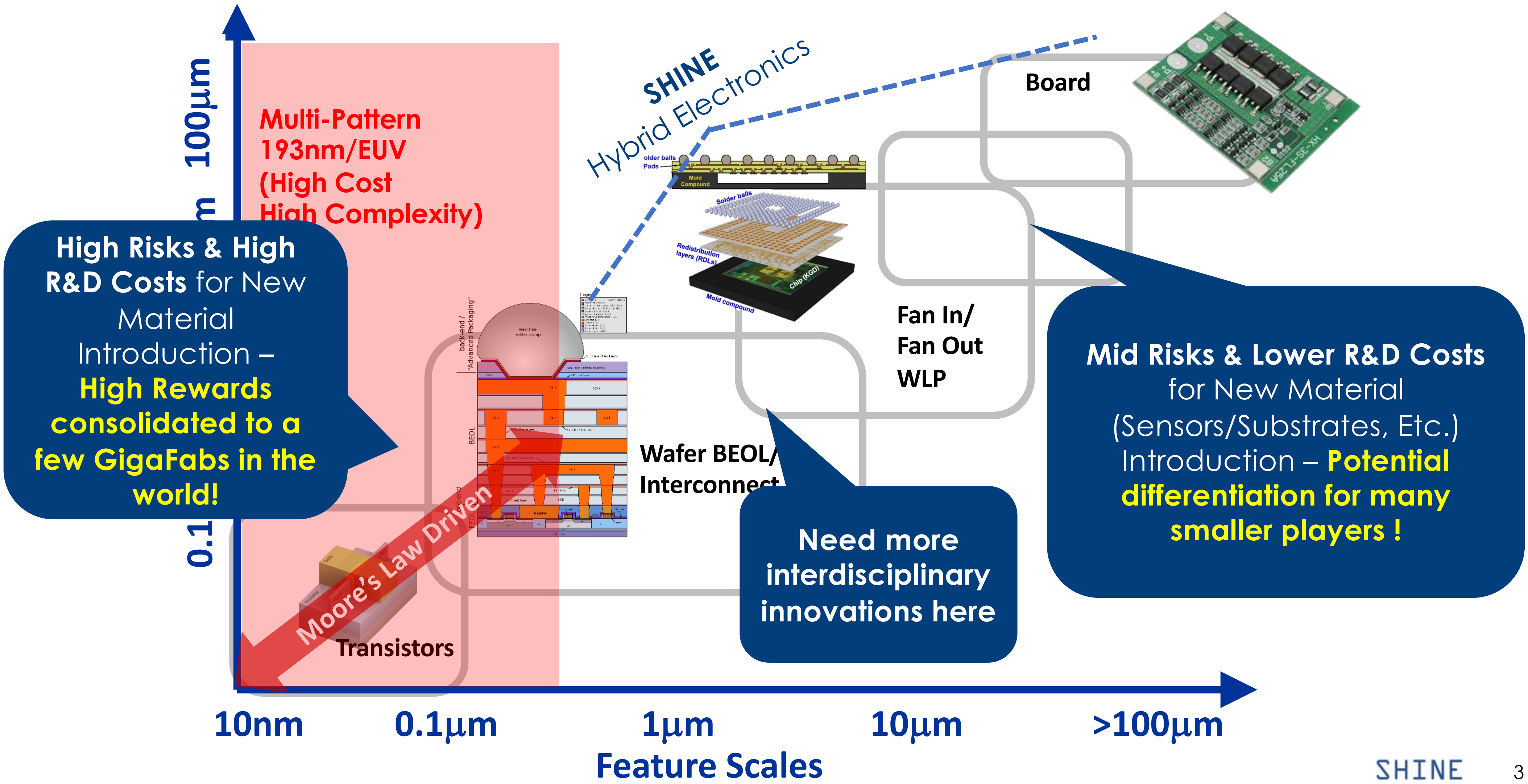
Singapore Hybrid-Integrated Next-Generation μ-Electronics (SHINE) Center - NRF Mid-Sized Research Center

Aaron Thean

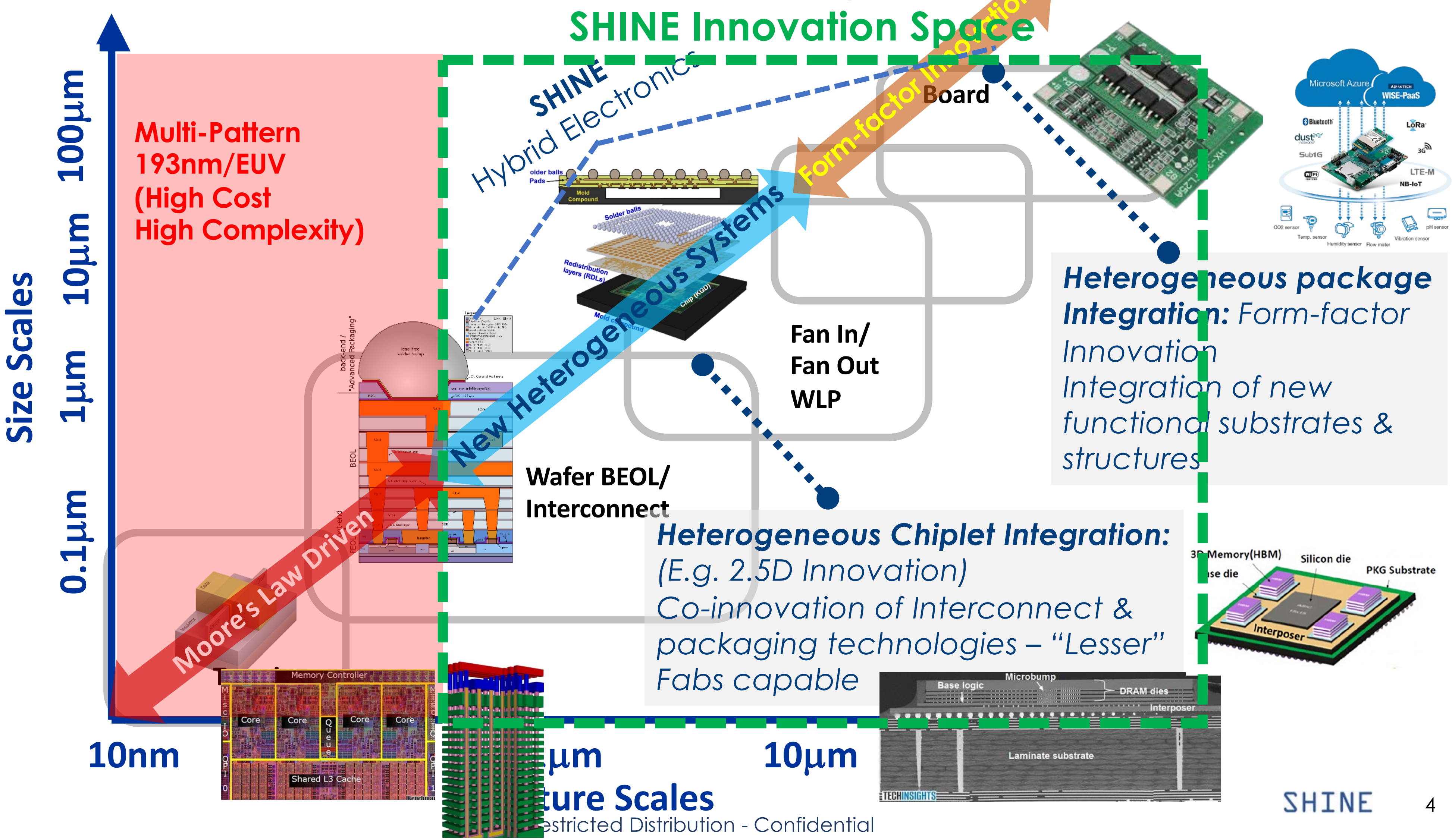
Multiple Levels of Integration



Multiple Levels of Integration

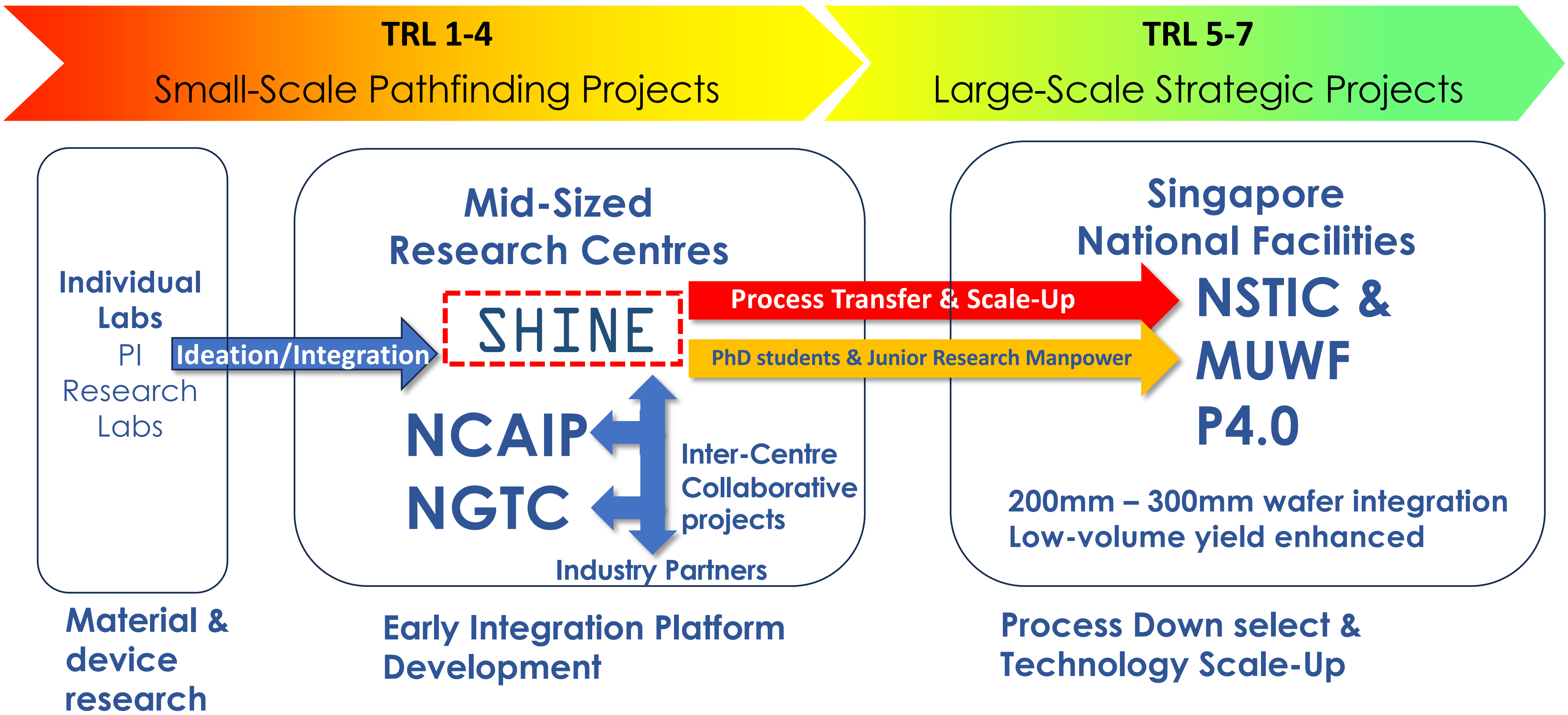


Multiple Levels of Integration



SHINE Partnerships

SHINE's Alignment to National Semi R&D Pipeline



Restricted Distribution - Confidential

As of 3 Oct 2024

Our Partners

Material/Process/Equipment Supply Chain

soitec

APPLIED MATERIALS® make possible

NEOCERA MAGMA

Design Services Supply chain

cadence

Technology Manufacturing Receptacle

Potential manufacturing partners

GLOBALFOUNDRIES®

amf ADVANCED MICRO FOUNDRY

Micron®

tsmc

Application Drivers/Receptacles

DSO

Continental

POET Technologies

MARVELL™

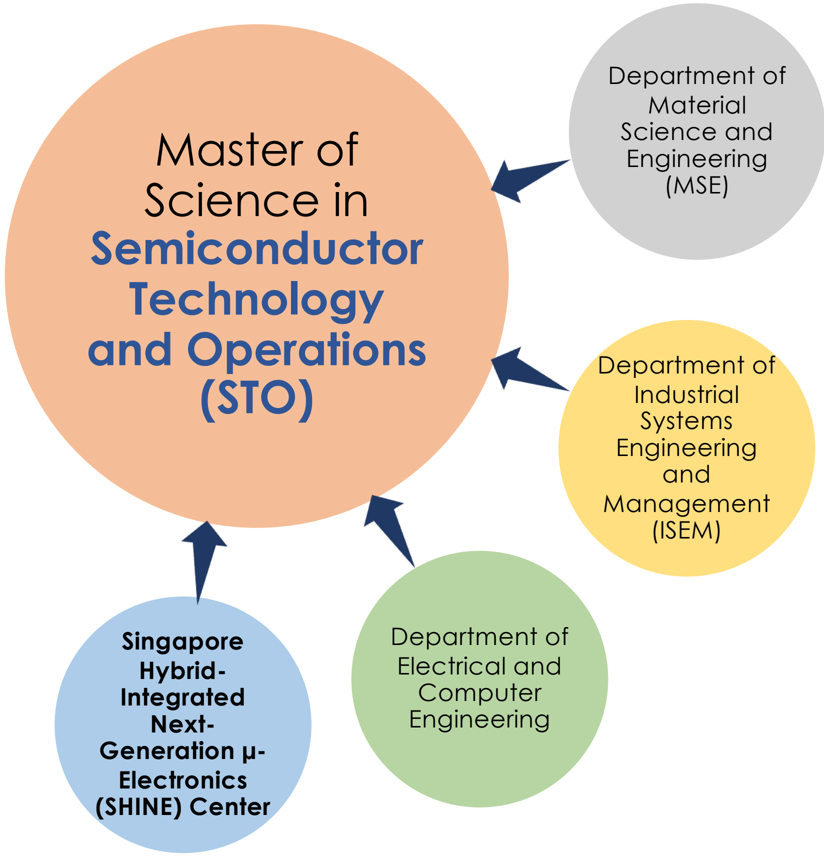
AMD

National Beneficiaries

MINDEF SINGAPORE

- Aerospace Industry
- Heterogeneous Microelectronics/ Packaging Industry

Bridging Academia with Industry for a Robust Talent Pipeline



Full-time Students: 1 year (min)/2 years (max)

Part-time Students: 2 years (min)/4 years (max)

Key Highlights

- Multi-disciplinary Training to Develop **Next Generation Semiconductor Talent** with Strong Technology and Operation skills
- An Executive-style Teaching Approach, Guest Speakers, and A Highly Interactive Environment with Veterans from Semiconductor Industry
- Job Scope Based **Graduate Certificates** Stackable to The MSc, and Option for **Internship** at Well-known Multinational Companies

Overview

Expected Cohort Size for August AY2025 Intake

100 Students
(YoY Growth of ~300%)

Launched in:
Aug 2024

Hosted by: NUS National University of Singapore – Department of Electrical & Computer Engineering, College of Design and Engineering; SHINE – Singapore Hybrid-Integrated Next-Generation μ-Electronics Centre

Industry Partners Interested in Providing Internships for SHINE Master Programme

Center Capabilities

SHINE's Shared Facilities & Infrastructures

NANYANG TECHNOLOGICAL UNIVERSITY SINGAPORE

SHINE @ NTU: School of Materials Science & Engineering

- ~200 m^2 class 10k cleanroom
- Soft Composite Material Processing System
- Customized Flexible Circuit Board Fabrication System
- Integrated Packaging System

SHINE @ NUS: Expansion of E6NanoFab

- 150 m^2 Class 10k cleanroom: Device Level Pick-&-Place Integration, On-Chip Integration of Lenses, Back-end-of-line Processing and Packaging, Non-Destructive MFI Fault Isolation
- Dry Laboratory: Unique Thermal Effect Investigation Capability, Co-Package Photonics Measurement Capability

NUS E6NanoFab

- Full 8" (200mm) Wafer Processing Capability
- Material and Device Characterization Labs
- Wide Range of Materials and Devices Processing Tools
- Clean Room Area: 1189 m^2
- Dry Lab area: 1081 m^2
- Wet Lab area: 477 m^2

NUS National University of Singapore


Nordson
NAT21- 0036
Nordson
DAGE
S250G

SHINE's Process Capabilities

SHINE's Heterogeneous Integration Capabilities (Die/Small Wafers)

Simulation/ Design

Interposer/Waveguide/Micro-ring resonator Fabrication

Deposition
- Ultra high vacuum metal and dielectric sputtering system, AJA UHJ
- E-beam evaporator, AJA UHV
- Atomic layer deposition (ALD), Picosun
- Plasma enhanced chemical vapour deposition (PECVD), Oxford
- Black magic CVD
- Molecular beam epitaxy system (MBE), ULVA

Annealing Process
- Rapid thermal processing(RTP), Annealsys
- Magnetic annealing system, TEL
- Horizontal Furnace, Ultech
- Rapid thermal annealing (RTA), MILA3000

Lithography
- Electron beam lithography(EBL), Raith
- EBL, Elionix
- MA8 Mask aligner, SUSS
- Laser writer, Hiedelberg DWL66+
- MA6 Mask aligner, SUSS
- MicroWriter, DMO ML3 Pro

Etching
- O3 stripper
- Ion beam deposition and etching, SCIA
- Xenon difluoride (XeF_2) etcher
- Plasma asher, Samco
- Integrated inductive couple plasma (ICP) etch, Oxford

Optical lens/Interconnects

3D Printing
- 3D printer, Optomec Aerosol
- High resolution 3D Printer, Nanoscribe

Assembly/HI Integration(mictorings, laser diodes)

BEOL
- Automatic grinder, single spindle, DISCO
- Fully automatic SD laser system, DISCO
- Fully automatic die separation system, DISCO
- **Auto Milling, Grinding and Polishing System(est delivery by June 2025)**

Packaging
- Fineplacer die bonder, Finetech
- Micro Transfer Printing, X-Celeprint
- Die & flip chip bonder, ASM Amicra NANO
- Laser solder jetting system, Pactech
- 4000Plus bond tester, Nordson DAGE
- Surface mount screen printer, ASMPT
- VSU35 infrared vacuum reflow soldering system, Invacu

Characterisation /FA/ Testing
- FESEM, FIB-SEM
- Ellipsometer
- 4 Point Probe Station
- Surface profiler
- AFM/SPM, Bruker & Park
- Raman/PL micro-spectroscopy
- Cryogenic Probe station
- XRD, RIGAKU SmartLab
- Infrared & thermoreflectance thermography system, Microsanj
- **Magnetic field imaging system, Neocera Magma(Commissioning in Mar 2025)**
- **Silicon photonics probing & measurement system***
- **Microfabrication system**

New Capabilities in 2025

Chiplet-to-Chiplet Photonics Communication and Computation

Si photonics interposer

Waveguides and MZI

1) PECVD deposition of Si3N4 layer on Si substrate
2) HSQ mask layer coating
3) Electron beam lithography for mask layer
4) ICP IRE Ar plasma etching

Interconnects

1) Ti/Al electron beam deposition
2) Photo litho
3) Dry etching
4) Rapid thermal annealing in N2

BEOL control circuit fabrication

1) Ti/Al electron beam deposition for bottom gate
2) Photo litho
3) Dry etching
4) ALD HfO2 gate dielectric layer
5) Annealing in Furnace
6) Photo litho
7) Dry etching
8) Sputtering of IGZO channel layer
9) XRD, AFM, Raman spectroscopy, EDX tests
10) Photo litho
11) Dry etching
12) ALD HfO2 gate dielectric layer
13) Photo litho
14) Dry etching
15) Ti/Al electron beam deposition for source and drain and interconnects
16) Photo litho
17) Dry etching
18) ALD HfZrO2 gate ferroelectric layer
19) Photo litho
20) Dry etching
21) Ti/Al electron beam deposition for top gate
22) Photo litho
23) Dry etching

LiNbO3 photonics components

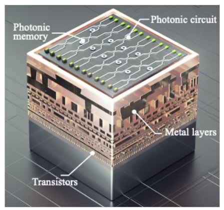
1) HSQ mask layer coating on LiNbO3 substrate
2) Electron beam lithography for mask layer
3) ICP IRE Ar plasma etching

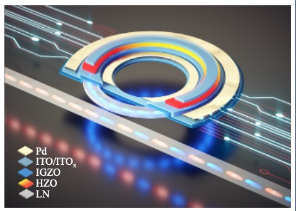
Component integration on Si interposer

1) Laser bonding on SiC heat spreading die
2) SiC heat spreading bonding on Si interposer
3) Solder jetting on contact pads on Si interposer
4) Chiplets flip-chip bonding on Si interposer
5) Photo detector bonding on Si interposer
6) 2 photon polymerization of optical interconnects from chiplets, lasers, photo detectors to waveguides
7) Ring resonator micro transfer on Si interposer

Top electrode and interconnects

1) Ti/Al electron beam deposition
2) Photo lithography
3) Dry etching
4) Die shear, optical, thermal, and electrical tests

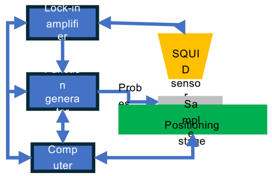


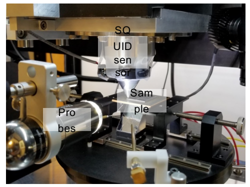


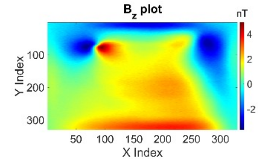
Machine Learning Guided Failure Analysis & Diagnostic Capability Development for Next-Gen 3D-IC Packaging

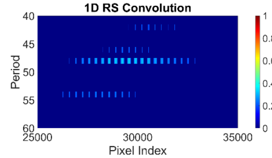
Machine Learning Guided FA & DCD for 3D-IC Packaging

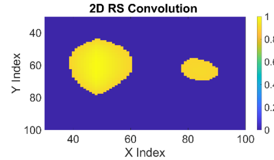
1. Bz data as obtained from SQUID measurement
2. Calculate fundamental period by 1D convolution of Ramanujan Sum vector with MFI vector
3. Generate magnetic cluster pair by 2D convolution of Ramanujan Sum circulant matrix with MFI
4. Calculation of Mahalanobis dispersion distance, DD, multiplied by pixel size gives Z height

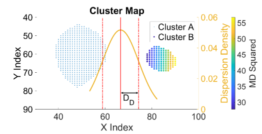












Hybrid Flexible RF System for the next generation communication

SiC interposer

CPW/interconnects

1) PECVD SiO2 dielectric layer
2) Ti/Al electron beam deposition
3) Photo litho
4) Dry etching
5) Rapid thermal annealing in N2

BEOL control circuit fabrication

1) Ti/Al electron beam deposition for bottom gate
2) Photo litho
3) Dry etching
4) ALD HfO2 gate dielectric layer
5) Annealing in Furnace
6) Photo litho
7) Dry etching
8) Sputtering of IGZO channel layer
9) XRD, AFM, Raman spectroscopy, EDX tests
10) Photo litho
11) Dry etching
12) ALD HfO2 gate dielectric layer
13) Photo litho
14) Dry etching
15) Ti/Al electron beam deposition for source and drain and interconnects
16) Photo litho
17) Dry etching

Interposer singulation

1) Back side grinding
2) Chemical mechanical polishing (CMP)
3) Stealth dicing
4) Die separation

Component assembly on interposer

1) Solder ball jetting
2) Flip chip bonding of RF power amplifier, phase shifter
3) Die shear, electrical, and thermal tests
4) Wire bonding and packaging

Component integration on flexible substrate

Integration of interposer

1) Plasma treatment
2) Aerosol jet printing of flexible metallic interconnects
3) Infrared vacuum reflow sintering
4) Surface mount screen printing of contact pads
5) Surface mounting of SiC interposer
6) Infrared vacuum reflow soldering

Integration of strain sensors

1) Plasma treatment
2) Aerosol jet printing of adhesive layer
3) Sensor transfer on flexible substrate
4) Aerosol jet printing of flexible metallic interconnects
5) Curing in Oven

Integration of antenna array

1) Plasma treatment
2) Aerosol jet printing of adhesive layer
3) Sensor transfer on flexible substrate
4) Aerosol jet printing of flexible metallic interconnects
5) Curing in Oven

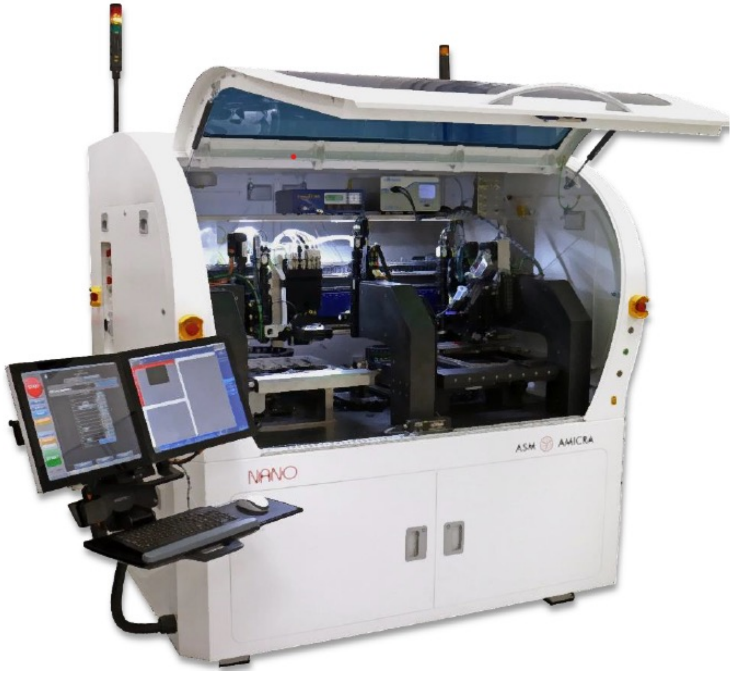
Thermal management structure integration

1) Plasma treatment
2) 3D printing of heat spreading polymer
3) Curing in Oven
4) 3D printing of polymer frame for PCM
5) Injection of PCM
6) Spray coating of carbon nanotubes layer on copper subtrate
7) Transfer of CNT layer
8) Thermal, RF, leakage, electrical tests

Special Additive Processing Capabilities

Strategic Packaging Capability Development:
Advanced BEOL-Packaging Capabilities

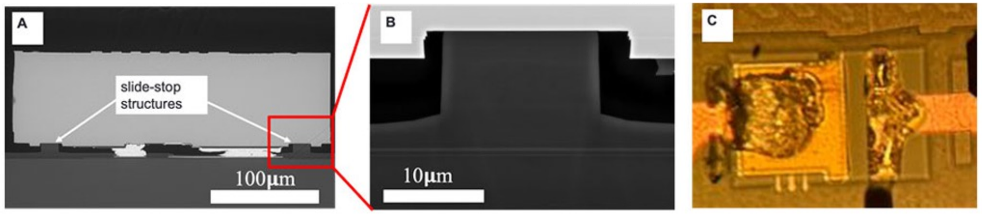
AMICRA Nano Ultra-Precision Die & Flip Chip Bonder



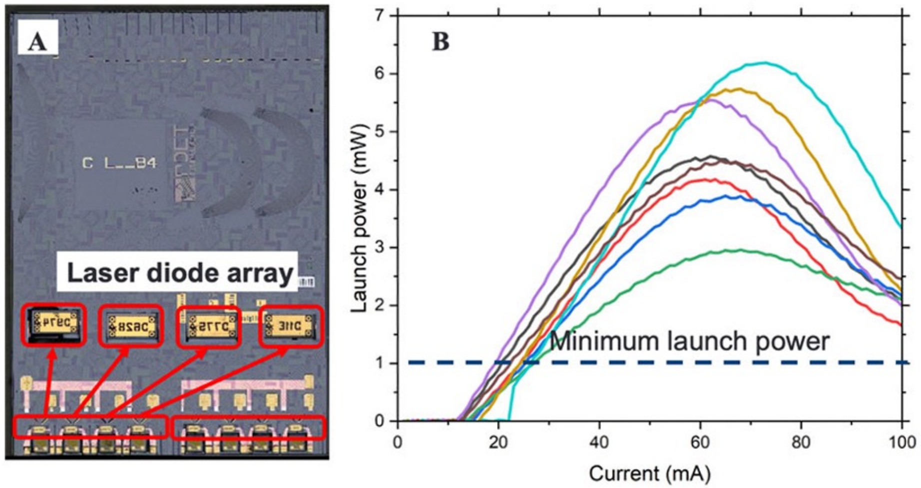
Highest Placement Accuracy in Its Class

Support ±0.3 µm @ 3 sigma placement accuracy

- Cross-section of bonded die-substrate



- Bonded laser bank of eight diodes & measured optical performance of the mounted diodes

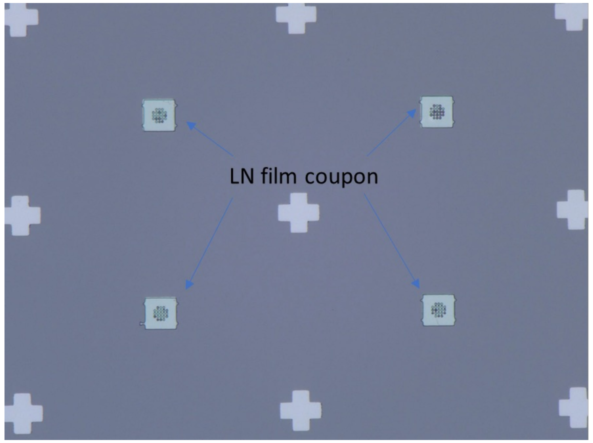


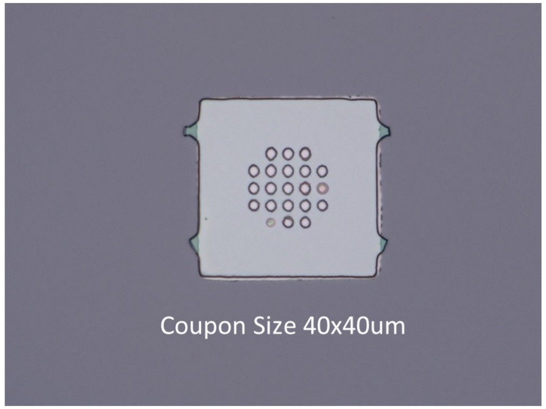
2022 European Conference on Optical Communication (ECOC).

Strategic Co-Packaged Optics Capability Development:
Micro Transfer Printing

AMICRA Nano
Micro Transfer Printing

Micro-Transfer Printing of Lithium Niobate (LN) on Silicon Photonic Integrated Circuits (PICs)





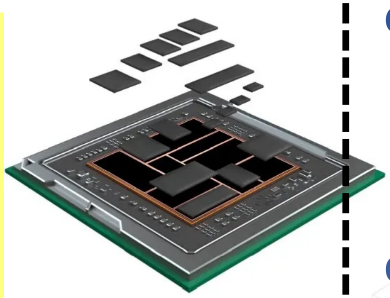
- Tight integration of large arrays of compound semiconductors (e.g., GaN, GaAs, SiC, SiGe, InP) with CMOS semiconductors and passive components (inductors and capacitors)
- Lower I/O density and higher current density interconnects.
- Ultra-thin, small footprint three-dimensional integrated circuits (3D ICs) versus a large footprint system-in-package (SiP).

Unpublished and confidential results.

Pick-&-Place Integration Scaling

Component Size & Thickness

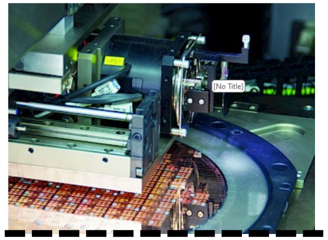
1cm	500 µm	Chips & Chiplets
5mm	100 µm	
1mm		Sub-Die Layers
		Sub-Die Components
0.1µm	< 50 nm	Lithography Limited Fragility Limited

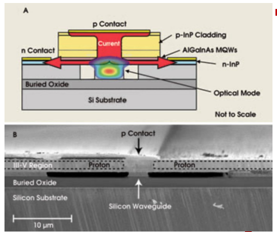


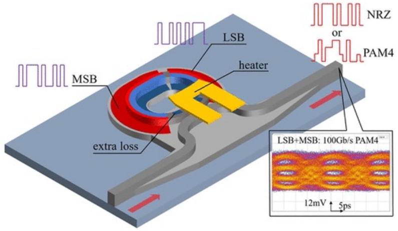
AMICRA NANO Die Bonder & Flip Chip Bonder

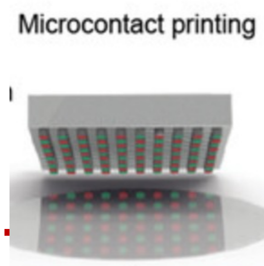
Placement accuracy $\pm 0.3\ \mu m$ @ 3 sigma and bonding of semiconductor components

Operational @ E6NanoFab (2023)









★ iTexel (At the Fragility Limit of Transfer)

0.1µm | 0.3µm | 0.5µm | 1µm

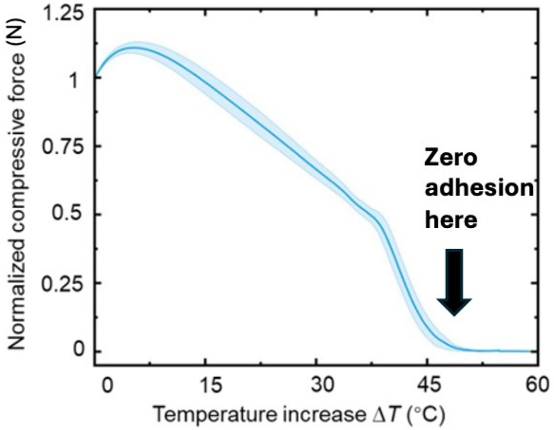
Alignment Accuracy

Next-Generation Micro-Contact Printing (in Research) iTEXEL

Breakthrough Dry Mass Transfer Printing Technology (By Assoc. Prof. Benjamin Tee)

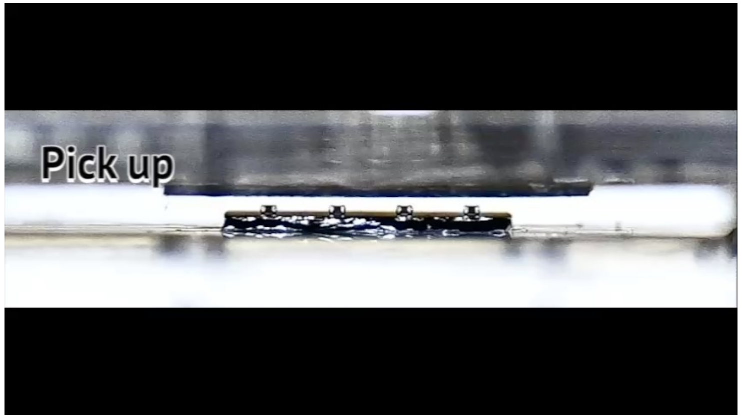
Key Features

- **Ability to Pick&Place Sub-100nm thick components !**
- **Real-time Programmable** – Photonics driven actuators
- **Precise** – Sub-100 micron resolution of pickup and placement
- **Consistency** – Multi-use, zero-adhesion capable transfers for micro/nano thin films

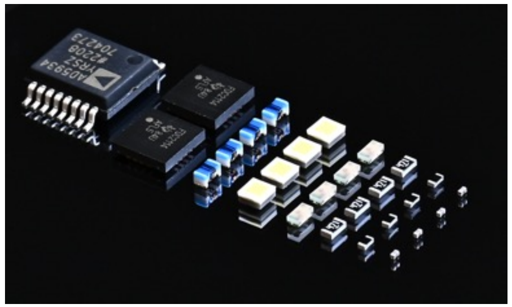


Low thermal budget (< 50C)

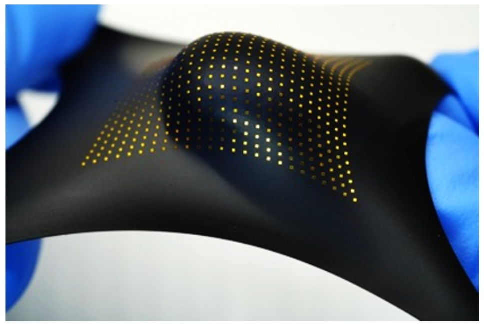
Transfer process video



Transfer SMD components



Transfer onto Elastic substrate



iTEXEL: Next-Generation Micro-Contact Printing (in Development)

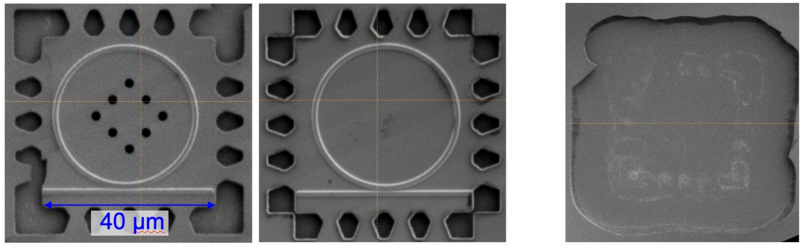
Demonstrated successful transfers of Fragile Thin-Film (300nm-600nm thick) lithium niobate photonic components (patterned)!

No Shearing Needed for Micro-transfers

High-speed Photonic Driven Actuations

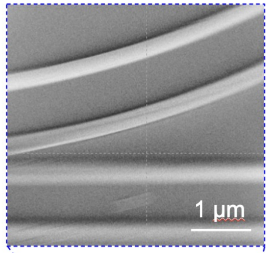
Scalable to 300mm (Goal)

Transfer < 100nm thick films (Goal)

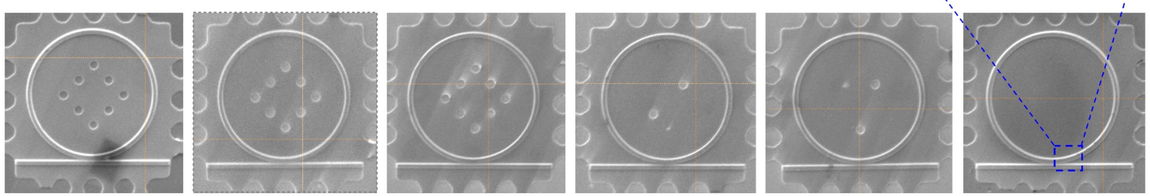


Fabricated micro-rings on wafer

After pick-up



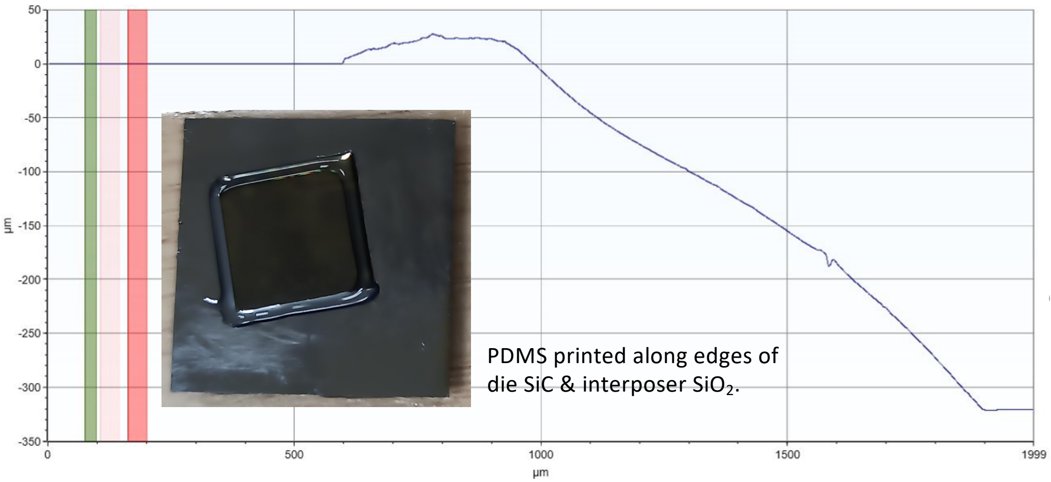
No nano-cracks post transfer!

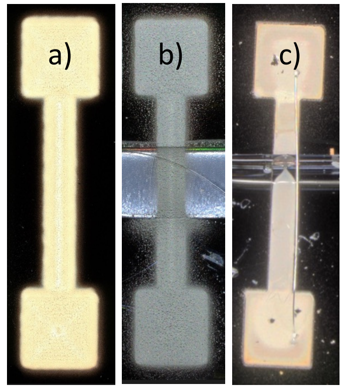


Released micro-rings on silicon substrate

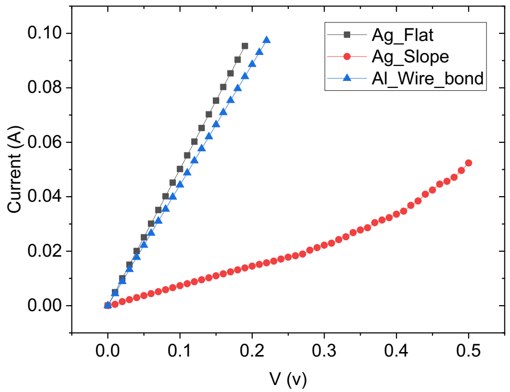
Strategic Co-Packaged Optics Capability Development:
Metallic Interconnect Printing for 2D & 3D Substrates

Optomex Aerosol Jet 3D Printing





Printed Ag on a) flat SiO_2 (hotplate sintered), b) PDMS slope (furnace sintered), c) Al wire bonded



Flat Ag print: R_s = 0.20 Ω/square, ρ = 1.40 µΩ.m (R = 2 Ω)
Slope Ag print: R_s = 1.38 Ω/square, ρ = 9.66 µΩ.m (R = 13.8 Ω)
Wire bonded Al: R_s = 0.23 Ω/square, ρ = 1.58 µΩ.m (R = 2.26 Ω)

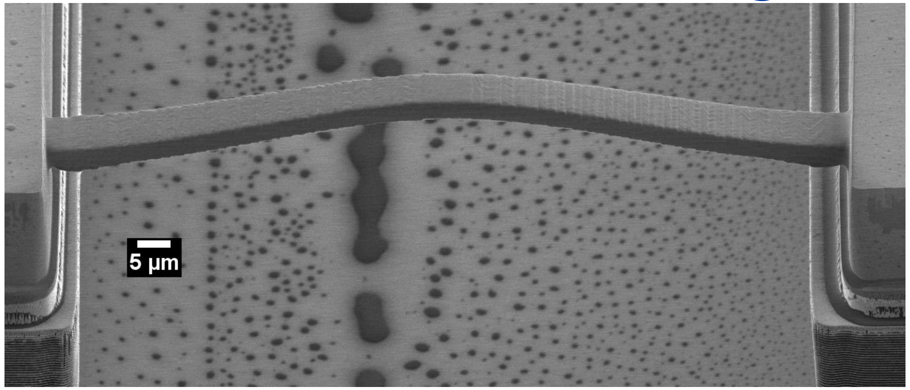
*parasitic limit practised by industry is 5 Ω/square

- Demonstrated metallic interconnects along the edges of die SiC and interposer SiO_2 with a resistance of 1.38 Ω/square, which meets industry standards for parasitic limits

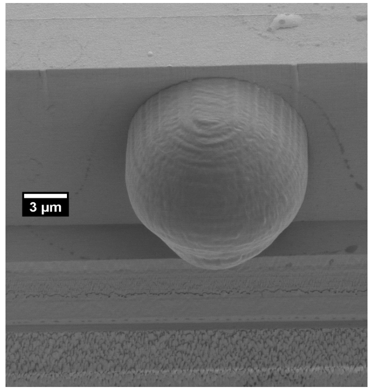
Unpublished and confidential results.

Strategic Co-Packaged Optics Capability Development:
On-Chip Hybrid Integration of Photonics using Lenses and PWB

3D Two-photon Lithography Printer – NANOSCRIBE GT2 (E6NanoFAB & Tee's Research Group)

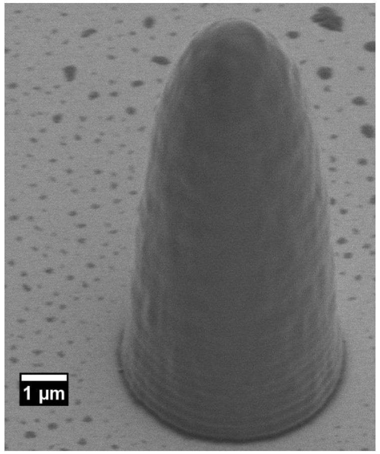


Chip-chip: Bridged PWB, 112x7x3.5 (µm)

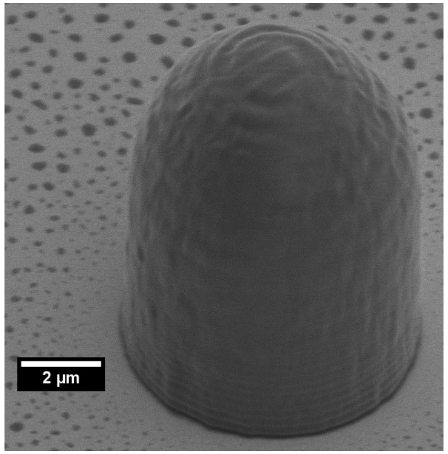


Lens at waveguide facet, dia 12µm

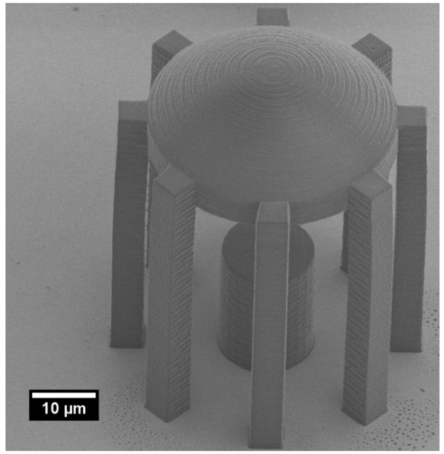
- Finest XY resolution 400 nm
- Finest vertical resolution 1µm



Parabolic High NA Lens (dia 5µm and h= 10µm)



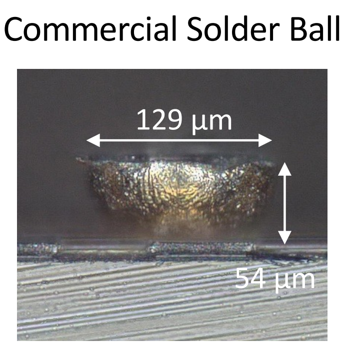
Hemispherical lens (dia 7µm, h= 12µm)

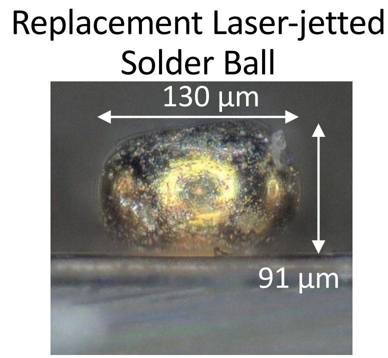


Beam Expander (dia= 40µm, h=60µm)

Low-Temperature Soldering Capability – Laser Integration
Advanced Laser Solder Jet Packaging Capabilities

- Support ±0.3 µm @ 3 sigma placement accuracy
- High solder alloy flexibility: Eutectic SnPb, high-lead SnBb, lead-free SnAg, SnAgCu, etc.
- Up to 10 balls/sec





shear strength	Commercial (g)	Laser-jetted (g)
Min	33.40	34.60
Max	43.86	48.74
Mean	39.23 ± 3.59	43.25 ± 4.71
Median	40.59	43.10
Range	10.47	14.14

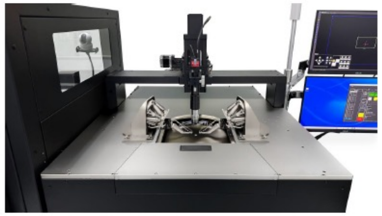
Extrapolation from AEC-Q100-010A standard:

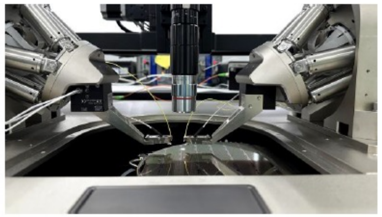
If diameter = 90 µm → shear strength = 20 g

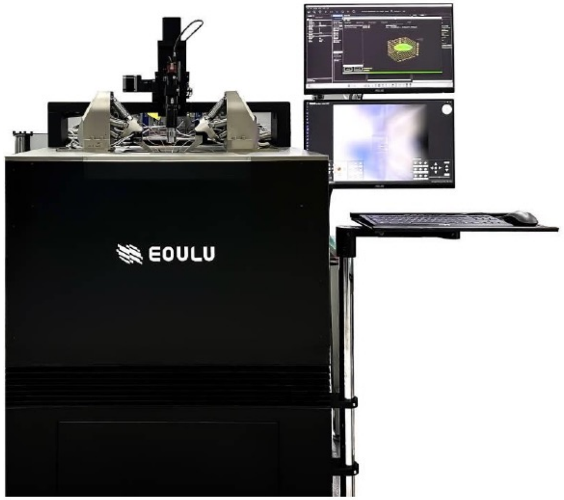
Special Test Capabilities

Strategic Co-Packaged Optics Capability Development:
Silicon Photonics Measurement and Probe System

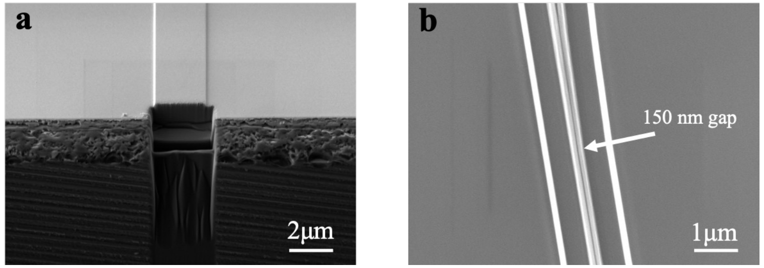
Integrates the functionalities and advantages of both measurement and probe systems into a single, efficient platform



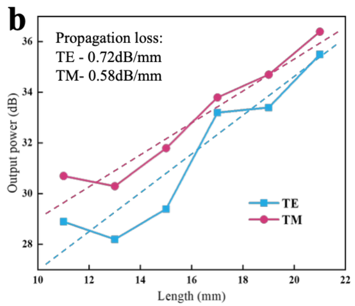




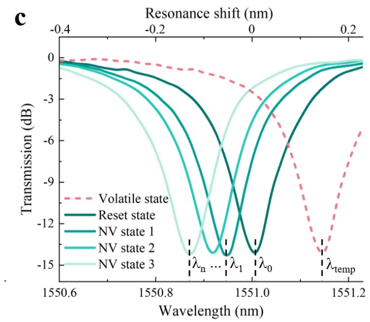
SEM images of critical areas of micro ring resonator (MRR)



Propagation Loss



MRR Transmission Spectra



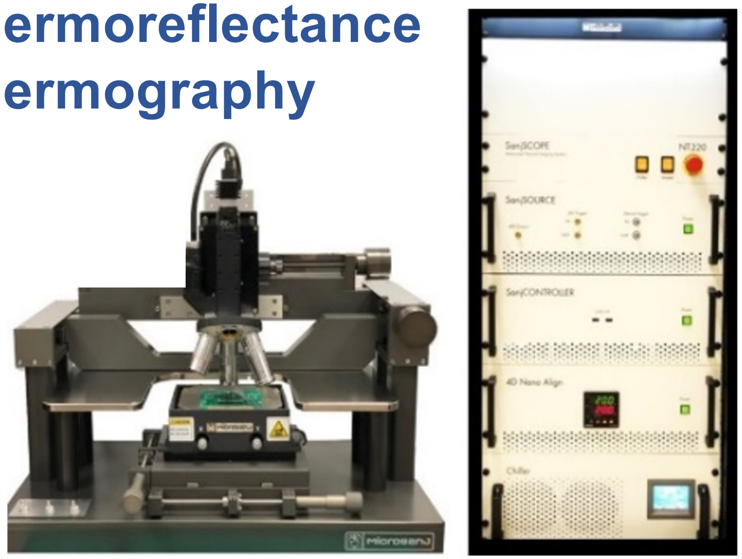
- Perfect for analyzing intricate photonic components like modulators, waveguides, and multiplexers.
- The futureC SIPH software ensures a user-friendly experience with its integrated control panel that manages both measurement and probing functionalities.

Unpublished and confidential results.

Strategic Metrology Capability Development:
Unique Thermal Effect Investigation Capability

Enable full spectrum thermal imaging and the study of heat conduction path.

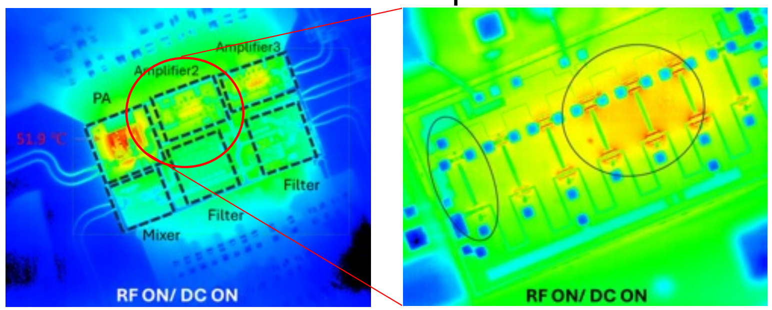
Infrared & Thermoreflectance Thermography



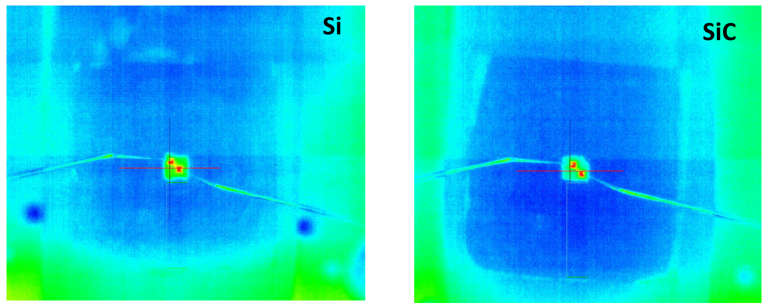
- Nanosecond Transient Thermal Imager for topside thermal imaging is a lock-in thermoreflectance-based (TR) system optimized in the visible band with diffraction-limited spatial resolution.

- Thermal failure analysis of through-silicon interposer for GaN and GaAs chips.

RF on Si Interposer



- In-situ heat spreading analysis of Si and SiC substrate



Unpublished and confidential results.

SHINE

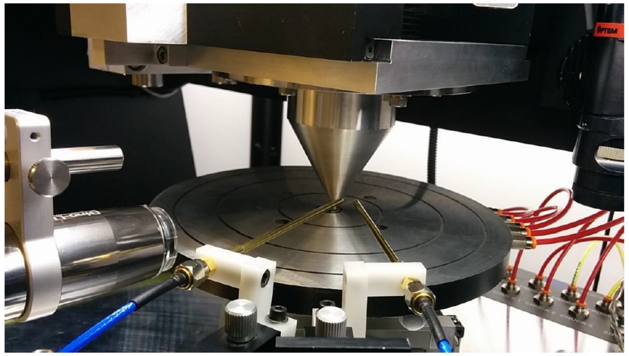
Non-Destructive Stacked-Chip Fault Isolation Capability (In development)

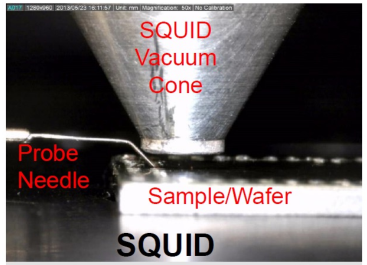
Magnetic Field Imaging

Fault **I**solation **S**olution using a single tool for all static electrical failures, opens, shorts, leakages

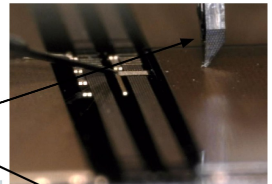
Est. delivery by July'25

SQUID for Packaged/assembled devices
Short Failure Localization

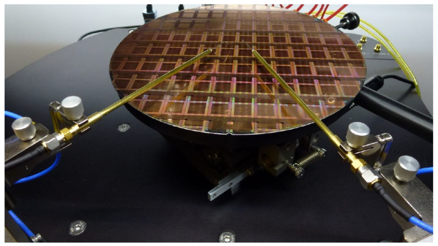


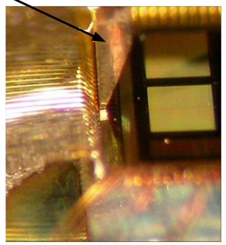


GMR for Wafer/Die
Short Failure Localization



GMR sensor





Research Activities/ Project Highlights

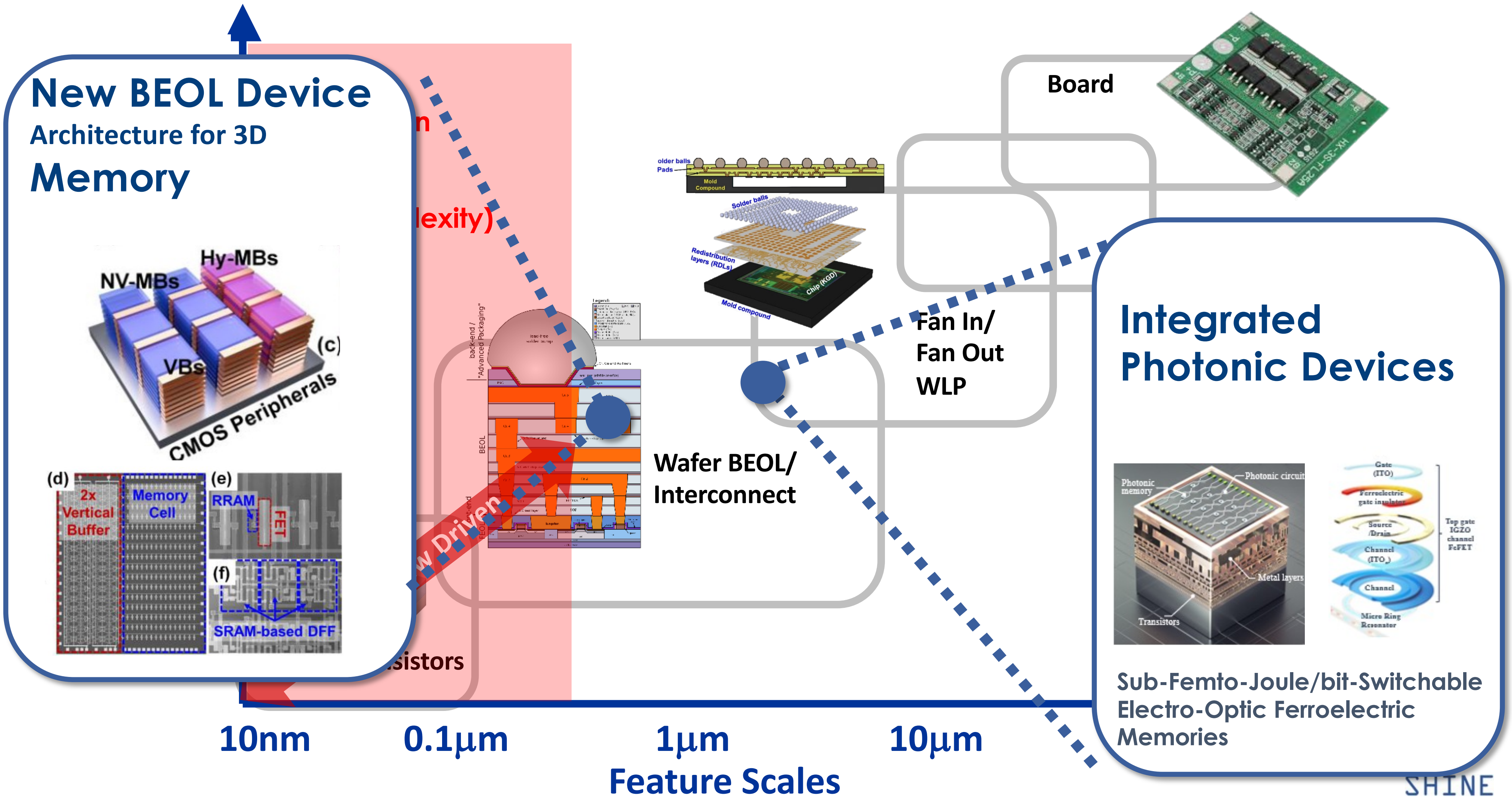
SHINE Research Activities

Area	2021	2022	2023	2024	2025	2026 and Beyond	
Low-Power Chiplet Platform				Capacitance Sensing Circuit		Low-Power Chiplet	
	One-Wire Inter-Chiplet Signaling		Over-the-chip HI of Harvester	Self-powered System-on-Wire	Battery-less Walking Step Counter	Power Modulation	
Flexible Hybrid Electronics			Resistive Strain Sensor	Wheatstone Bridge Sensing Circuit	Capacitive Bending Sensor	Topological Adhesion Conductor-Substrate	
	Flexible Capacitive Sensor		Ultrathin Stretchable Conductors	Low-hysteresis Tactile Sensor	Universal Nano-Anchor for LM	Morphology-Adaptive Conductor	Silk Fibroin Film With Engineered Rigid-island Structure
Novel and Nano-Materials Integration				CNT Transistor	3D-1T1R	2D Materials	
	SiC-Si Direct Bonding		SiC-Si Low-T Bonding	Hybrid MonoC-PolyC SiC Interposer	BEOL FeFET	FeFET	In-Memory Computing
Thermal		Radiative Cooling	Integration of Heat Spreader / PCM	Thermal Mapping with TRIR	Integration of Heat Pipe	Interposer- and package-level active + passive thermal management	On-chip thermal characterization / modelling
	TIM Ink Formation		Stretchable TM Ink	Board-level TM Antenna System	3D-printable TM Ink	3D-printable thermoelectric ink	Integrated laser diode thermal management
mmWave and RF			Tx / Rx Architecture Design	L-band 4x4 Dipole Array		Highly flexible active phase arrays	Smart sensing surface
	Flexible Patch Antenna with Springs / Spacers		Flexible Phased Array Antenna	L-band 8x1 Patch Array	X-band Phased Arrays	Active reconfigurable intelligent surface	
Packaging		Stealth Dicing	Through-SiC-Interposer	Rework of UBM		EIC + PIC Packaging	Optical Interconnect On Flexible Substrate
		D2D PnP	Solder Ball Jet	Micro-Transfer-Printing	SiC Interposer Fabrication	Flexible FOWLP platform	
Advanced Photonic Device			LN Process	Freeform PWB	Silicon Photonics Testing Capabilities	LNOI Integration	
			LNOI Modulator	Freeform Lens	Surface-to-Edge Coupler Printing	Modelling and design of vertical adiabatic coupler	

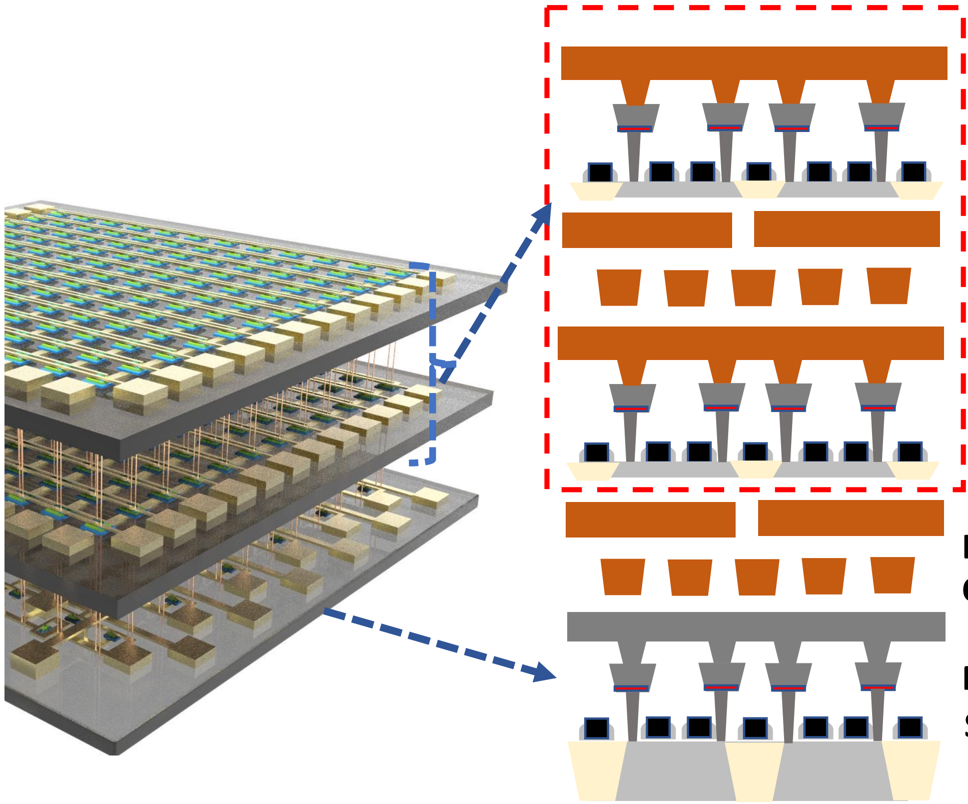
SHINE Current Capabilities (2021–2025)

SHINE 2.0 Key Focus (2024 – 2026 and Beyond)

SHINE's 2024 Research Highlights



M3D-IC: **BEOL** Transistor-Interconnect **Thermal Budget Dilemma**

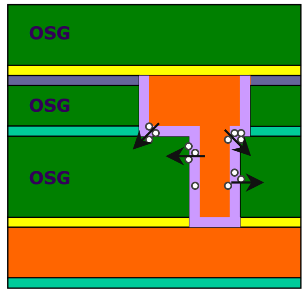


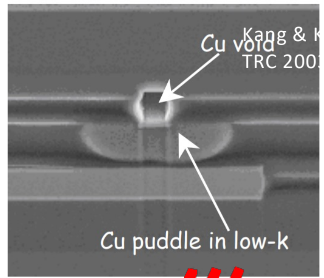
Need New Low-Thermal Budget <u>Back-End-of-Line (BEOL)</u> Transistors & Memory

Low-k & Cu Interconnect

Memory Si Transistors

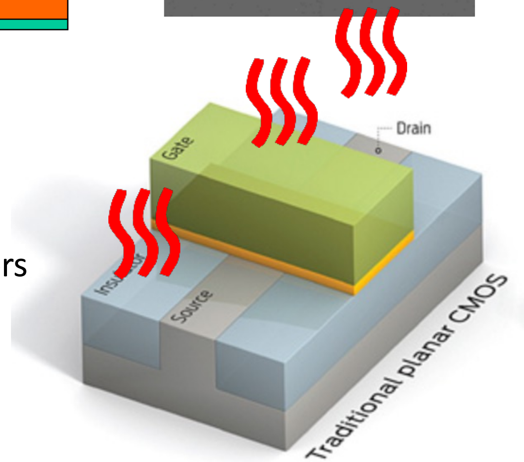
T>400°C Enhanced Interconnect Cu out-diffusion to low-k along the Cu/dielectric interface → Reduced TDDB and Temperature Instability





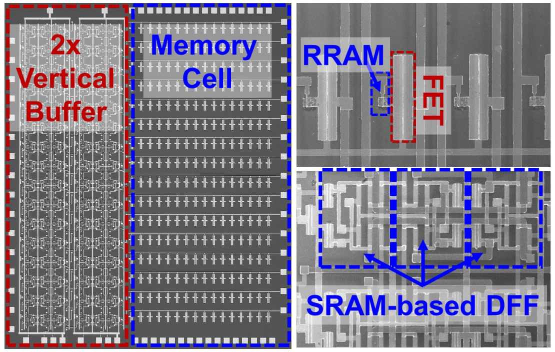
< 400°C Processing

Base CMOS Transistors (Silicon) High-T processed (900-1000°C)



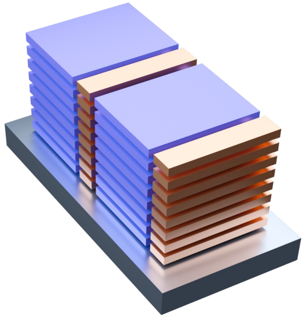
A. Thean *et al.*, "Low-Thermal-Budget BEOL-Compatible Beyond-Silicon Transistor Technologies for Future Monolithic-3D Compute and Memory Applications," *2022 International Electron Devices Meeting (IEDM)*, pp. 12.2.1-12.2.4, doi: 10.1109/IEDM45625.2022.10019511.

Monolithically-stacked 3D 1T1R ACiM for 100TOPS/W

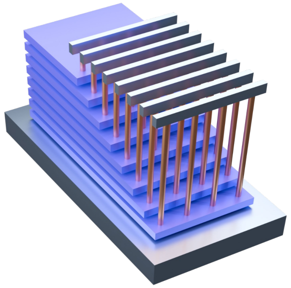


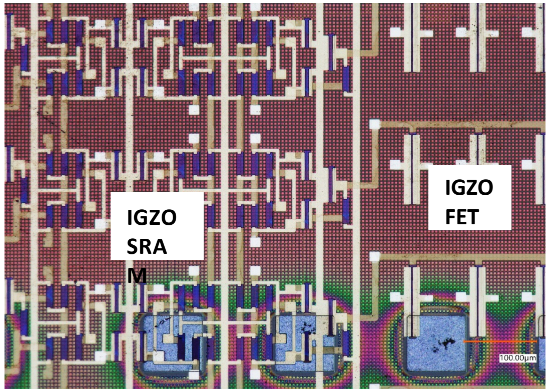
NV-MBs and VBs

This Work



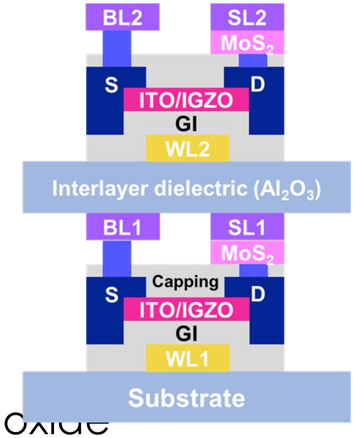
Conventional Stacking





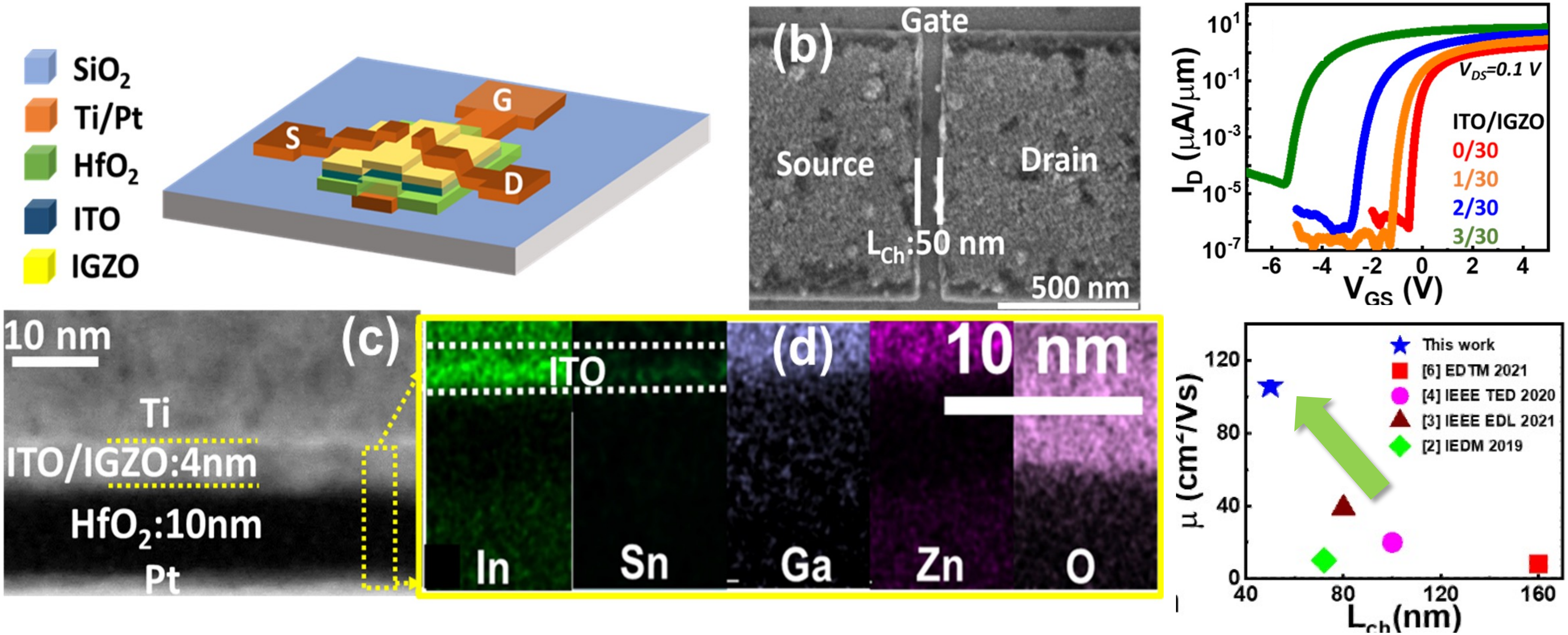
ITO-IGZO SRAM on Chip

Stacked 1T1R



- Accomplishments in this project:
  - Achieved wafer-scale, low-temperature (<400 °C) monolithic 3D integration of oxide and 2D materials with strong device performance.
  - Developed low-voltage, CMOS-compatible 1T1R memory cells with IGZO FETs and MoS2 RRAMs, requiring <100 µA and <1 V for switching.
  - Proposed a 2T0C1R DRAM-RRAM hybrid with dual-gated IGZO FETs to improve RRAM endurance.
  - Designed an all-IGZO buffer enabling 3D data pipelining for efficient multi-stack operations.
  - Demonstrated 3D analog compute-in-memory with 121 TOPS/W efficiency and 4.73 TOPS throughput, reducing ADC energy overhead.

Bilayer Heterojunction Oxide Channel **(ITO-IGZO)** Enhancement



Bilayer channel achieves record IGZO electron mobility and **hysteresis-free** SS performance, **I_{DS} = 800 μA/μm (1.0V V_{DS}) with μ = 106 cm²/V-s**

Double-Gated Ferroelectric IGZO Memtransistor

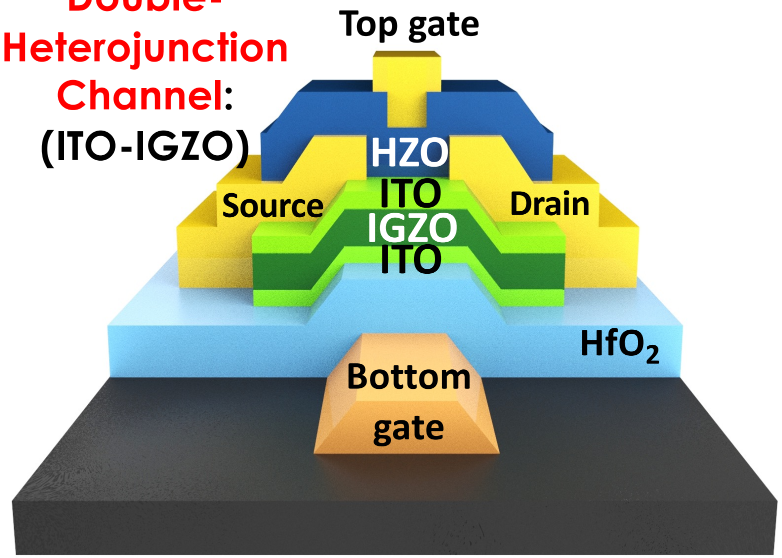
First Demonstration of Ultra-low D_{it} Top-Gated Ferroelectric Oxide-Semiconductor Memtransistor with Record Performance by Channel Defect Self-Compensation Effect for BEOL-Compatible Non-Volatile Logic Switch

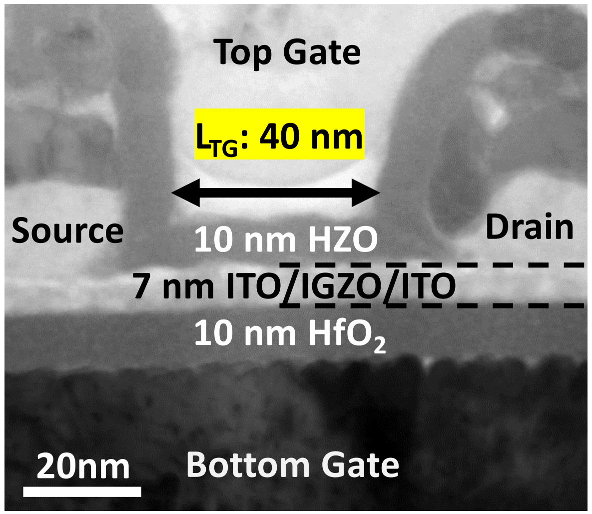
Chun-Kuei Chen†, Zihang Fang†, Sonu Hooda†, Manohar Lal, Umesh Chand, Zefeng Xu, Jieming Pan, Shih-Hao Tsai, Evgeny Zamburg, and Aaron Voon-Yew Thean*
Department of Electrical and Computer Engineering, National University of Singapore (NUS), Singapore 117583
†Equal contribution; Email: Aaron.Thean@nus.edu.sg

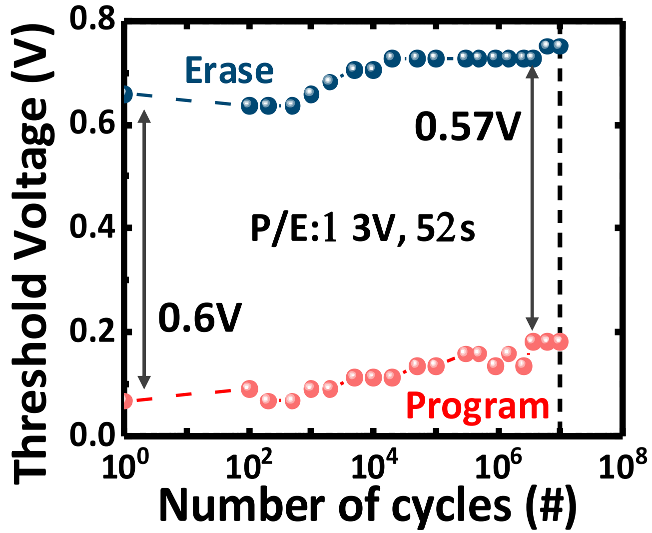
2022 International Electron Devices Meeting (IEDM), 6.1. 1-6.1. 4

2022 San Francisco

Double-Heterojunction Channel: (ITO-IGZO)

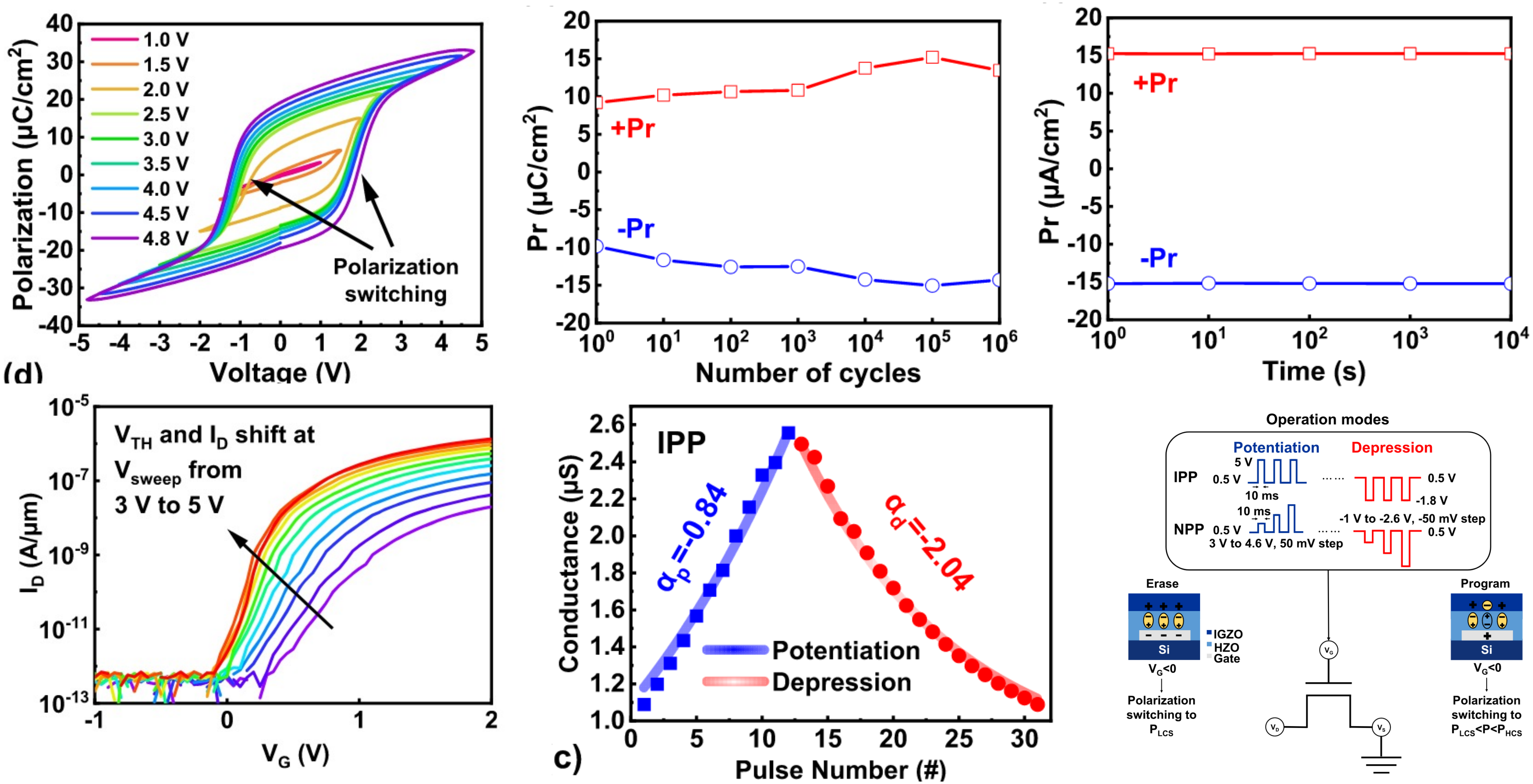






- **Overcome a fundamental issue of top-gated interface Dit by heterojunction engineering**
- Enables new multi-gated devices with new system application possibilities

Low-Thermal Budget **Ferroelectric HZO-IGZO Memtransistor**



Stress-Memorized HZO for High-Performance Ferroelectric Field-Effect Memtransistor SH Tsai, Z Fang, X Wang, U Chand, CK Chen, S Hooda, M Sivan, J Pan, ... ACS Applied Electronic Materials 4 (4), 1642-1650 (2022)

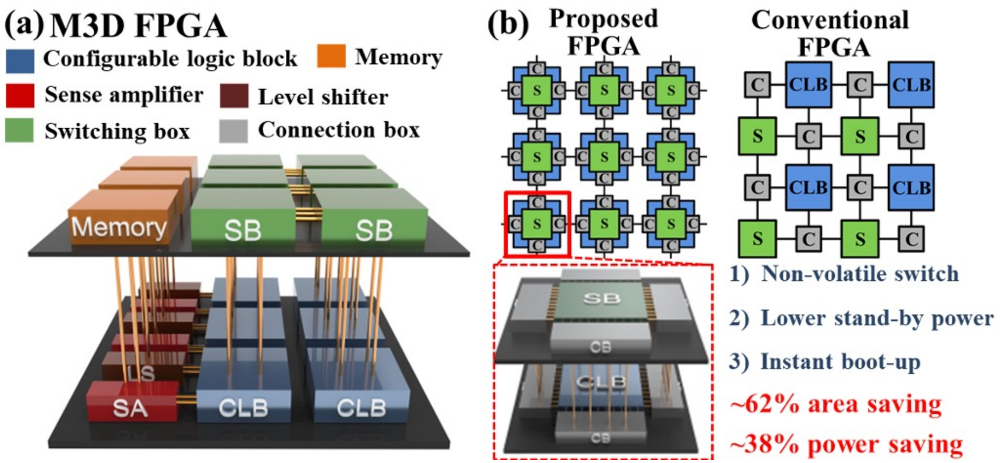
Dynamic Reconfigurable Interconnect by M3D Nonvolatile Switch

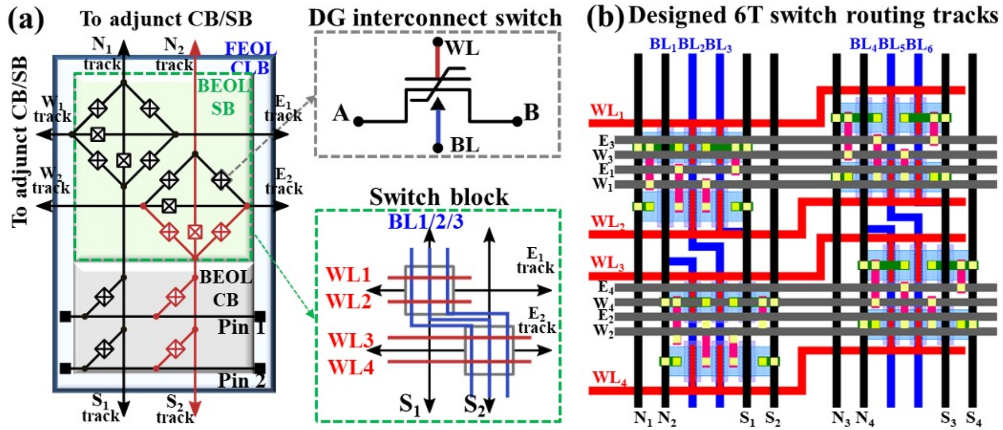
First Demonstration of Ultra-low D_{it} Top-Gated Ferroelectric Oxide-Semiconductor Memtransistor with Record Performance by Channel Defect Self-Compensation Effect for BEOL-Compatible Non-Volatile Logic Switch

Chun-Kuei Chen[†], Zihang Fang[†], Sonu Hooda[†], Manohar Lal, Umesh Chand, Zefeng Xu, Jieming Pan, Shih-Hao Tsai, Evgeny Zamburg, and Aaron Voon-Yew Thean*
Department of Electrical and Computer Engineering, National University of Singapore (NUS), Singapore 117583
[†]Equal contribution; Email: Aaron.Thean@nus.edu.sg

2022 International Electron Devices Meeting (IEDM), 6.1. 1-6.1. 4

2022 San Francisco





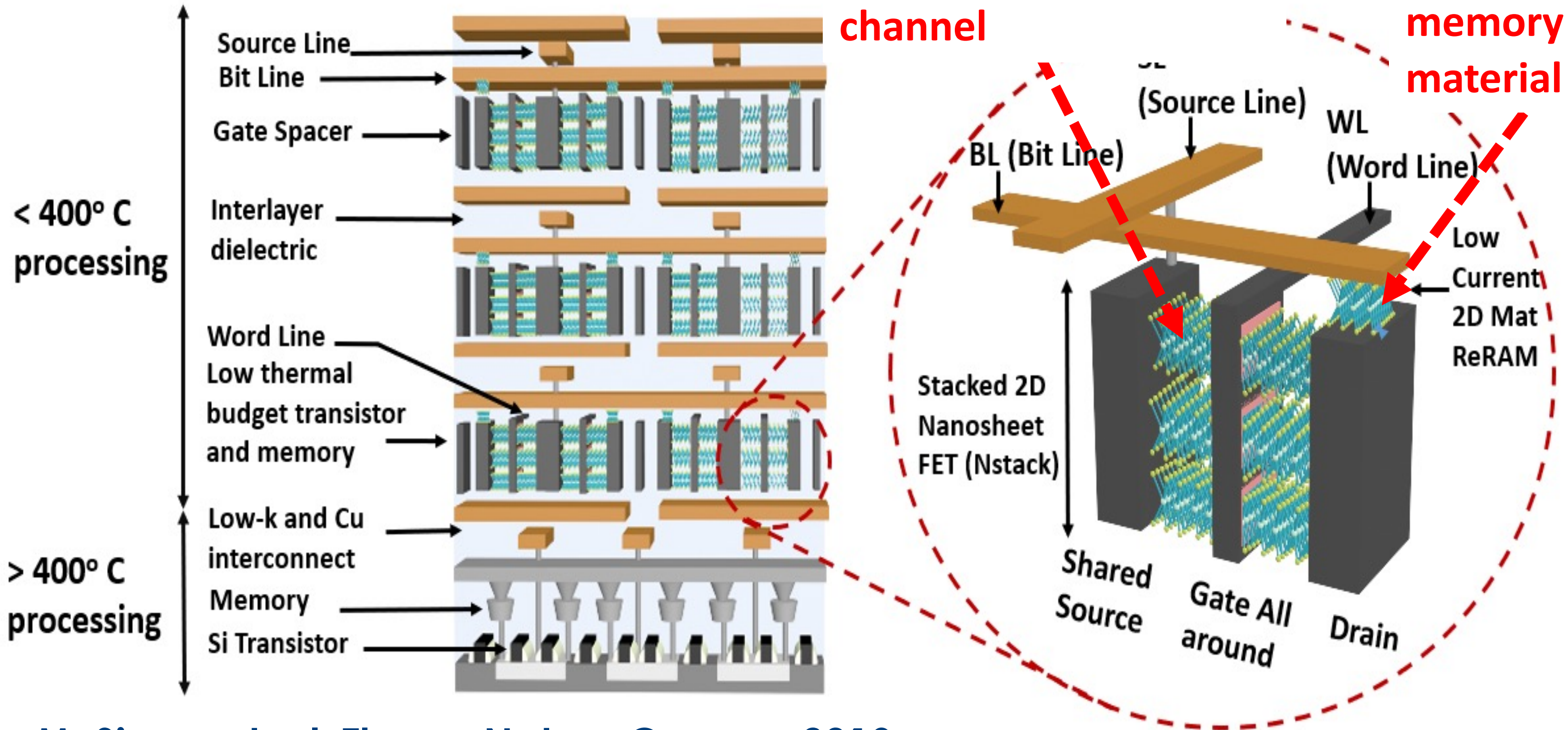
- **Dynamically-Reconfigurable Interconnect with M3D-compatible Double-Gated FeFET**

CK Chen, S Hooda, Z Fang, M Lal, Z Xu, J Pan, SH Tsai, E Zamburg, ...IEEE Transactions on Electron Devices 70 (4), 2098-2105

Vision of 2-D Material Monolithic 3D Memory Systems

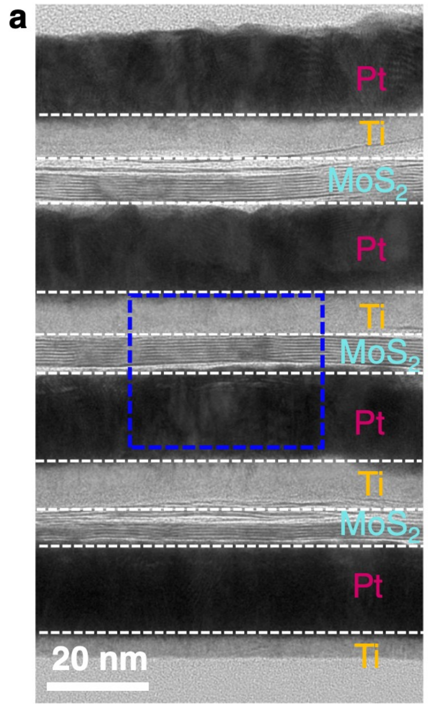
Need high-quality TFT channel

Need defect-enabled memory switching material



M. Sivan, et. al. Thean, Nature Comms, 2019

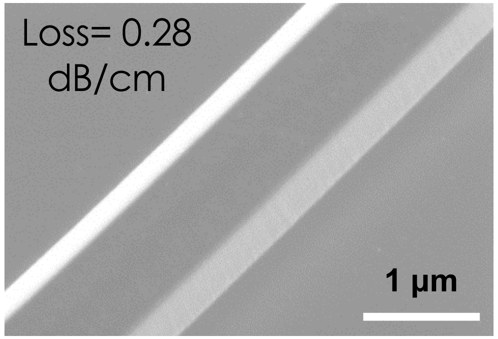
Stacked memories (3D Memristors) demonstrated



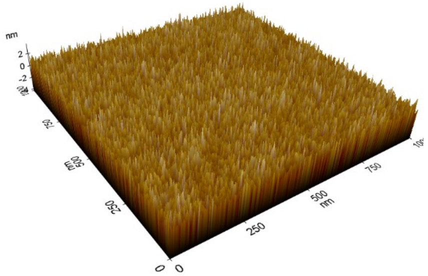
B. Tang, et. al. Thean, ...
Nature Communications 13 (1), 1-9, 2022

Ultra-Low Loss (Record) Lithium Niobate Photonic Waveguides & Modulators Photonics

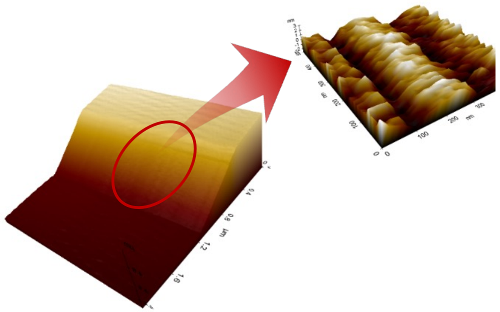
(CLEO 2025)

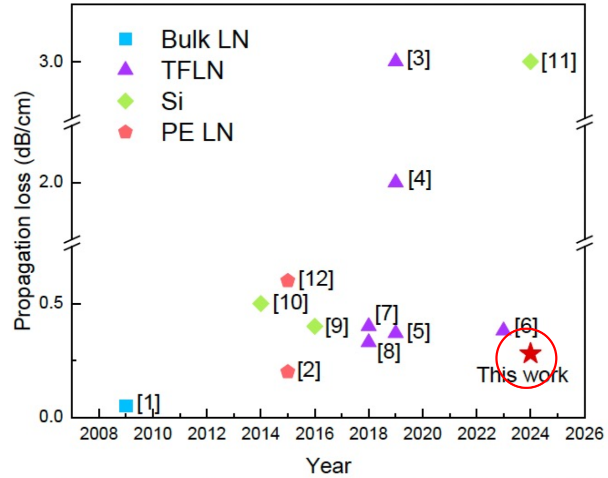


Surface Ra: 0.043

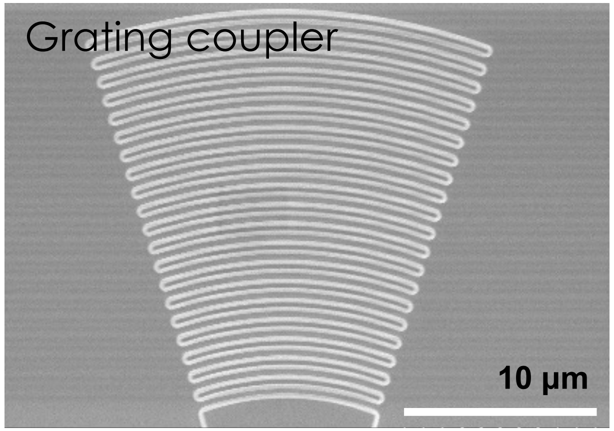


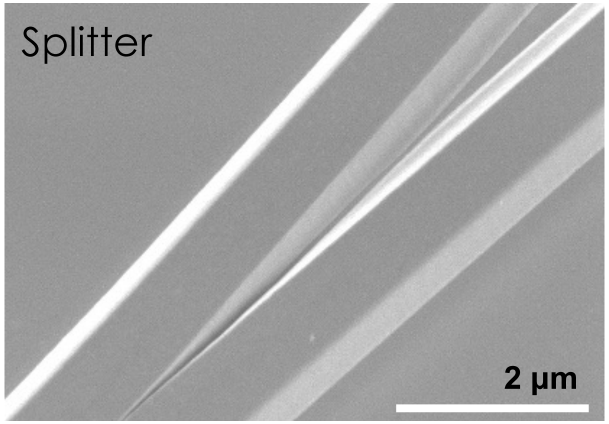
Sidewall Ra: 0.841





Waveguide propagation loss [1-12]





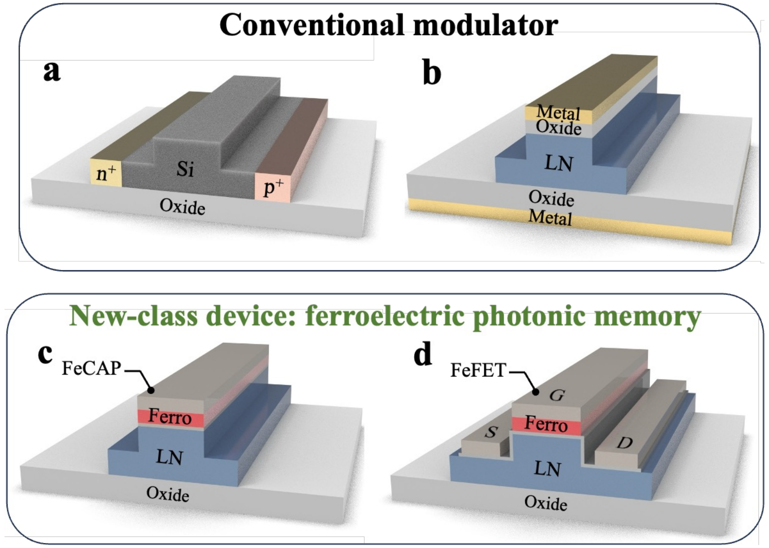
- Developed New Dry etch technique to achieve Lithium Niobate sidewall roughness about 1 nm for record ***ultra-low propagation loss (0.28 dB/cm)***

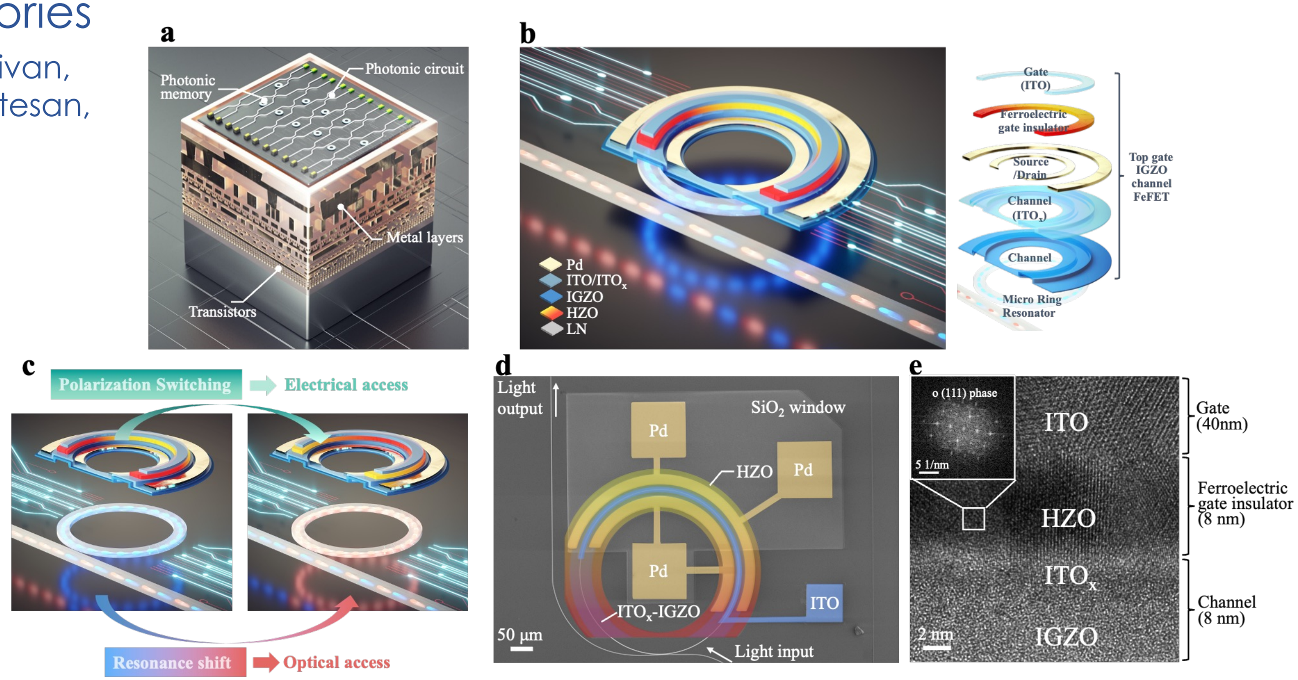
Unpublished and confidential results.

Low-voltage Hybrid Ferroelectric Photonic Memories

Femto-Joule/bit-Switchable Electro-Optic Ferroelectric Multi-State Photonic Memories

Zefeng Xu, Chun-Kuei Chen, Hong-Lin Lin, Maheswari Sivan, Evgeny Zamburg, James Yong-Meng Lee, Suresh Venkatesan, Aaron Danner, Aaron Voon-Yew Thean





Under Review Nature Photonics

- Offers a 100× reduction in switching energy
- Achieve switchable and non-volatile multiple optical memory states (5 states minimum) with ultra-low energy cost of 0.6 fJ/bit, while achieving robust 10-year data retention and read-write endurance exceeding 10^7 cycles

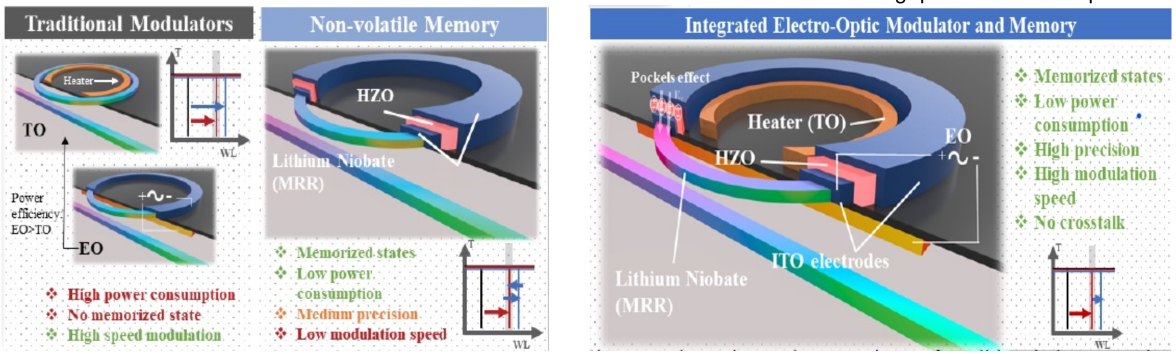
New Hybrid Integrated Optoelectronics Capabilities

IEEE International Electron Devices Meeting (IEDM) 2023

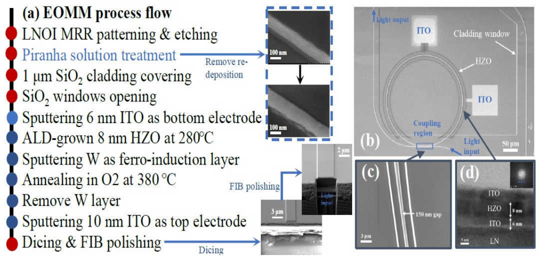
First Demonstration of HZO-LNOI Integrated Ferroelectric Electro-Optic Modulator and Memory to Enable Reconfigurable Photonic Systems

Zefeng Xu[1,2,6†], Chun-Kuei Chen[1,6†], Hong-Lin Lin[1†], Yuan Gao[1], Wei Ke[3], Baochang Xu[1,6], Pavel Dmitriev[4], Arbiz Carlan[5], Evgeny Zamburg[1,6], Steven Touzard[4], Xinlun Cai[3], James Lee[5], Suresh Venkatesan[5], Aaron Danner[1], Aaron Voon-Yew Thean[1,2,6*]

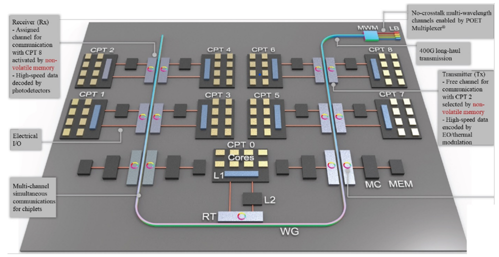
[1]Department of Electrical and Computer Engineering, National University of Singapore (NUS), [2]Integrative Sciences and Engineering Program, NUS Graduate School, [3]School of Electronics and Information Technology, Singapore 117583, Sun Yat-Sen University, China 510275, [4]Centre for Quantum Technologies, NUS, [5]POET Technologies, [6]Singapore Next-Generation Hybrid μ-Electronics Center (SHINE), Singapore 117583. [†]Equal contribution.



Schematics and comparison of traditional thermo-optical (TO)/electro-optic (EO) modulator, LNOI non-volatile memory, and LNOI Integrated EOMM.



(a) The key process steps of fabricating LONI EOMM. The SEM images of (b) LNOI EOMM, (c) micro-ring resonator (MRR) coupling region, (d) ferroelectric Hafnium Zirconate (HZO) memory capacitor integrated on MRR.



Benchmark of LNOI EOMM against state-of-the-art non-volatile photonic memory.

Ref.	Waveguide material	Method	Q-factor	Extinction ratio	Efficiency	Multi-Level	Retention	Endurance	No-crosstalk modulation	Nonlinear effect	BEOL compatibility	Thermal stability
[11]	Si_3N_4	GST: absorption	10^4	1.55 dB	N/A	Yes	N/A	N/A	No	No	No	Low
[12]	Si	Poly-Si: floating gate	10^4	12.7 dB	15 pm/V	Yes	N/A	N/A	No	No	Yes	Low
[13]	Si	Sb_2Se_3: phase shift	10^3	7 dB	N/A	No	N/A	N/A	No	No	No	Low
[14]	Si	ITO: floating gate	N/A	10 dB	N/A	No	N/A	N/A	No	No	Yes	Low
[7]	SOI	HAO: charge trapping	10^3	8.9 dB	34 pm/V	No	10 years	10^8 cycles	No	No	No	Low
[8]	Si	BTO: phase shift	10^5	12 dB	8 pm/V	Yes	10 years	10^7 cycles	No	No	No	High
[9]	Si_3N_4	HZO: absorption	N/A	9.4 dB	N/A	Yes	N/A	N/A	No	No	No	Hight
This work	LNOI	HZO: Pockels effect	10^5	13.3 dB	66 pm/V	Yes	10 years	10^9 cycles	Yes	Yes	Yes	High

Highlights of this work

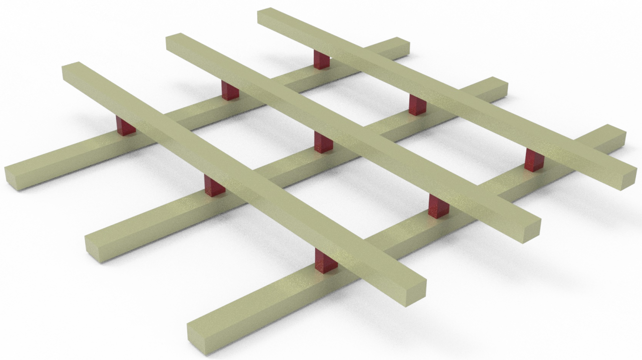
- Record-high photonic memory efficiency of 66 pm/V
- High extinction ratio of 13.3 dB and full width at half maximum of 0.10 nm
- At least stable 9 memorized states @ driving voltage 2-4 V
- Record-high endurance >10^9 cycles; retention >10 years
- First Lithium Niobate on Insulator (LNOI) electro-optic memory based on 2nd order nonlinear effect, Pockels effect
- First electro-optic modulator and memory all-in-one solution
- Low thermal budget process <400℃
- Integration of electro-optic modulator and memory (EOMM) with POET 400G Tx/Rx engines
- Simulated chiplet-interposer photonic interconnect system with low power consumption demonstrated

SHINE

Lithium-Niobate-IGZO Based Photonic-Electronic Integrated Compute-In Memory Systems (Fine-Pitch LN-Electronics Integration)

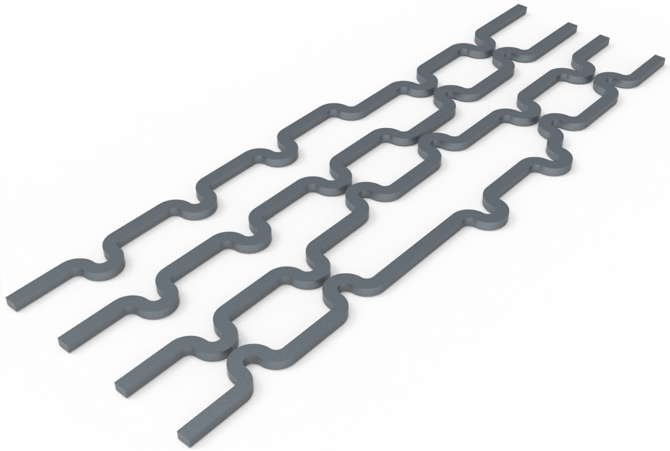
VLSI 2025

RRAM CIM



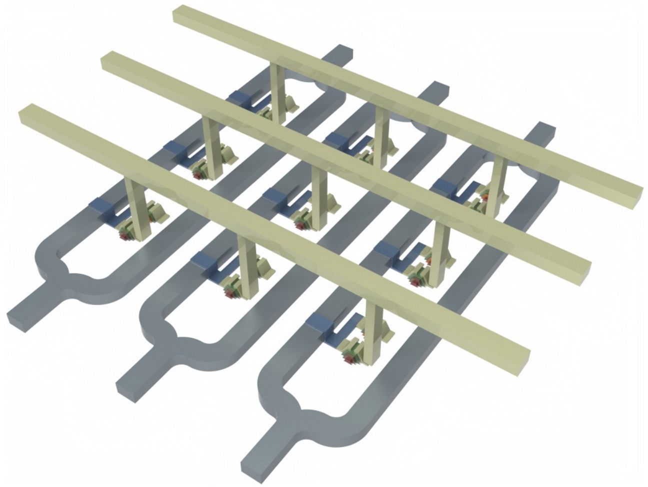
High density ✓
IR drop ✗
High I_{off} ✗

MZI array



Low density ✗
No IR drop ✓

Hybrid array



High density ✓
No IR drop ✓

Lithium-Niobate-IGZO Based Photonic-Electronic Integrated Compute-In Memory Systems

VLSI 2025

- Problem Statement:
  - The scalability is often hindered by escalating IR losses caused by the increasing wire resistance in larger arrays and advanced nodes.
- Innovation:
  - A novel two-transistor-one-modulator photonic-electronic hybrid architecture using an NFET for initialization, a FeFET operating at sub-threshold region for in-memory multiplication with enhanced linearity and ultra-low-loss lithium niobate on insulator photonic modulator for phase-domain summation.

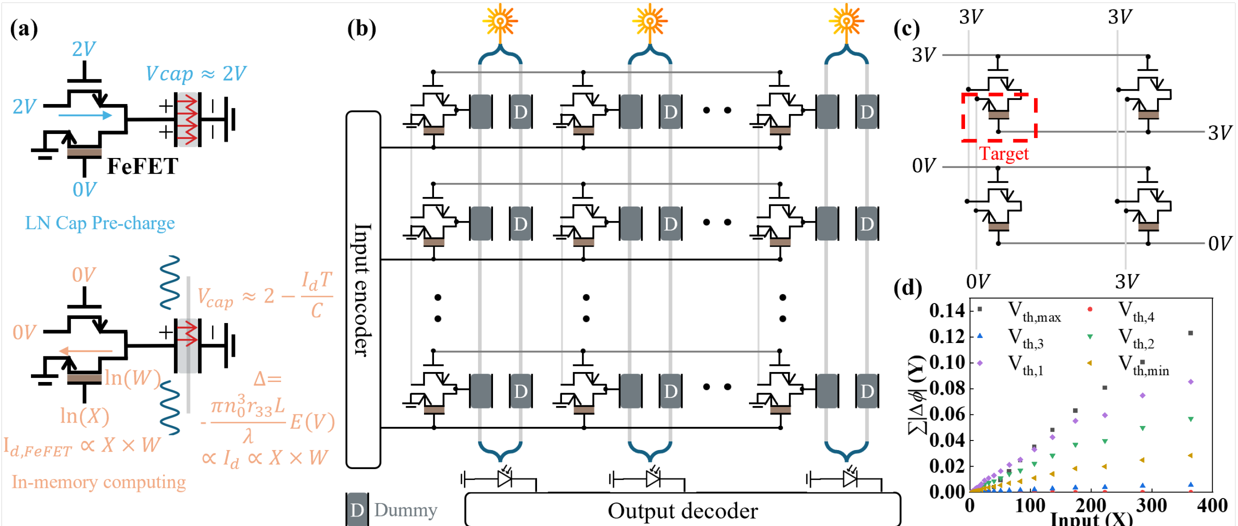
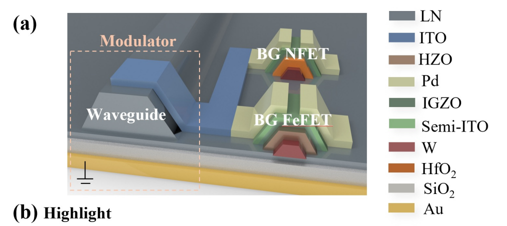


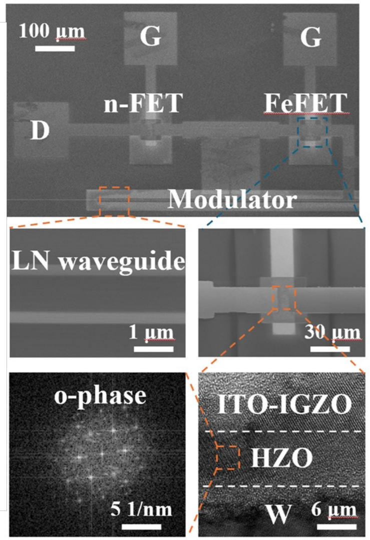
Fig. 7. (a) Pre-charge and FeFET computing phase (refractive index n_0, electro-optic coefficient of z-cut LN r_{33}, LN length L, electric field E. (b) 2T1M array architecture. (3) Programming scheme. (4) Total phase change (MAC results) vs. input (X) and weight multiplier (W).



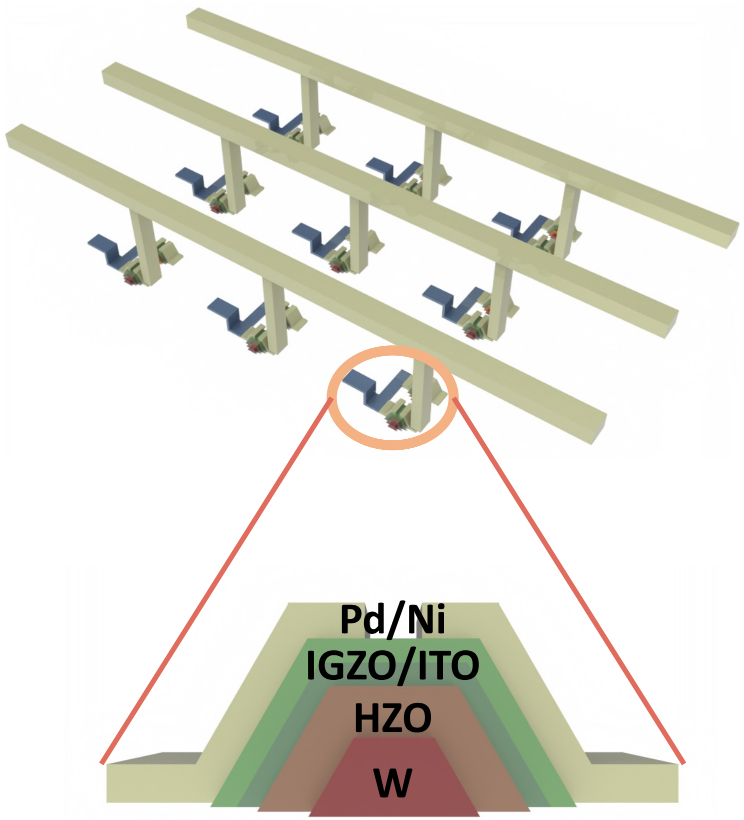
(b) Highlight

1. Record-high scalability (up to 150x larger array)
2. Zero voltage drop per WL
3. Exceptional multiplication linearity using subthreshold region> 0.99
4. First demonstration of transformer on CIM array with seamless compatibility
5. 0% accuracy loss when mapping the largest layer (30K × 128)
6. Up to 37X power saving over SOTA
7. 164 TOPS/W performance efficiency
8. High endurance >109 cycles ; retention > 10 years
9. Record-low light propagation loss 0.28 db/cm

Fig. 2. (a) 3D schematic of 2T1M cell. (b) Highlight of this work.

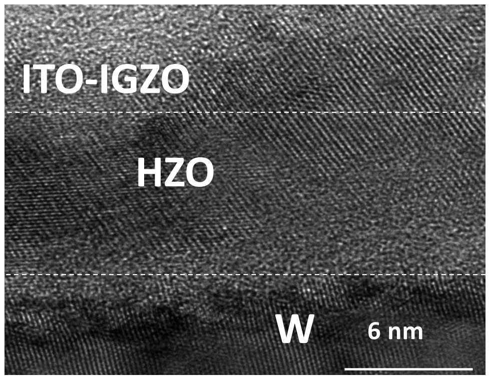


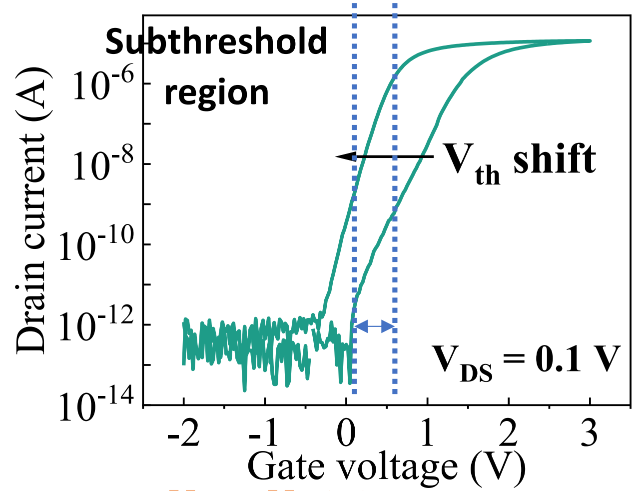
FeFET-based in-memory computing



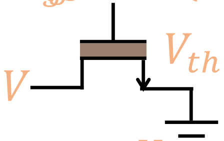
Lower off-current than RRAM ✓

- ▶ Sputter W as FETs BG
- ▶ ALD-grown 8 nm HZO at 280°C
- ▶ HZO etching using diluted HF
- ▶ ALD-grown 10 nm HfO_2 at 250°C
- ▶ HfO_2 etching using diluted HF
- ▶ Sputtering 2 nm ITO / 5 nm IGZO as FETs channel
- ▶ Channel etching using diluted HCl
- ▶ E-beam growing Ti / Pd as FETs S/D electrodes
- ▶ Annealing in O_2 at 380 °C





$V_{gs} = \ln(X)$



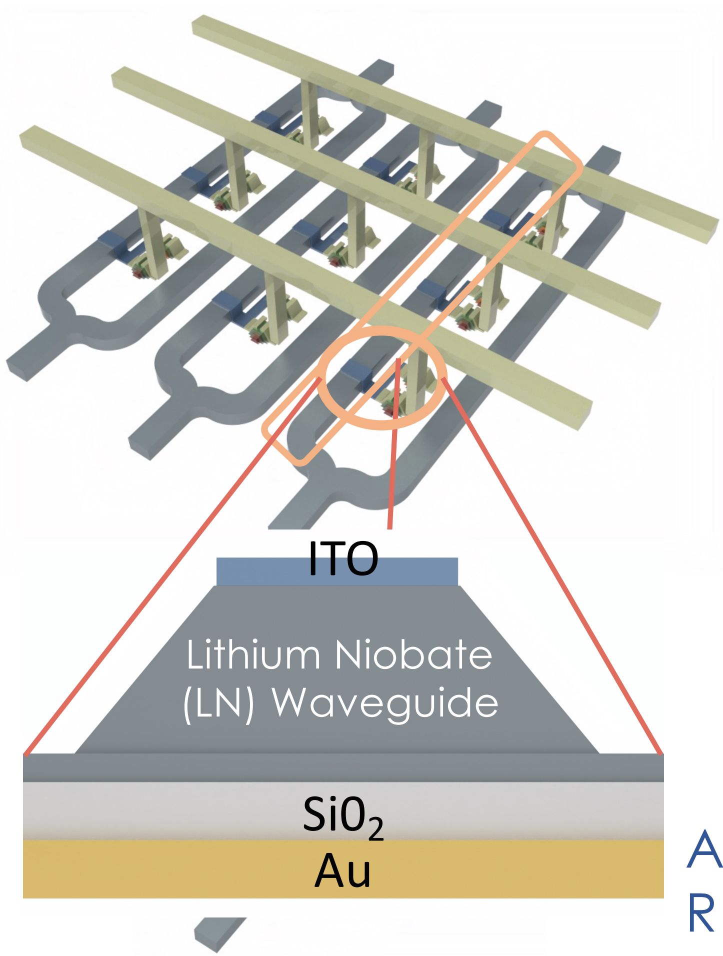
$V_{th} = \ln(W)$

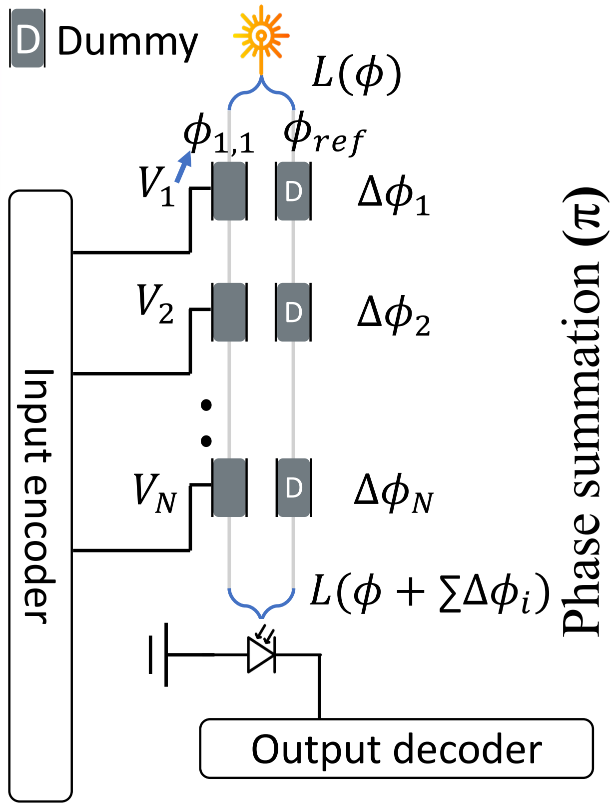
$V_{ds} > 0.1V$

$$I_{d,FeFET} \propto e^{V_{gs}} \cdot e^{-V_{th}}$$
$$\propto e^{\ln(X)} \cdot e^{\ln(W)}$$
$$\propto X \times W$$

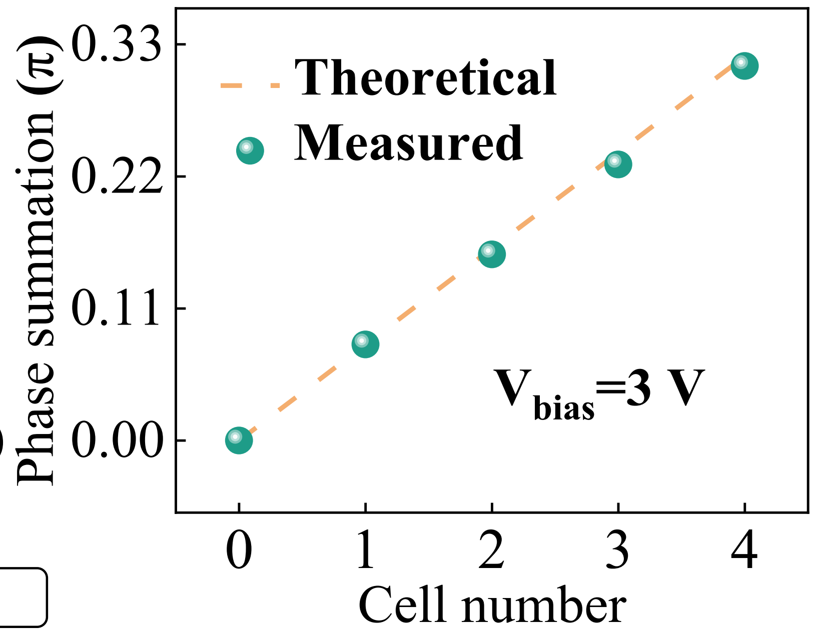
Linear multiplication in subthreshold region ✓

Photonic “lossless” in-phase summation



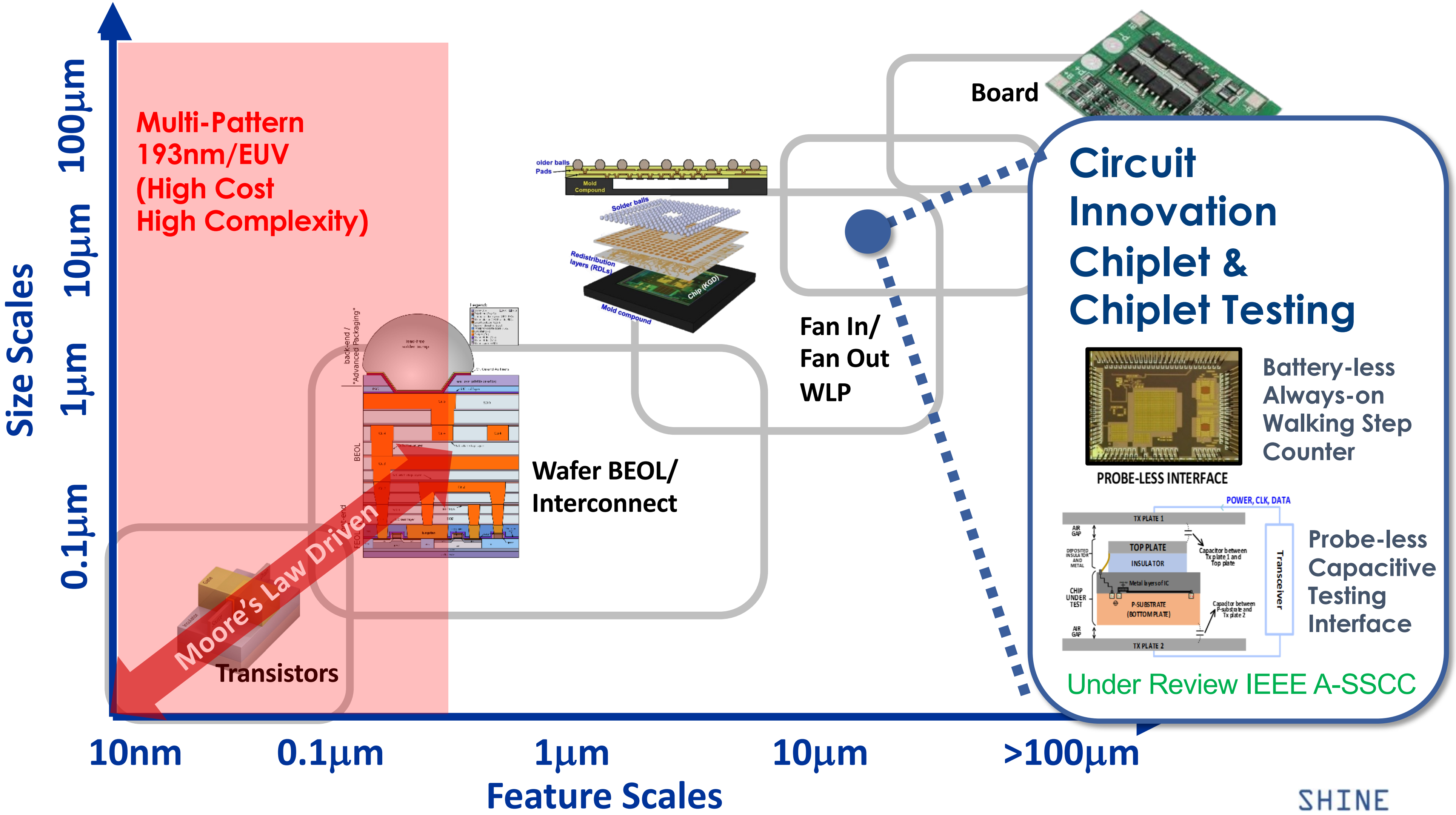


Total phase change vs. no. of cells



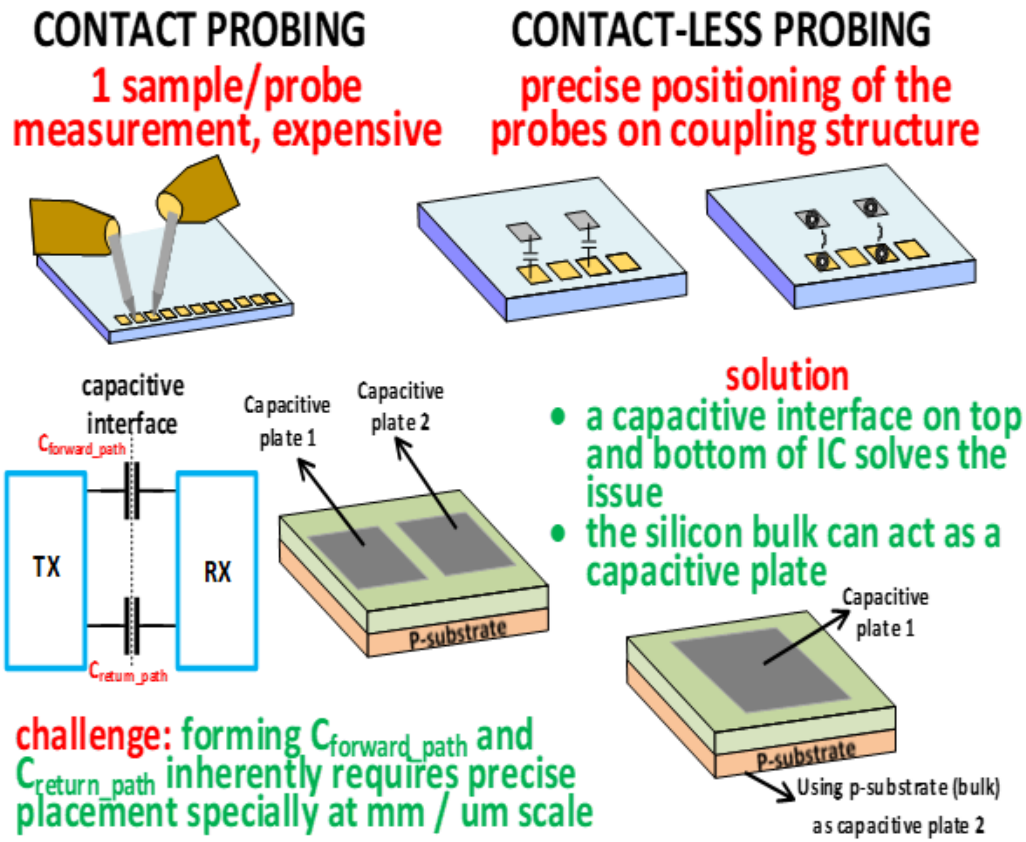
Applicable to any memory/CIM architecture e.g. RRAM, FeFET, SRAM readout

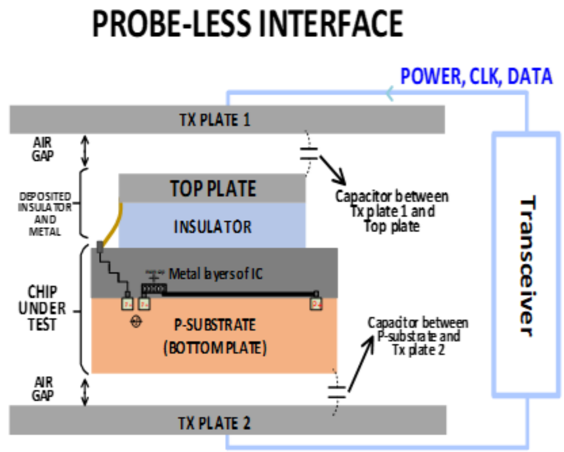
SHINE's 2024 Research Highlights



Probe-less Capacitive Testing Interface. (Prof. Massimo Alioto)

Submitted to IEEE A-SSCC

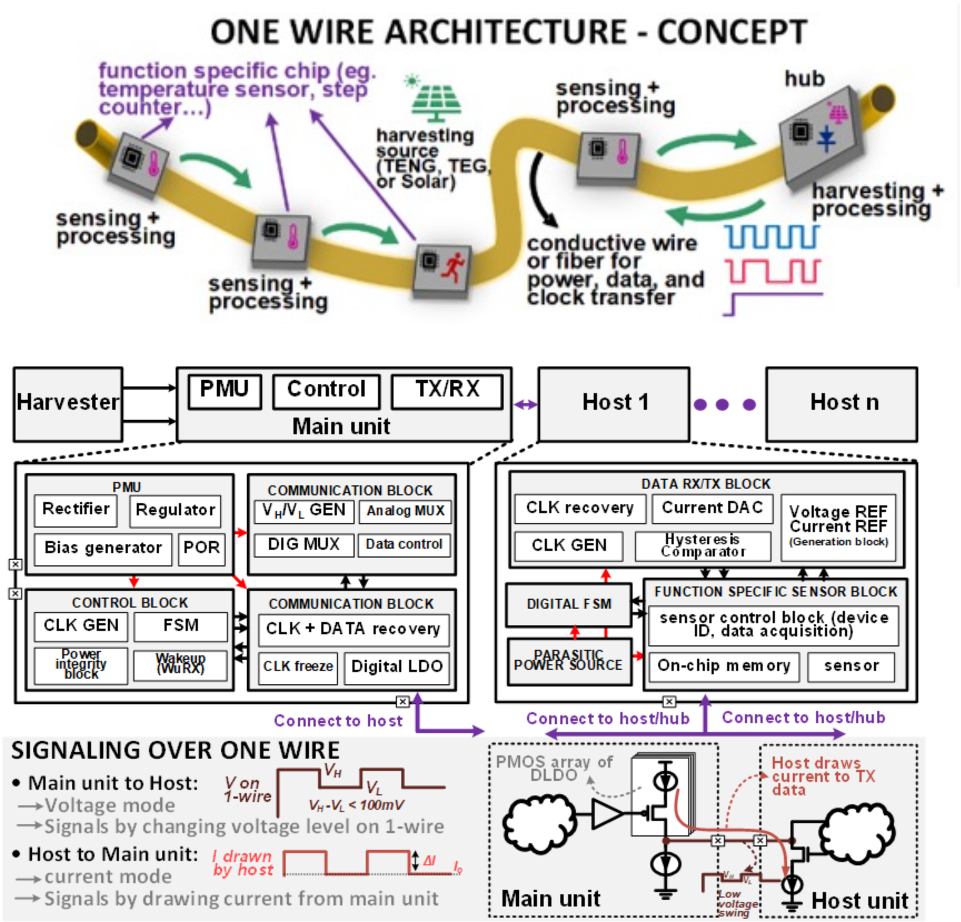


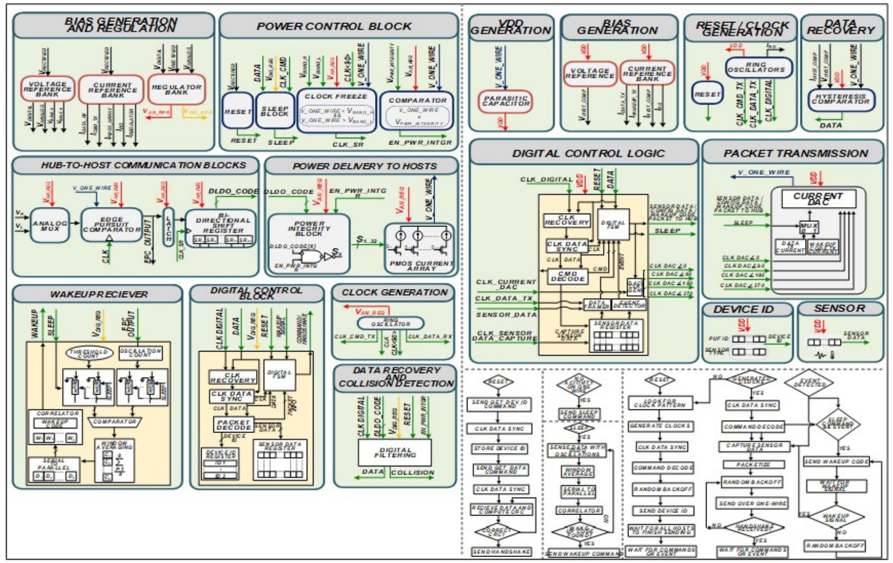


Highlight of This Work

- ❑ Successfully tested probe less/touch-less massive chiplet testing setup with placement invariant capacitive coupling interface
- ❑ No packaging or probing needed (Cost Reduction)
- ❑ Probe-less testing at speed including power consumption demonstrated
- ❑ Multi die testing with uniques chip ID and random backoff transmission (Clock recovery, forward, and backward data communication with BER<10-7 demonstrated experimentally.

Thrust 1: Self-Powered System-on-wire (On-going Work, Prof. Massimo Alioto)

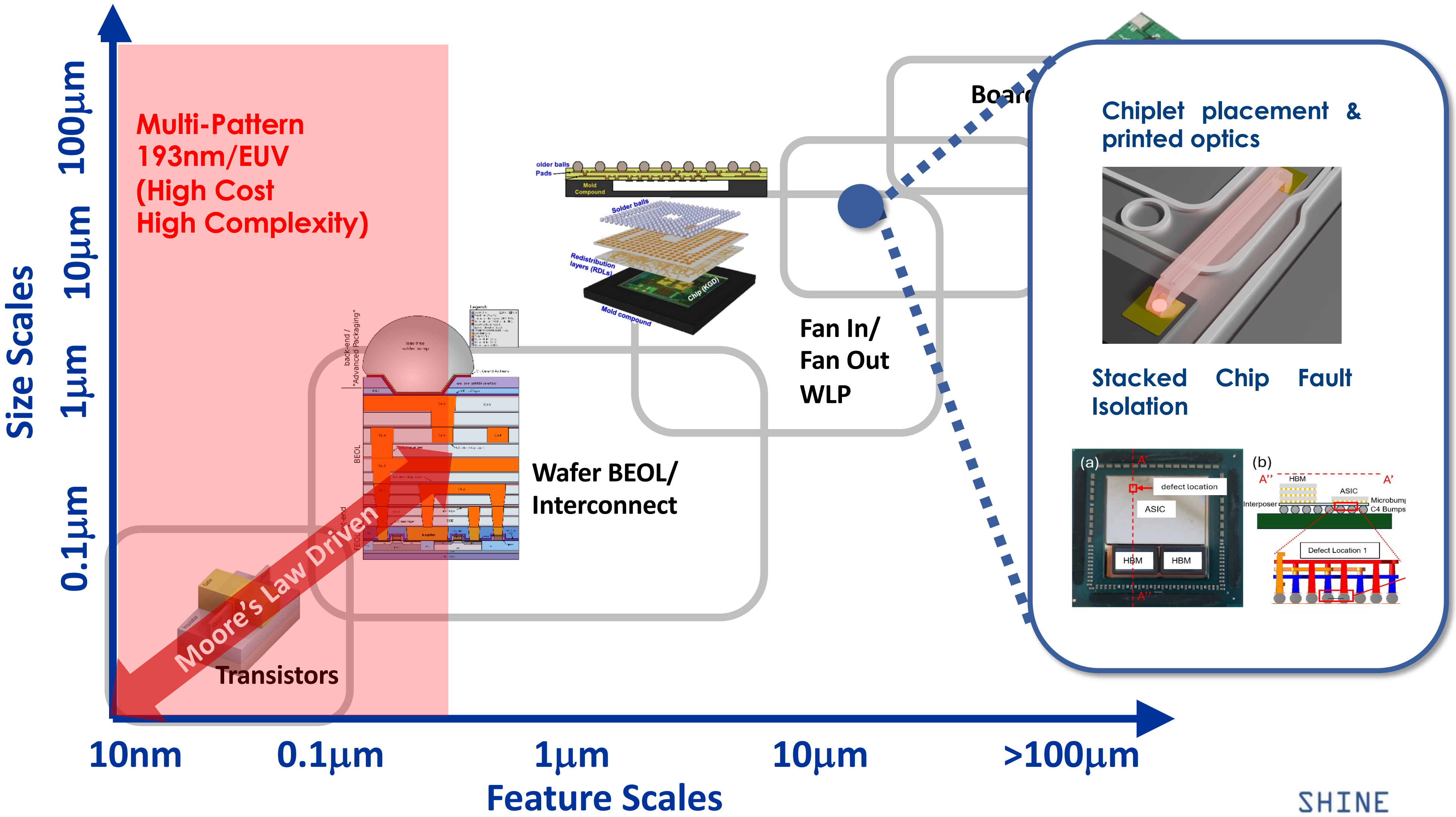




Highlight of This Work

- Fully autonomous, self-powered system on a single wire.
- This system can be distributed along a conformable fiber and is capable of simultaneously harvesting energy, transferring power, transmitting data, and synchronizing clocks over this single wire within a distributed network.
- Introduces an architecture for a chiplet-based system where functional units (hosts) with sensing capabilities connect to a central chiplet (hub) using a single-wire protocol.
- This approach simplifies the design of a low-power, low-bandwidth multi-modal system by combining power delivery and communication on the same wire.

SHINE's 2024 Research Highlights



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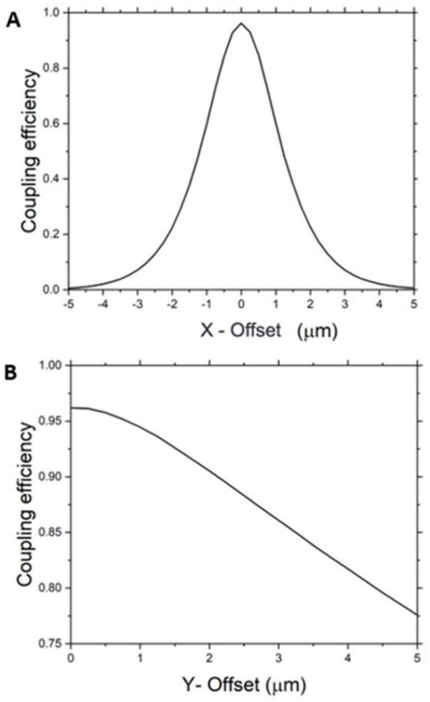
New Hybrid Integrated Optoelectronics Capabilities

Problem statement

Passive alignment is cost effective for laser diode alignment, however, coupling loss with respect to misalignment must be taken care of.



Journal of Lightwave Technology

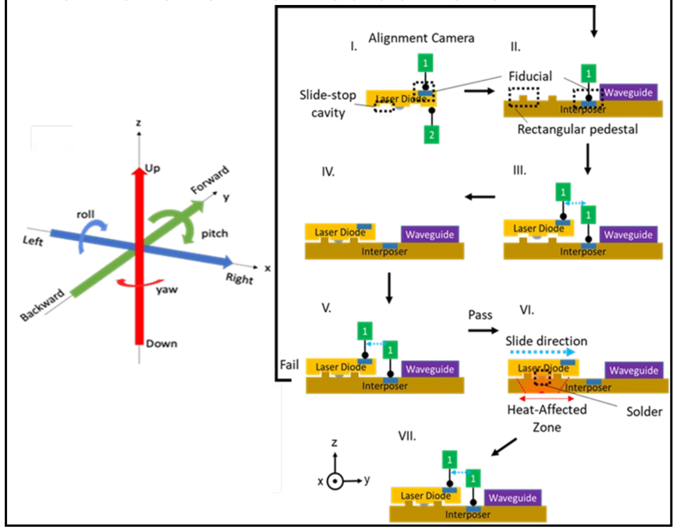
Multi-axial Elastic Averaging for Sub-micron Passive Alignment of Photonic Components

*[1]Simon Chun Kiat Goh, *[2]Chun Fei Siah, *[2]Baochang Xu, [2]Yu Zhang, [2]Mei Er Pam, [1]Enrico Guevarra, [1]Edwin Sze Ping Goh, [1]Lin Wang, [1]Brian Pile, [1]Arbiz Carlan, [1]James Yong Meng Lee, [1]Suresh Venkatesan, [2]Yeow Kheng Lim, [2]Aaron Voon-Yew Thean

[1]POET Technologies, [2]Singapore Hybrid-Integrated Next-Generation µ-Electronics Centre, National University of Singapore

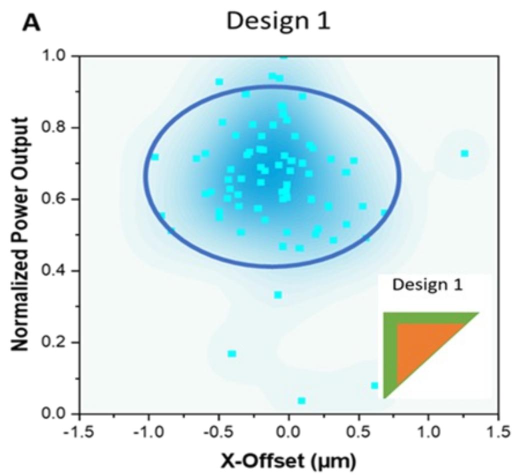
Innovation

Develop pedestal-cavity pair for multi-axial elastic averaging to eliminate thermal error from solder reflow.



Result

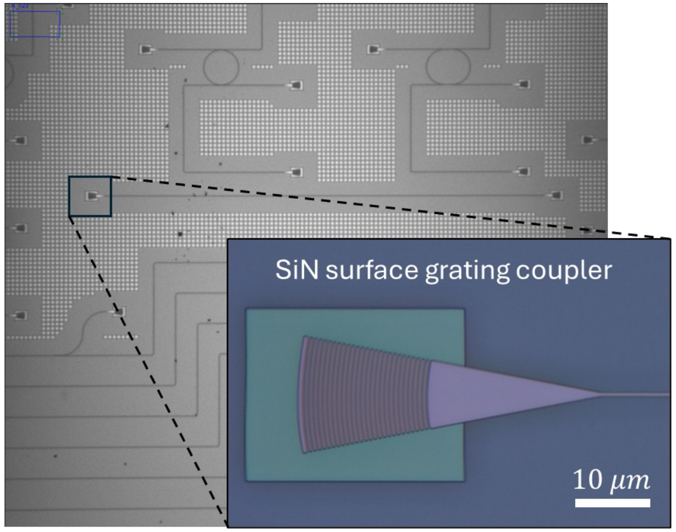
Narrower optical power output distribution of P-down bonded lasers with triangle slide-stop guided design .



Advanced Freeform Optical Waveguide Coupled with Facet Microlens Development and Testing

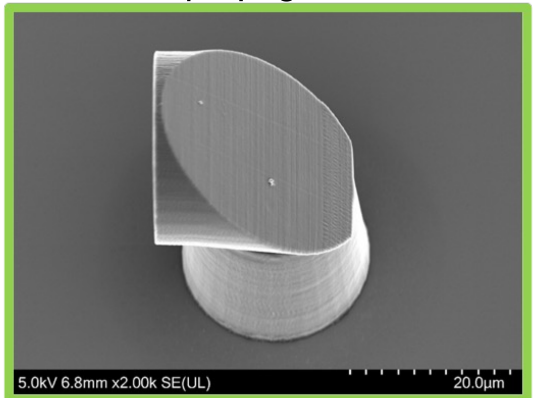
Problem statement

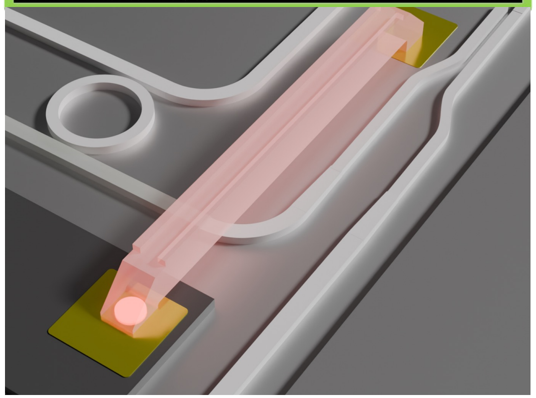
Conventional optical interconnect relies on silicon nitride (SiN) is based on planar fabrication methods. Alignment of external light source to SiN waveguide can be time consuming.



Innovation

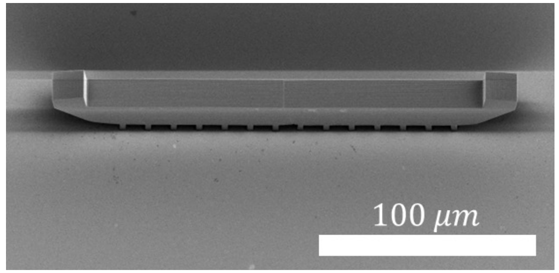
Freeform lens can be printed using 2-photon polymerization to divert light to another axis of propagation.

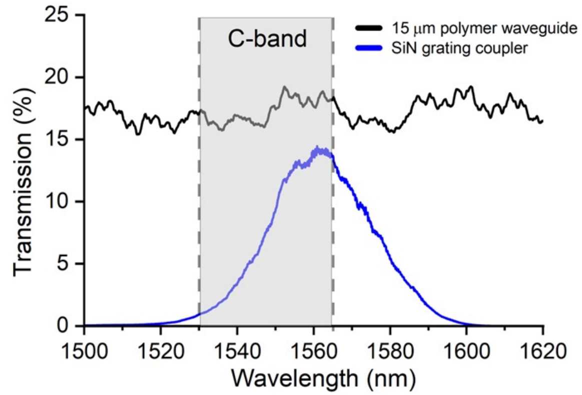




Result

Fabricated and characterized low loss broadband multimode surface-surface coupling waveguide which aims at reducing the complexity of coupling surface emitting components



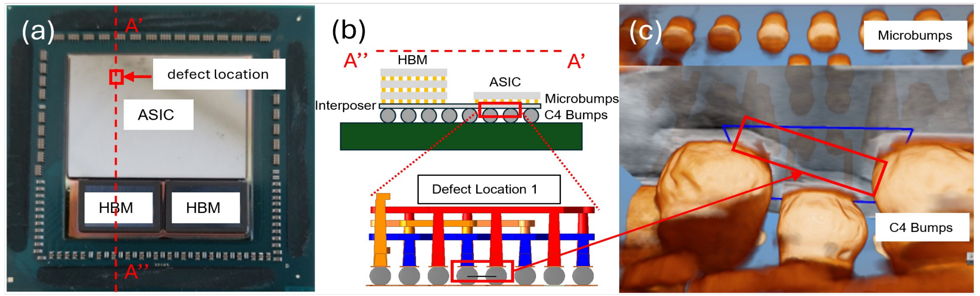


Thrust 4: Machine Learning Guided Failure Analysis & Diagnostic Capability Development for Next-Gen 3D-IC Packaging (Cont'd)

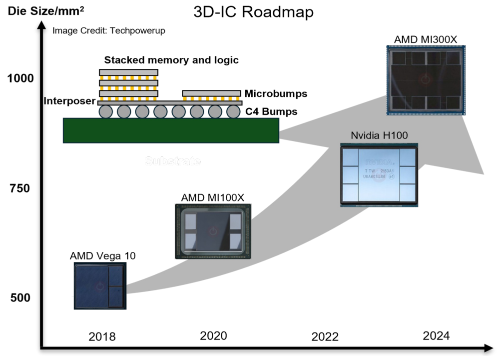
IEEE Electronic Components and Technology Conference (ECTC) 2025

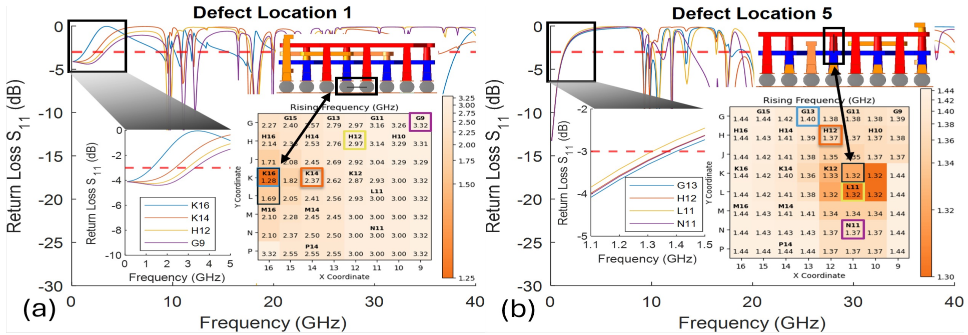
First Proof of 3D-IC Power Plane Defect Localisation via Frequency Domain Spatial Heat Mapping

Z.S. Shi, L. Lum, B. Zee, J.M. Chin, Y.K. Lim

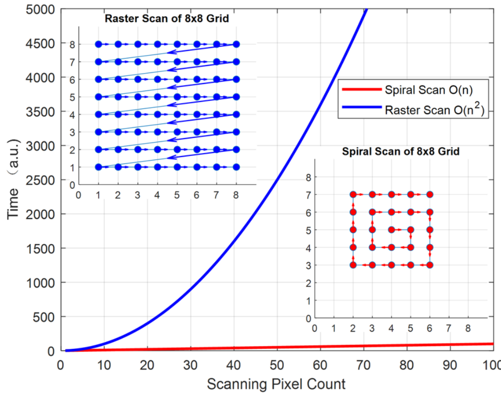


(a) A stacked graphics processing unit consisting of two high bandwidth memory (HBM) stacks and an application specific integrated circuit (ASIC) on a silicon interposer. (b) Defect location 1 in simulation corresponds to the actual published defect location, (c) where 3D XRM reveals an actual defect between two solder balls.

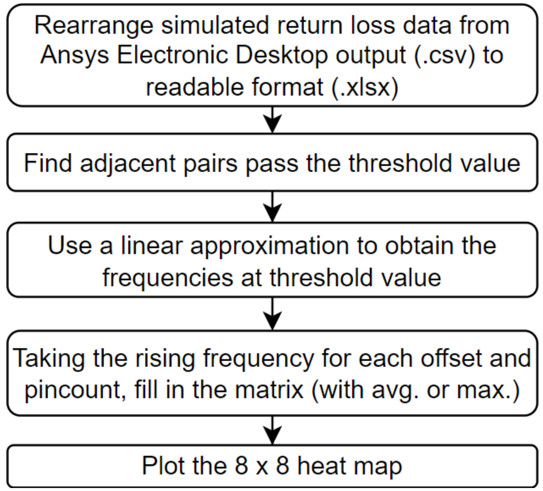




(a) Increased impedance from increased defect distances increases the resonant frequency. (b) The pins closest to the defects have the lowest impedance and lowest resonant frequency.



Big-O time complexity of raster scan versus spiral scan.



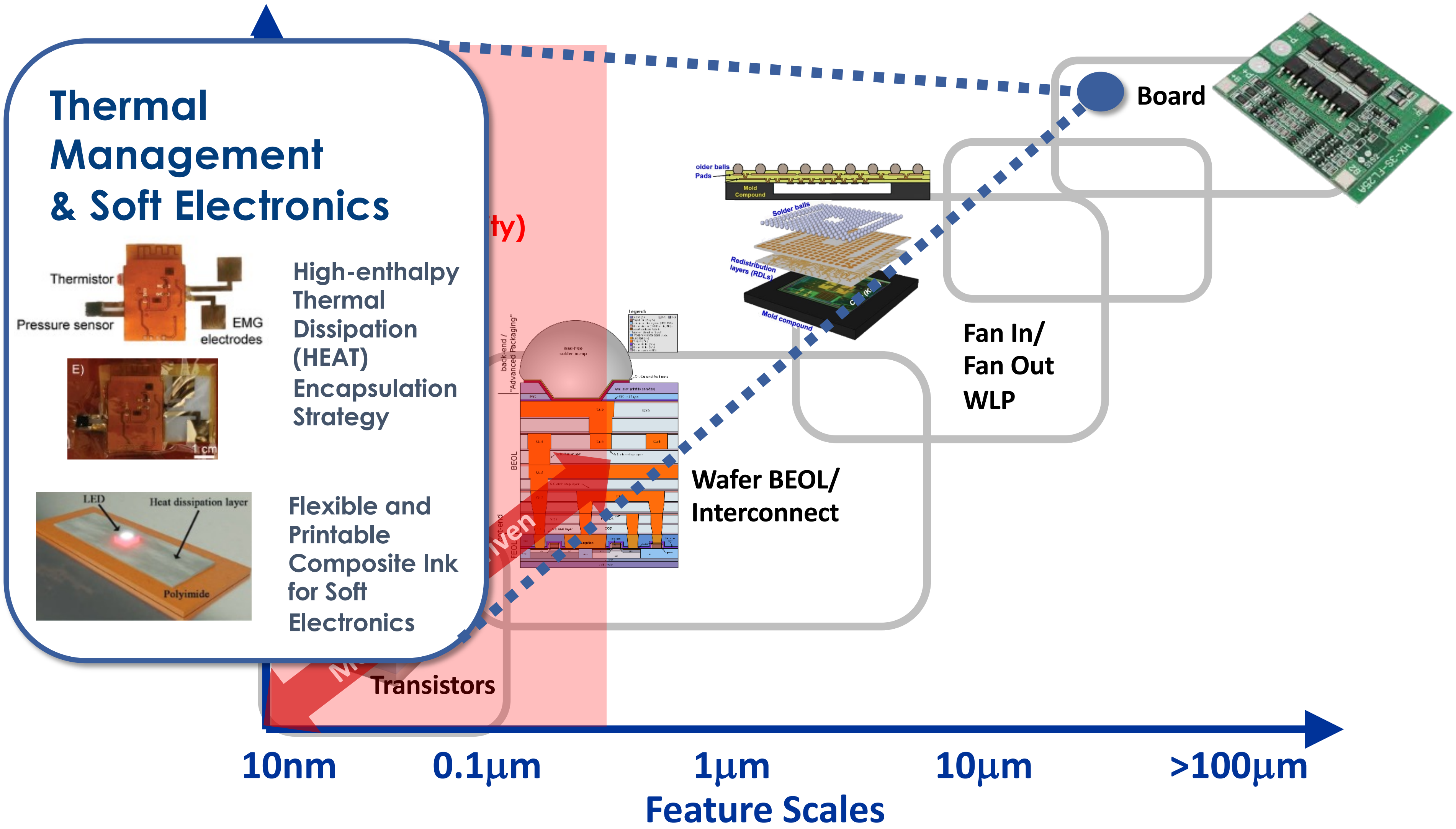
Flowchart of Python program extracting and parsing the simulated return loss data into a heat map by recording frequencies of individual pins past a threshold value.

Highlights of this work

- First proof solution of a challenging problem in 3D-IC power plane FA
- A novel signal processing method using heatmap to visualise return loss data to readily localise power plane defects
- A new spiral scanning method is proposed in place of conventional raster scanning to improve NDT scan time by one order of magnitude
- This work paves the way to predict defect locations using advanced frequency domain analysis

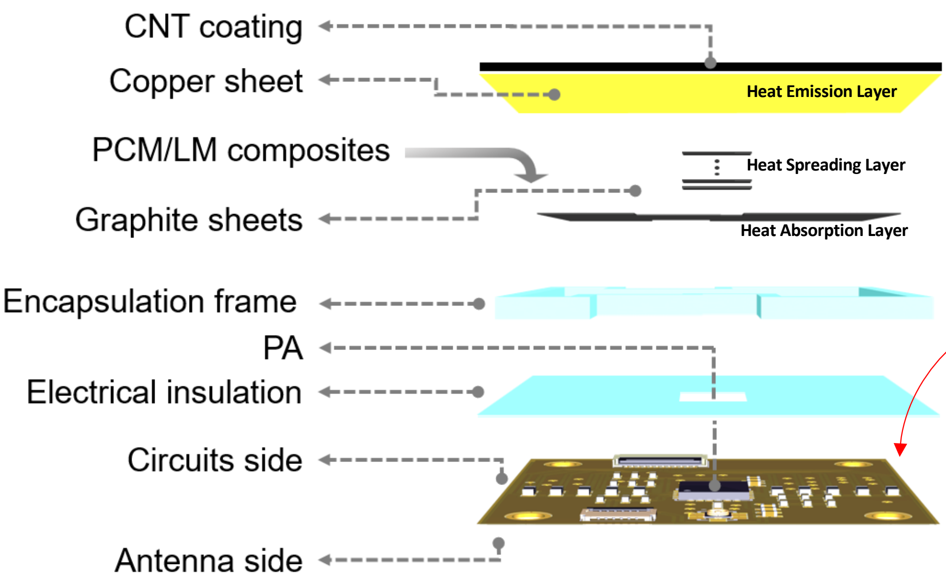
SHINE

SHINE's 2024 Research Highlights



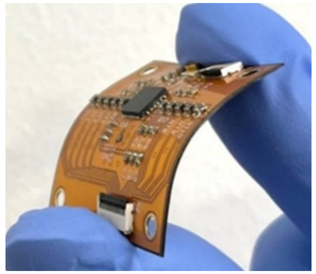
Integrate Thermal Solution for Flexible Antenna System (On-going Work)

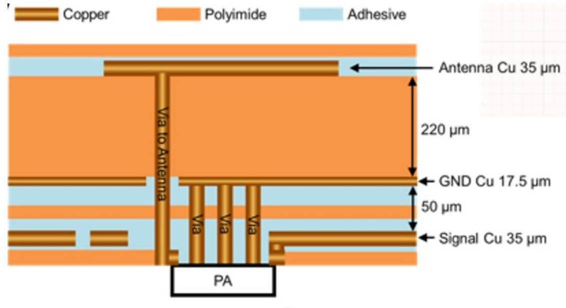
Advanced Heat Spreaders and Sinks with TIM



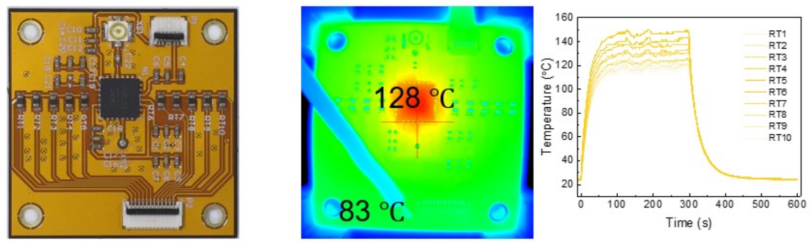
- Temperature distribution becomes more uniformed
- Overheating is delayed by 4.6 times and the equilibrium temperature is reduced to below 150 ℃
- PA continued operating for more than 5 minutes

Proposed Flexible Antenna

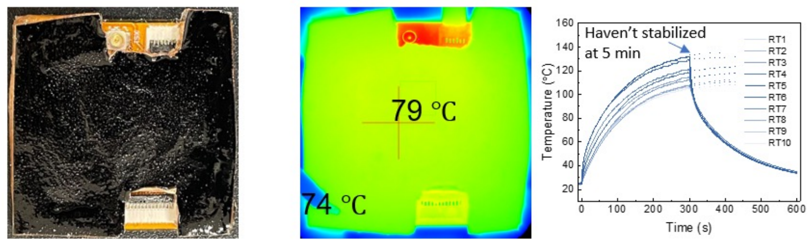




Without Thermal Management



With Proposed Thermal Management



High-Speed Die Temperature control for GPU Wafer-level Testing Through Liquid-Thermoelectric Hybrid Chuck System

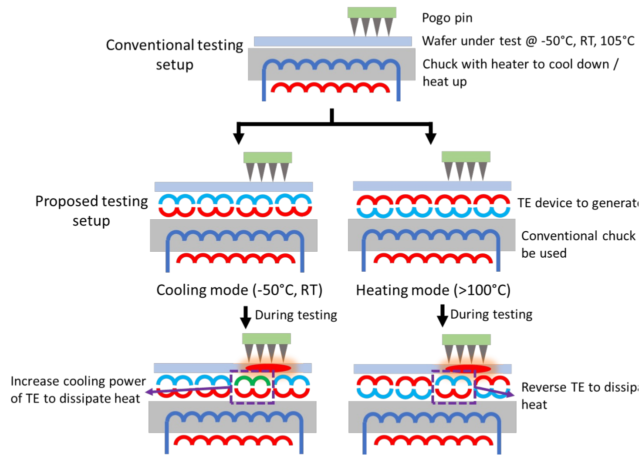
Wafer-level testing is a critical stage in the semiconductor manufacturing process, involving the testing of multiple ICs on a single wafer before the devices are separated into individual chips.

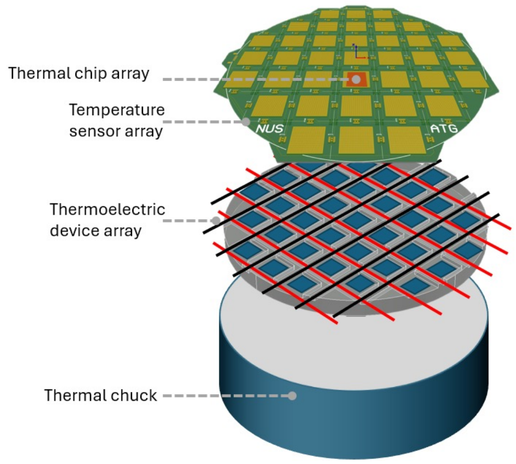
Problem: Advanced chip wafer testing generates significant localized heat, causing thermal stress and potential cracking of the wafer.

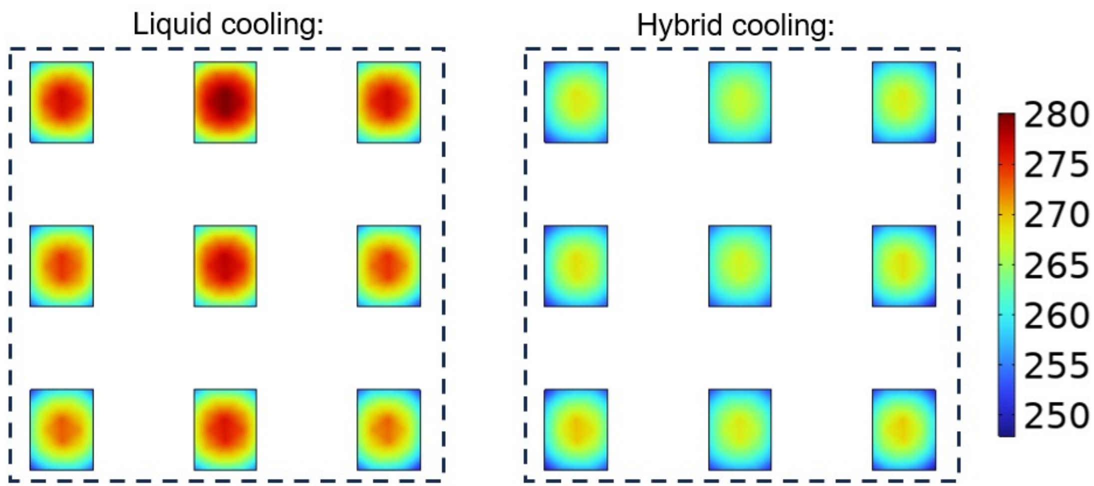
Innovation: Cutting-edge combination of speed, precision, and adaptability positions thermoelectric systems as a game-changing solution for advanced thermal management at wafer or chip scale, where performance outweighs cost and energy concerns.

- **Smart Heat Control:** Thermoelectric systems offer precise, programmable thermal management by controlling heat flow via DC current, allowing for dynamic heat transfer and real-time adjustments in direction and intensity.
- **Ultra-Fast Thermal Response:** Leveraging the Peltier effect, these devices provide rapid and efficient heating and cooling, enabling quick thermal stabilization with minimal lag.
- **Adaptive Localization:** Thanks to their flexible design, thermoelectric devices can be custom-shaped to target and cool specific micro-areas, offering ultra-precise thermal control for advanced testing scenarios.

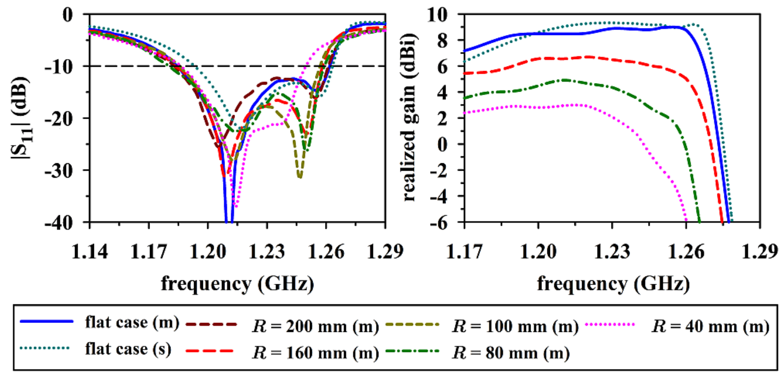
SHINE



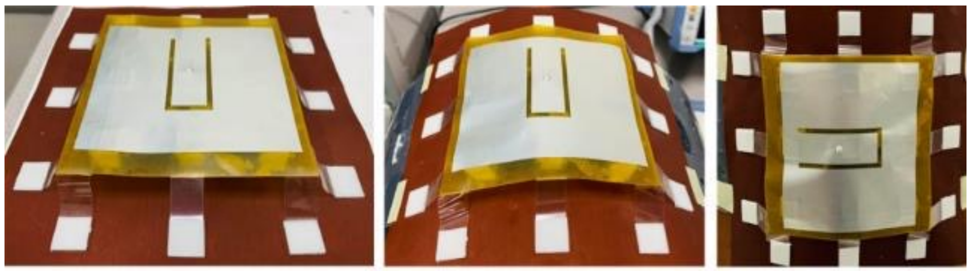




Flexible Antenna Design: Flexible L-band Phased Array



(a) (b)



(a) (b) (c)

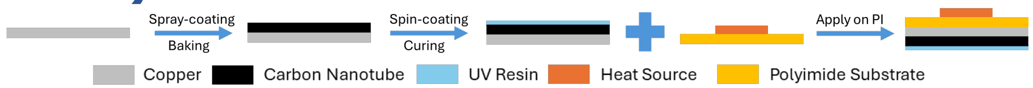
(a) (b)

(c) (d) (e)

Highlight of This Work

- ❑ Various L-band flexible and foldable antennas have been designed and tested, enabling low-cost experimentation and selected candidates will be translated to C-band and X-band in the future.
- ❑ Highly Flexible and Foldable Antenna Array using Corrugated CCPM-based Patches is designed and tested. Accepted for ISAP 2024.
- ❑ Multilayer and Lightweight Conformal Antenna Using U-Slotted Patch and Stacked Polyimide Films is designed and tested. Accepted for ACAP 2024.
- ❑ Highly Flexible and Deployable Antenna Array Using Double-arch-shaped PTFE Films is designed and tested. Accepted for APMC 2024.

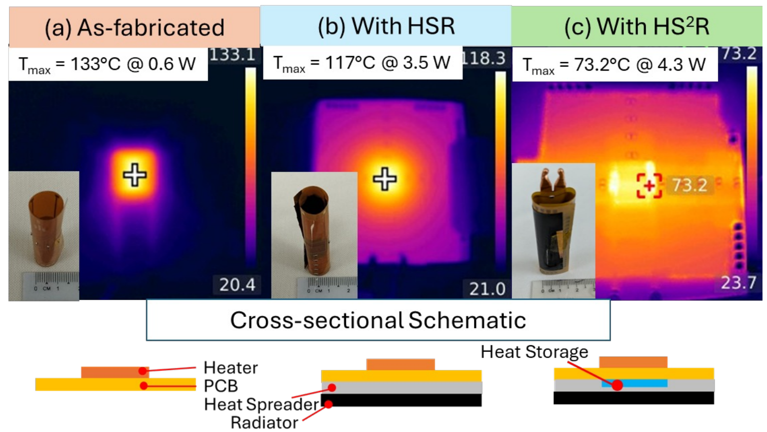
A Heat-Spreader, Storage & Radiator (HS2RTM) for Flexible Electronics: First Demonstration

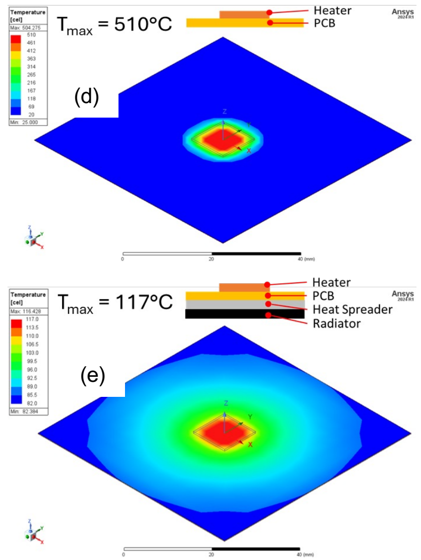


Schematic of fabrication processes

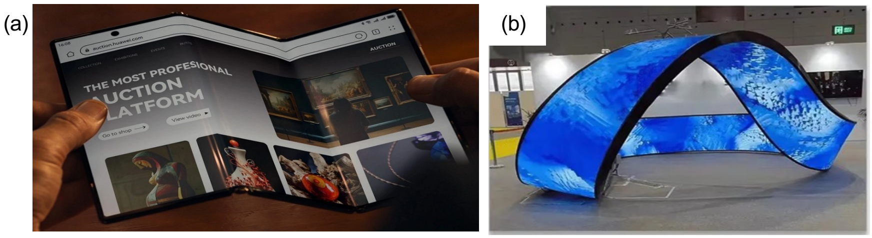
Highlights of this work

- **First demonstration of passive thermal management solution for flexible electronics** (up to 4.5 W, power consumption of phone: 0.2 W (idle) 1 W (making call))
- Passive thermal management is achieved through **integration of heat-spreader, heat storage, and printed radiator**
- Heat-spreader & radiator (HSR) **are shown to be scratch- and water-resistant**
- Substrate can be rolled up to a **bend radius of 0.5 cm**
- **It opens the possibilities for high power applications on flexible substrate**

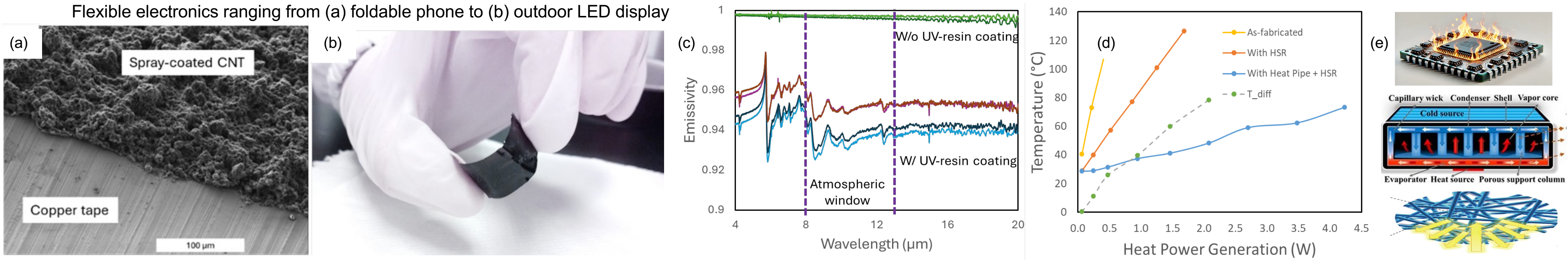




Thermal characterizations of (a) as-fabricated, (b) HSR-applied, and (c) HS²R-applied PCB (inset: stowed mode at 1cm diameter); Simulation comparison of PCB (d) w/ and (e) w/o thermal solution at 3.5 W

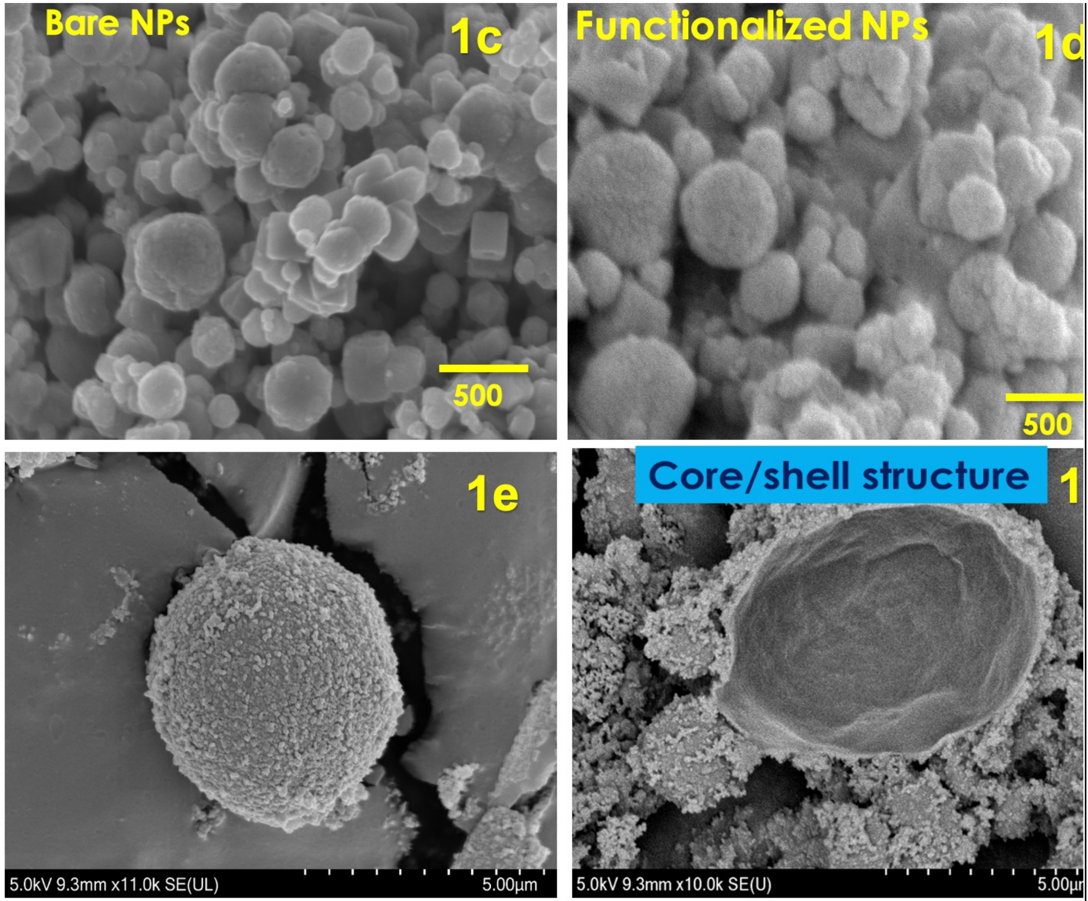


Flexible electronics ranging from (a) foldable phone to (b) outdoor LED display



(a) Morphology of CNT-based radiator under SEM; (b) Flexible fabricated HSR; (c) Emissivity of HSR; (d) Thermal performance under various conditions; (e) Stacked layers of HS²R

(New)Engineered Magnetic Nanoparticle Suspension with thermal phase-change property – For Magnetic actuated Liquid Cooling



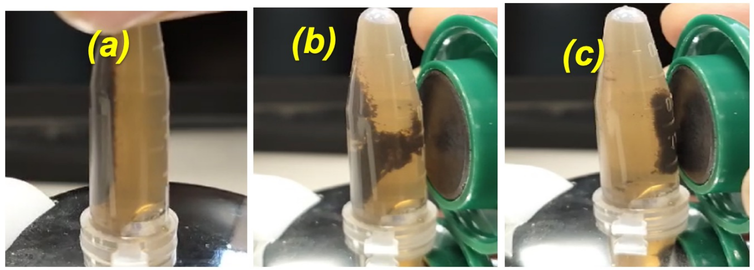
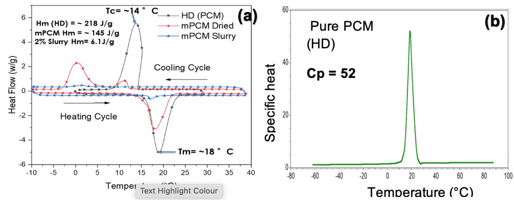
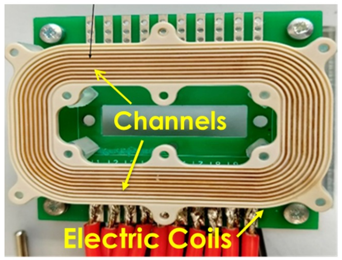
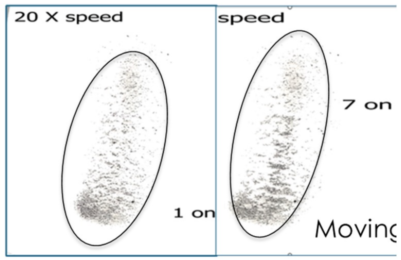


Fig. 4. Magnetic IONP-decorated microcapsules in water: (a) All microcapsules attached to the wall under the magnetic field, (b) Microcapsules detaching and flowing through the water toward the magnet, (c) All microcapsules attached to the wall on the opposite side under the magnetic field.







Multiple Levels of Integration