Institute of Microelectronics
A*STAR IME

R&D Catapult Platforms for SiC and Piezo-MEMS

Navab Singh, PhD
Deputy Executive Director (Research),
IME, A*STAR, Singapore

R&D Catapult platform for Silicon Carbide

- ❑ SiC a material of choice for medium and high voltage Power Electronics
- ❑ Major Challenges in SiC power technology development
- ❑ Key Highlights of our 200 mm SiC Open R&D Pilot Line
  - State-of-the-art Epitaxial Quality with High Throughput
  - Industrial grade SiC Process Modules
  - SiC Power MOSFET Demonstration
- ❑ Summary

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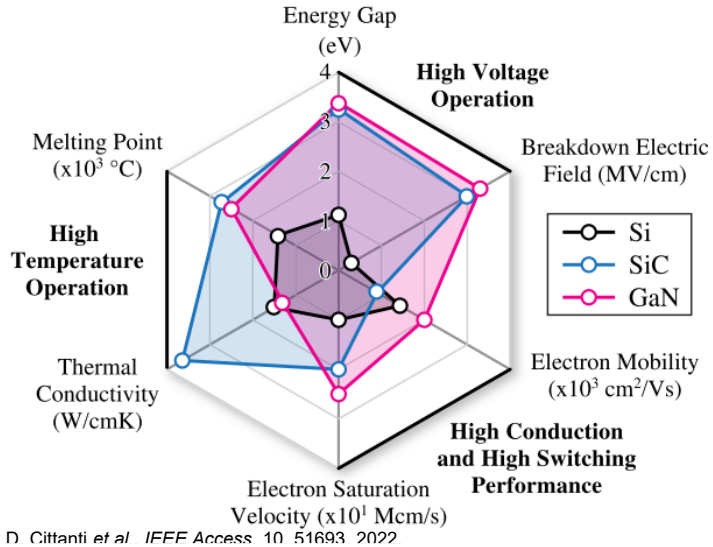
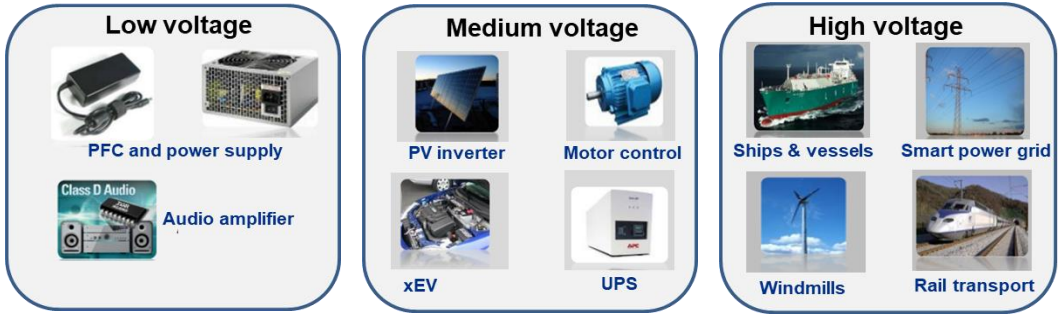
SiC a material of choice for power electronics

Parameter	Description	Si	SiC	GaN
E_g (eV)	Bandgap	1.12	3.26	3.39
μ_n (cm²/Vs)	e⁻ mobility	1430	900	2000
υ_n (Mcm/s)	e⁻ saturation velocity	10	20	25
E_c (MV/cm)	Critical field	0.3	3.0	3.3
κ_{th} (W/cmK)	Thermal conductivity	1.5	3.7	1.3
T_m (°C)	Melting point	1414	2730	2500

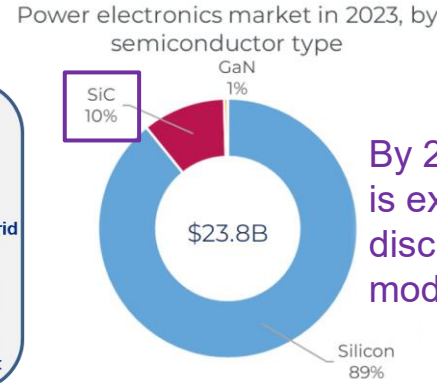


D. Cittanti *et al.*, *IEEE Access*, 10, 51693, 2022

Applications categorized by voltage range:



2020 Yole report



By 2029, up to 25% is expected for SiC discrete and power module.

2024 Yole report: Status of the Power Electronics Industry

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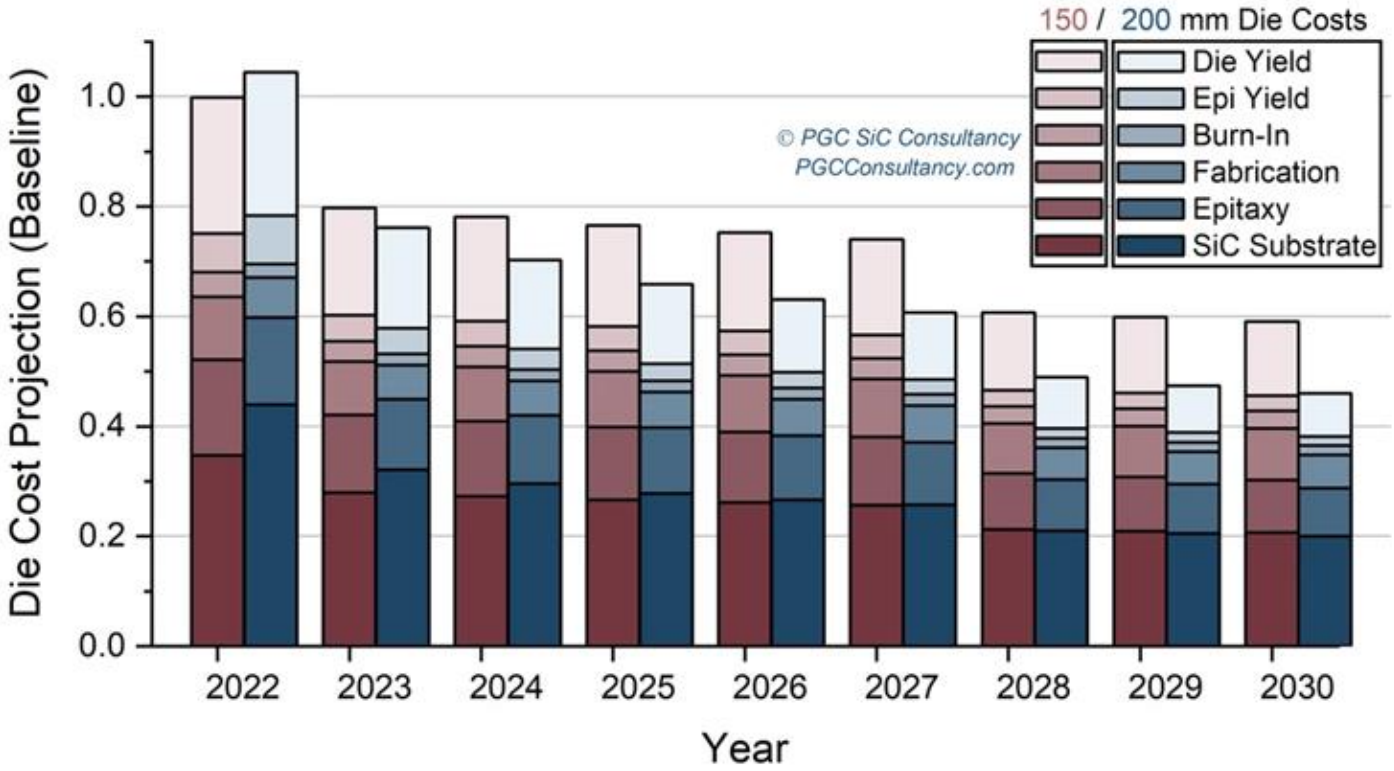
Major Challenges for SiC Power Technology – Cost

Driving force behind 8” wafer scaling

For a 32 mm² die, 200 mm wafer provides 1.89x more devices than 150 mm wafer

Assuming identical yield, 200 mm is expected to provide ~ 20% lower die cost than 150mm by 2030
(for 1200 V/100 A rated device)



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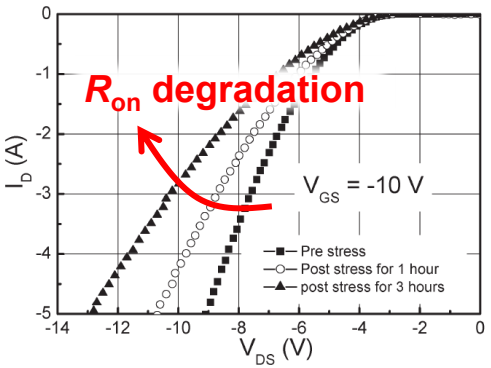
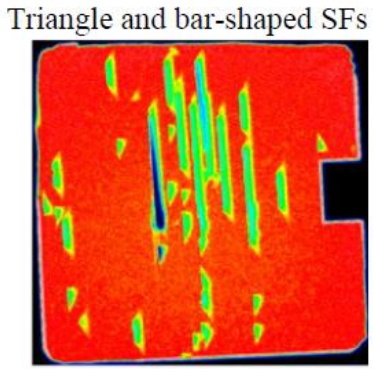
Major Challenges in SiC Power Technology – Bipolar Degradation

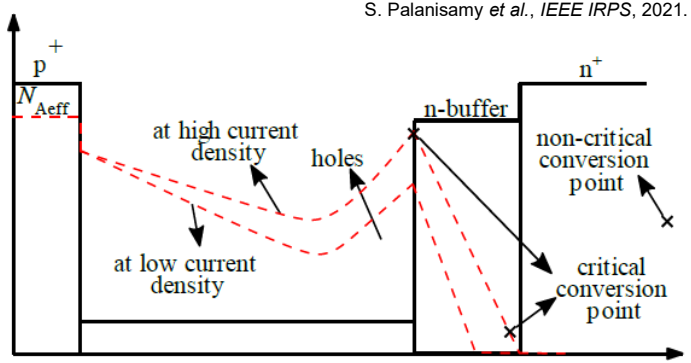
Consequence of bipolar degradation – stacking fault formation – performance drop

A. Agarwal *et al.*, *IEEE EDL*, 28, 587, 2007.



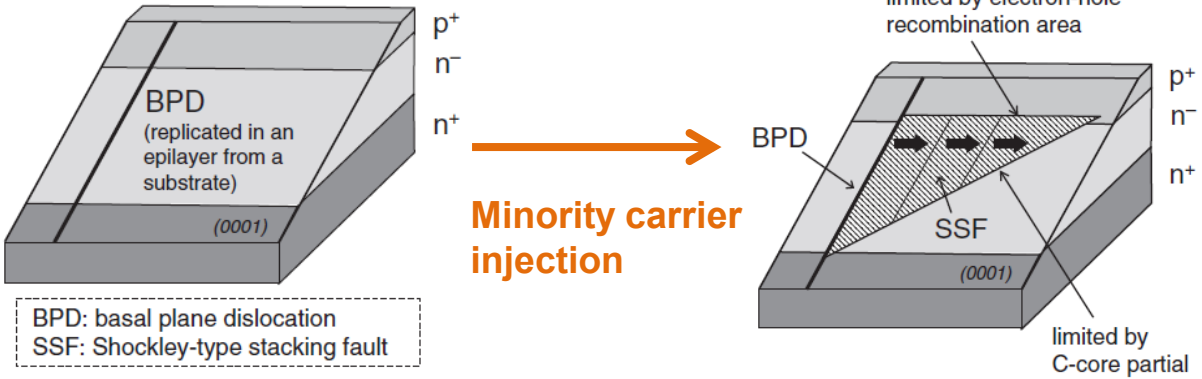


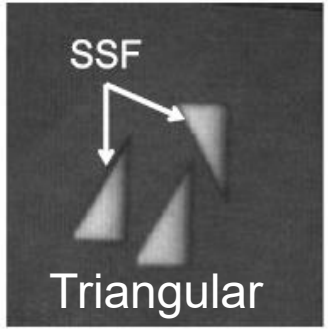
S. Palanisamy *et al.*, *IEEE IRPS*, 2021.



Recombination enhanced stacking fault expansion

T. Kimoto *et al.*, *Jpn. J. Appl. Phys.*, 54, 040103, 2007.

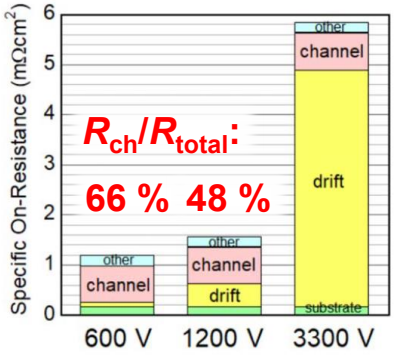




Reducing BPD is required to mitigate unwanted bipolar degradation.

Major Challenges in SiC Power Technology – MOS Interface & Oxide Reliability

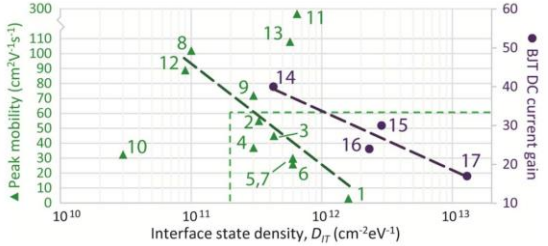
Limited inversion carrier mobility due to interface and near interface oxide traps



T. Kimoto *et al.*, *Appl. Phys. Express*, 13, 120101, 2020.

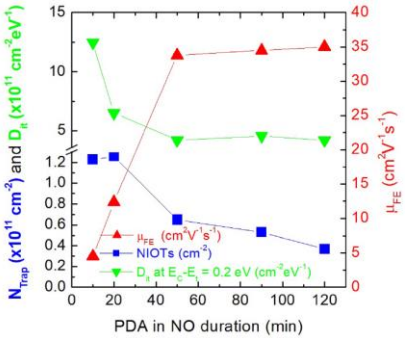
Route cause:

Interface trap:



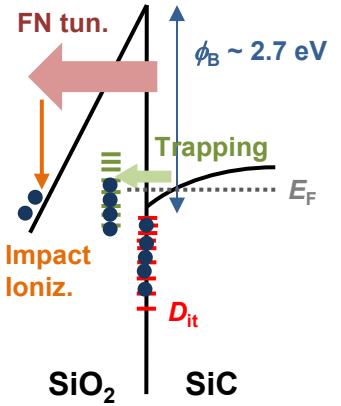
A. Siddiqui *et al.*, *IEEE TDMR*, 16, 419, 2016.

Near interface oxide trap:



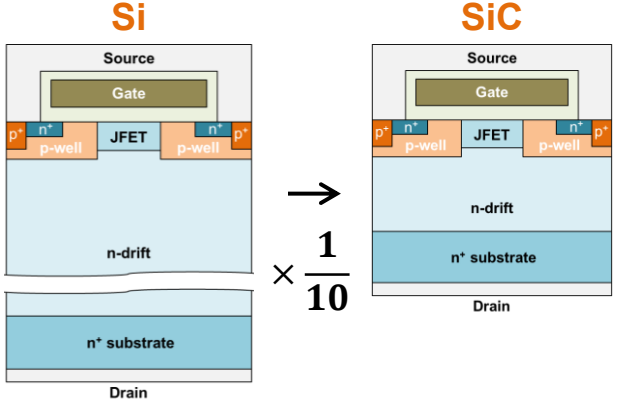
P. Fiorenza *et al.*, *Mater. Sci. Semicond. Process.*, 169, 107866, 2024.

Gate oxide reliability: bias temperature instability and oxide lifetime



1. Higher oxide electric field governed by: $E_{ox} = (\kappa_{SiC}/\kappa_{ox})E_{SiC}$ with E_{SiC} ~ 2-3 MV/cm.
2. Larger D_{it} and NIOTs: Severe BTI and trapping-related transient effects.
3. Smaller conduction band offset: Larger leakage current.
4. Earlier trigger of F-N current: impact ionization and oxide lifetime degradation.

Major Challenges in SiC Power Technology – Avalanche Ruggedness



For same voltage and current rating, both epitaxy thickness and device area are reduced when using SiC devices.

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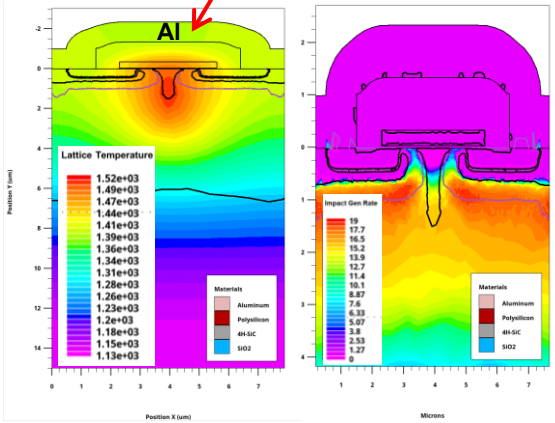
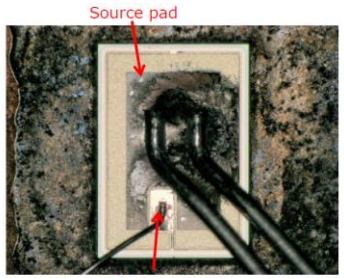
Higher current density aggravates heat buildup, and thus, causing concerns in its avalanche ruggedness

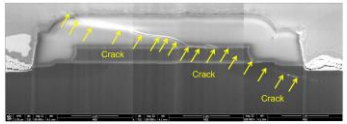
Short circuit withstand time:

Estimated temperature > 1200 K



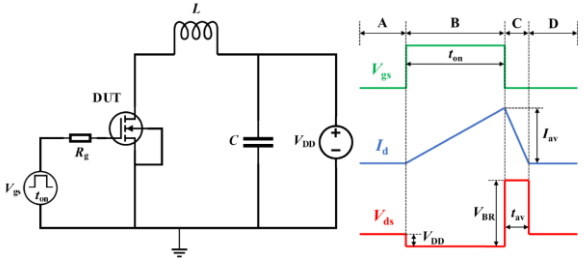


M. Namai *et al.*, *Jpn. J. Appl. Phys.* 57, 074102, 2018.

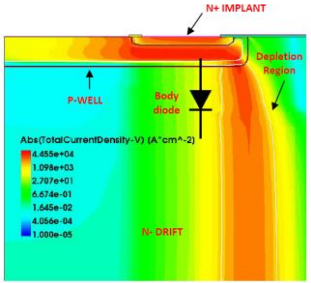


P. D. Reigosa *et al.*, *Microelectron. Reliab.*, 88, 577, 2018.

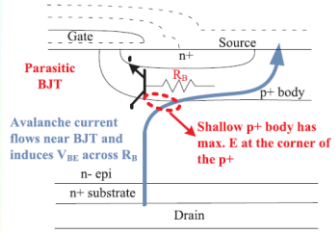
Avalanche energy:



H. Wu *et al.*, *IEEE TED*, 70, 1181, 2023.



A. Fayyaz *et al.*, *IEEE WiPDA*, 2016.



N. Ren *et al.*, *Solid State Electron.*, 152, 33, 2016.

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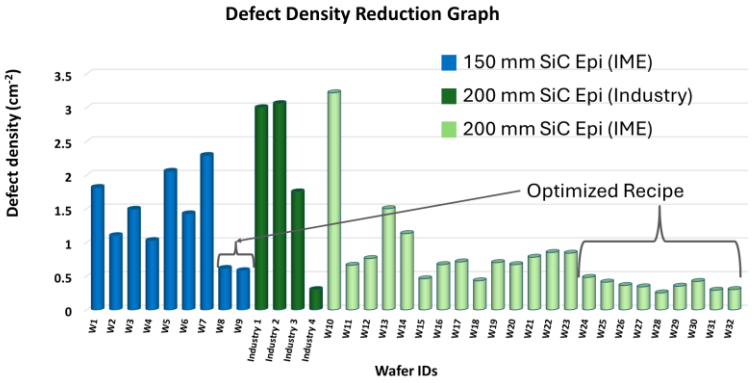
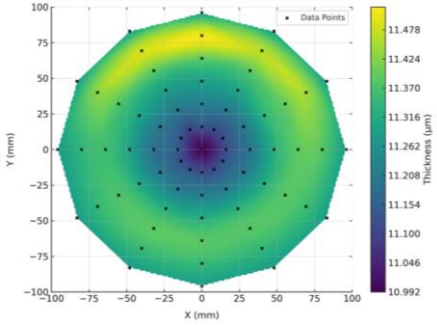
High Throughput SiC Epitaxial Growth with Low Defect Density

State-of-the-art epitaxy quality with ≥ 50 μm/hr



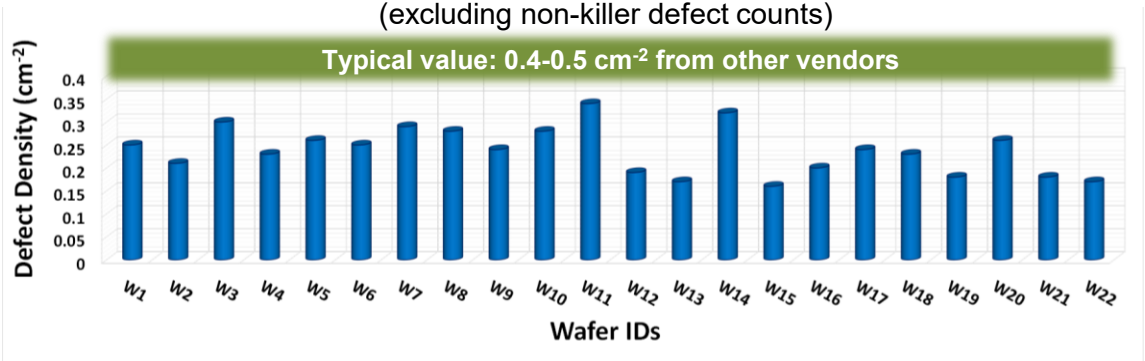
Average thickness: 11.3 μm



Thickness nonuniformity (σ/μ): 0.93 %

Historical data from optimized recipe

(excluding non-killer defect counts)



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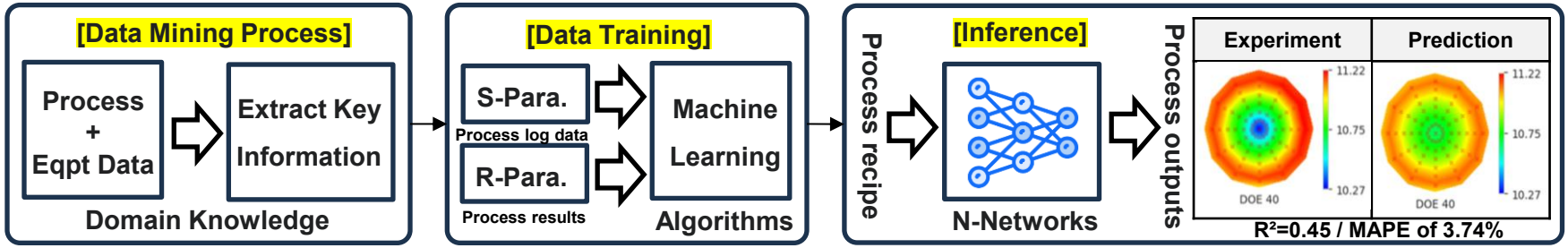
AI/ML-Based Improvement of SiC Epitaxy Thickness Uniformity

1. SiC Epitaxy Thickness Prediction Model Development:

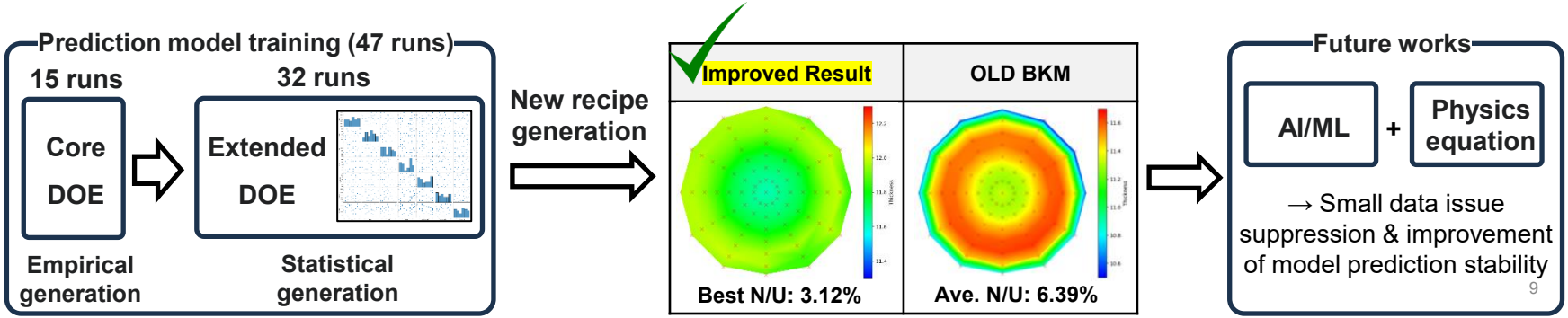
→ Neural network-based process prediction model development using ASM PE1O8 Equipment (6/8-Inch Wafers)



2. Process Improvement Using AI/ML Prediction Models:

→ Prediction model-based recipe development and validation **(N/U: 6.39% → 3.12% improvement (N/U=3σ/Mean))**

→ Integration of physics equations in progress for further improvement of the prediction model



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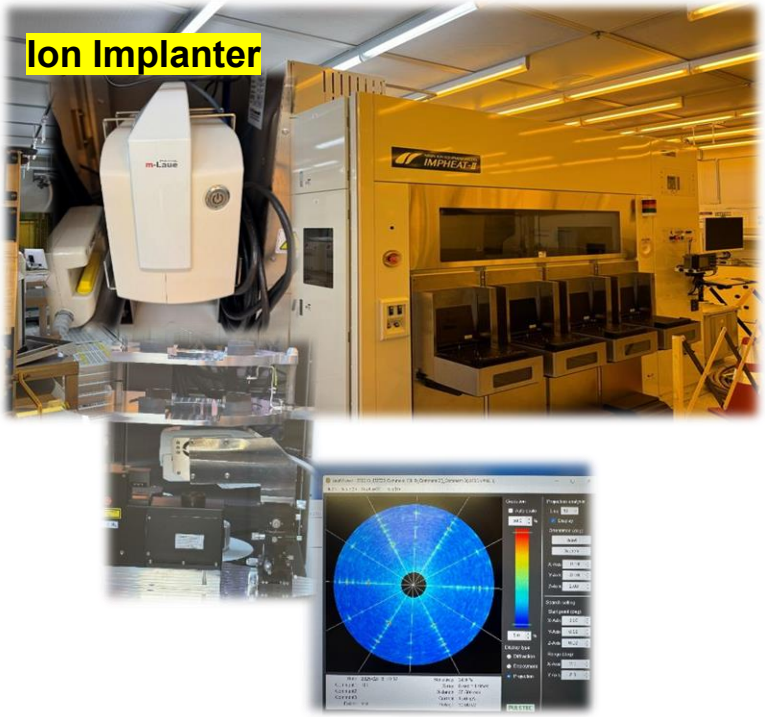
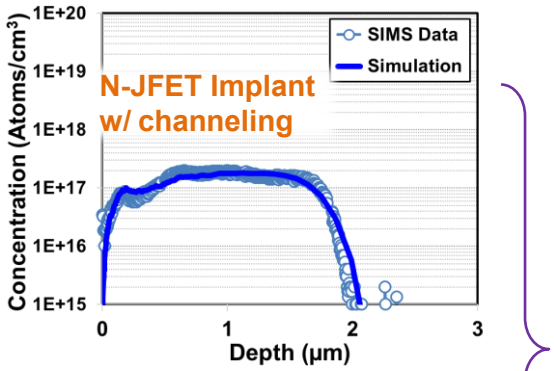
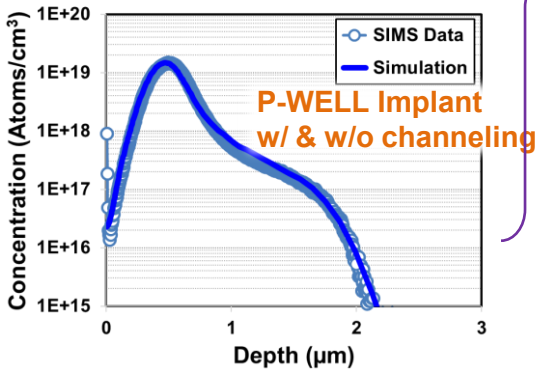
Precise Implantation Control with In-situ XRD



- *in-situ X*-ray diffraction system (Laue's diffraction)
- To accurately calibrate the tilt angel for channeling implantation

- **B, N, Al, P and Ar implant.** on Si and SiC
- Energy Range: **10 ~ 960 keV**
- Temperature: **25-500 °C**
- Tilt angle: **0-60°,** Twist angle: **0-270°**
- Qualified process for 200 mm SiC and Si wafers





Good matching between experimental and simulated results

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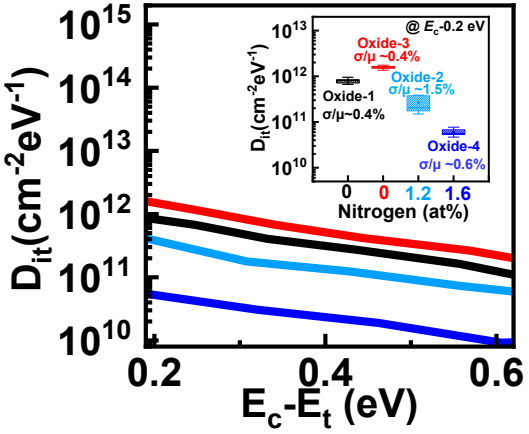
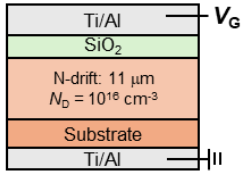
Gate Oxide Interface: Reduced Interface Trap through Deposited Oxide Scheme



S/N	Oxide	Annealing	Thick. (nm)	[N] (cm^{-2})
D1	Thermal	-	50	-
D2		NOPOA	50	1.16×10^{14}
D3	LPCVD (Deposited)	-	42	-
D4		NOPOA	40	1.26×10^{14}



Hi: f = 1 MHz
Lo: Quasi-Static
$E_{ox} = (V_G - V_{FB}) / d_{ox}$

Ref.	Oxide Deposition Technique	Post Treatment Gas/Tem(°C)/ Time(min)	t_{ox} (nm)	J_G (A/cm^2)	D_{it} (cm^{-2}eV^{-1})
This Work	LPCVD	NO/1300/30	40	5×10^{-10}	5×10^{10}
Ref-4	LPCVD	NO/1175/120	55	-	4×10^{11}
Ref-5	Sputter	CO_2/1250/240	33	1×10^{-9}	2×10^{11}
Ref-6	PECVD	N_2/1175/120	30	-	3×10^{11}
Ref-7	PECVD	N_2/1400/45	30	1×10^{-9}	4×10^{10}
Ref-8	LPCVD	NO/1250/120	50	1×10^{-9}	2×10^{11}
Ref-9	CVD	N_2/1300/600	45	1×10^{-9}	4×10^{11}

(Published in ICSCRM'24)

(To be presented in ICSCRM'25)

Low D_{it} of 5×10^{10} cm^{-2}eV^{-1} is achieved by LPCVD oxide

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Singapore's first 200 mm SiC Power MOSFET

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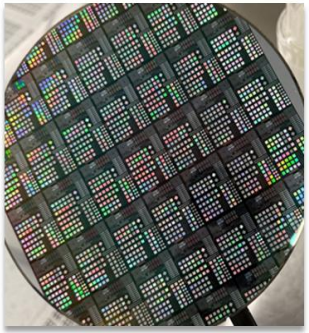
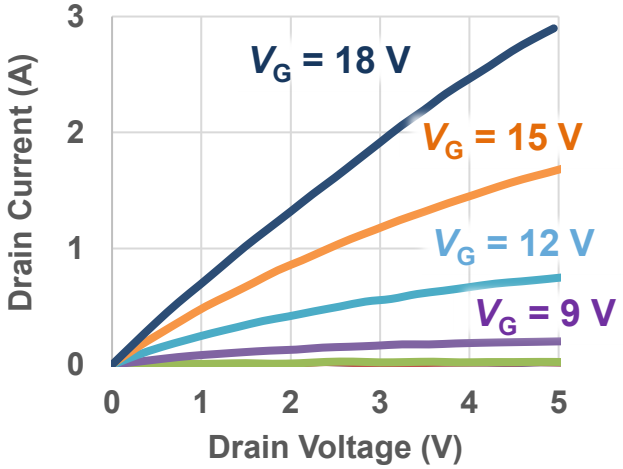
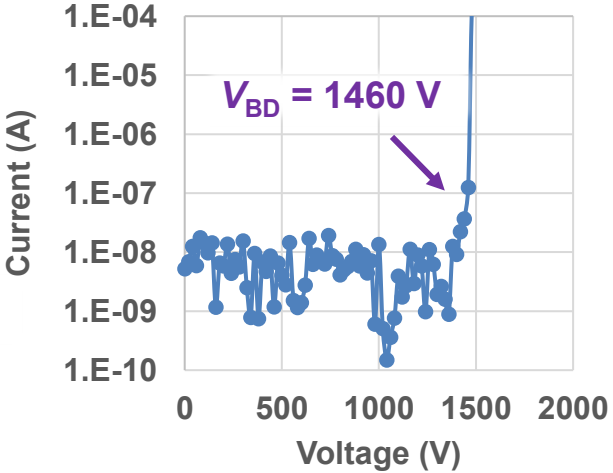
SiC MOSFET on 8-inch wafer



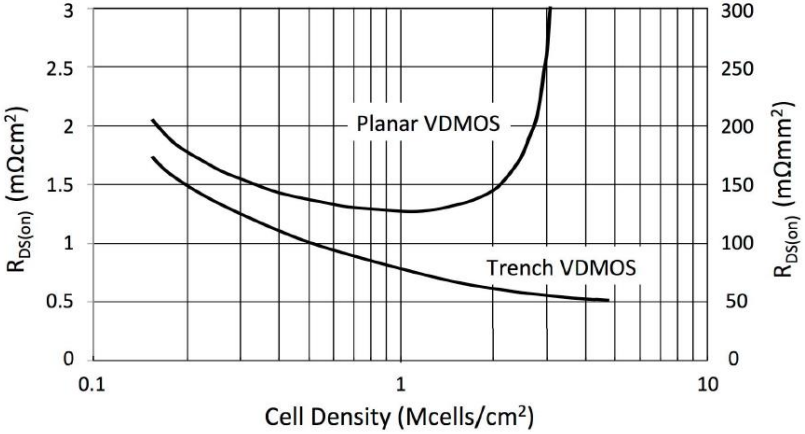


Simulated V_{BD} = 1485 V, Impact ionization model: Calibrated Okuto-Crowell model



Moving Towards SiC Trench Gate Technology for On Resistance Improvement

Scaling of specific on-state resistance



R. K. Williams *et al.*, *IEEE Trans. Electron Devices*, 64, 674, 2017.

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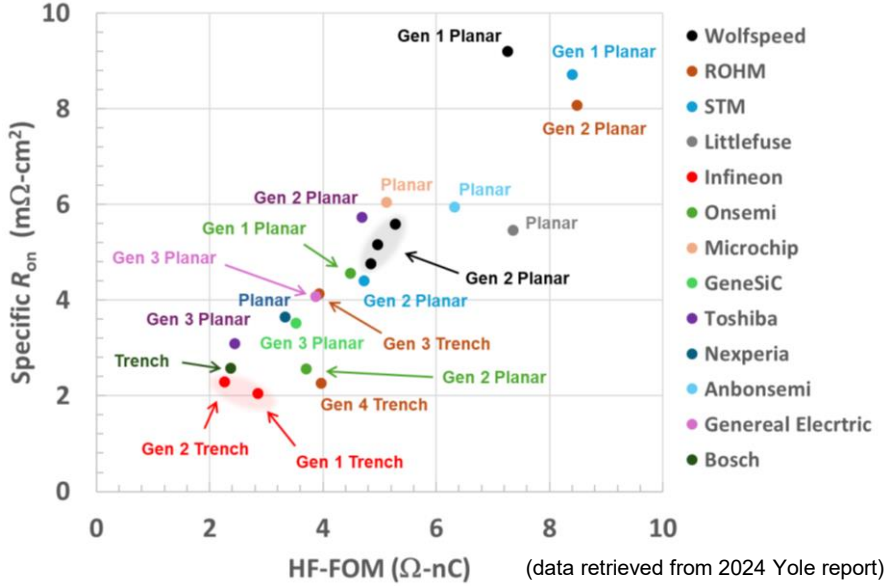
Trench technology allows one to pack more cells without compromising $R_{DS(on)}$

↓

Continuous improvement of B-FOM

1.2 kV-class SiC MOSFETs benchmarking



(data retrieved from 2024 Yole report)

Trench gate technology promises improvement in both B-FOM [= $V_{BD}^2/R_{DS(on)}$] and HF-FOM [= $R_{DS(on)}Q_G$]

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Summary

- **A*STAR has successfully established the world's first 200 mm SiC open R&D pilot line with following key achievements:**
  - SiC epitaxy: high throughput of **≥ 50 μm/hr** with a killer defect density of **≤ 0.4 cm^{-2}**
  - Ohmic contact: Ni-based ohmic contact with a specific contact resistivity **< 10^{-5} Ωcm²**
  - Gate stack: SiO_2/SiC interface trap density of **~ 5×10^{10} $cm^{-2}eV^{-1}$** using deposited oxide scheme
  - Readiness of the line is demonstrated using planar gate MOSFETs with V_{BD} **> 1400 V**

- **A*STAR is committed to continuously developing translational solutions for advancing SiC industry with our 200 mm SiC open R&D pilot line. We invite you to collaborate with us.**

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R&D Catapult platform for MEMS (Micro Electro Multiphysical Systems)

Vibration

Pressure

Acoustic

Ultrasound

Particle

Acceleration

Rotation

Flow

& more

Sensor

digitize the real world

MEMS Transducer

Electrical signals

Actuator

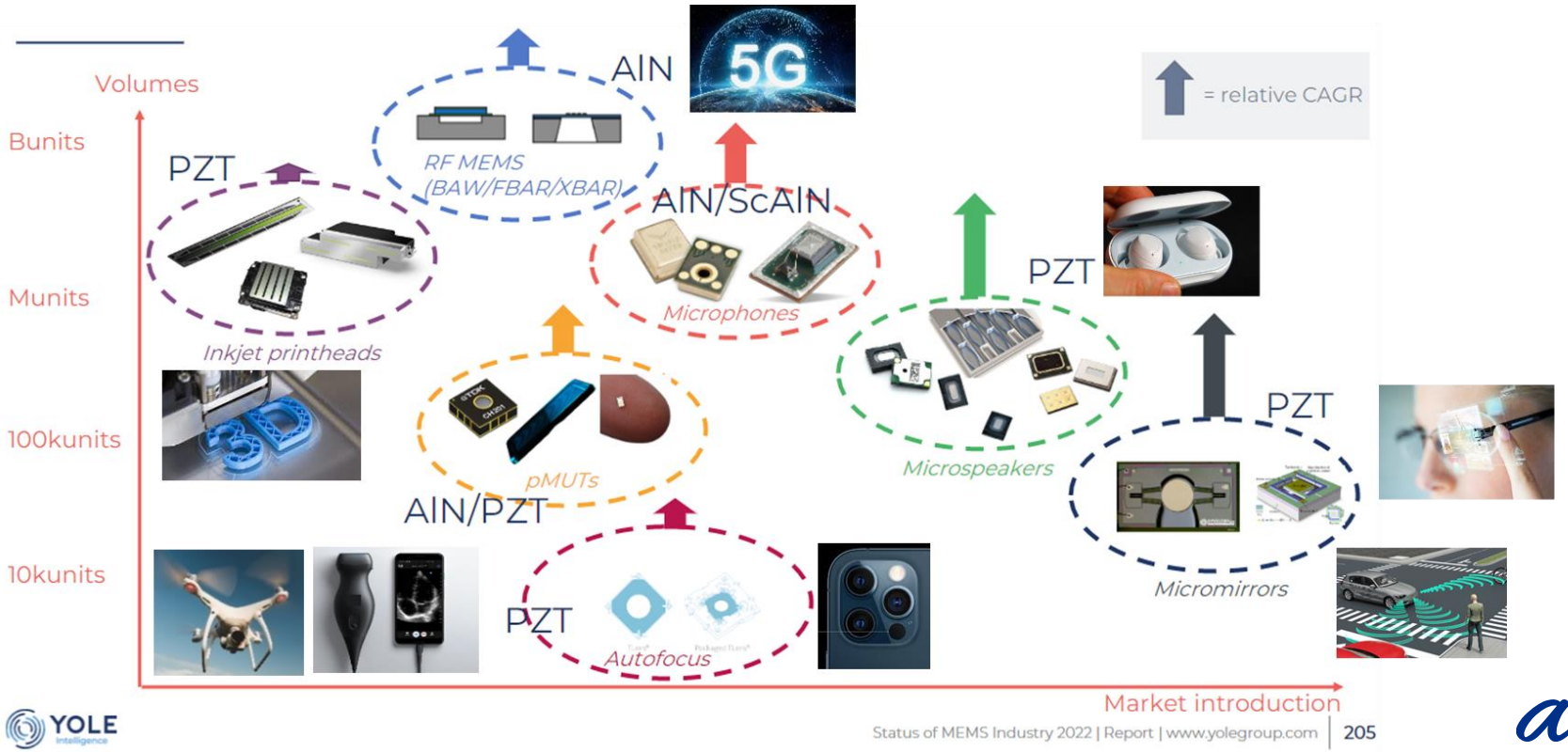
Interact with the virtual world

- ❑ Semiconductor process to produce thousands of devices simultaneously on a wafer
  - ✓ Low cost
  - ✓ Small form factor
  - ✓ Well controlled dimension and performance
  - ✓ Low power consumption

Conventional vs MEMS ultrasound transducer

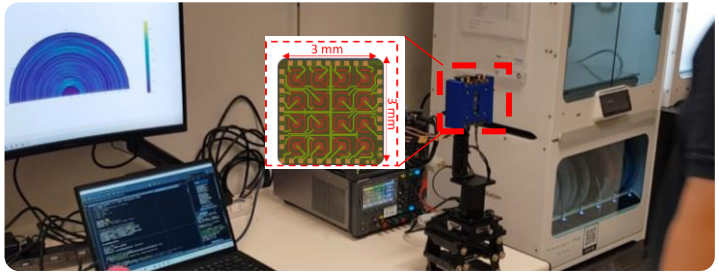
PiezoMEMS is the key technology to drive MEMS growth

✓ **Miniaturization** ✓ **Low driving voltage** ✓ **Integration compatibility**

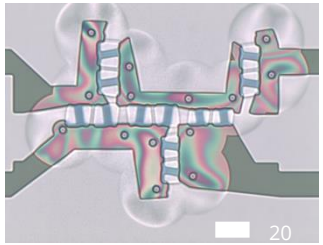


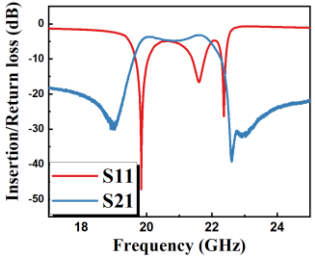
MEMS Device Demonstration

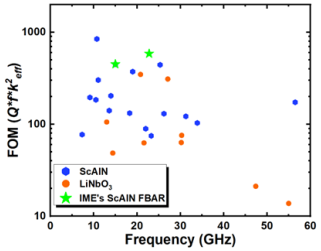
3D sensing – ultrasound beam steering, works in dark environment, ultra-thin chip down to 0.2mm, fully customizable array size and configuration.



mmwave filter – 20 GHz FBAR filter with 3.2 dB loss, 11% BW, highest figure-of-merit among all acoustic resonators > 15 GHz.

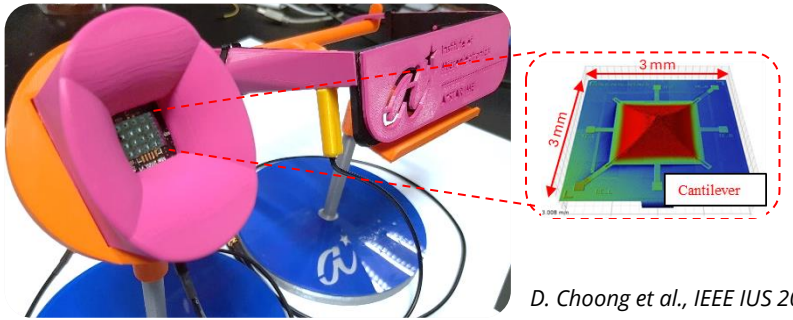






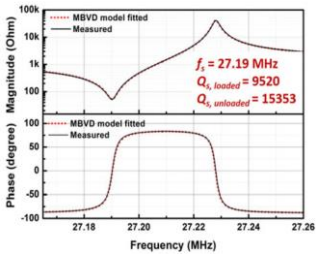
C. Liu et al., IEEE IEDM 2024

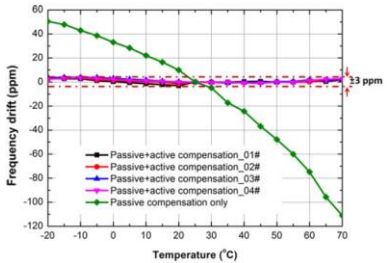
Microspeaker – ultrasound with amplitude modulation, lead-free piezoelectric material (ScAlN), up to 100X lower driving current than PZT.

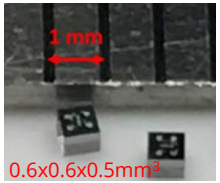


D. Choong et al., IEEE IUS 2025

Timing – MHz resonator with Q of 10k, AlN on cavity SOI, temperature stable with passive and active compensation







H. Wu et al., IEEE Trans. Ind. Electron.

PiezoMEMS Commercialization Challenges

- Technical challenges – functional piezoelectric thin film process and integration
- Limited standardisation (lack of PDK) and availability of open innovation platform
- Long lab-to-fab development time and cost

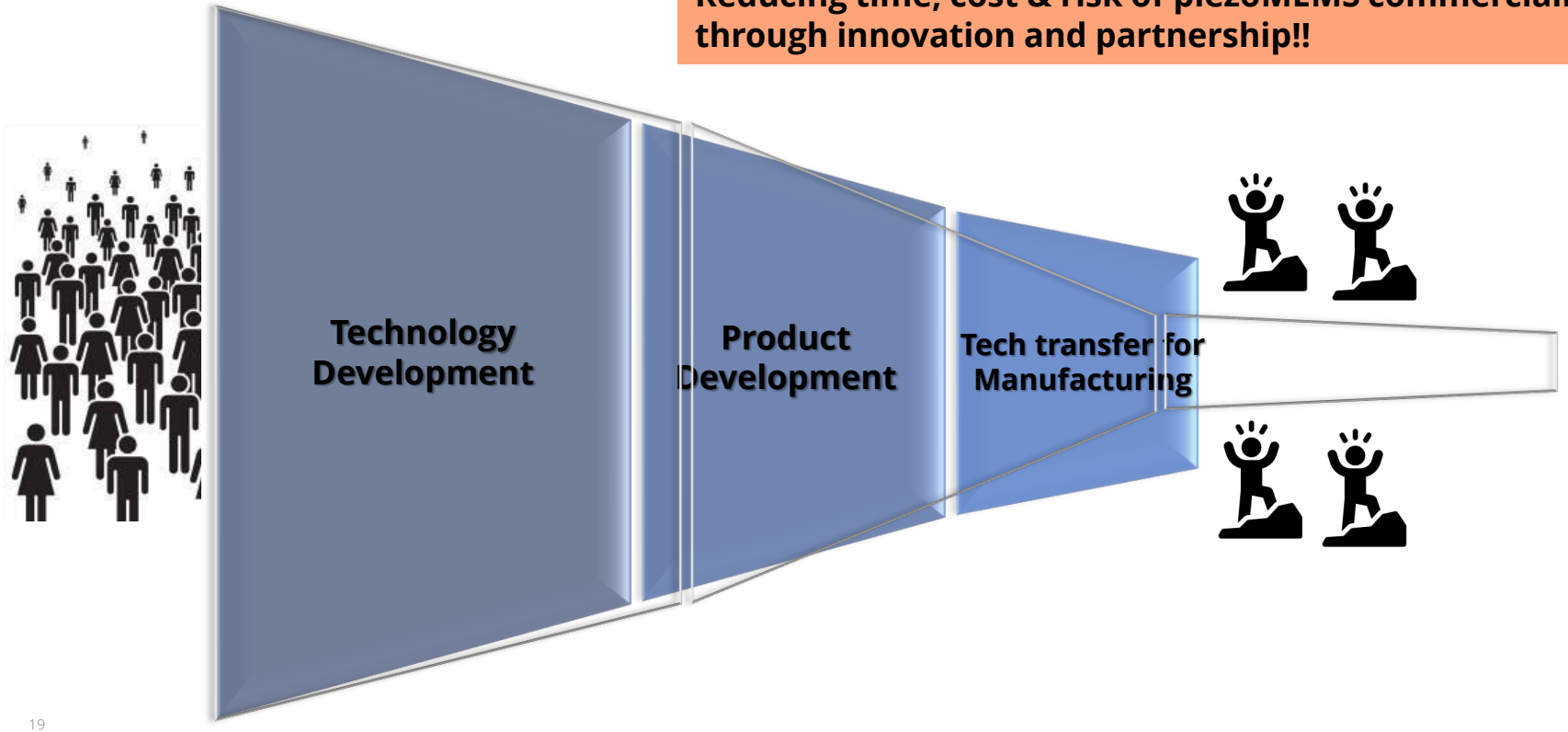
Technology Development

Product Development

Tech transfer for Manufacturing

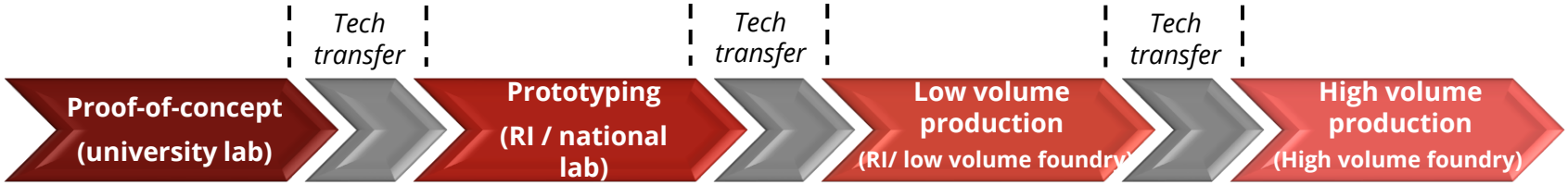
Tackling PiezoMEMS Commercialization Challenges

Reducing time, cost & risk of piezoMEMS commercialization through innovation and partnership!!



Designed for Scale: Starting the Development at Lab-in-Fab with the End in Mind

Conventional "Lab-to-Fab" model



Shorter path to commercialization with lower risk

IME-STMicroelectronics "Lab-in-Fab" model

ULVAC

- ~2000sqm cleanroom physically located in STMicroelectronics Singapore Fab
- Jointly operated by STMicroelectronics and IME
- R&D and manufacturing performed in the same fab, using the same equipment, and operated by the same team
- Providing customized device/process development
- Enable companies to commercialize their devices more quickly and with lower risk

Prototyping with Proven MEMS Platforms for Predictable Outcomes

Evaluating the technology using available sample device chips

Zero waiting time, minimum cost

Proof of concept using readily available platform, e.g. MPW

Fast d...

100% of companies returned for initiating follow-up projects after prototyping with us in the past one year

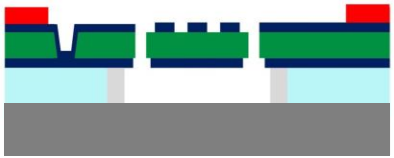
Improving the performance with process-design co-optimization

Customized manufacturable process, seamless transfer for production

ScAlN/PZT on Si platform

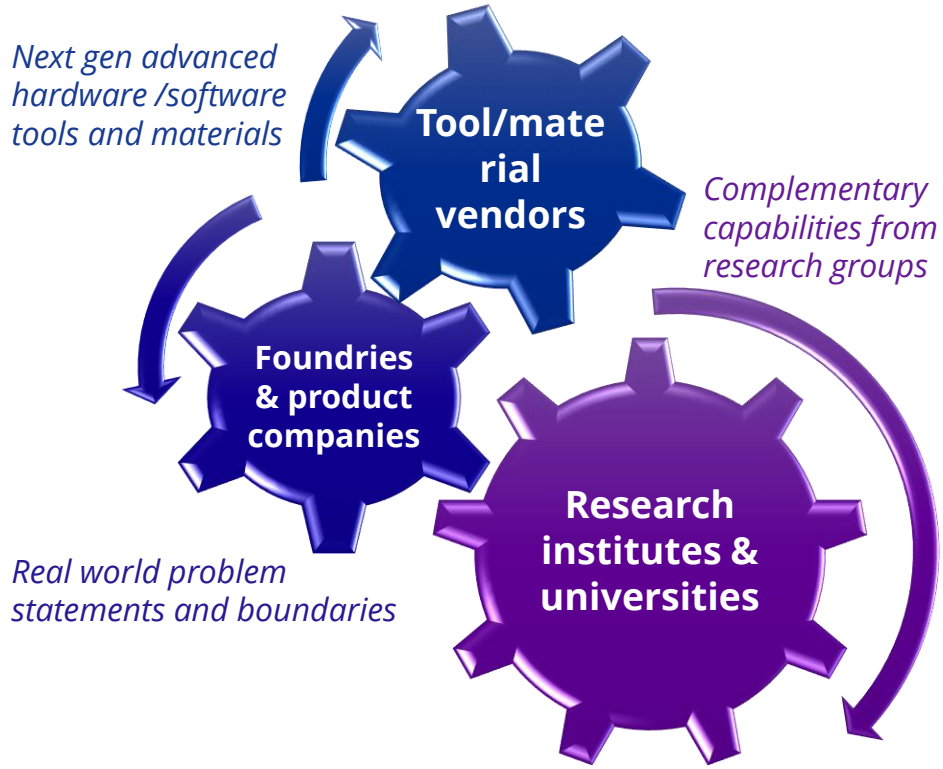
- Electrode-ScAlN-electrode-Si stack
- Backside Si etch cavity creation or cavity SOI
- Ideal for sensing and actuating applications

Thin-film ScAlN platform



- Electrode-ScAlN-electrode stack with minimum loading
- Frontside release for cavity creation
- Ideal for RF MEMS (GHz resonator & filter) and resonator-based sensors

Shaping the Frontier of PiezoMEMS & Nurturing the next Generation Talents Through Collaborative Innovation



- ✓ In 2025, signed MOU with TSRI and The Institute for NanoSystems Innovation at Northeastern University for joint research collaboration and talent development.

TSRI NARLabs 國家實驗研究院 台灣半導體研究中心 Taiwan Semiconductor Research Institute

The Institute for NanoSystems Innovation Northeastern University

- ✓ In 2024, offered PZT and ScAlN MEMS Multi-Project Wafer (MPW) to 14 participants across the world.
- ✓ Committed to continue the MPW offering to democratize piezoMEMS research.

We are open for partnership.

Let’s innovate together to create greater impact!