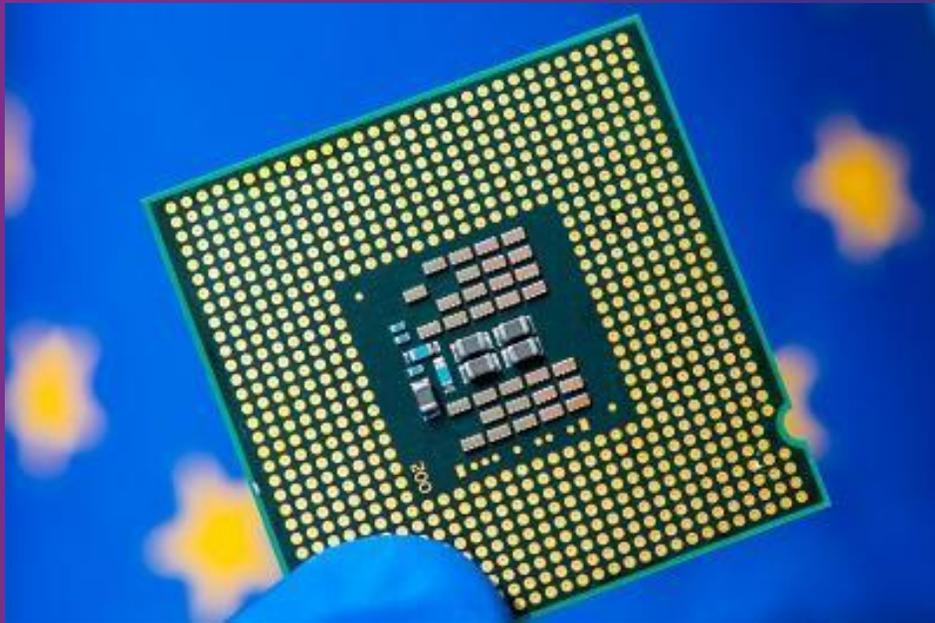




European  
Commission



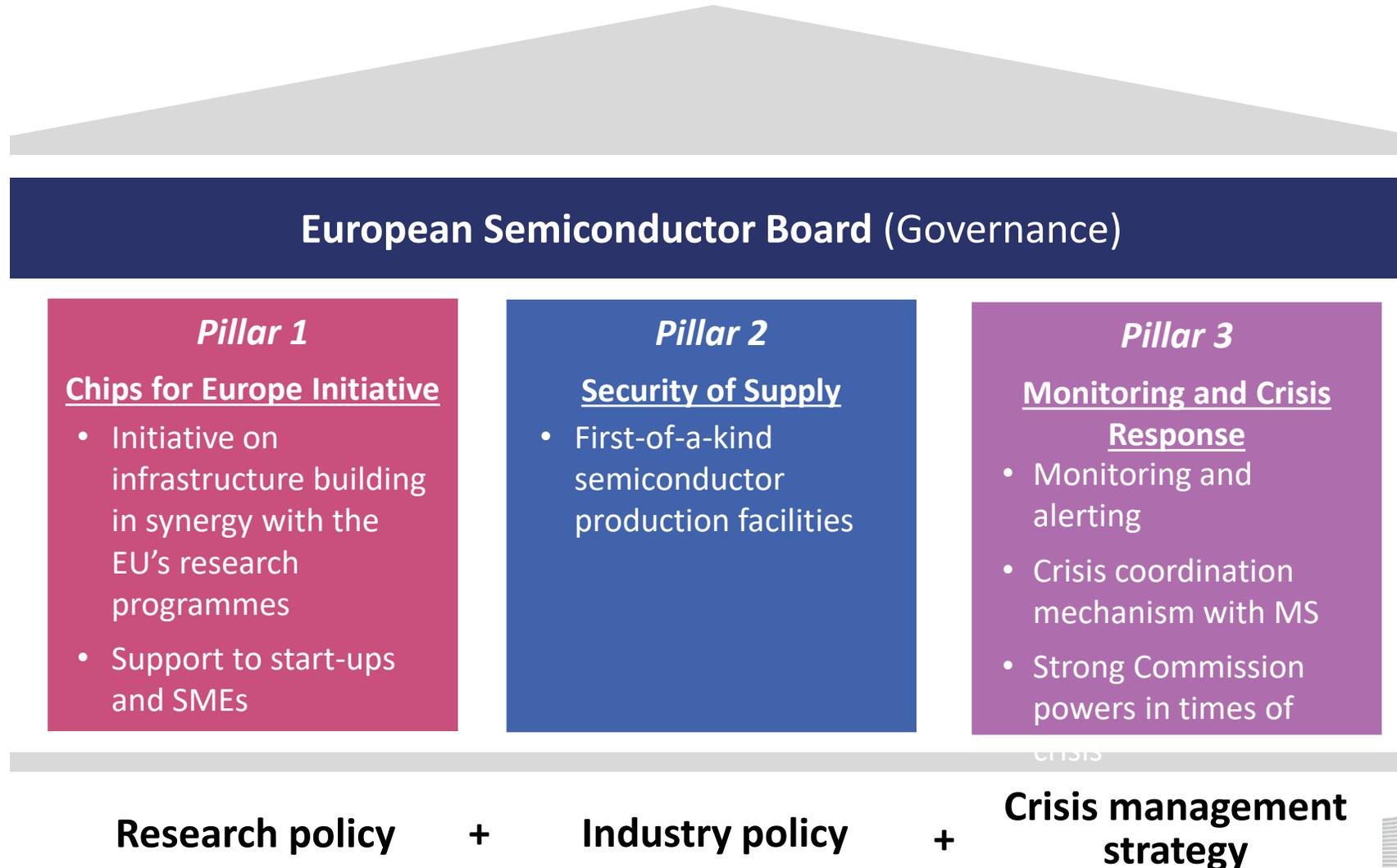
# EU-Singapore Joint Researchers Workshop on Semiconductor

**Pierre Chastanet**

**Head of Unit, Microelectronics & Photonics**

*DG CNECT – Communications Networks, Content and Technology,  
European Commission*

# State of play of the European Chips Act



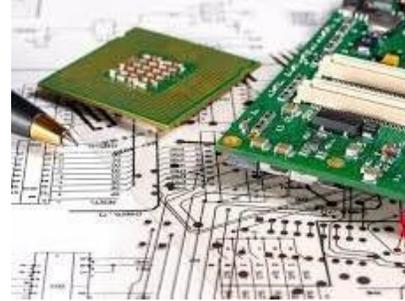
# Pillar I – Chips for Europe Initiative

## Infrastructures open to a wide range of EU users

**5 launched**

### Pilot lines

Prototyping of validated designs  
Testing of equipment  
Validation of process flows



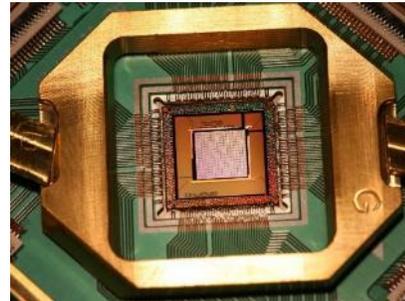
### Design Platform

Help designing semiconductor devices, via access to Electronic Design Automation tools and IP libraries

**Operational  
summer  
2026**

### Competence centres

Access to technical expertise, helping companies to approach and improve design capabilities and developing skills



### Quantum chips

Technology and engineering capacities for accelerating innovative development of quantum chips

**6 quantum  
chips pilots  
selected**

**27+ launched**

Basic  
Research

Applied  
Research

Prototyping

Pilot lines

Production

# Pillar II – Security of supply and resilience

## State aid for production facilities



**First-of-a-kind facility (FOAK):** offers innovation in terms of products or process (e.g. environmental performance) not yet present in the Union

All stages of semiconductor production are eligible



**Planned** investments by major manufacturers exceeding **EUR 80 Billion**

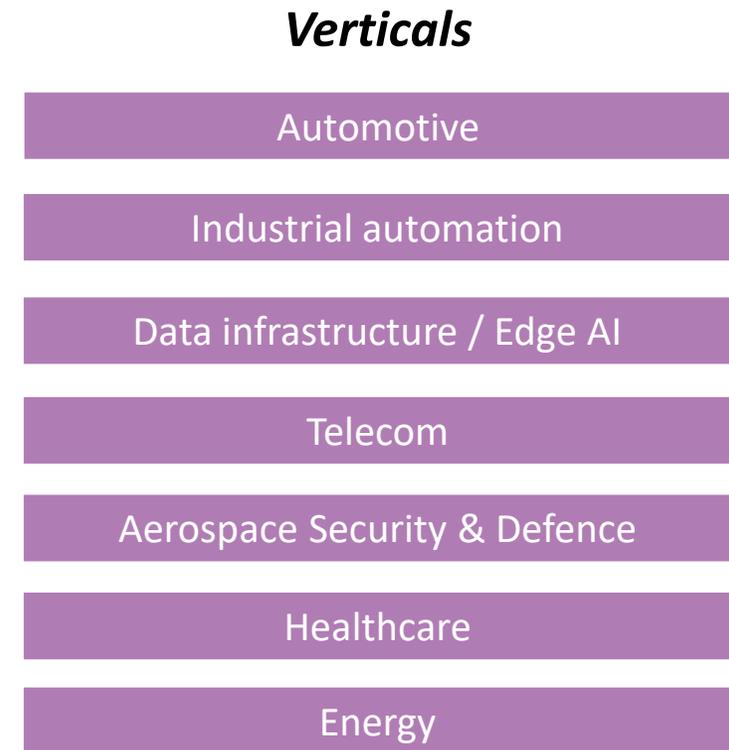
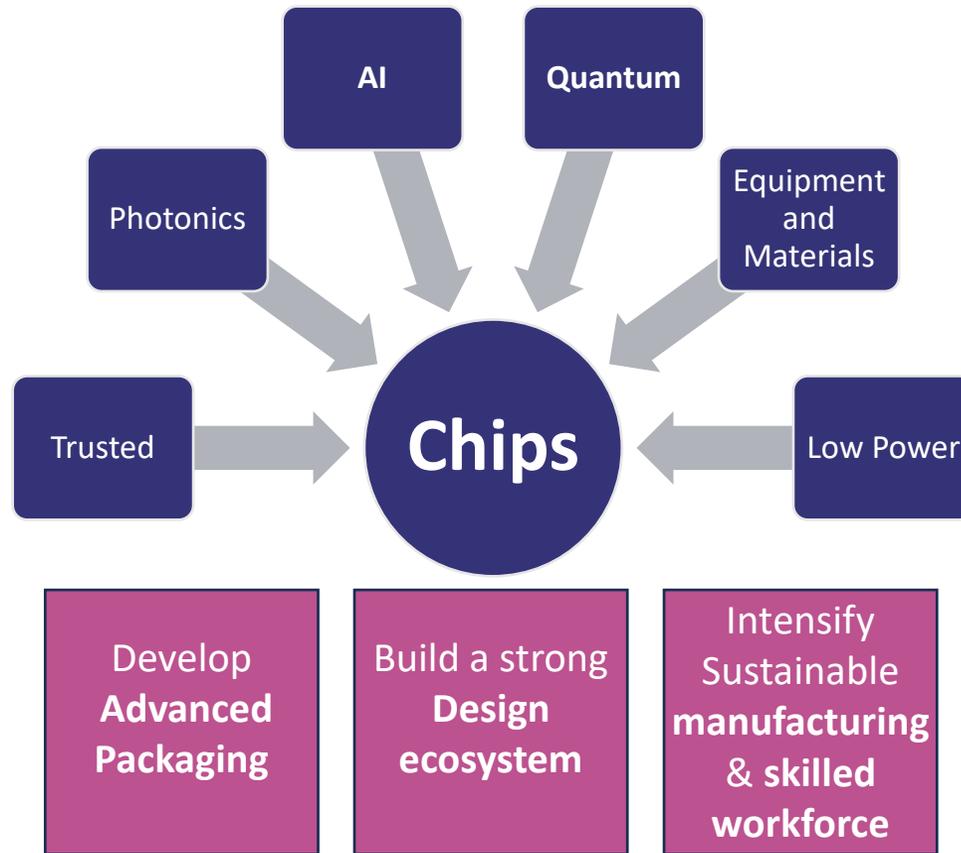
The Commission **approved** state aid for the following projects so far:

	Company	MS	Location	Investment (EUR Billion)	Technology
	ST Microelectronics	IT	Catania	0.73	SiC wafer
	ST Micro & GlobalFoundries	FR	Crolles	7.5	300-mm FD-SOI
	ST Microelectronics	IT	Catania	5	SiC devices
	ESMC (J.V. TSMC + Bosch/Infineon/NXP)	DE	Dresden	>10	CMOS, FinFET
	Silicon Box	IT	Novara	3.2	Advanced packaging
	Infineon	DE	Dresden	4.46	Discrete, analog/mixed signals
	ams Osram	AT	Premstätten	0.567	CMOS
				<b>EUR 31.5 Bn</b>	



More projects in the pipeline,  
Further, IPCEI ME-CT started in 2023 with over **EUR 21 Billion** investments

# Possible Future Priorities



- Need to address strategic priorities, critical dependencies, and industry verticals
- Strengthen our competencies on **essential chips** and develop novel capacities on **cutting-edge chips**
- Attracting **investments**

# EU-Singapore cooperation

DG CNECT contributed to the **SEMICON Southeast Asia 2025**, the region's premier semiconductor industry event taking place this year in Singapore, with a vision of "Stronger Together" and an attendance of over 20,000 participants from the SEA region and worldwide

## On R&I

Leveraging the EU-Singapore Digital Partnership, both parties can deepen collaboration in research and development, focusing on chip technologies on mature node size platforms such as photonics, sensing and packaging including for emerging applications in AI and quantum computing.

## On investments

Both ecosystems benefit from mutual investments, enhancing overall supply chain resilience.

Examples: Soitec, Silicon Box, NXP, ST, Infineon

