Institute of Microelectronics
A*STAR IME

Advanced packaging and heterogeneous integration via fan-out, 2.5D interposer and 3D stacking

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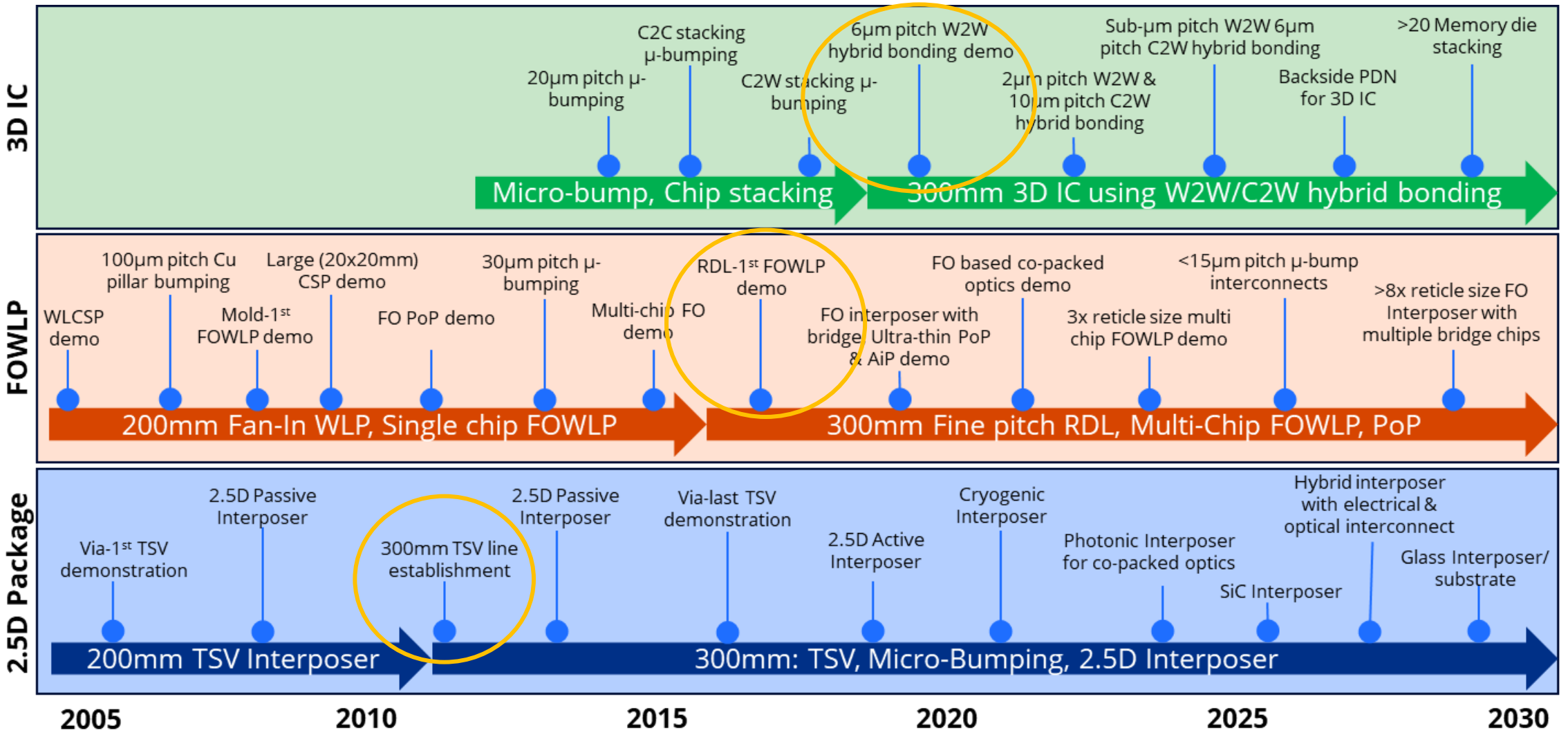
Our Advanced Packaging Journey



- Driving the interconnect roadmap over the years through more than 50 consortia projects with >100 companies across the value chain.

Our Methodologies to Accelerate R&D in Heterogenous Integration

1 Accelerated equipment innovations with Industry Joint Labs within full fledged adv pkg line

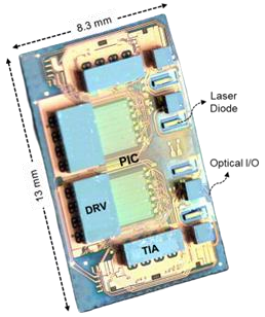
4 Prototyping and SVP access to Start-ups, fabless, consortium members to speed up product development

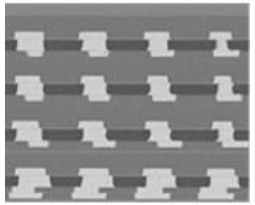
Litho | Etch | CVD | PVD | Copper Plating | CMP | ALD | Wet Clean | Plasma Activation | Bonding/ Stacking | Reflow/ Anneal | Dicing | Adv. Assy | Metrology & Testing | Reliability | Prototyping/ Small-vol

3D HI Approaches

FOWLP
2.5D
3DIC
C2W
W2W
•
•
•

Access to beta equipment from OEM partners





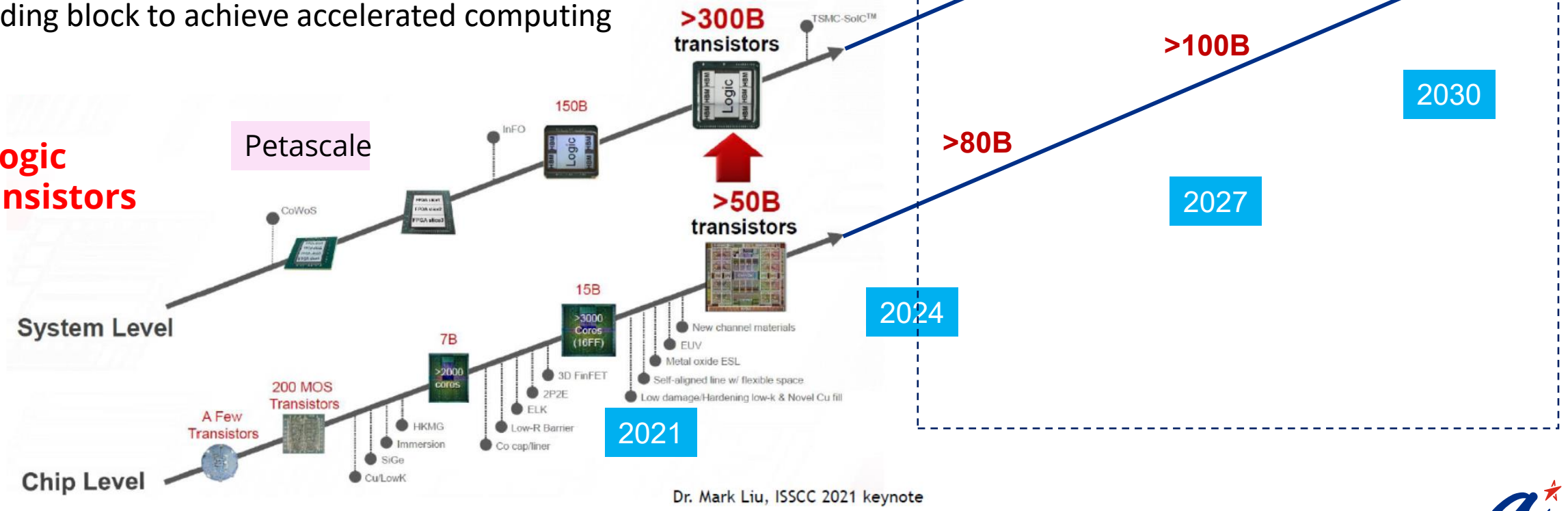
ETM Models, PDK, DTCO, STCO | Plating Chemicals | CMP Slurries | Inorganic Dielectrics | Photo Dielectrics | Underfill | Overmold | TIM

2 Accurate package design enablement

3 Advanced materials evaluation and optimization for next-gen packages

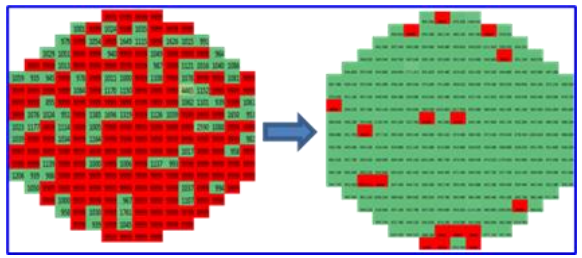
Compute Performance Drives Package System Scaling

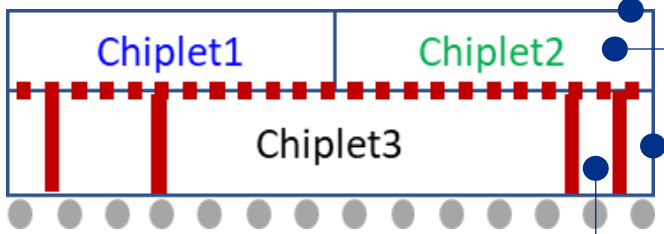
- Generative AI demands increasing compute system performance (2X every year) to reach Zetta Scale Computing
- Exascale to Zetta-Scale Compute performance drives Package integration to reach >1T transistors in Advanced Package
- Ultra Large Multi-chiplet System in Package the key building block to achieve accelerated computing



Interconnect scaling for 3D packaging using Hybrid Bonding

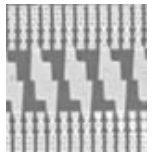
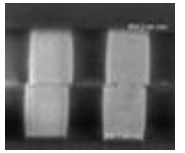
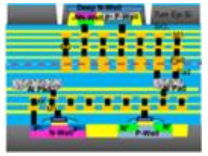
Challenges
- Yield for hybrid bonding
- Access to 3D HI technology for product path-finding





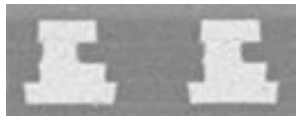
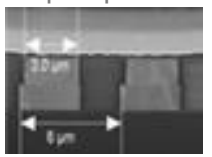
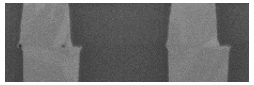
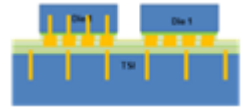
W2W HB

2.5µm pitch → 1.5µm pitch → **0.4µm pitch (today)** → 0.25µm pitch (2026)

C2W HB

10µm pitch → 6µm pitch → **2.5µm pitch (today)** → ≤2µm pitch (2026)

TSV

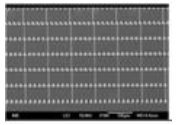
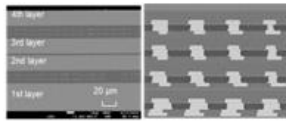
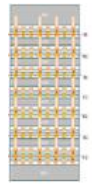
10X100µm → 5X50µm → 2X40µm → **1X15µm (today)** → 1X20µm (2025)



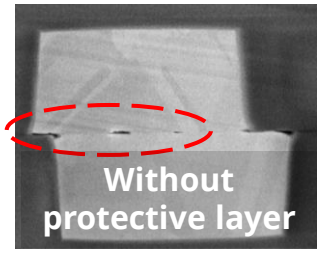


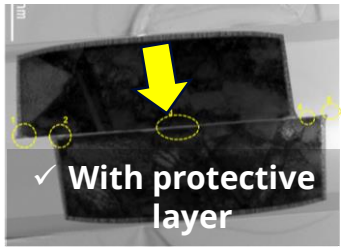
Stacking

C2W µBump TCB: 16 die stacking → **W2W/C2W HB: 4 die stacking (today)** → W2W/C2W HB: ≥12 die stacking (2026)

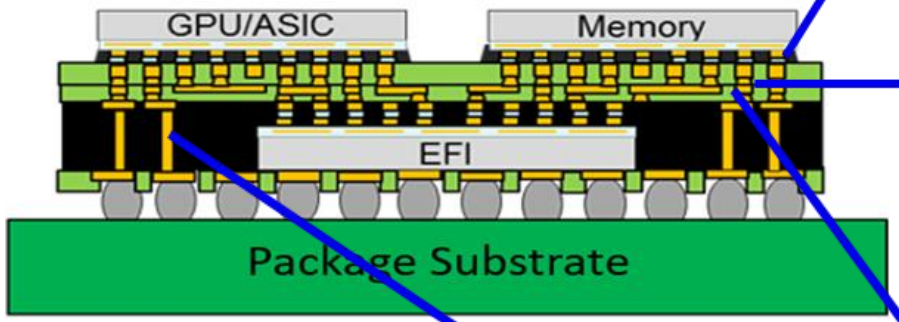




Novel protective layer to significantly improve bond yield & quality for fine pitch hybrid bonds

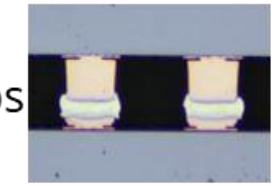


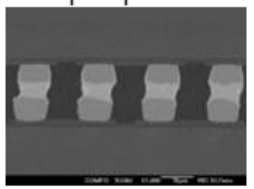


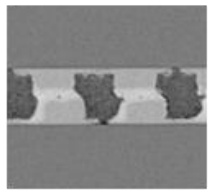
Interconnect Scaling for High Density Fan-Out Interposer

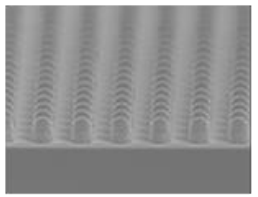


μ-bumps

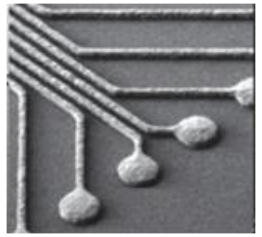

30μm pitch

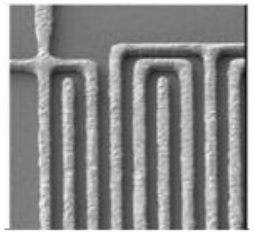

20μm pitch

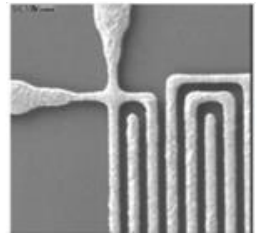

15μm pitch (Today)

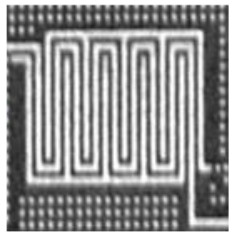

8μm pitch (2025)

RDL L/S

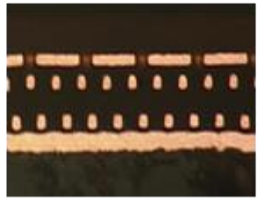

2μm L/S

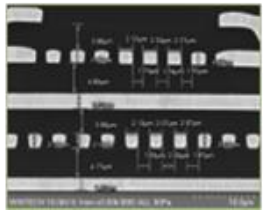

1μm L/S (Today)

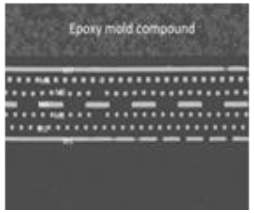

0.8μm L/S (Today)


0.4μm L/S

# of RDLs


4 Layers

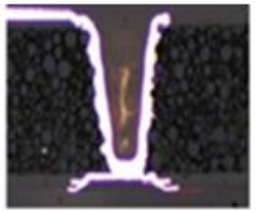

5 Layers

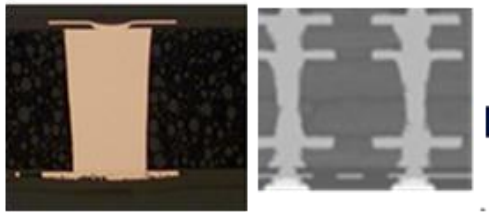


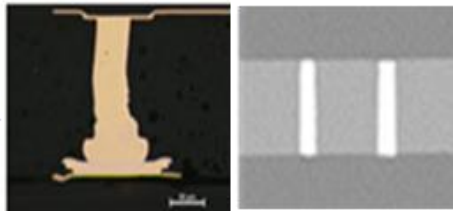
7 Layers (Today)

10 Layers (2026)

TMIs

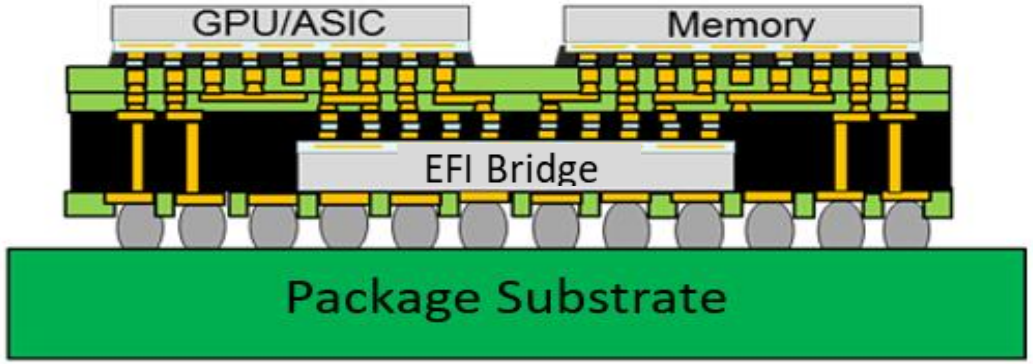

≥300μm pitch


200-250μm pitch


≤100μm pitch (Today)

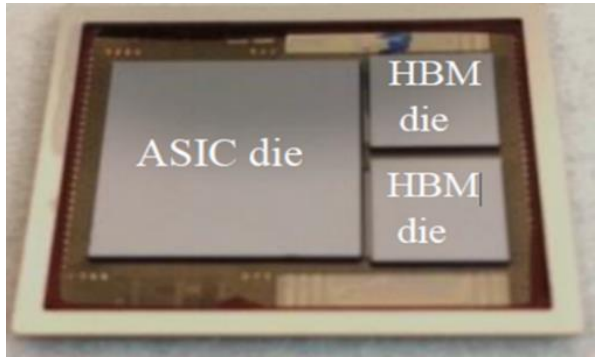
Embedded Fine-pitch Interconnect (EFI) Bridge 2.5D Interposer

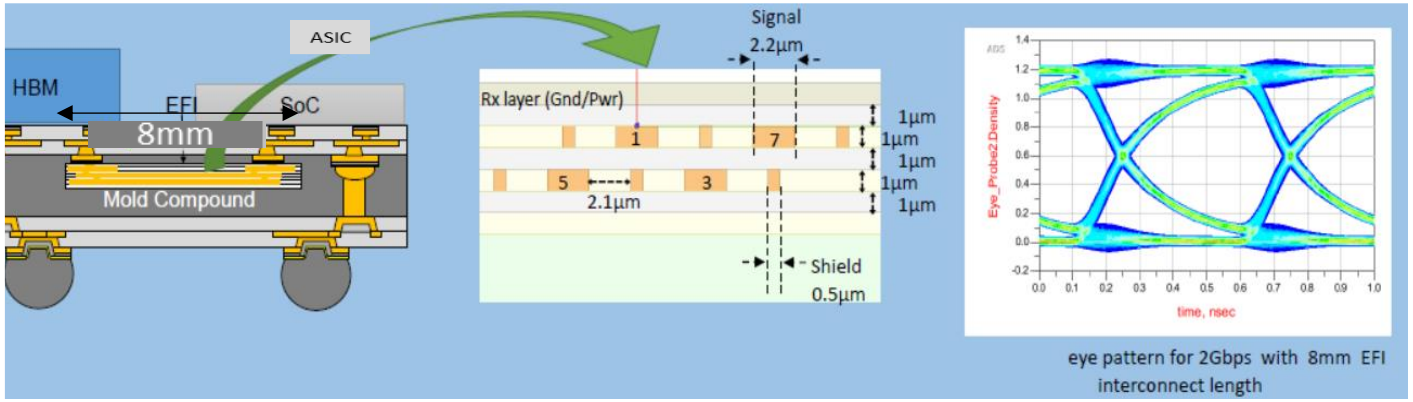
- Silicon interposers have been a go-to but expensive option for 2.5D integration.
- We developed cost-effective wafer level bridge interposer package in 2018.



- Embedded Fine-pitch Interconnect (EFI) Bridge Interposer Features
  - EFI bridge for dense short fine-pitch interconnections (pitch=1μm).
  - RDL for long coarse interconnects.
  - Can be scaled up to >6X reticle size >5000mm2 interposer size and beyond.

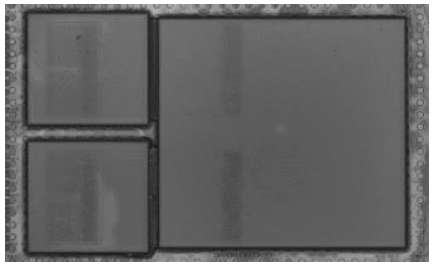
EFI Bridge Interposer Performance and Reliability



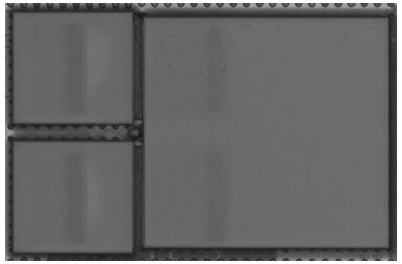


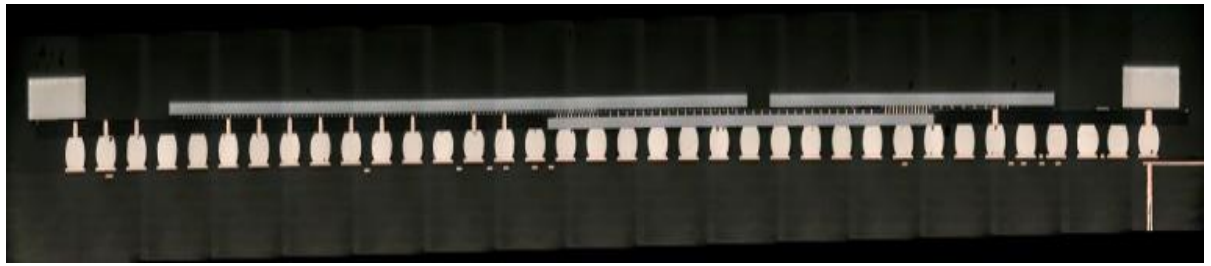
eye pattern for 2Gbps with 8mm EFI interconnect length

CSAM after MSL3 test

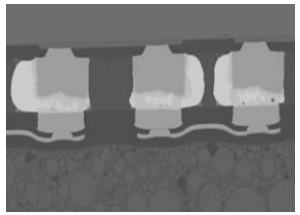


CSAM after TCoB test





		TCOB testing (Board level)			
Group	Wafer info	250 cyc	500 cyc	750cyc	1000cyc
1	Material A	0 / 7	0/ 7	0/6	0/6
2	Material B	0 / 5	0 / 5	0/4	0/4



Cross-section verification after TCOB testing

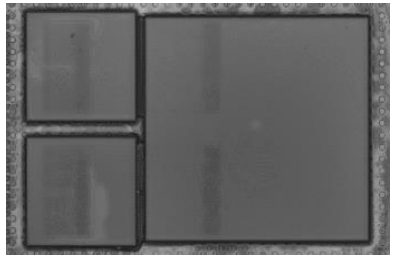
EFI bridge interposer is a scalable platform for large 2.5D Interposers for Ultra Large HPC/AI systems (>5X reticle size).

From Components to Systems for AI Hardware

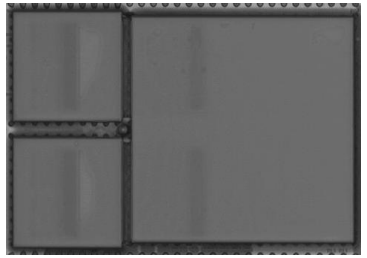
Challenge
- Access to 1-stop shop to integrate heterogeneous components for energy efficient adv packages

3D Integrated Chiplets (3D-IC) by Chip-to-Wafer and Wafer-to-Wafer Hybrid Bonding

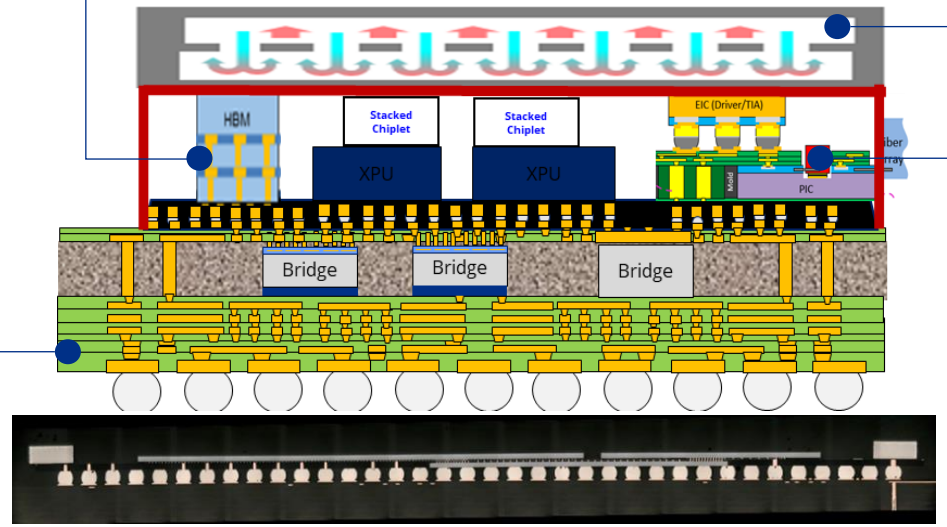
CSAM after MSL3 test



CSAM after TCoB test

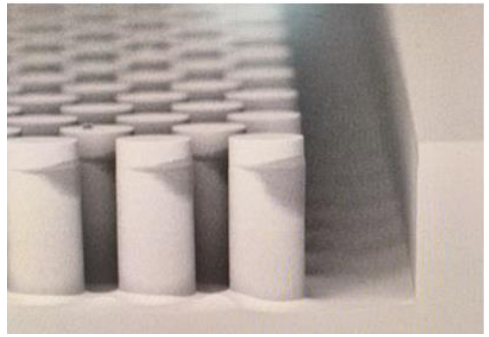


Reliability



Large 2.5D Re-constituted Interposer (can scale > 5X reticle size)

Thermal Solutions >2kW



Silicon Micro Cooler

ECTC'25 session 12.1

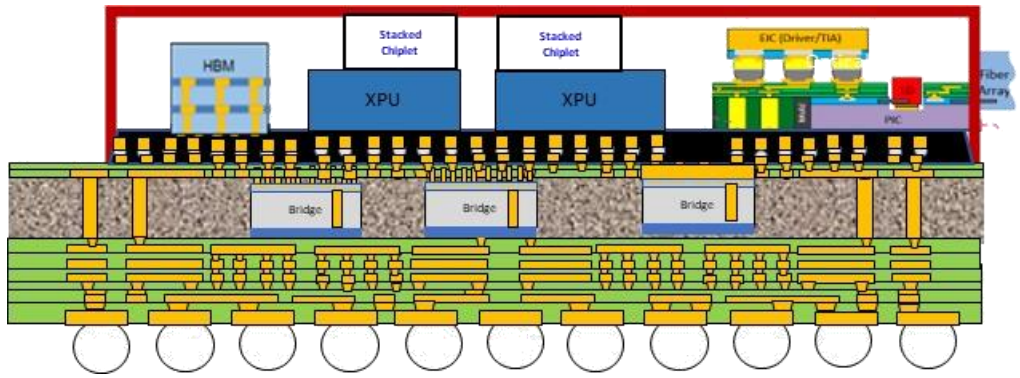
Co-Packaged Optical Engines (6.4Tbps and beyond)

Solution: Full-fledged Advanced Packaging line at IME to bridge gaps in integration of heterogeneous components into energy efficient systems

Development through consortiums: 2.5D/3D Chiplets-HI Consortia

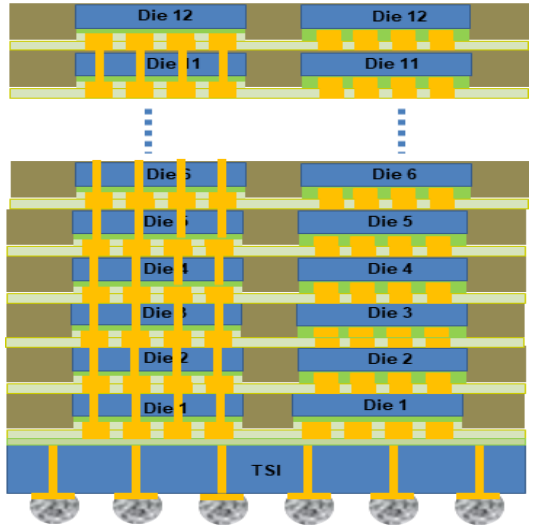
- Pre-competitively address industry needs
- More than 20 member companies across supply chain – Fabless, IDM, foundries, OSAT, materials and equipment.

HPC and CPO Chiplets Integration Consortium



Heterogenous Integrated Chiplet package

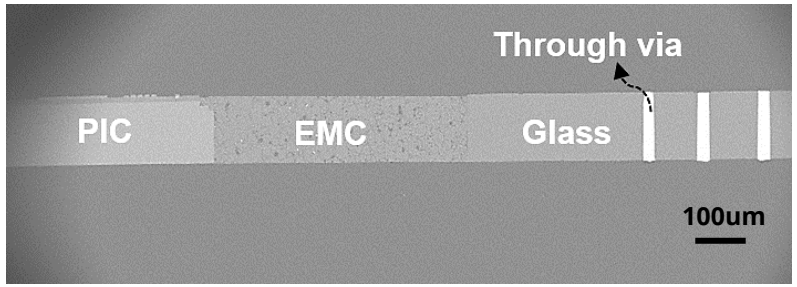
Chip-to-wafer Hybrid Bonding Consortium For 3D Stacking

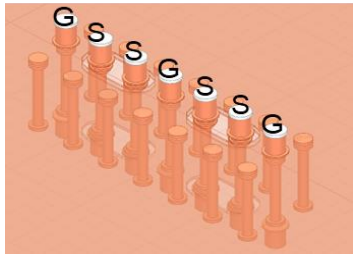


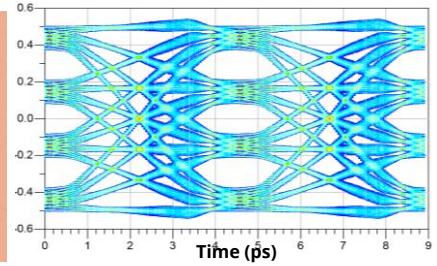
C2W HB memory chip stacked modules

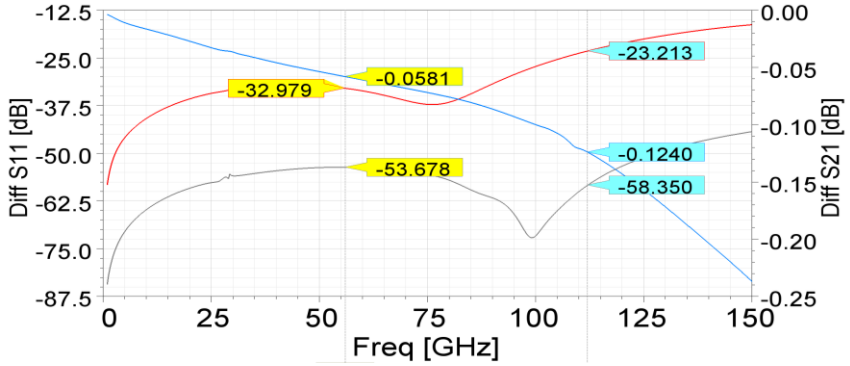
Next-Generation Interconnects for Optical Engines

400 Gbps OE interconnects



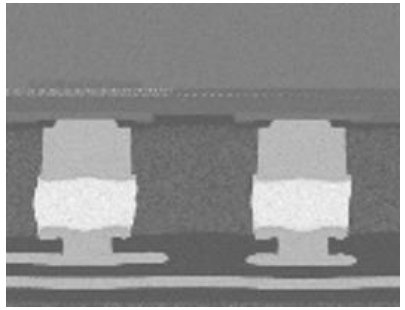




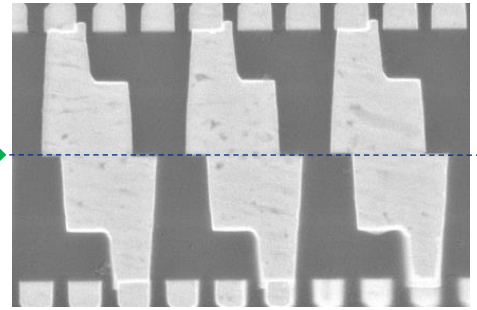


- High density TGV
- Good dielectric properties, improved mechanical strength for the package.

Hybrid Bonded OE

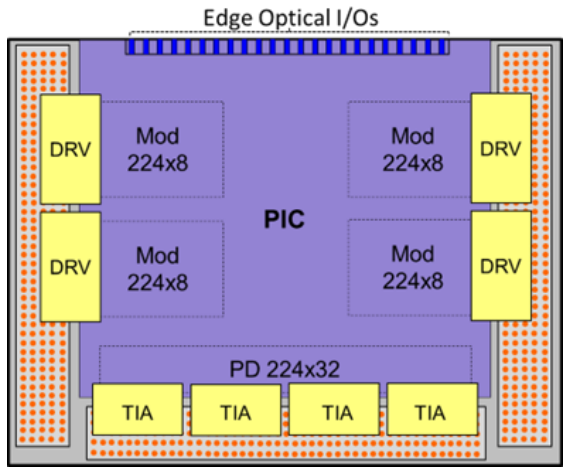


IL @ 112GHz= -0.4dB

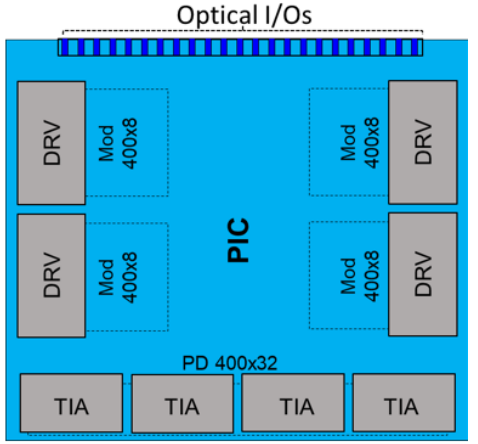


IL @ 112GHz= -0.003dB

- High density interconnects between EIC- PIC - Interposer
- Reduced EIC-PIC interconnect parasitics
- Very-low insertion loss at high frequency - Support higher bandwidth

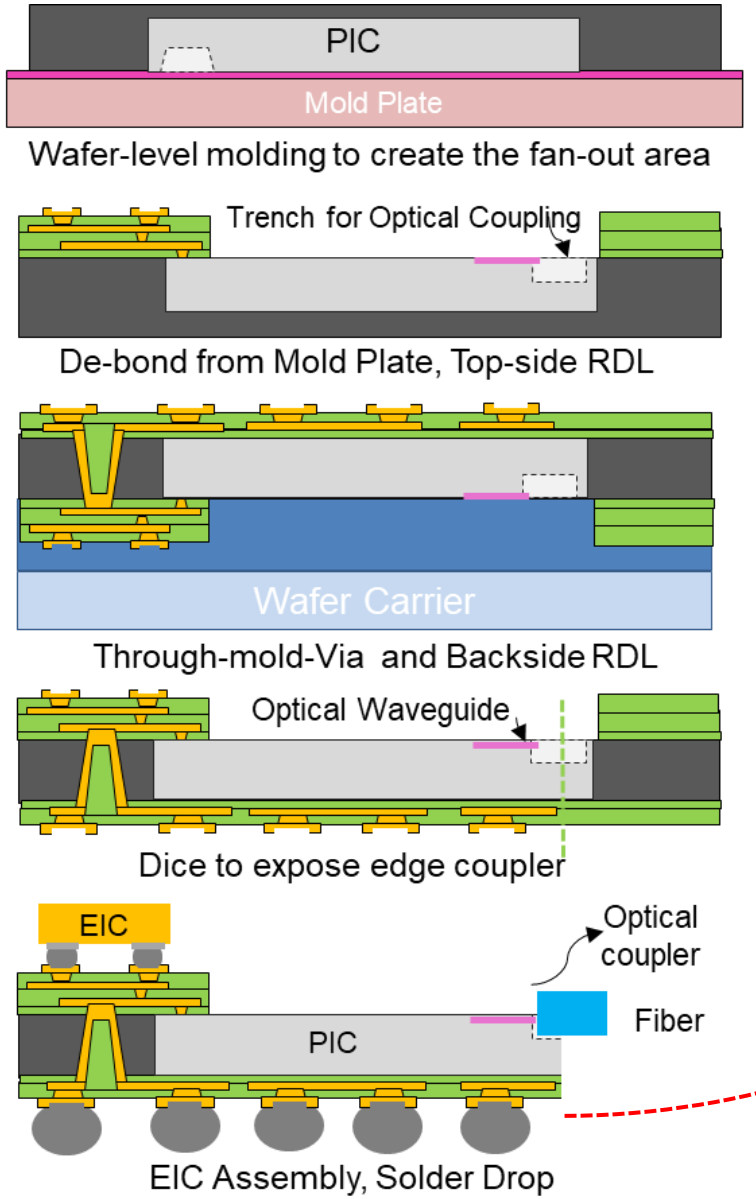


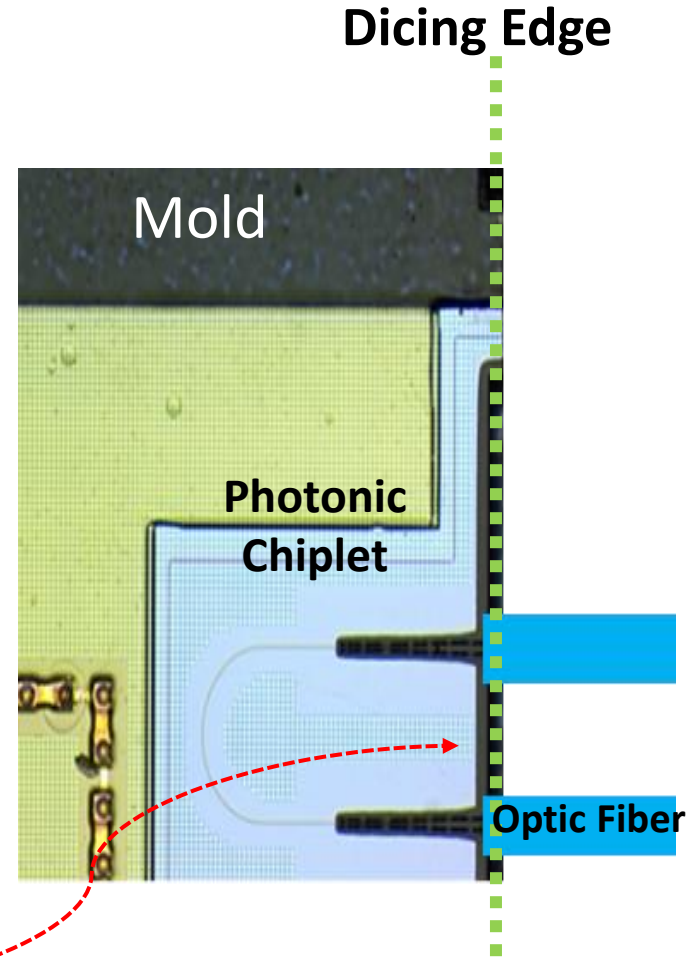
6.4Tbps optical engine package design

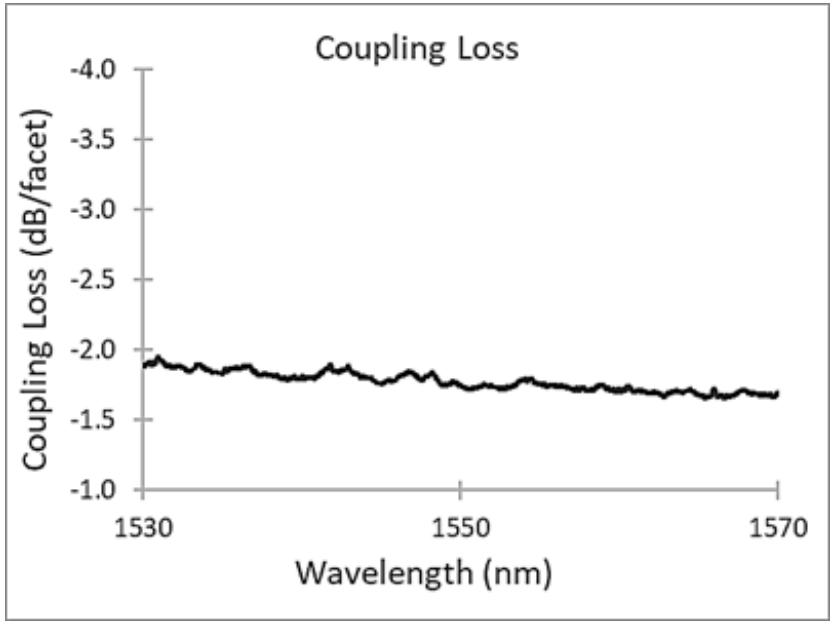


12.8Tbps optical engine package design

Optical Engine Process Flow & Edge Coupler Performance







Fabricated Test Vehicle
Optical Coupling loss from Fibre to Package ~1.7dB

Optical Coupling for 9mmx15mm 1.6T package

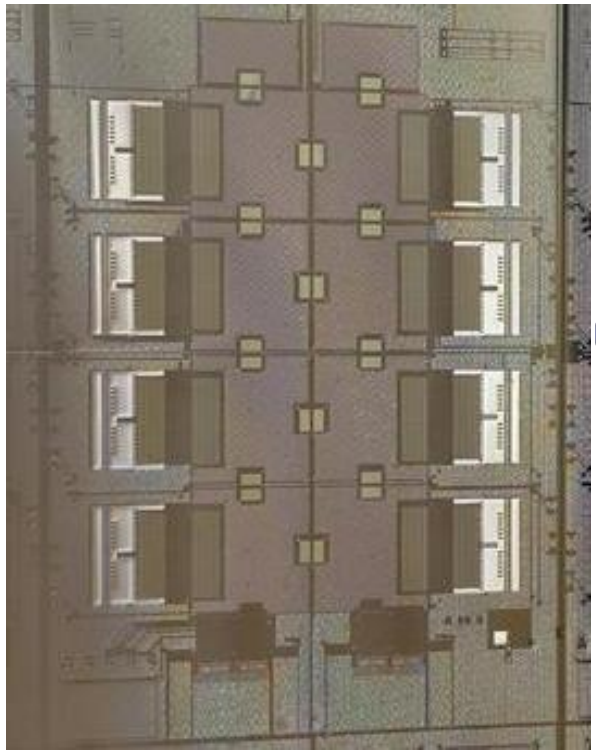
2.5D Interposer Scaling Up for AI and HPC

Past

1X reticle size
3 chiplets

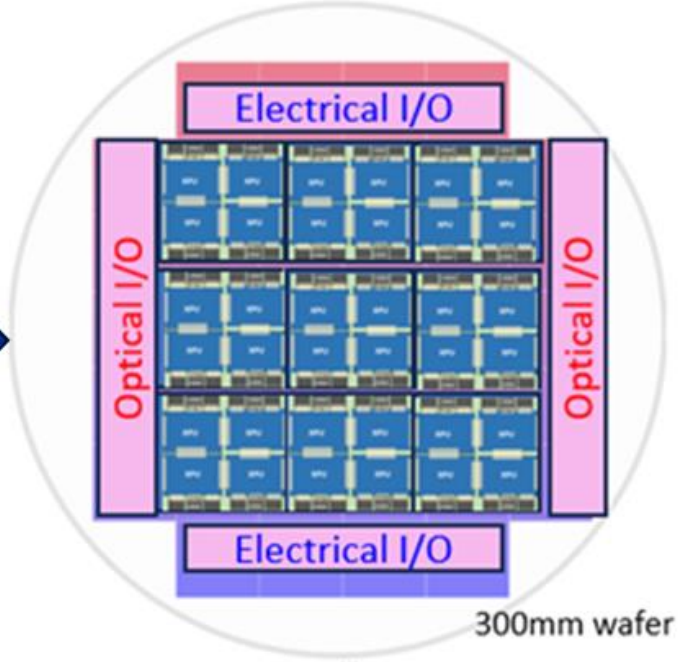
~3X reticle size
12 chiplets

Present



System on 5X Reticle Interposer

Future (2028)



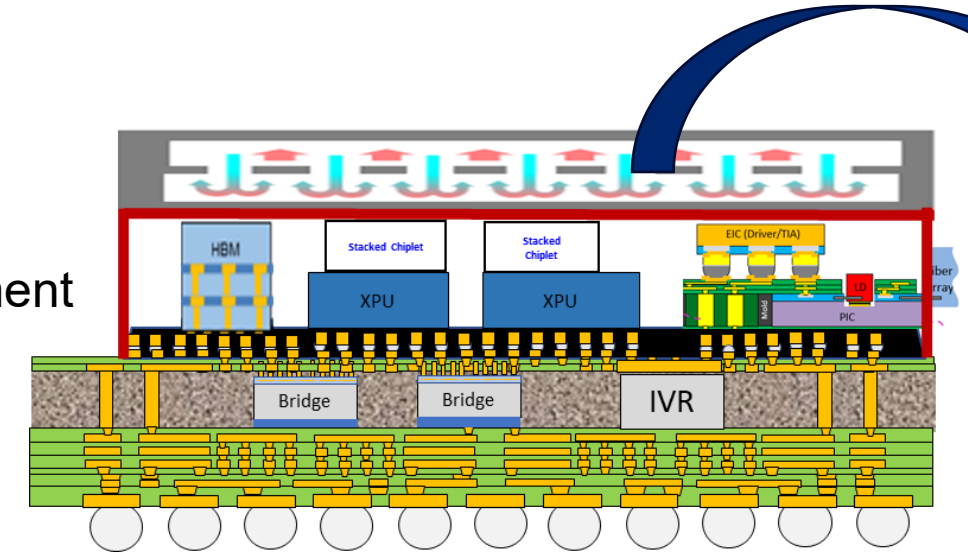
System on 300mm Wafer with
100s of Chiplets

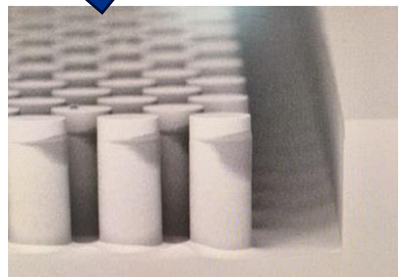
Key Challenge: Wafer Scale Interposer with Electrical and Optical wiring to integrate XPUs, HBMx, IVR, peta-scale optical I/O, Thermal Cooling.

System Thermal solution for Heterogeneous Integration

Thermal Challenges

- High power dissipation requirement
- Limited space for cooling structure arrangement
- Severe in-package temperature gradient



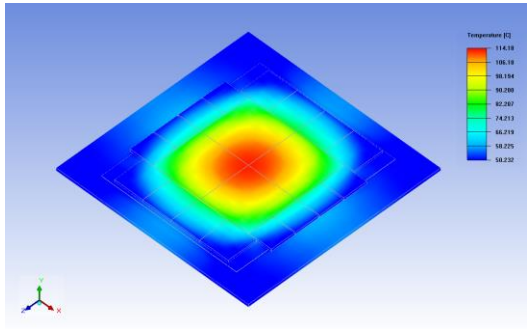


Silicon Micro Cooler

Schematic image of micro-fluid cooling solution for high power dissipation

Approach

- ➢ Thermal performance evaluation and improvement
- ➢ Si Micro cooling technology targeting main heat cores
- ➢ Package integrated cooling for effective heat dissipation
- ➢ IVR integrated within interposer



Package power > 2000W

Tmax_xPU < 110℃

Tmax_HBM < 90℃ Tmax_OE < 80℃

Typical Specs

- ✓ To achieve heating power dissipation **>2000W**
- ✓ To handle thermal issue of large Interposer **>70mm x 70mm**

Summary

- AI-HPC hardware drive Package Level System Scaling enabled by Multi-Chiplet Heterogeneous Integration packaging for Compute, Memory, OE, IVR and Thermal Cooling.

- IME's Advanced packaging line provides ready access to Heterogeneous Integration Technologies to Industry and Academia.

- We cherish deep collaborations across the advanced packaging ecosystem - critical to develop broad, deep new capabilities to address current/next generation AI hardware challenges.
  - ✓ Consortia to address pre-competitive challenges facing Industry
  - ✓ Product prototyping and Tech-transfer.
  - ✓ Working with Academia to accelerate exploration and pathfinding in heterogeneous integration


Agency for
Science, Technology
and Research
SINGAPORE
Looking forward to expanding our ecosystem of partnerships to accelerate innovations in Heterogeneous Integration!
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ASTAR-SG