

# GaN Technology for Power Electronics Applications

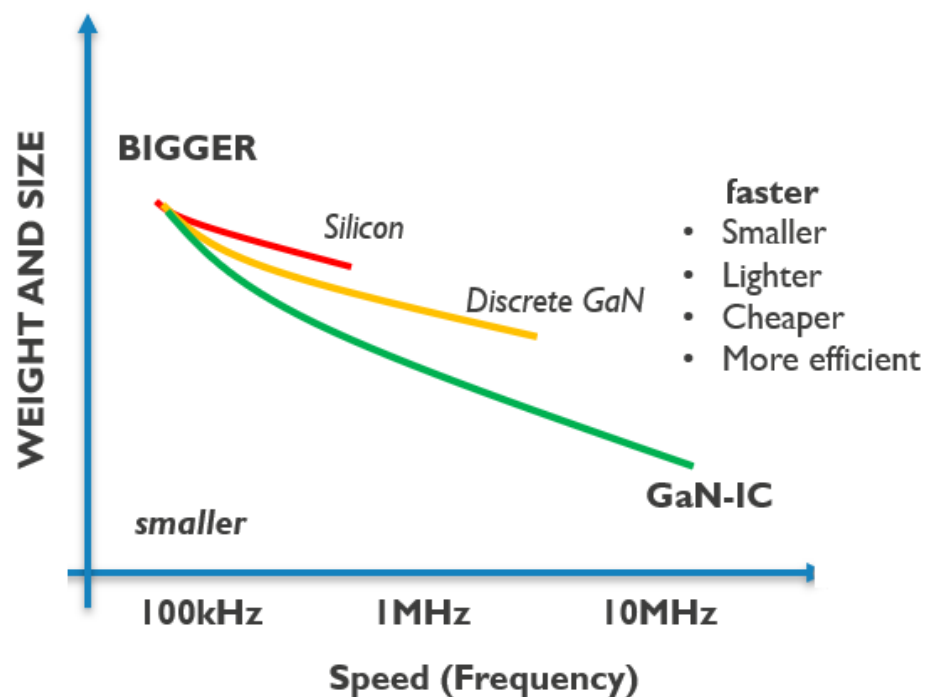
Dr. Urmimala Chatterjee,  
R&D Engineer  
IMEC, Leuven, Belgium



Brussels  
8-9th July, 2025



## GaN Technology: A breakthrough for PE Application



### Higher integration

- Enables higher frequency operation
- Integrate higher power

### More efficient

- Less parasitic reduces gate ringing & switching loss

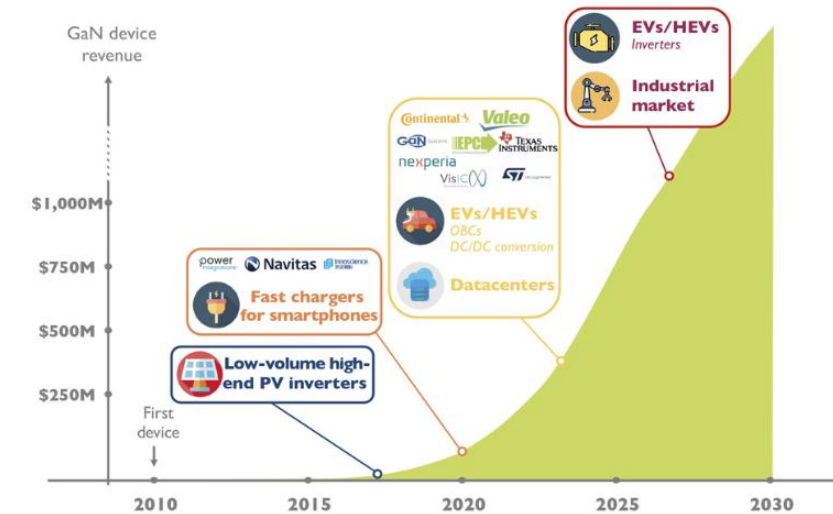
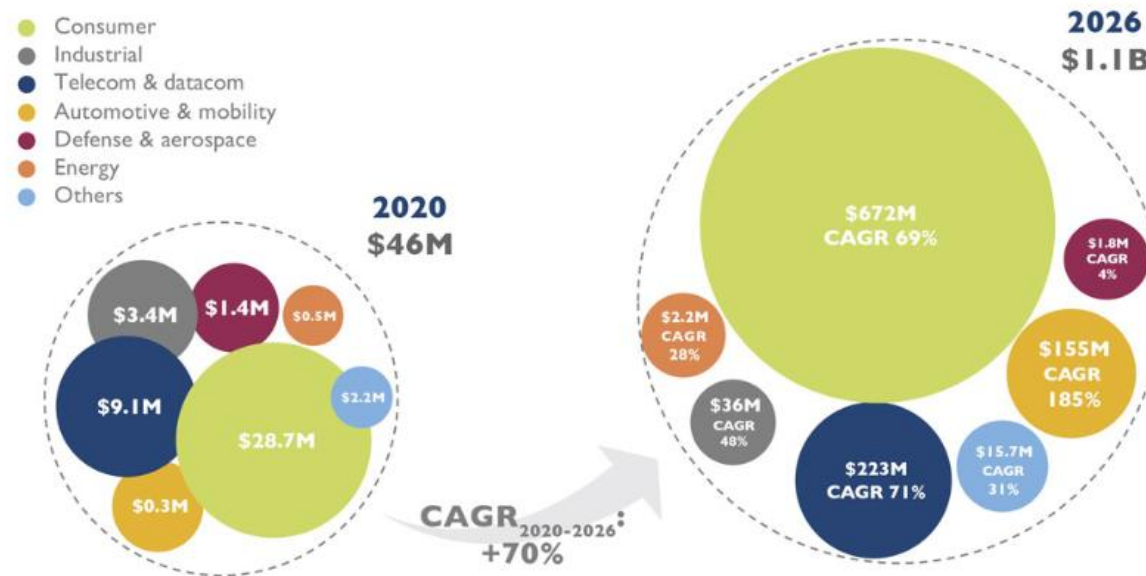
### Compact & cost-effective

- Higher frequency, higher power density
- Further reduction in filter size & cost

### Easy to control

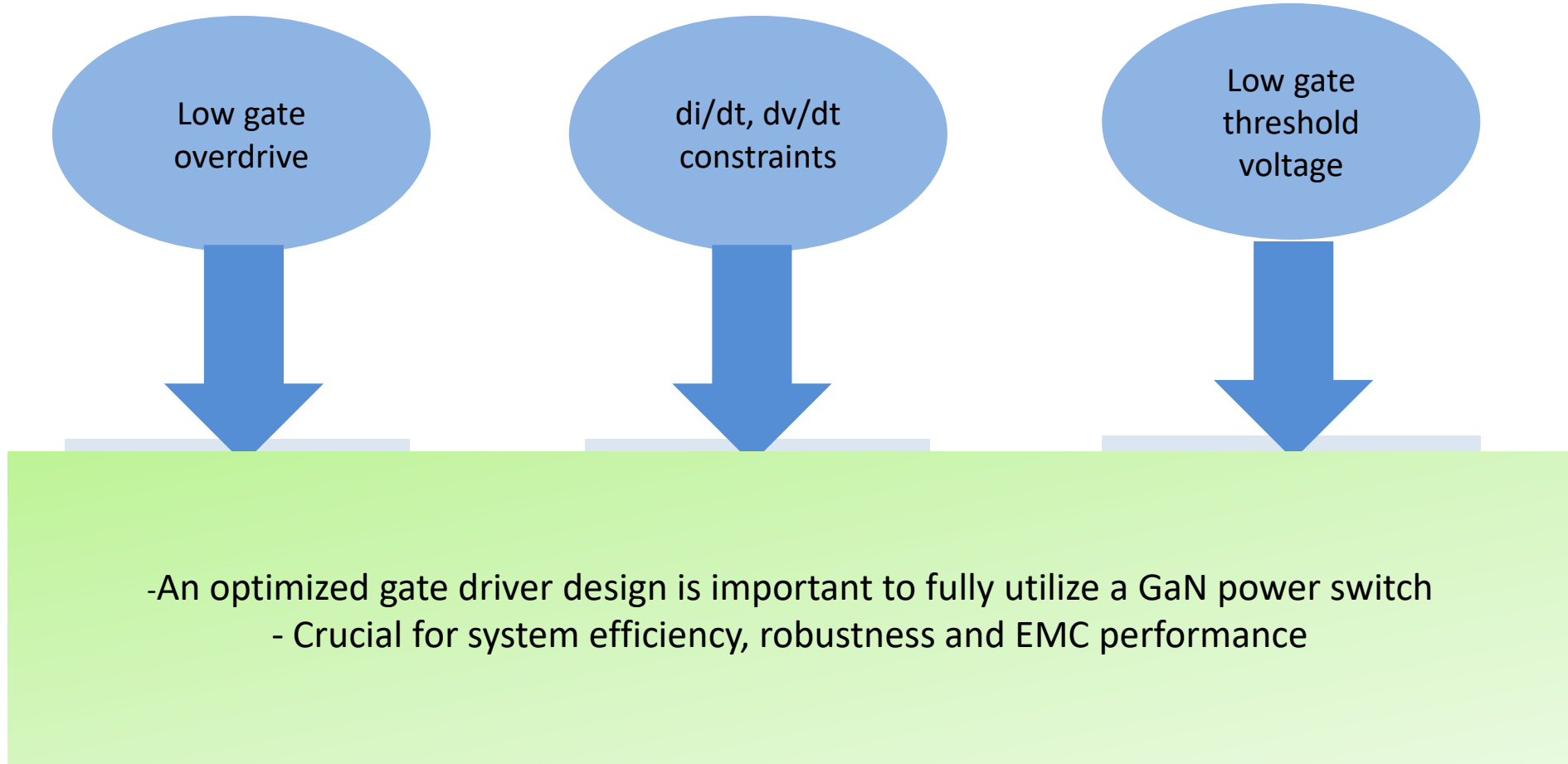
- Reduce gate overshoot undershoot
- Easier control due to reduced ringing

## GaN Market Share



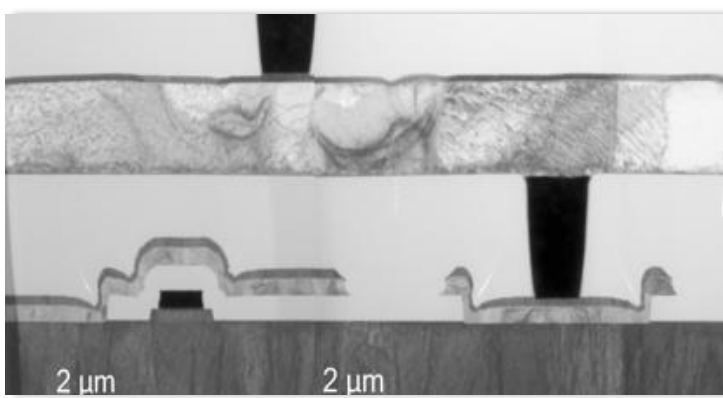
Source:: GaN power 2021, Yole Development, 2021

# Operating a GaN Power Device

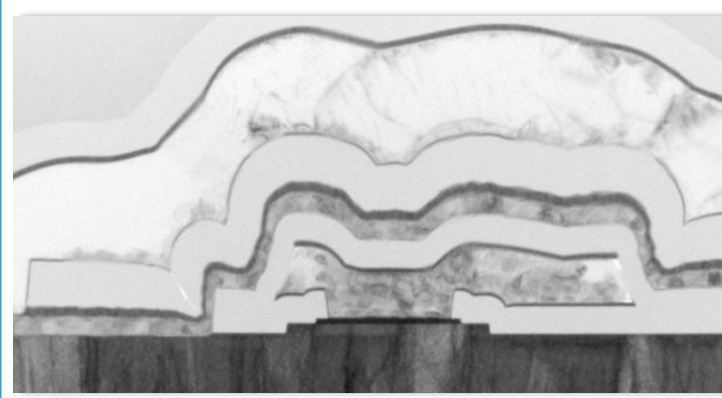




## 40V/100V p-GaN HEMT



## 200V/650V p-GaN HEMT

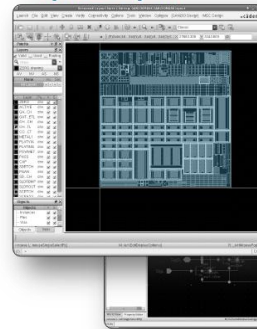


## Monolithic integration (GaN-IC)

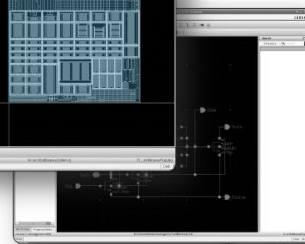


\*J. Thone, PWR SOC 2021

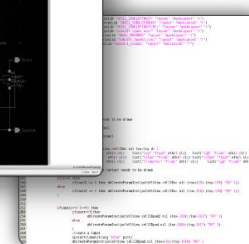
### Physical layout



### Schematic layout

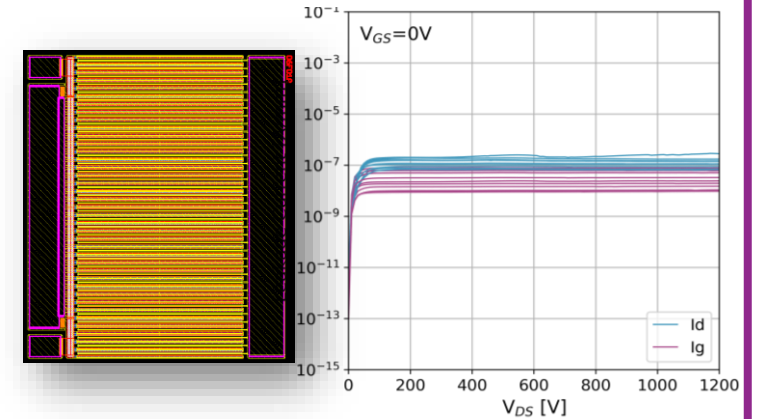


### Skill-code PCells

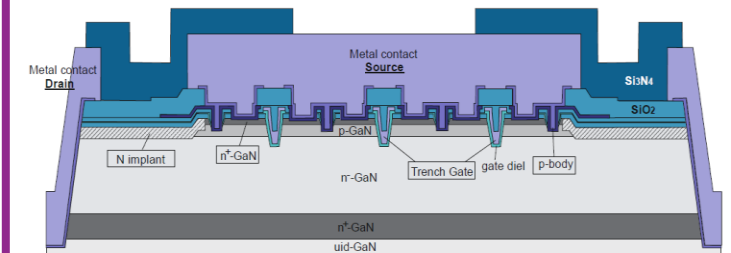


## 1200V GaN under development

### Lateral p-GaN HEMT



### Vertical GaN FET



- Discrete Power Devices & more
- Towards Integration: GAN Power ICs
  - Monolithic integration
  - GANIC demonstrator
  - Extended GANIC platform

# Discrete Power Devices & More

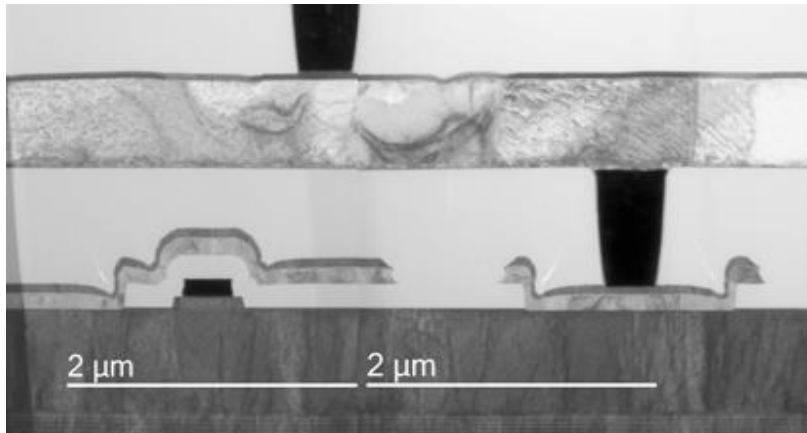


# Discrete Device Development

## Low Voltage Platform 40V/100V

P-GaN gate with Schottky contact  
TiN/W gate  
No gate field plate  
Planarized back-end :

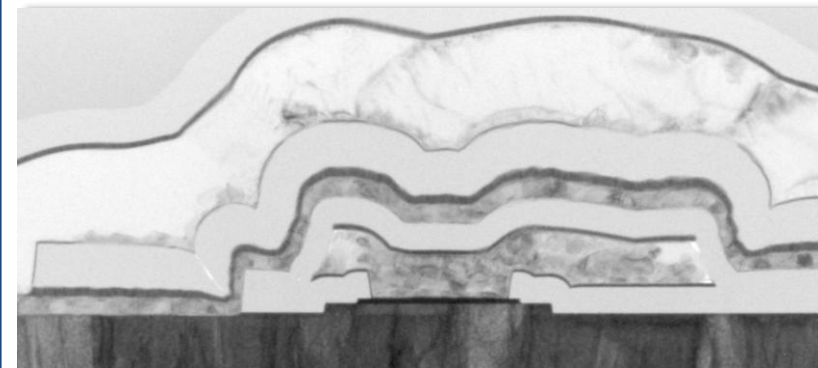
- Oxide CMP
- W-plugs



## High Voltage Platform 200V/650V

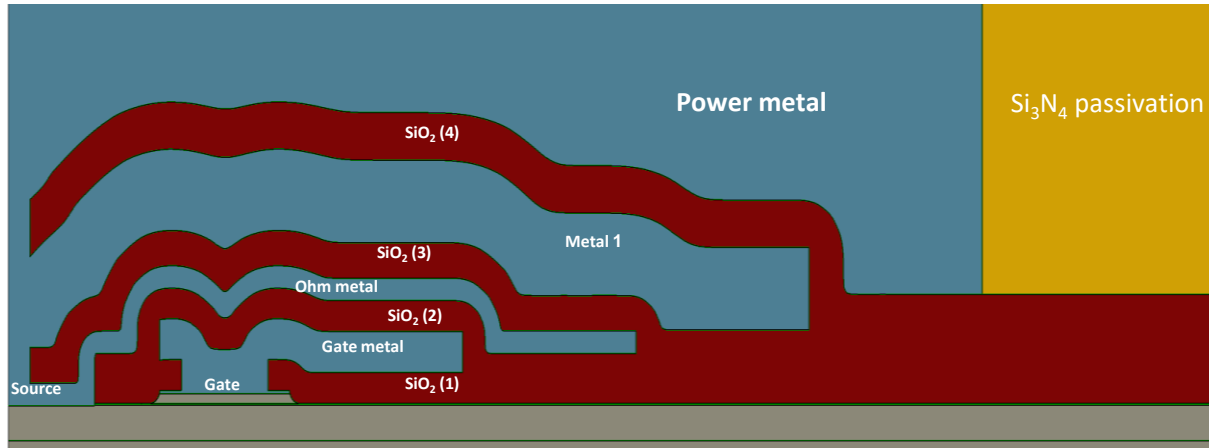
P-GaN gate with Schottky contact  
TiN electrode and Al-base gate metal  
Gate field plate  
Conformal back-end:

- Field plates closer to 2DEG
- Low-cost

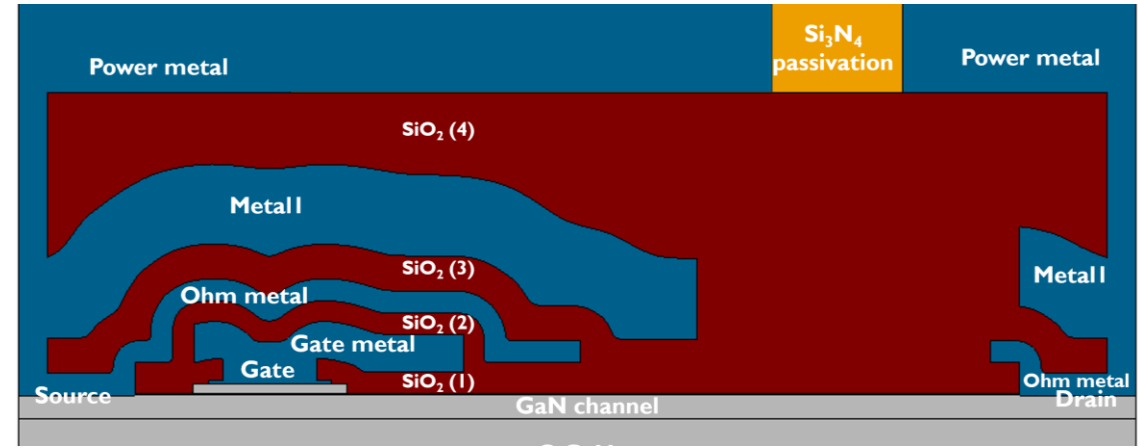


\*N. Posthuma, *et al*,  
An ind-ready..pow  
tech, *ISPSD 2018*,  
doi:  
[10.1109/ISPSD.2018.8393658](https://doi.org/10.1109/ISPSD.2018.8393658)

## Discrete devices on Si

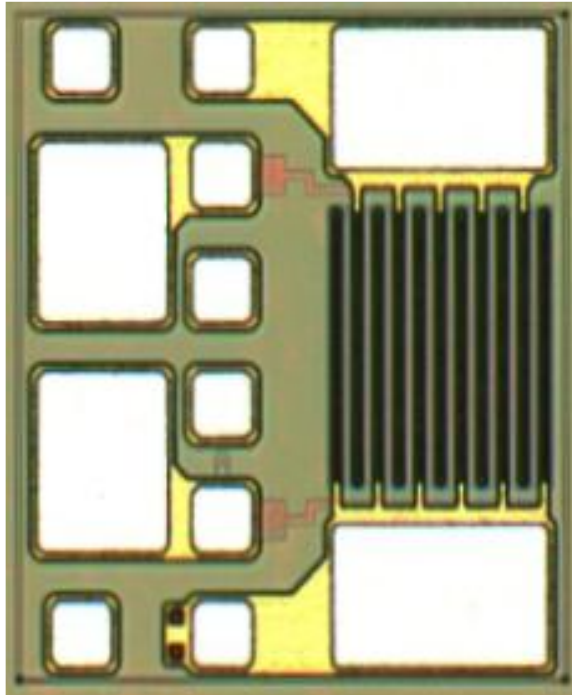


## GaN-IC devices



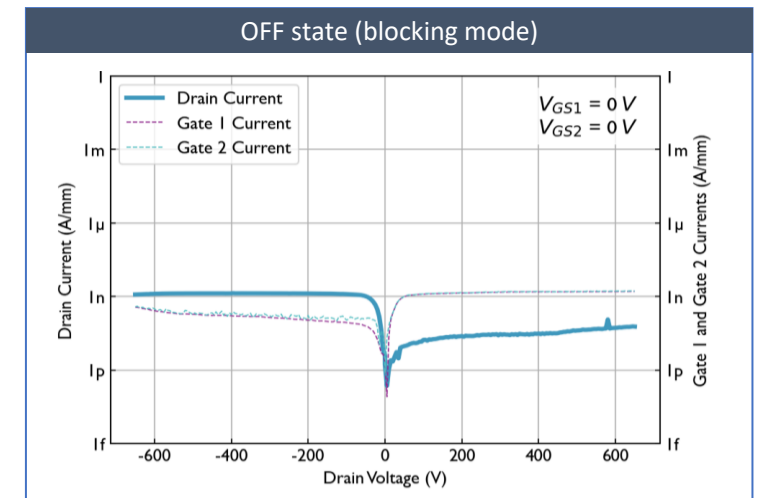
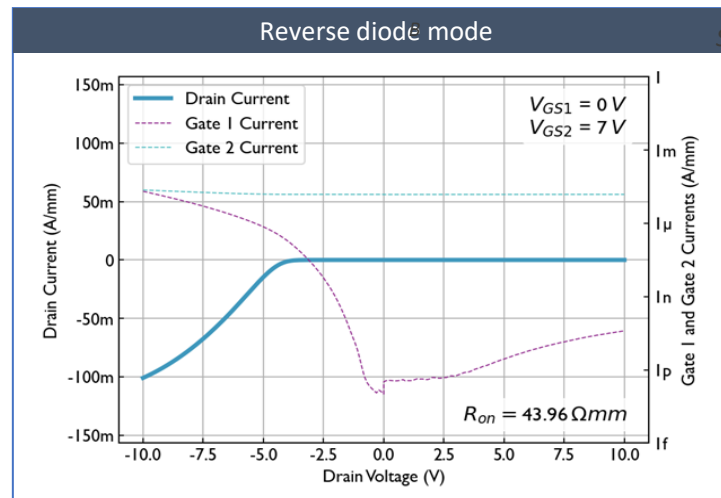
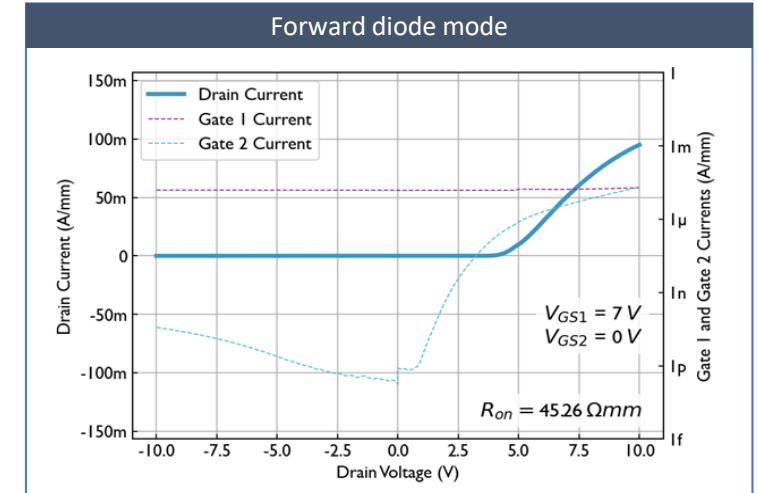
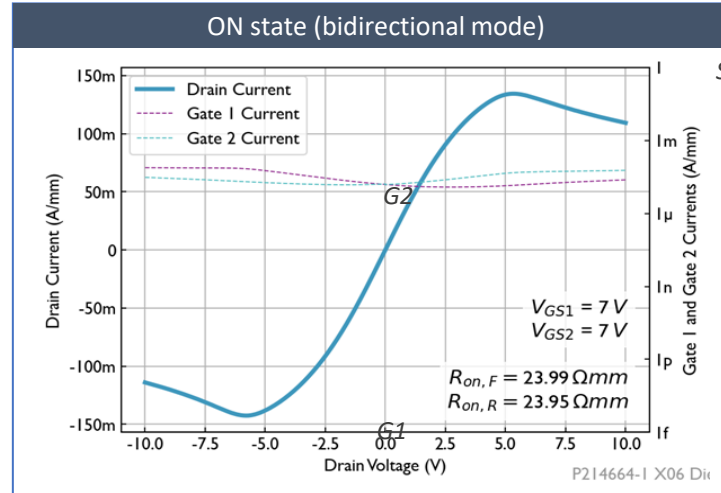
- Basic device architecture is based on a pGaN gate type E-mode HEMT
- Same field plate configurations
- During deep trench isolation, an additional IMD planarization after Metal I is done in GaN-IC platform
  - Difference  $\text{SiO}_2$  thickness between Metal I and Metal 2

# GaN Bidirectional Switch

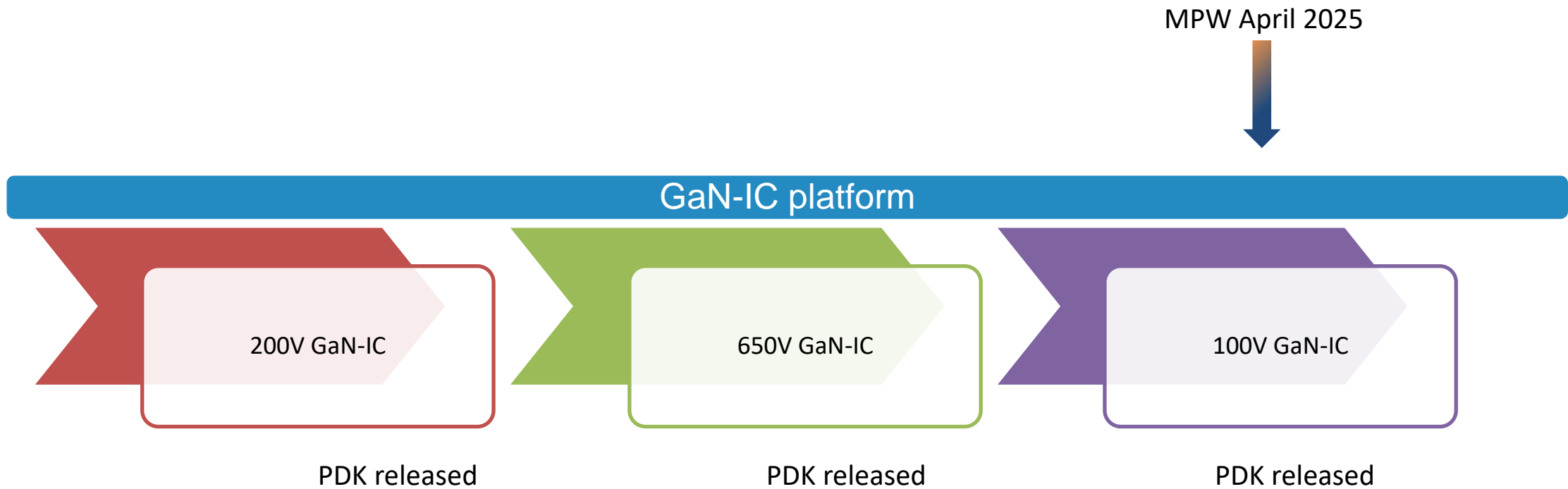


Microscopic image of a dual gate bidirectional switch

\*G. Baratella, U. Chatterjee *et al*,  
“Monolithic 650V dual gate p-GaN  
bidirectional switch” IEEE TED,  
[10.1109/TED.2024.3456077](https://doi.org/10.1109/TED.2024.3456077).

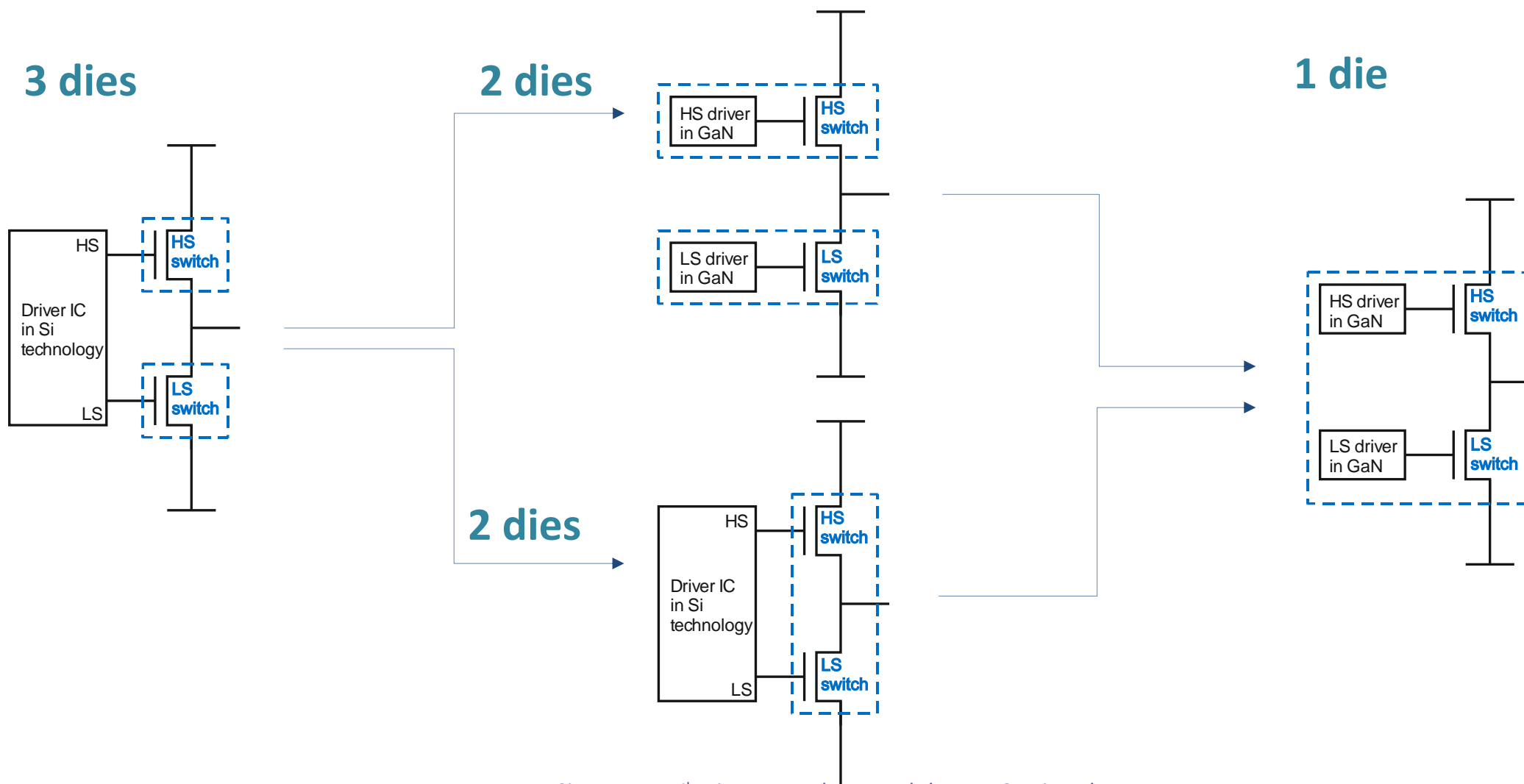


# Towards Integration: GaN Power ICs

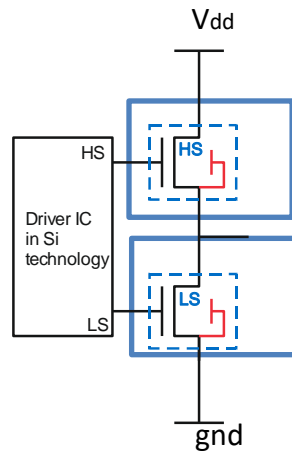




# Discrete components to GaN-ICs

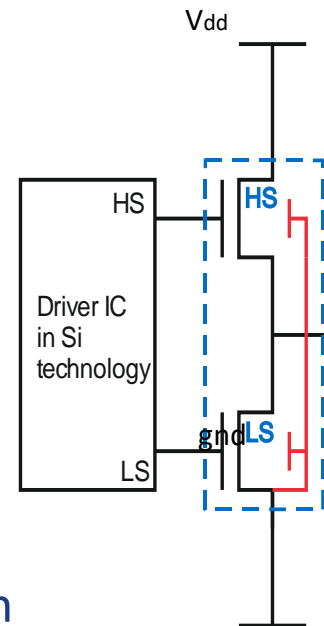


## Technological Challenges



Discrete devices :  $V_{SB} = 0$  Volt

- Back-gating effects
- Low-voltage analog circuits that integrates with device
- Suitable passive components



Example for  $V_{in} = 400$  Volt.  
When HS switch is ON, and  
LS switch is OFF :

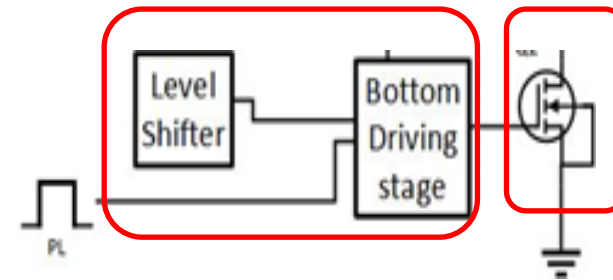
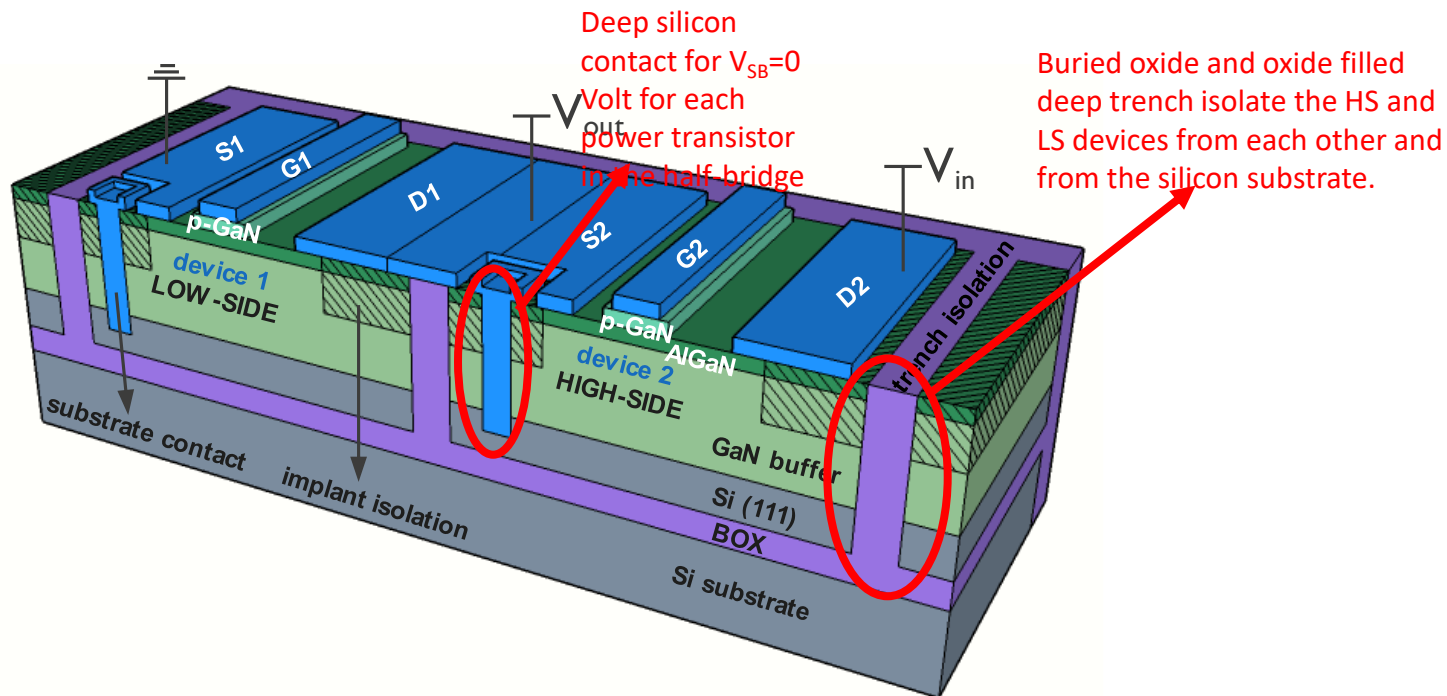
$$V_{S\_LS} = 0 \text{ Volt}$$

$$V_{SB\_LS} = 0 \text{ Volt}$$

$$V_{S\_HS} \sim 399 \text{ Volt}$$

- Current in substrate
- Disconnect substrate from Source\_HS, then  $V_{SB} = 399$  Volt

## SOI substrate for isolation

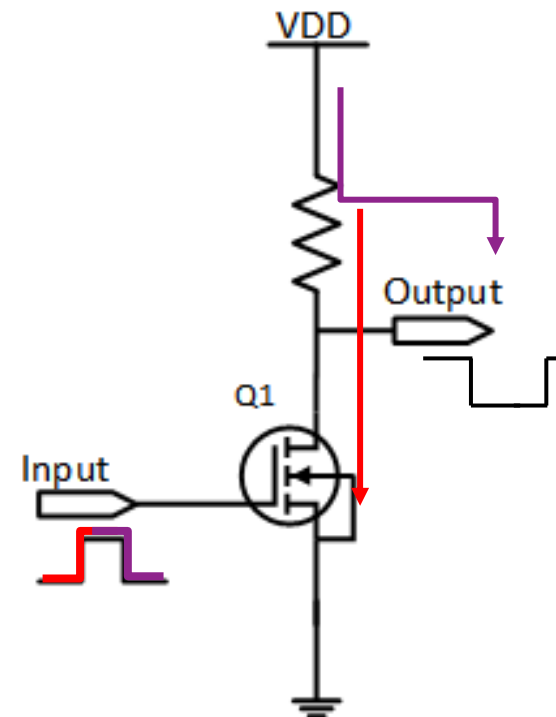


\*X. Li, *et al*, "200V enh..integration"  
IEDM,38.7 (2017): 918-921.

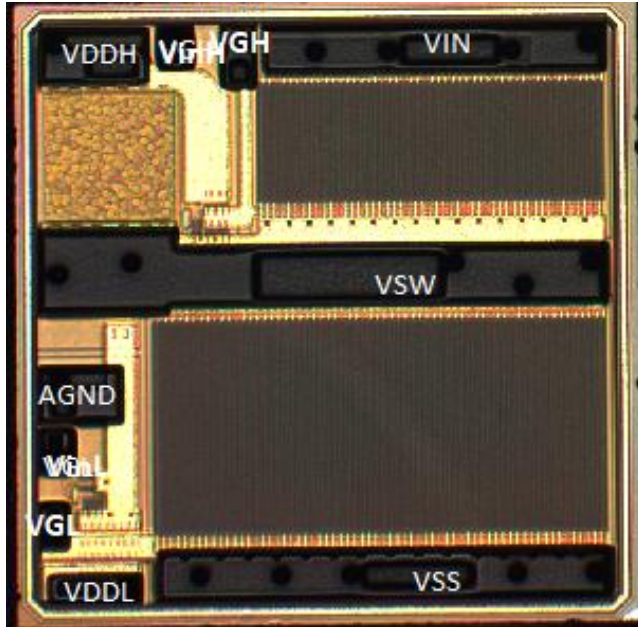
# Monolithic Integration:

## Circuit level challenges

- No complementary device
  - Use RTL based design
  - Trade-off between switching speed and power dissipation in dimensioning the resistors
- Difficulties in driver design
- Difficulties in logic gates/analog sub-circuits

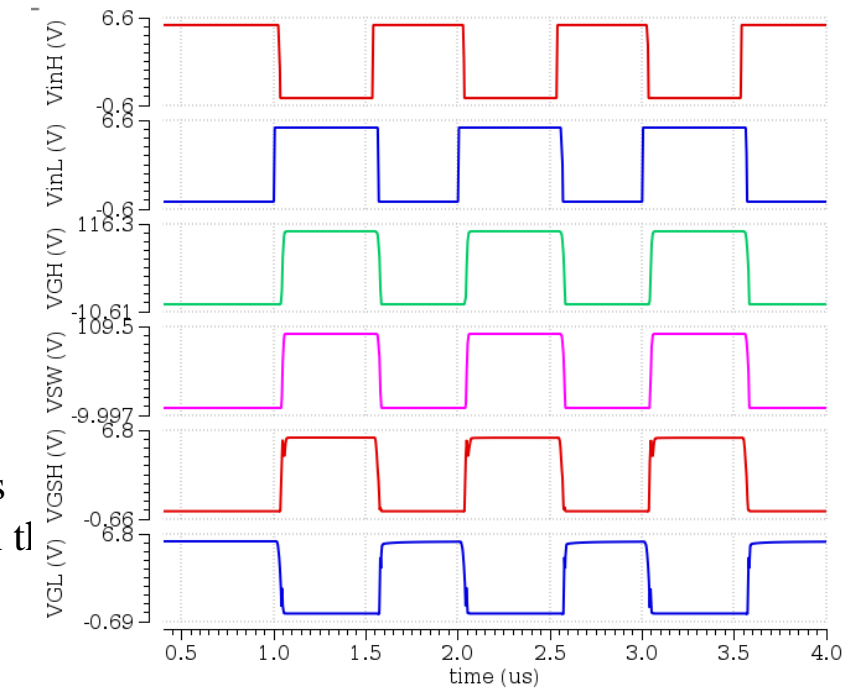


- $RL$  increases  $\Rightarrow$  gain & transition delay increases
- $RL$  increases  $\Rightarrow V_{OL}$  & power dissipation decreases



GaNIC sample

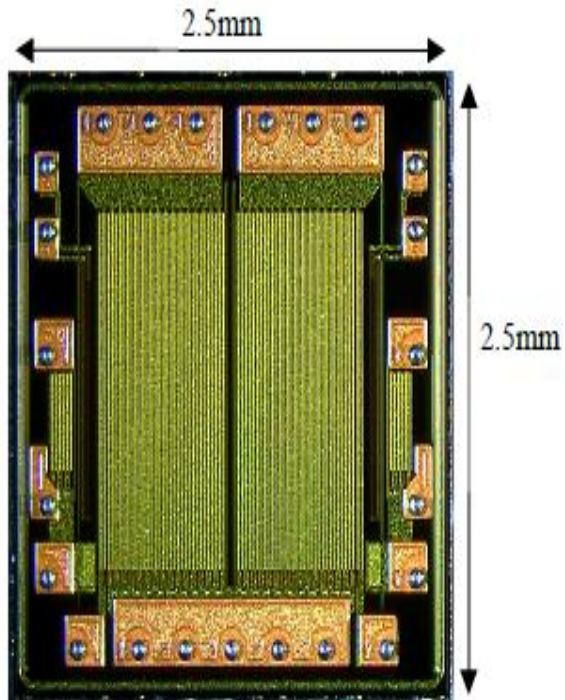
Thermal vias  
and metal on the  
back



## 200V Asymmetric Half-Bridge switch with integrated driver for synchronous power converters

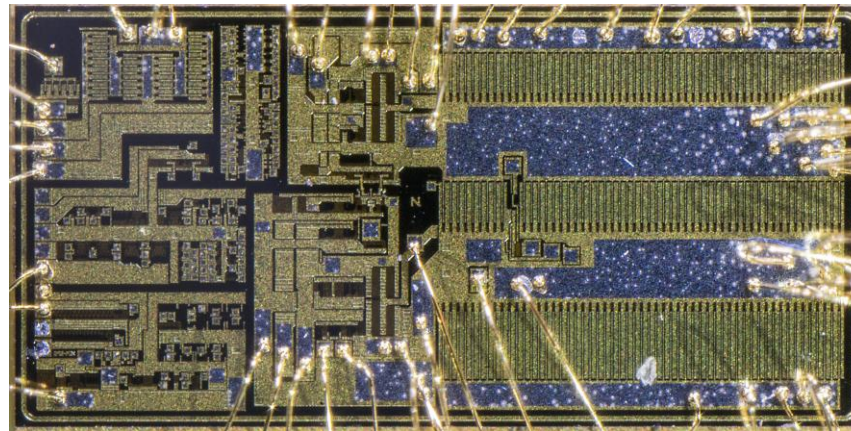
\*U. Chatterjee, *et al*, Elsevier SSE,  
<https://doi.org/10.1016/j.sse.2023.108707>





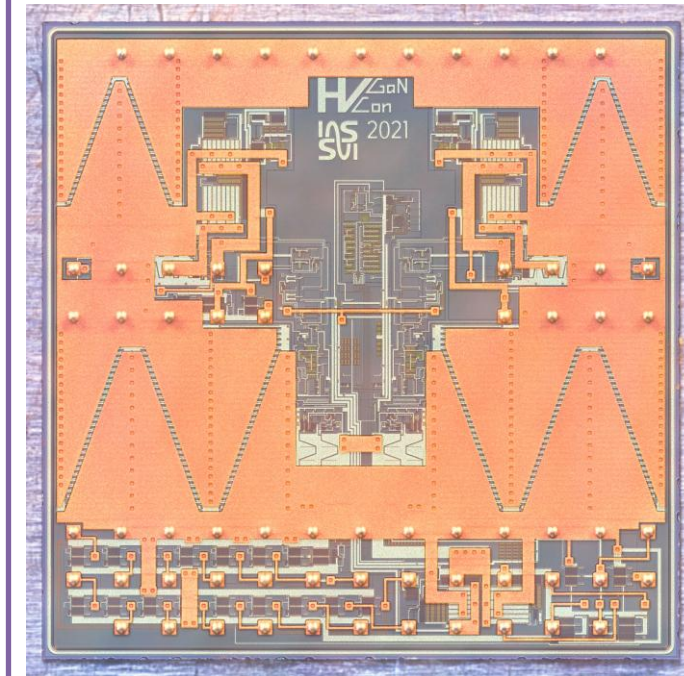
Monolithic Royer-circuit switching cell

\*M. Rueß, University of Stuttgart,  
WIPDA 2023



400V, 1MHz, 200W high-efficiency totem-pole  
PFC converter

\*M. Basler, N. Deneke, University of Hannover, IEEE  
Open J. Pow. Electron. 2023



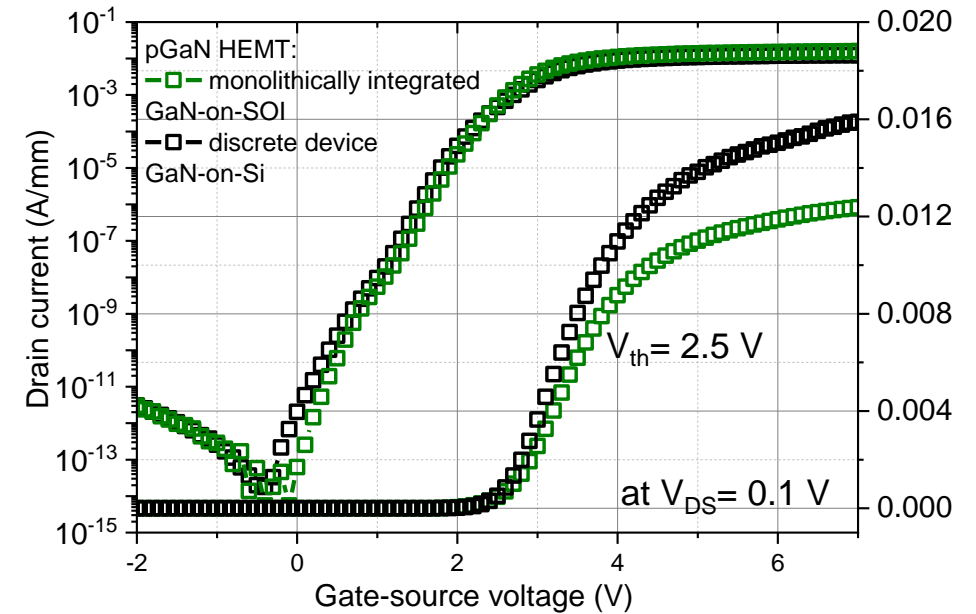
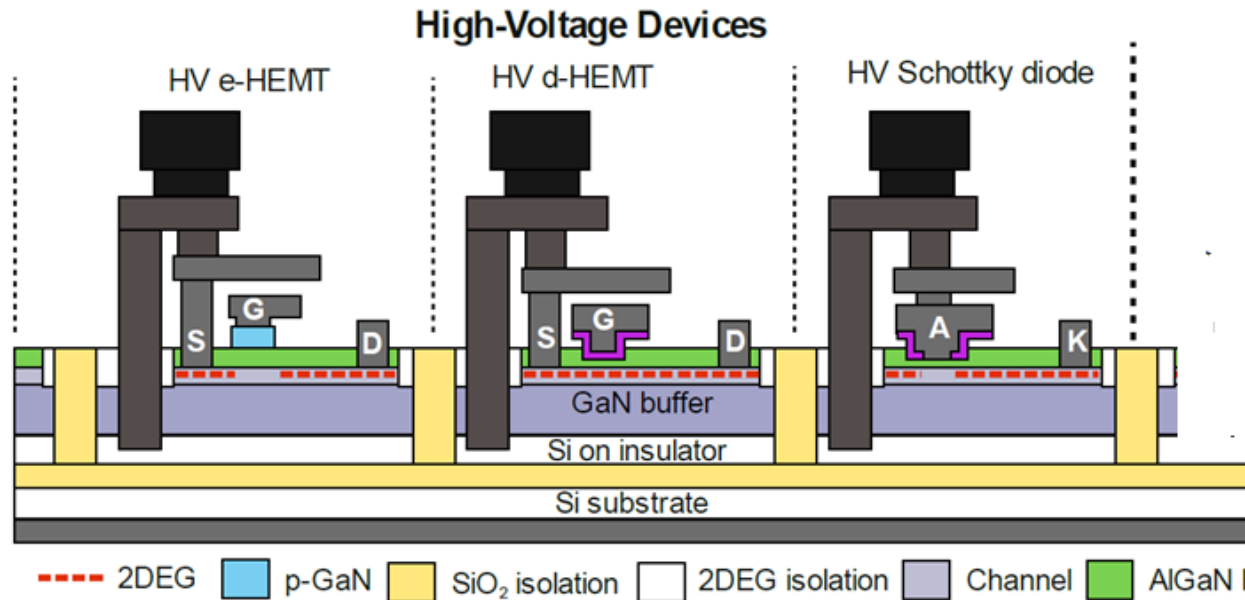
Monolithically Integrated  
Dual Half-Bridge Converter

\*J. Grobe, University of Aachen,  
2023

Access through MPW service



<http://euopractice-ic.com/mpw-prototyping/power-electronics/>



## Transfer Characteristics

\*T. Cosnier, *et al*, IEDM 2021, doi:10.1109/IEDM19574.2021.9720591

\*O. Syshchyk, *et al*, ESSDERC 2022, doi:10.1109/ESSDERC55479.2022.9947150, 2022

\*P. Vudumula, *et al*, SSE 2023, doi:org/10.1016/j.sse.2022.108496





## IMEC (founded in 1984)

- World-leading R&D center in **nano-electronics**
- **International top talent** in a unique **2B€ leading-edge fab infrastructure**
- Delivering **industry relevant technology** solutions serving ICT, Healthcare and Energy markets serving 600+ companies
- **>500 M€** R&D budget, **85%** direct from **industry**
- **5000+** people
- **HQ** in Leuven, Belgium
- **8 sites** worldwide



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Or here some other text



A close-up, angled view of a semiconductor chip, showing a complex grid of circuitry in various colors like blue, purple, and gold.

# THANK YOU



*This project has received funding from the European Union's Horizon Europe research and innovation programme under GA N° 101092562*

**EU – Singapore – 1<sup>st</sup> Joint Researchers Forum on Semiconductors**

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