Pathfinding R&D to enable transition from lab-to-fab

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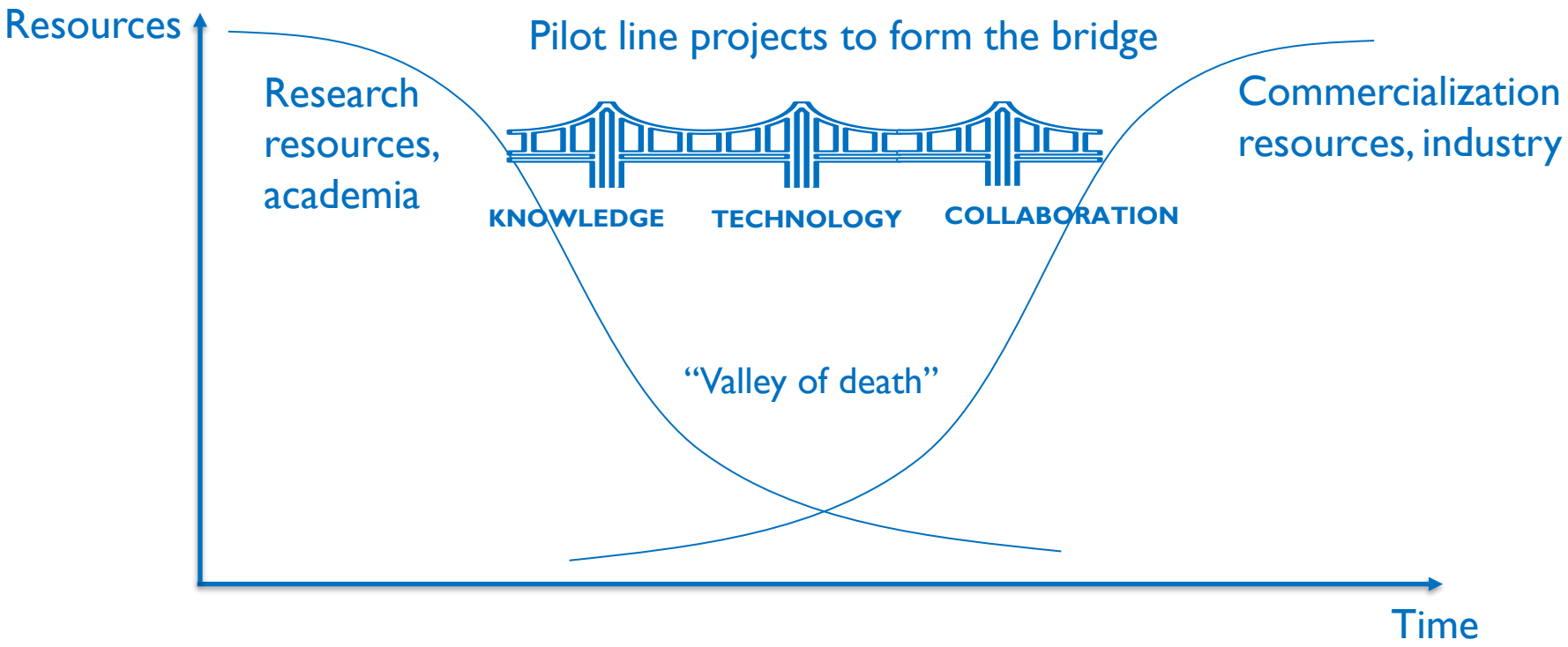
NanoIC

2D PILOT LINE
FROM THE GRAPHENE FLAGSHIP

Outline

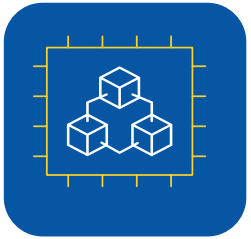
- Bridging the gap from lab-to-fab
- Technology development from materials screening to prototyping
- Approach followed by pilot line projects – NanoIC pilot line and 2D-pilot line project
- Education and training

Moving R&D from lab to the fab



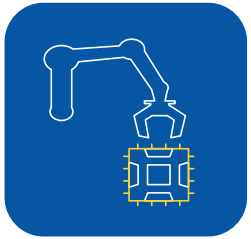
Technology development

progress requires extensive research into various fields

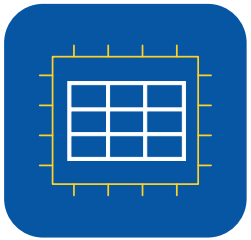


New materials

Process modules



Equipment

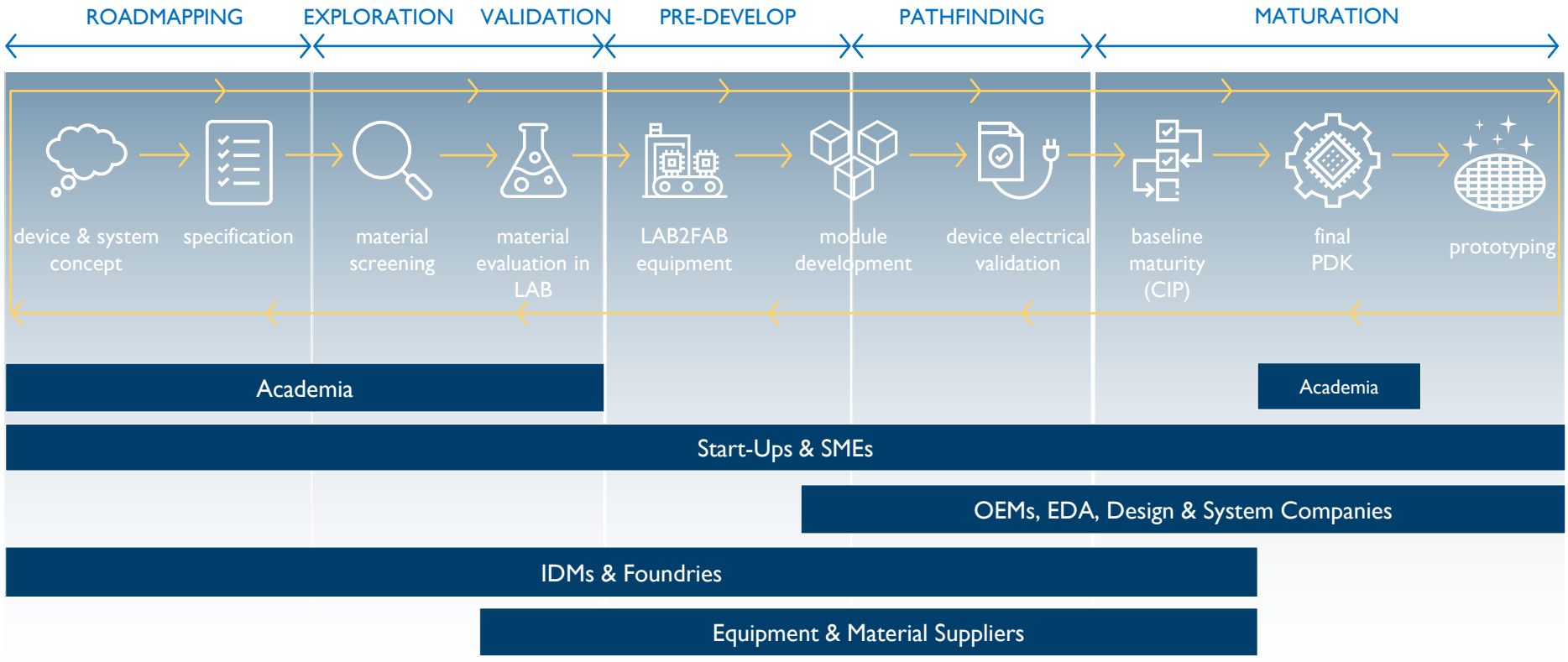


patterning capabilities

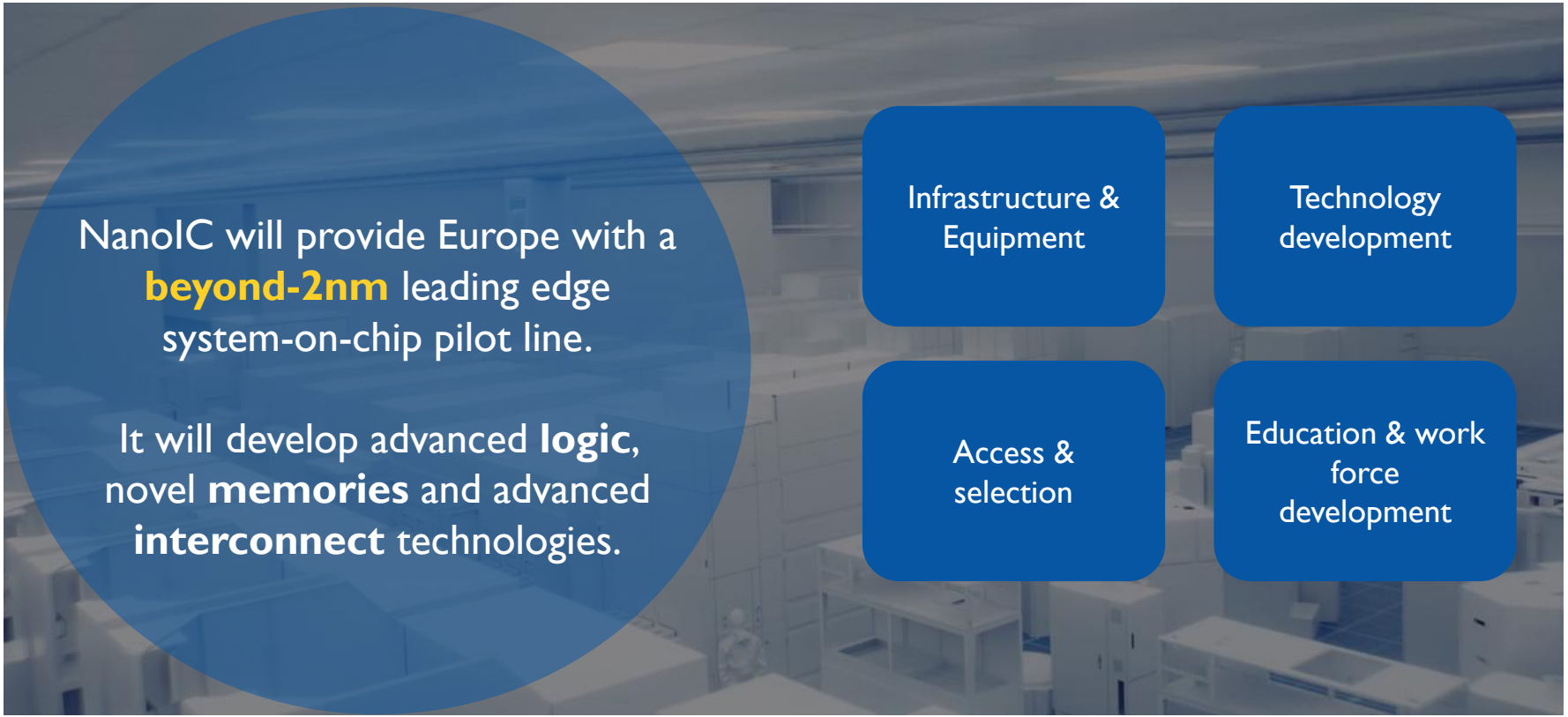
TRL

Low → High

From idea to prototyping



The NanoIC pilot line



NanoIC's below-2nm objective on imec's logic technology roadmap

2018 2020 2023 2025 2027 2029 2031 2033 2035 2037 2039

N7 | N5 | N3 | N2 | A14 | A10 | A7 | A5 | A3 | A2 | sub-A2

DEVICE AND MATERIAL INNOVATIONS

FinFET → **NanoSheet** → **CFET** → **2DFET, ?, …**

	FinFET			NanoSheet			CFET			2DFET, ?, …	
	Introduction	Scaled	Extended	Introduction	Scaled	Extended	Introduction	Scaled	Extended	Introduction	Scaled
Metal Tracks	6	6	6	5	5	5	4	<4	<4	<4	<4

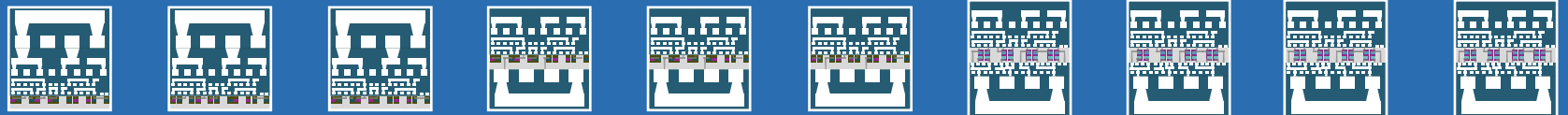
CONTINUED DIMENSIONAL SCALING

0.33NA EUV → 0.55NA EUV → 0.75NA EUV ?

Metal Pitch [nm]	40	28	23	22	21	18	18-16	18-14	16-12	16-12	14-10

CHIP INTERCONNECT ARCHITECTURE

Back-side Power - Global interconnects → Back-side Power - Local signal lines

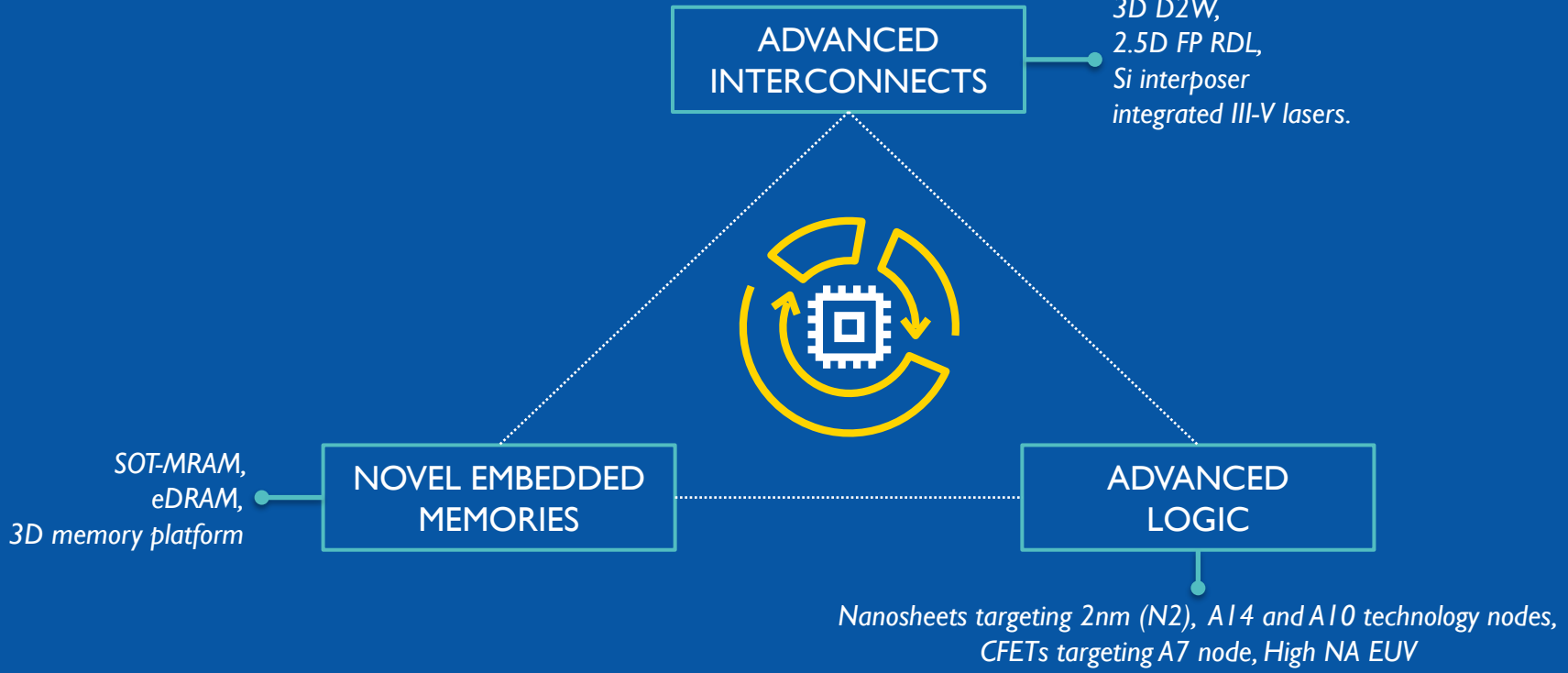


Back-side Metal Pitch estimate [nm]	-	-	160-65	115-45	90-42	40-34	40-28	tbd	tbd

…

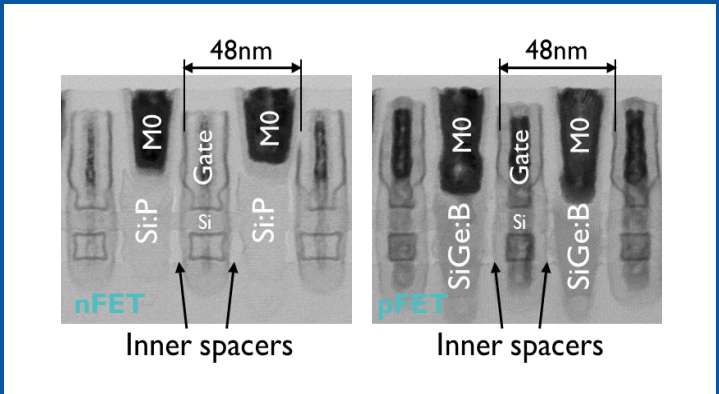
imec NanoIC

Technology platforms in NanoIC scope:

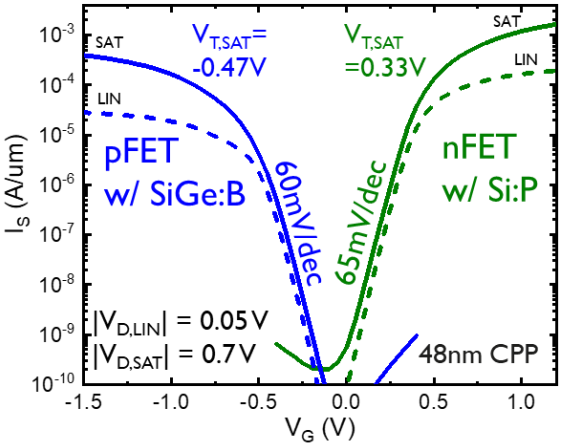


Advanced logic: nanosheet FET

- Functional CMOS demonstrated
- Test Vehicle → ready for further process and module exploration w material and tool suppliers
- Electrical result → N2 research PDK



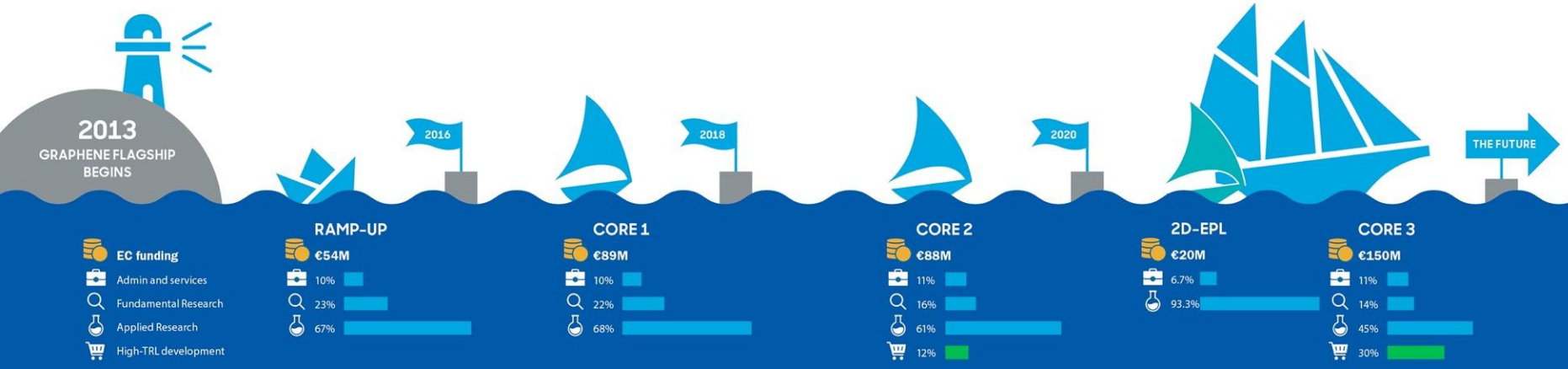
H. Arimura et.al. IEEE VLSI, 2024



GRAPHENE FLAGSHIP

Funded by the European Union

The Evolution of the Graphene Flagship

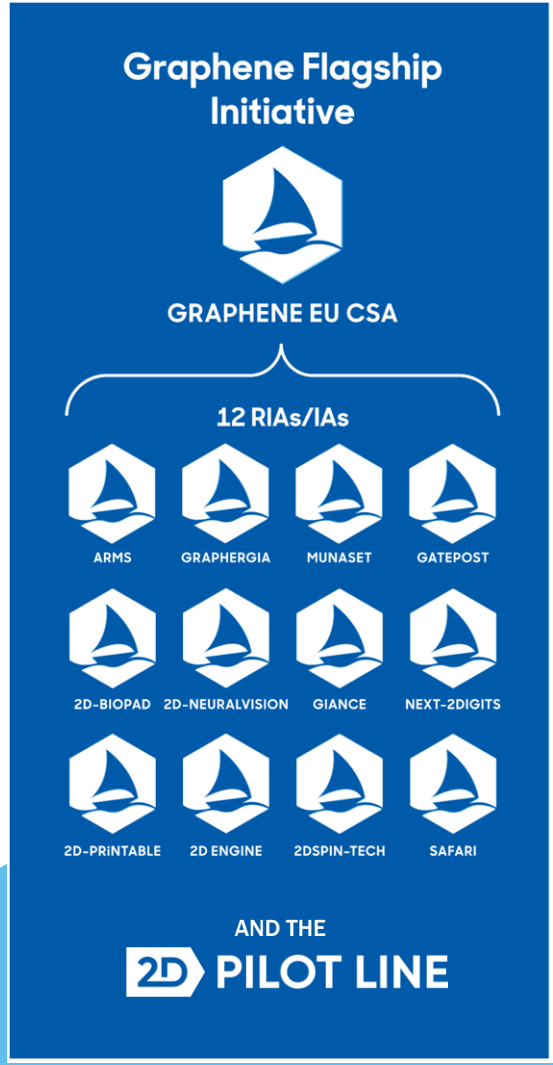


SHAPING FUTURE TECHNOLOGY

- **12 Research and Innovation Actions (RIAs) and Innovation Actions (IAs)** work to integrate graphene and other 2D materials in a variety of areas including:
  - Electronics and Photonics
  - Energy
  - Biomedical
  - Composites
  - 2D materials of tomorrow
  - Safe by design

- **Graphene Europe in the Lead (GrapheneEU)** a Coordination and Support Action (CSA) guarantees overall coherence of the Graphene Flagship and provides common services and support functions.

- Teams working on **standards, industrialisation, road mapping** and **dissemination**.



Bringing 2D-materials from lab to fab

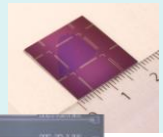
Trajectory followed at imec

Generating the ecosystem for 2D material integration

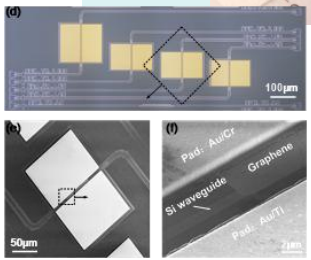
2014	2016	2018	2020	2023	2024
• Graphatar	• GF core 1	• GF core 2	• GF core 3 • 2D-EPL	• 2D-Neuralvision	• 2D-PL

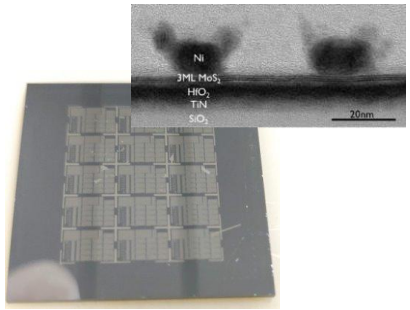
Graphene *Graphene & TMDC*

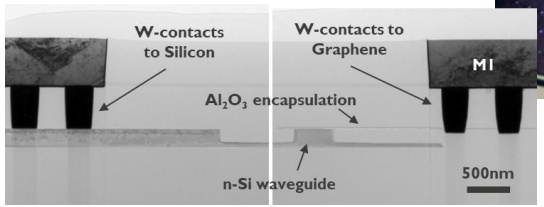
LAB FAB

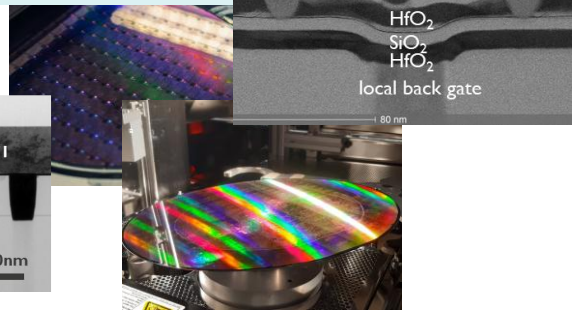


Lab processing enables pathfinding process screening for fab integration.









Schematic of generic integration flow

Application specific integration demands

< *Target wafer formation*

2DM - deposition

MX2-
direct growth

- Growth on sacrificial wafer
- Layer transfer process
- Polymer residue removal

- Growth on sacrificial wafer
- Layer transfer process
- Polymer residue removal

Active

- Interlayer deposition
- Gate dielectric deposition
- Active patterning
- Oxide encapsulation and CMP

- Passivation layer
- Active patterning

Contacts

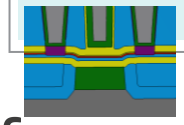
Damascene contacts

- Side contact etch
- Metal deposition
- CMP

- Side contact etch
- Metal deposition
- Clear out

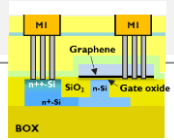
Application specific

Damascene gate metal

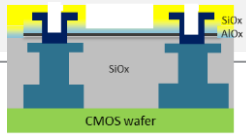


- Gate etch
- Gate Metal deposition
- CMP
- VIA & probe pads

Damascene Si- contact



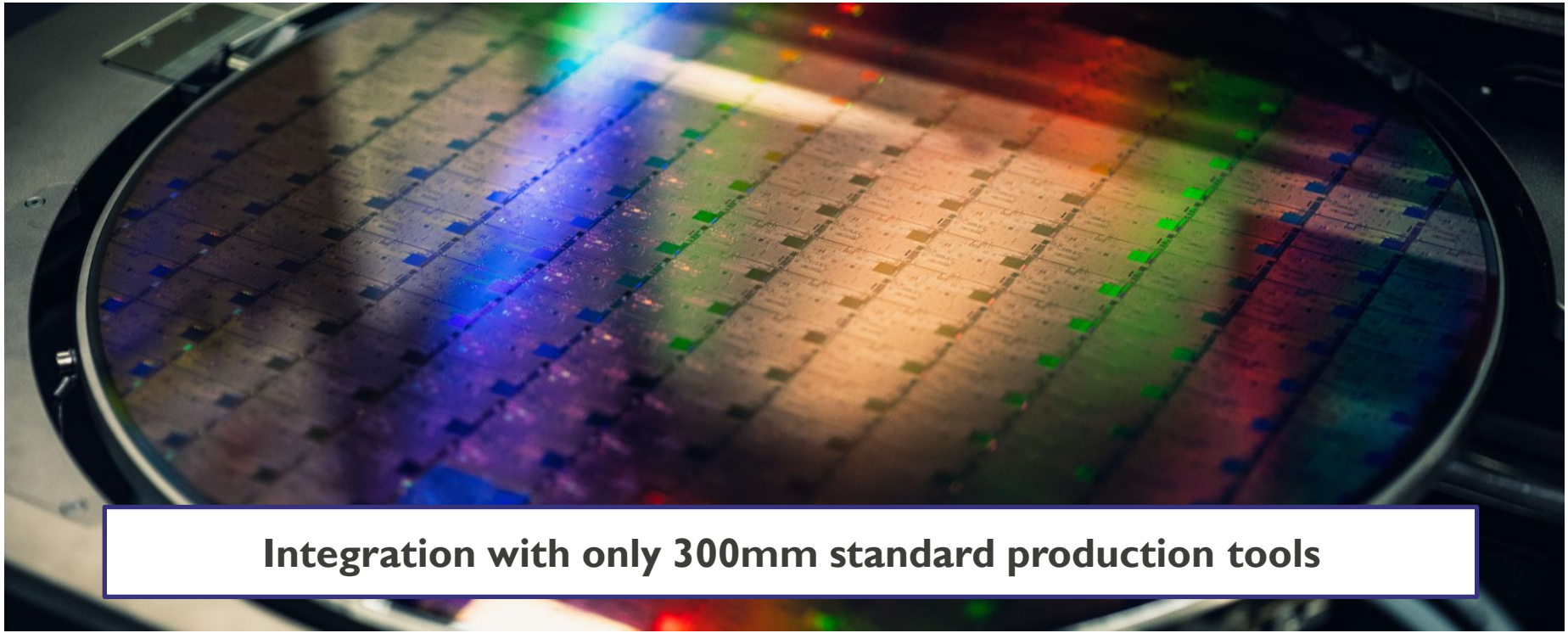
- Si-contact etch
- Metal deposition
- CMP
- VIA & probe pads



- SiOx deposition
- Bond pad open
- Oxide open
- QD-functionalization

imec

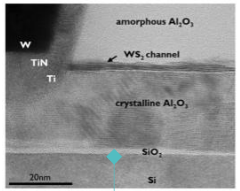
Wafer scale integration



Wafer scale integration in 300 mm fab

From morphological demonstration to lot-to-lot variability

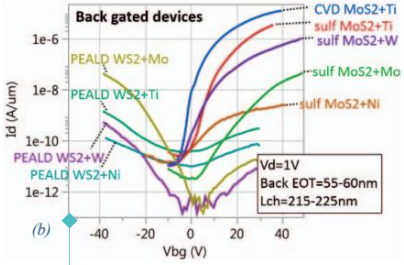
1st morphological demonstrator



Schram et al. 2017, ESSDERC

2017

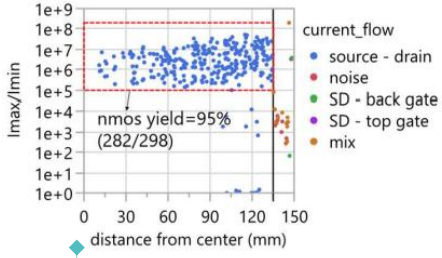
Material screening via Fab – Lab – Fab route



Huyghebaert et al. 2018, IEDM

2018

Wafer yield and process uniformity

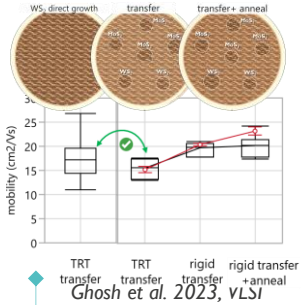


Schram et al. 2021, IEDM

2021

2022

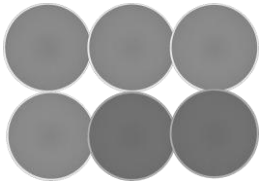
Epitaxial MoS2 integration enabled via CoD2W transfer



Ghosh et al. 2023, VLSI

2023

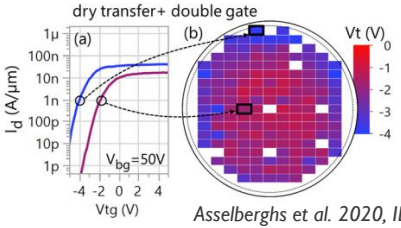
Uniformity and reproducibility



Ghosh et al. 2024, VLSI

2024

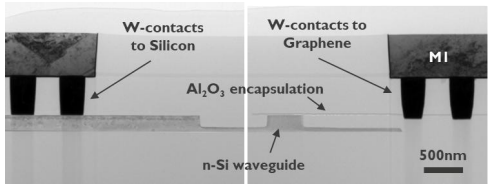
1st fab integration of full 300 mm transferred WS2 layer



Asselberghs et al. 2020, IEDM

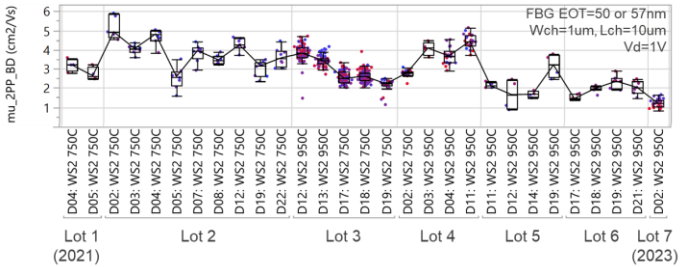
2020

SLG EAM modulator BEOL graphene integration



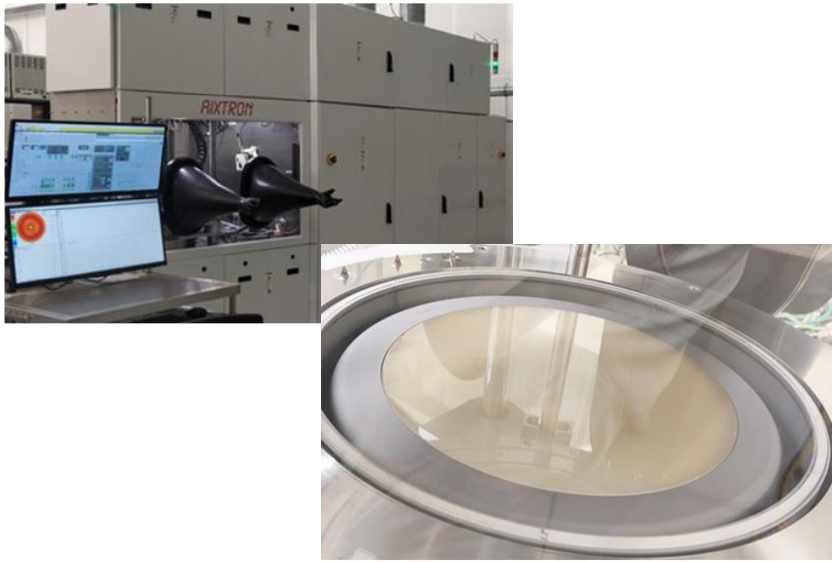
Wu & Pantouvaki et al. 2021, VLSI

Lot-to-Lot variability



Smets et al. 2023, Graphene week

Dedicated equipment



Above: The new 300 mm reactor by AIXTRON installed in the 300 mm cleanroom at imec. Credit: AIXTRON
Below: First reported WS_2 growth on a 300 mm sapphire wafer in the new AIXTRON 2D reactor at imec.

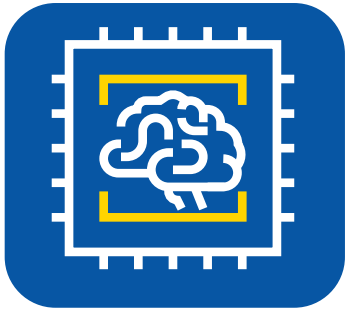
Suss MicroTec's 200/300 mm automated tool for debonding 2D materials (TMDCs) from a growth wafer.

Reference: annual report graphene flagship 2023

Education and training

PDK WORKSHOPS

PHDs



INTERNSHIPS

EXPERT COURSES

N2 PDK – Pathfinding PDK for future logic devices

An explorative design environment for 2nm Gate All Around (GAA) Transistors

NanoIC project provides a comprehensive PDK environment for

- **designing,**
- **experimenting** with, and
- testing **innovative IC solutions**

The PDKs are **continuously benchmarked**
with physical devices (fabricated in imec's cleanrooms),
for maximum adherence to **realistic electrical behavior**

Free access

PhDs and internships under NanoIC

Collaboration with other initiatives

imec

The acquisition and operation of the NanoIC pilot line are jointly funded by the Chips Joint Undertaking, through the European Union's Digital Europe (101183266) and Horizon Europe programs (101183277), as well as by the participating states Belgium (Flanders), France, Germany, Finland, Ireland and Romania. The 2D-pilot line is funded through projects 2D-EPL (952792) and 2D-PL (101189797).

Funded by the European Union. Views and opinions expressed are however those of the author(s) only and do not necessarily reflect those of the European Union or Chips Joint Undertaking or the Communications Networks, Content and Technology (CNECT) granting authority. Neither the European Union nor the granting authority can be held responsible for them.

Discover more at **nanoic-project.eu**

NanoIC

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2D PILOT LINE
FROM THE GRAPHENE FLAGSHIP

GRAPHENE FLAGSHIP

(Co)-funded by the European Union

Chips JU

Flanders
State of the Art