



ENERGIZE – EU-ROK collaborative project to enable energy efficient neuromorphic two-dimensional devices for edge computing

Dmitry Chigrin, AMO GmbH, Aachen, Germany



Funded by the European Union



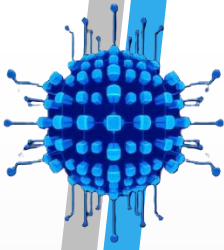
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ENERGIZE

Energy-efficient Neuromorphic 2d Devices
And Circuits For Edge AI Computing

What

Expertise

Materials, Devices and
Circuit Modelling



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High-quality Material Growth

EPFL



Advanced Device Fabrication



EPFL

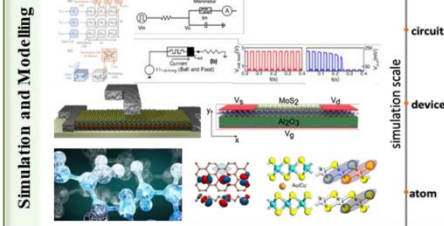


Cutting-edge Circuit Design

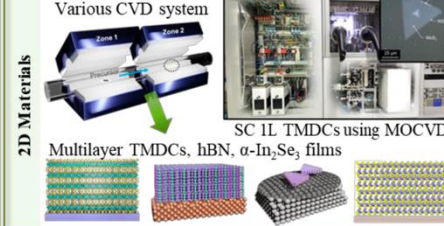


SOGANG
UNIVERSITY

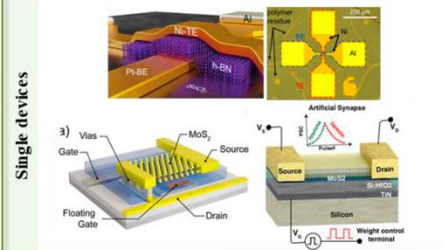
A multi-scale modelling framework



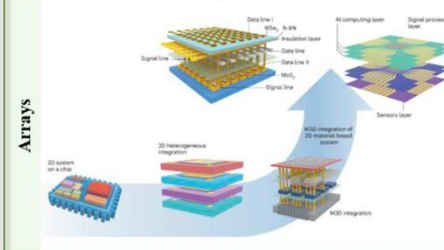
Wafer-scale, high-quality 2D films



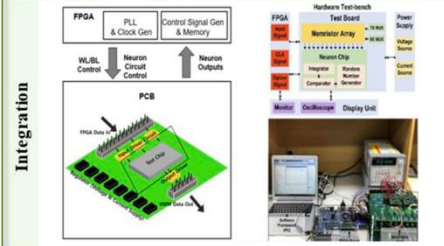
2D two-terminal and three-terminal devices



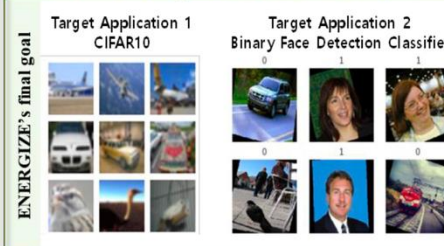
Large-scale Synapse and Array



Neuromorphic Circuits and System



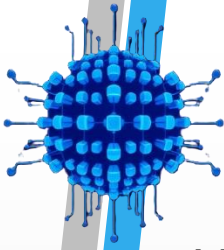
Benchmarking for devices and circuits



2D Devices and Circuits for edge AI computing



ENERGIZE's vision is to leverage the potential of **wafer-scale, 2D materials-based neural networks** to develop **energy-efficient neuromorphic devices and circuits for edge AI computing**.

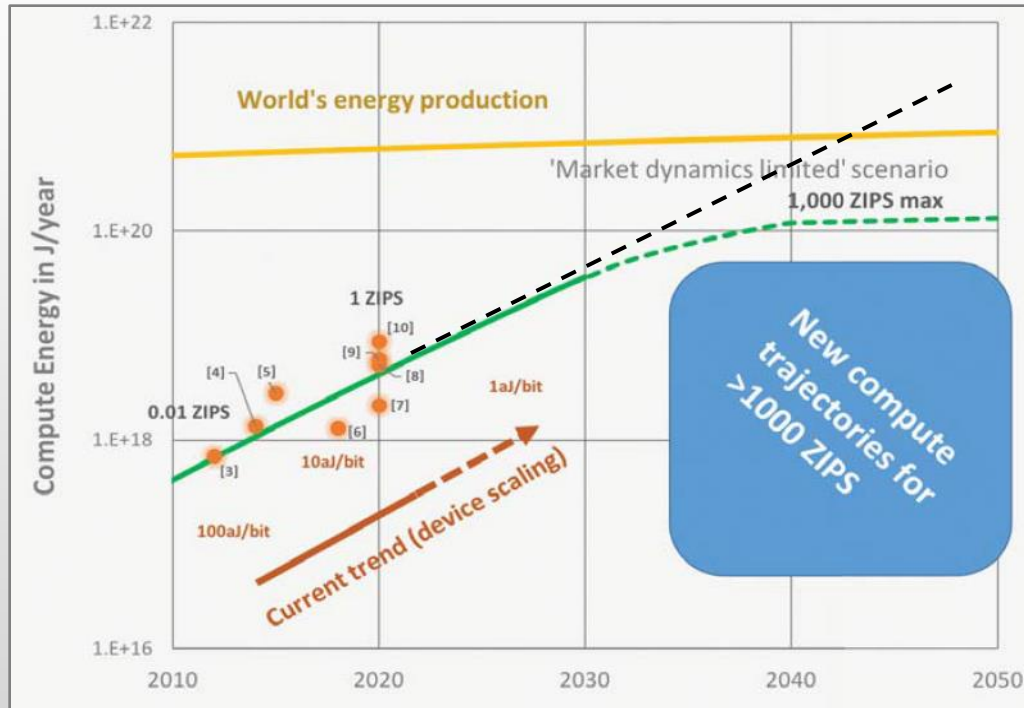


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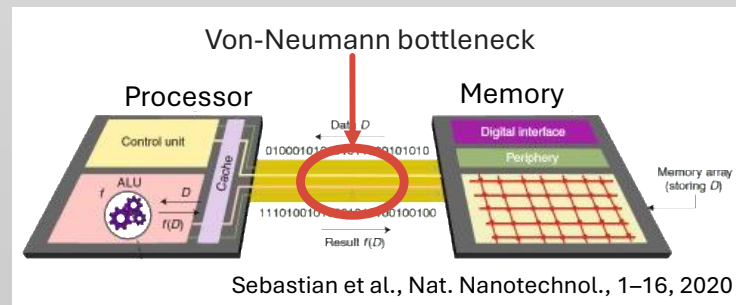
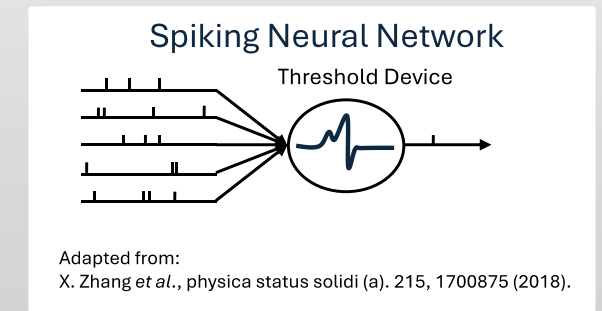
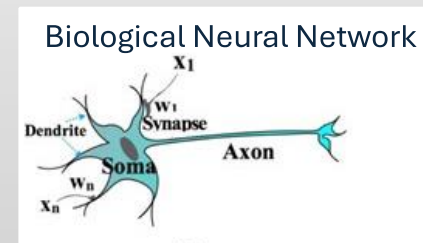
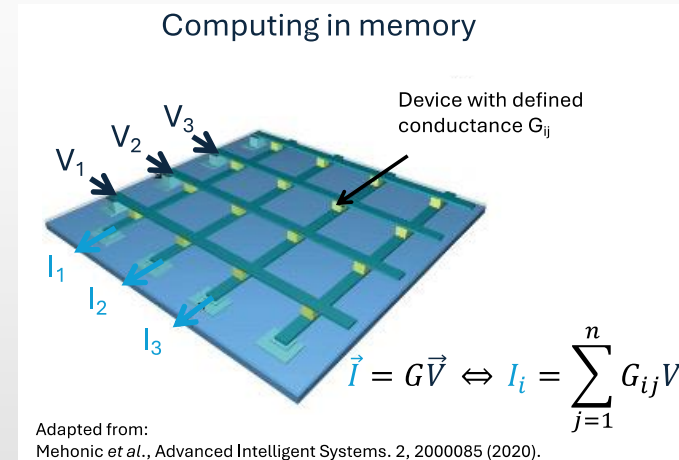
Energy-efficient Neuromorphic 2d Devices
And Circuits For Edge AI Computing

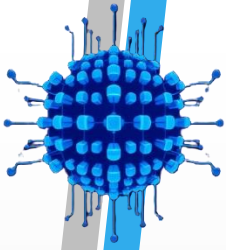
Why

Machine Learning and Artificial Intelligence need new hardware → Neuromorphic Computing



Source: SRC Decadal Plan, 2020





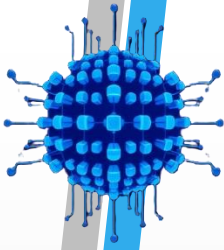
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Energy-efficient Neuromorphic 2d Devices
And Circuits For Edge AI Computing

Who



- AMO GmbH (AMO)
- Università di Pisa (UNIPi)
- Universidad de Granada (UGR)
- École Polytechnique Fédérale de Lausanne (EPFL)
- Sungkyunkwan University (SKKU)
- Korea University (KU)
- Gwangju Institute of Science and Technology (GIST)
- Sogang University (SGU)



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Energy-efficient Neuromorphic 2d Devices
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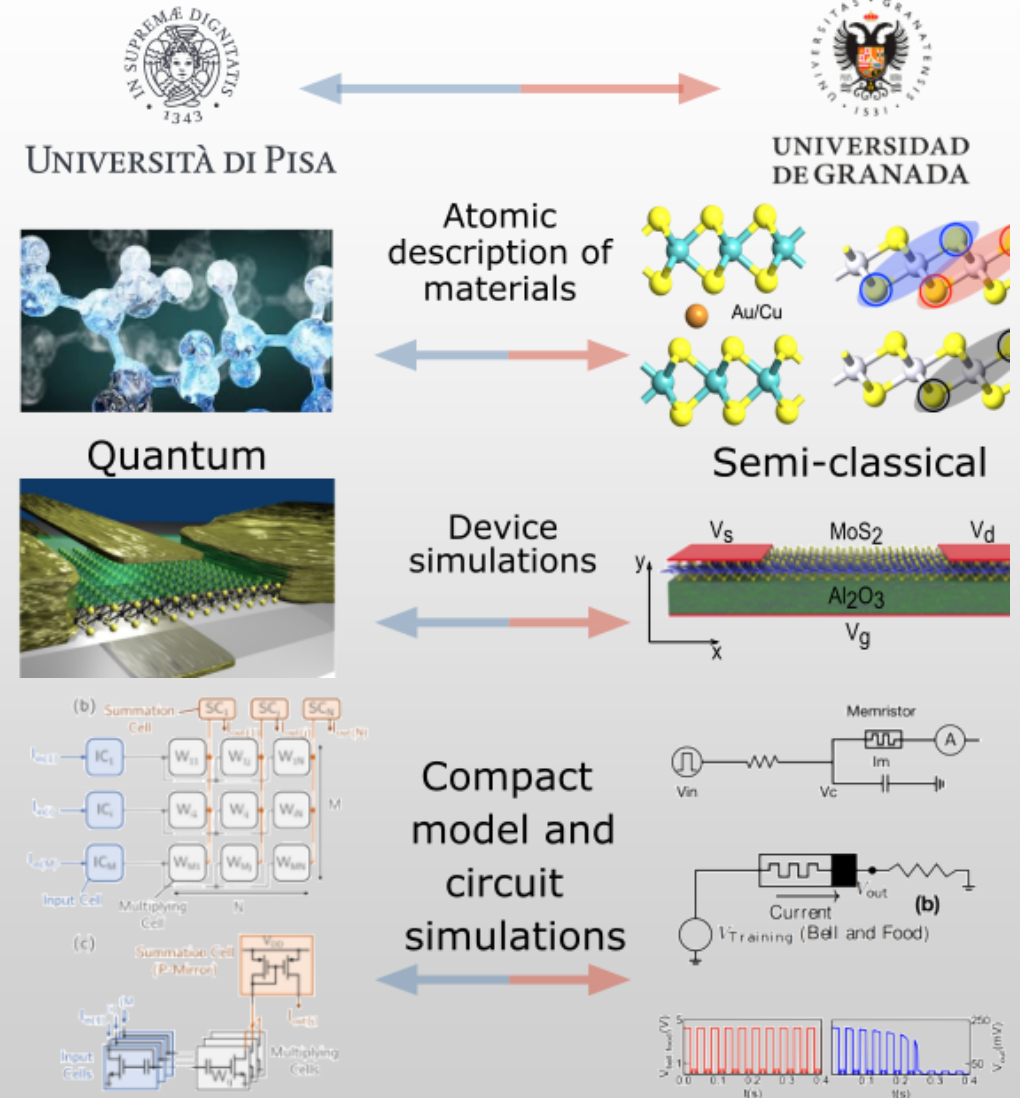
Objective:

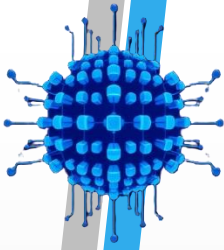
- To provide a multiscale simulation approach for the study of devices for neuromorphic electronics, spanning from atomistic to large scale circuit emulations.

Partners:

- UNIPi:** Atomistic simulations of 2DMs, multiscale transport simulation of devices up to circuit level.
- UGR:** Simulation of 2DMs, devices and circuits, compact modelling of devices and validation.

Simulation and Modelling





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Energy-efficient Neuromorphic 2d Devices
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Objective:

- To develop wafer-scale growth of multilayer 2DMs, including semiconducting TMDCs, insulating hBN, and ferroelectric α -In₂Se₃, for neuromorphic devices and circuits.

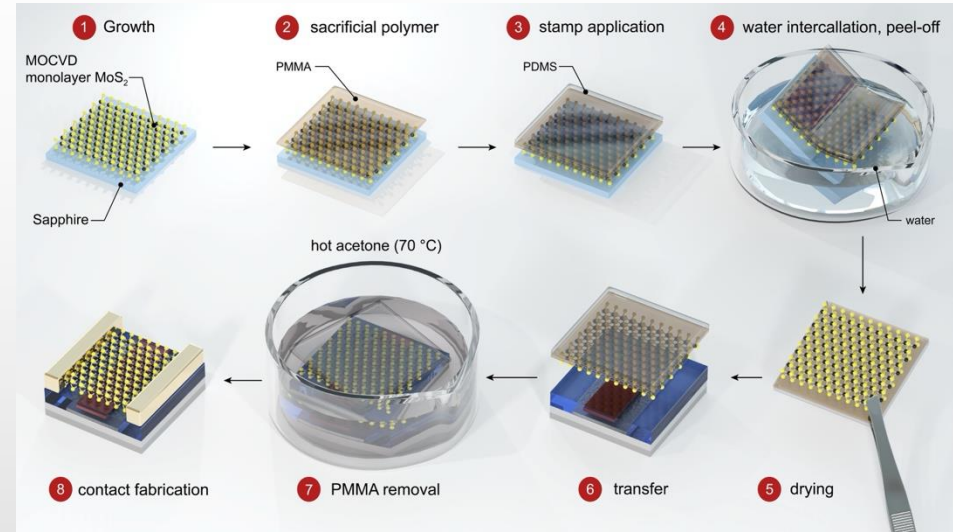
Partners:

- EPFL:** Devices and circuits **fabrication** based on 2DM, electrical and optical **characterization**
- SKKU:** Wafer-scale, high-quality **2DMs growth**, qualitative and quantitative characterization of the materials, three or more terminal **memtransistor array** and its application for neural network.

2D Materials

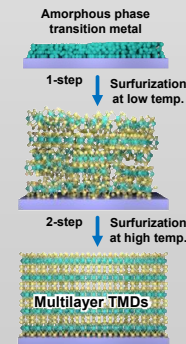
EPFL

MOCVD growth & transfer



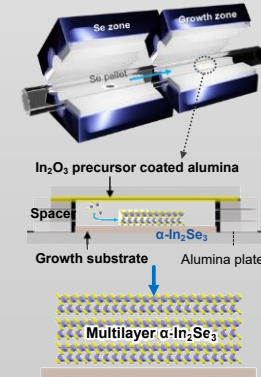
A. Multilayer TMDs

Amorphous phase crystallization (APC)



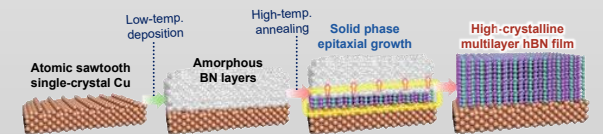
B. Multilayer α -In₂Se₃

Phase controlled growth

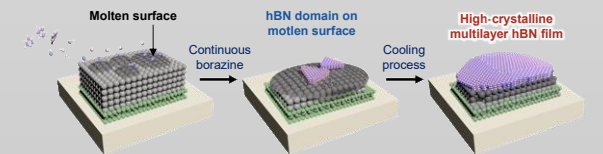


C. Multilayer hBN

I. Solid phase epitaxy (SPE) strategy



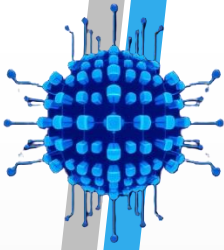
II. Precipitation-driven growth on molten surface



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Objective:

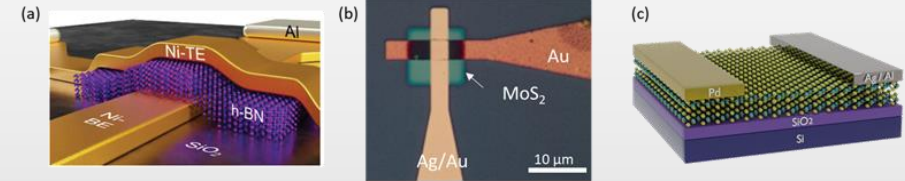
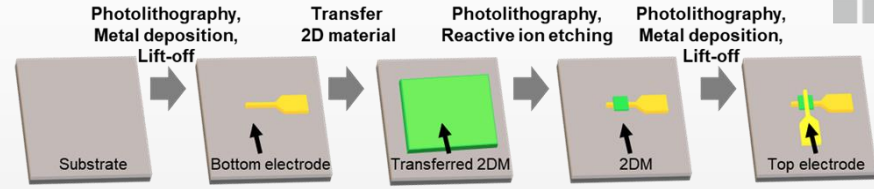
- To establish reliable fabrication and characterization processes for 2D two-terminal and three-terminal devices.

Partners:

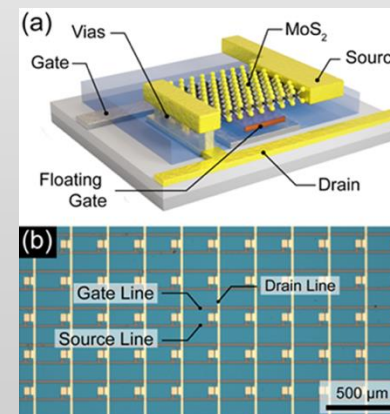
- AMO:** Fabrication of devices based on 2DMs, 2DM film deposition, material and device characterization
- EPFL:** Devices and circuits fabrication based on 2DM, electrical and optical characterization

2D-based Devices

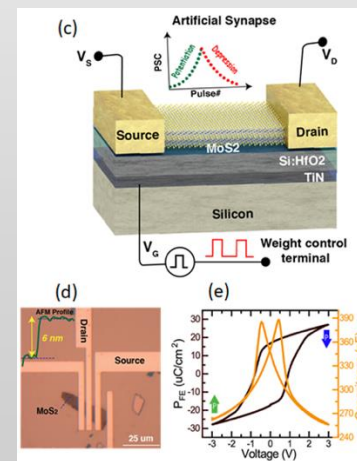
2D two-terminal memristive devices

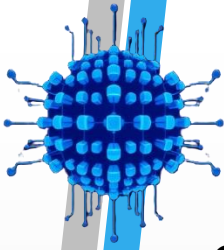


2D three-terminal FGFET



2D three-terminal FeFET





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Objective:

- To develop 2D two-terminal and three-terminal arrays with reliable performance.
- To implement a neuromorphic system that integrates 2DM-based neurons and synapses

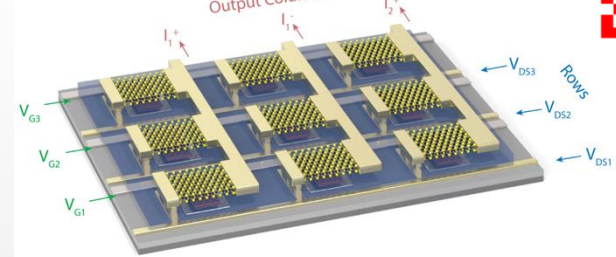
Partners:

- KU:** Non-volatile memory, **memristor**, memristive **array**, reservoir array, 1D/2D **heterojunction** device.
- GIST:** Neuromorphic **circuits and systems design** employing memristive devices.
- SGU:** **Neural network** compression, digital circuit design, software-to-hardware mapping, **software-hardware co-optimization**.
- EPFL & SKKU**

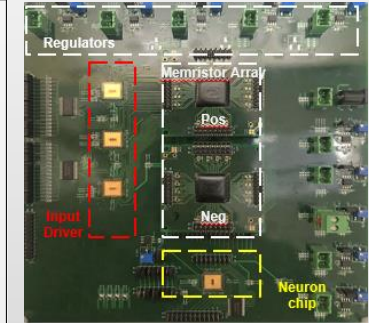
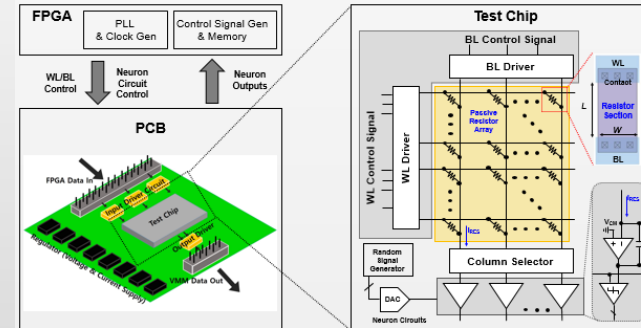


Large-scale Synapse Array

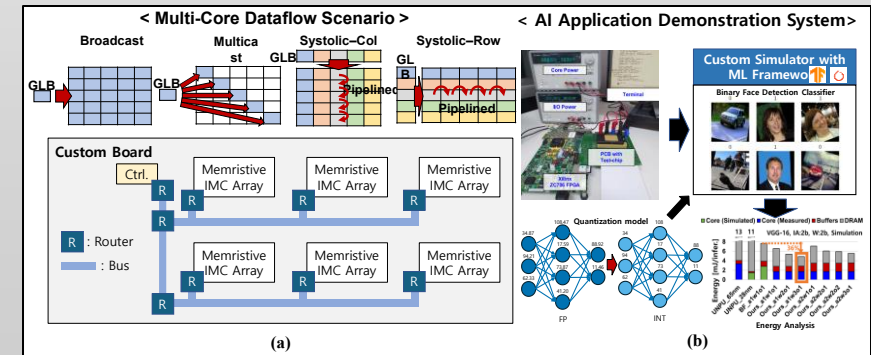
Array integration



Synapse device based VMM Circuit Design



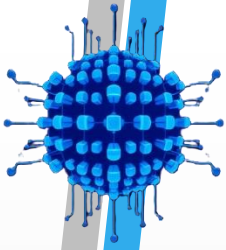
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Large-scale synapse array

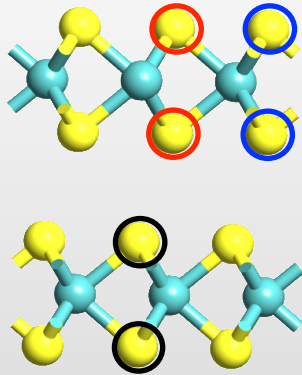


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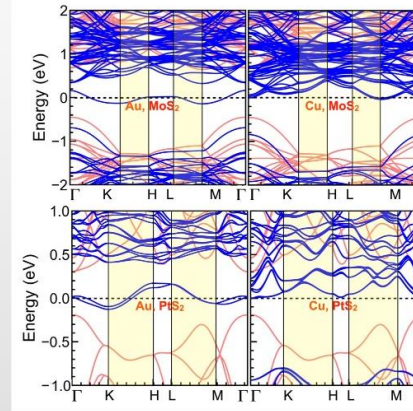
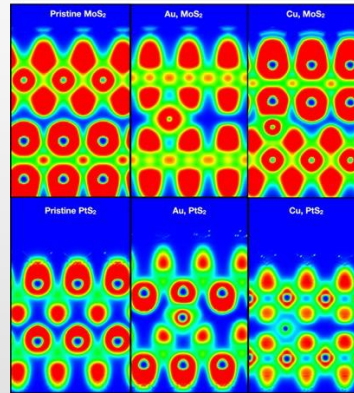


Atomistic simulations of Point Defects and Grain Boundaries in Resistive Switching Mechanisms of 2D Transition Metal Dichalcogenides

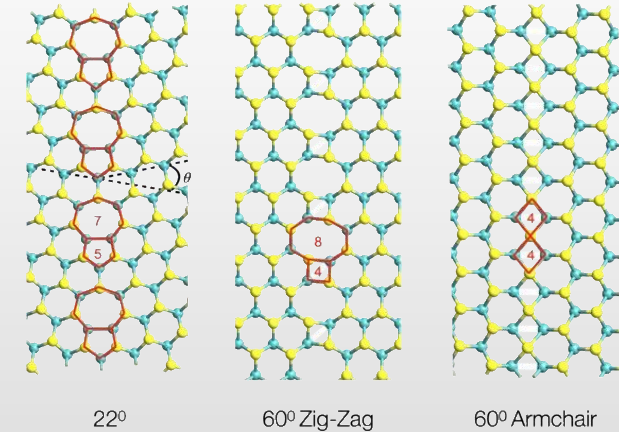
Vacancy Filament



Metal Filament



Grain Boundaries



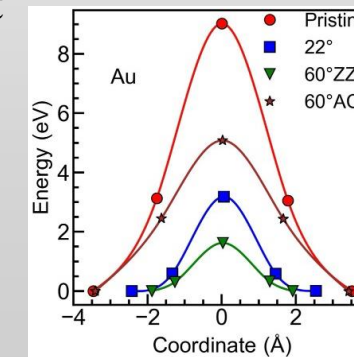
Intrinsic Vacancies alone are insufficient for significant conductivity change; metal atom intercalation is crucial

Trade-off: Grain boundaries can lower switching voltage but also reduce the switching ratio

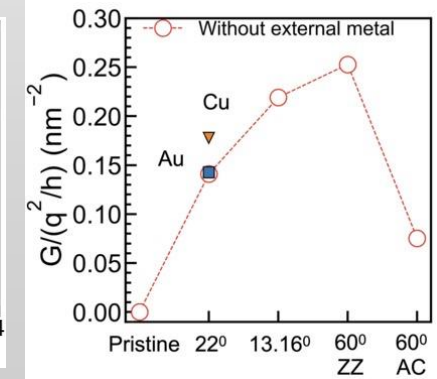
M.D. Ganeriwala *et. al.*, *ACS Applied Nano Materials* (2024), 7(21), 24857-24865

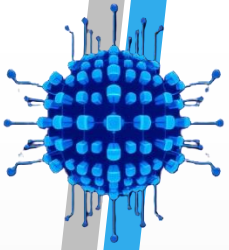
M.D. Ganeriwala *et. al.*, *Nanoscale* (2025) (accepted)

Diffusion Barriers



Conductance





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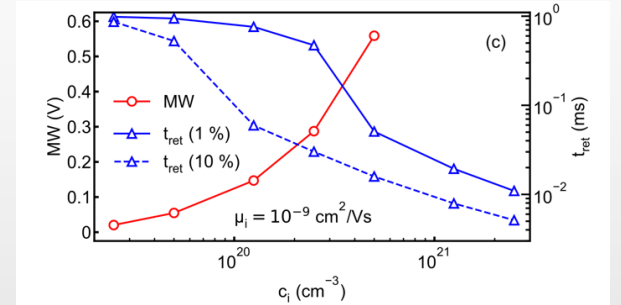
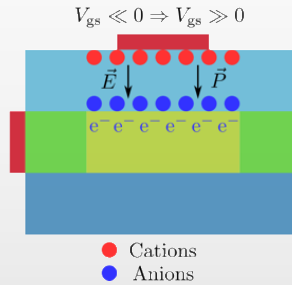
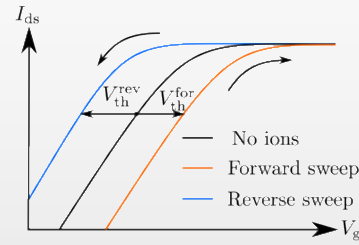
Highlights

In-house tools for mesoscopic numerical simulations (contact: agodoy@ugr.es)



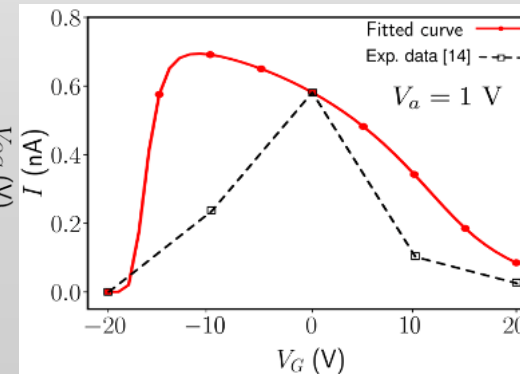
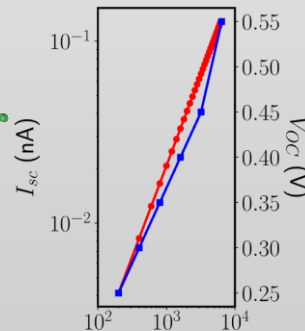
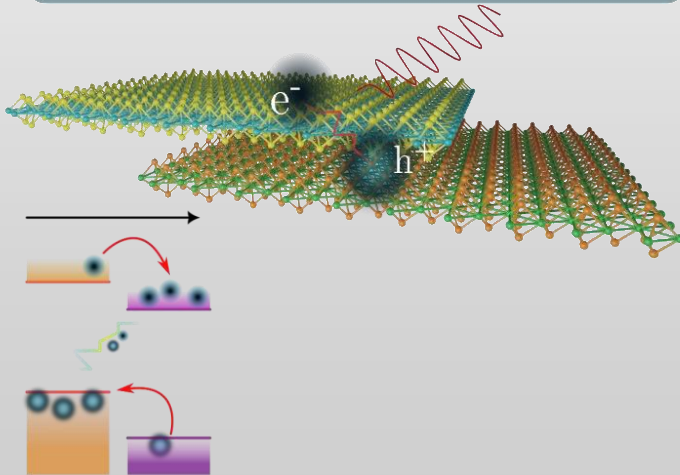
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$$\begin{aligned}\nabla \cdot (\epsilon \nabla V) &= -\rho \\ \nabla \cdot \vec{J}_n &= \nabla \cdot [q\mu_n n \nabla E_{F,n}] = +q \frac{\partial n}{\partial t} \\ \nabla \cdot \vec{J}_p &= \nabla \cdot [q\mu_p p \nabla E_{F,p}] = -q \frac{\partial p}{\partial t} \\ \nabla \cdot \vec{J}_i &= \nabla \cdot [-z_i q D_i e^{-\phi_i} \nabla (c_i e^{\phi_i})] = -z_i q \frac{\partial c_i}{\partial t}\end{aligned}$$



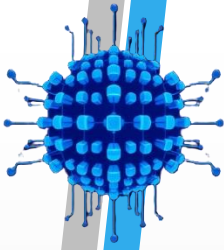
In-house simulator for coupled ionic-electronic simulations.
Showing the working of ferroelectric-like device as memristor

J. Cuesta-Lopez et. al. J. Appl. Phys. 2024, 136 (12), 124501



In-house simulator to
analyze 2DM-based
heterojunction as
photodectors

A. Diaz-Burgos et. al. ESSERC. 2024



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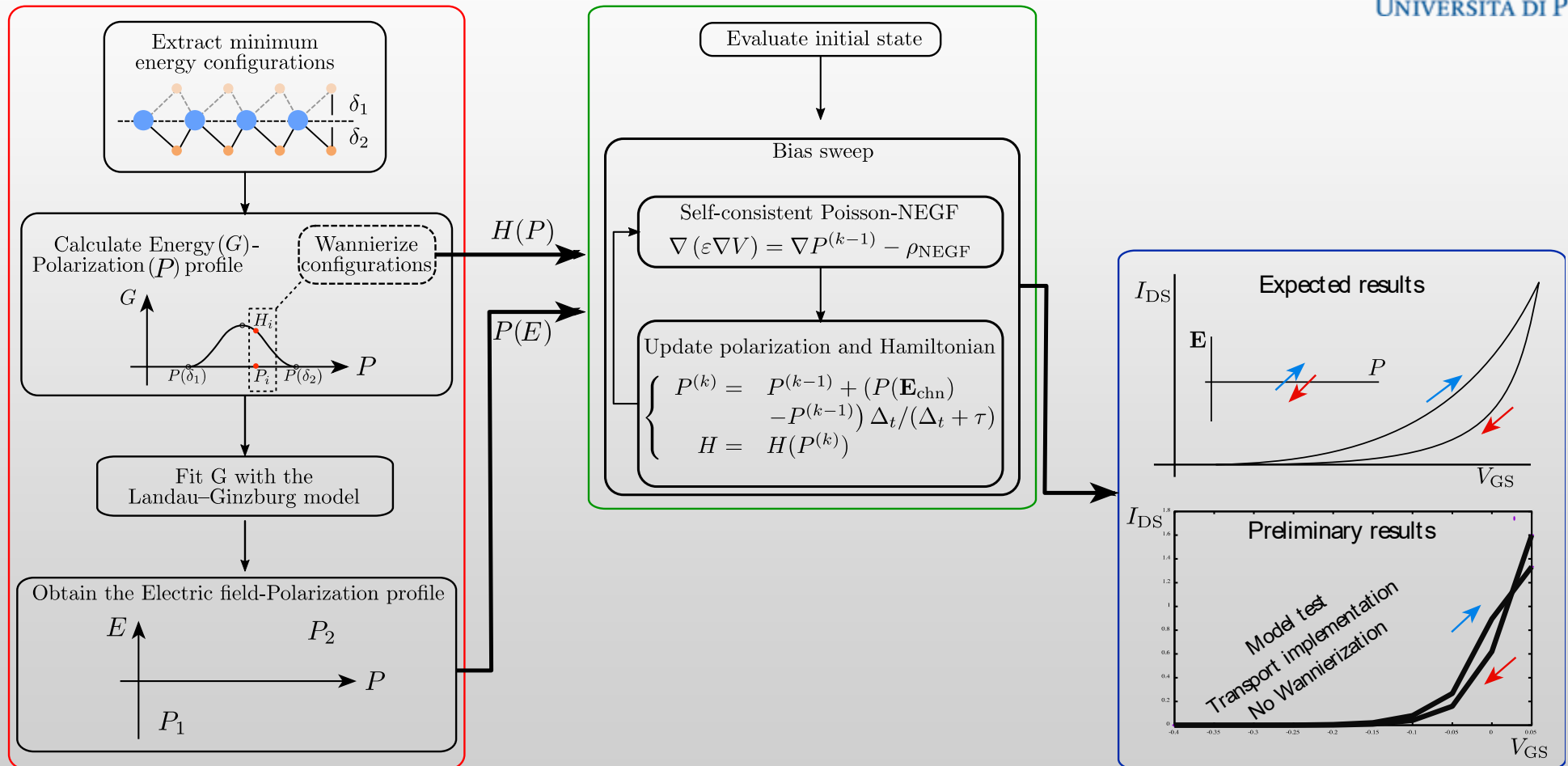
Energy-efficient Neuromorphic 2d Devices
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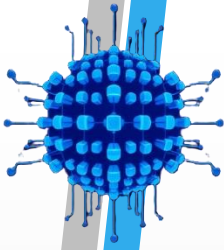
Highlights



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Fully multiscale simulator for Ferro-electrics 2D-based devices





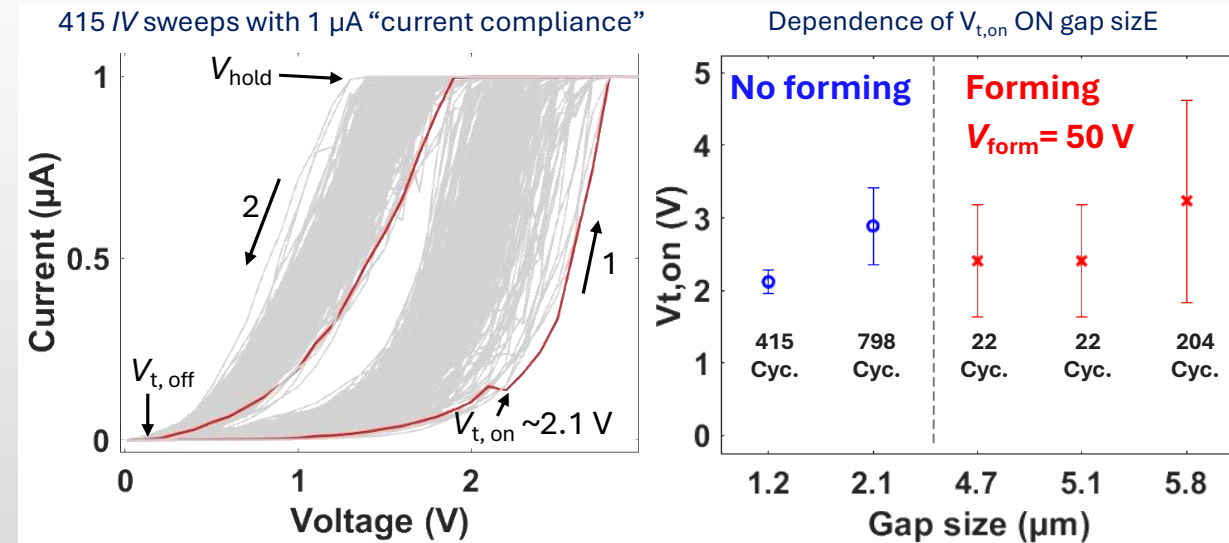
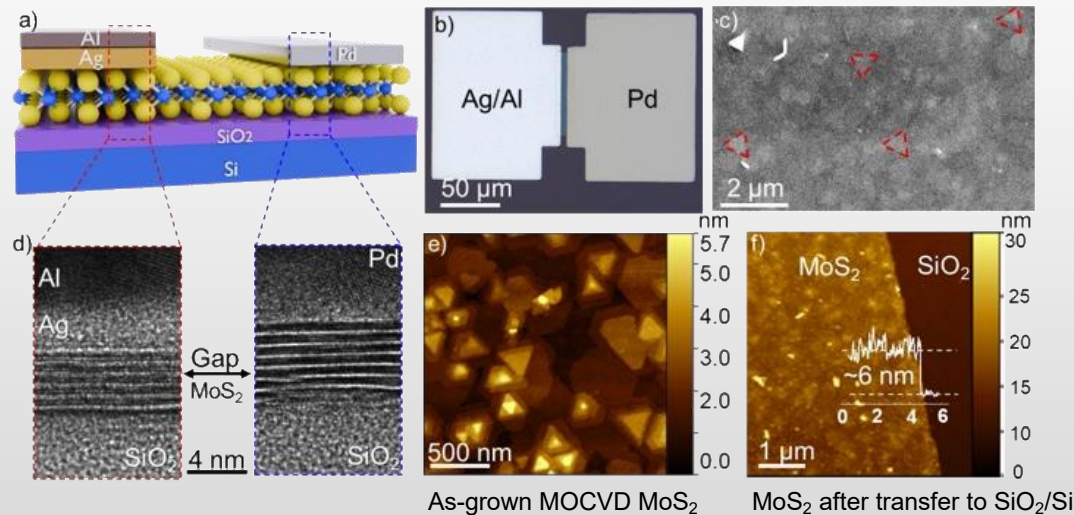
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Highlights



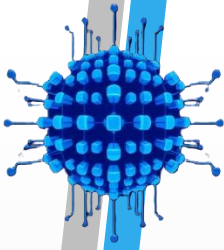
Ion Transport in lateral layered MoS₂



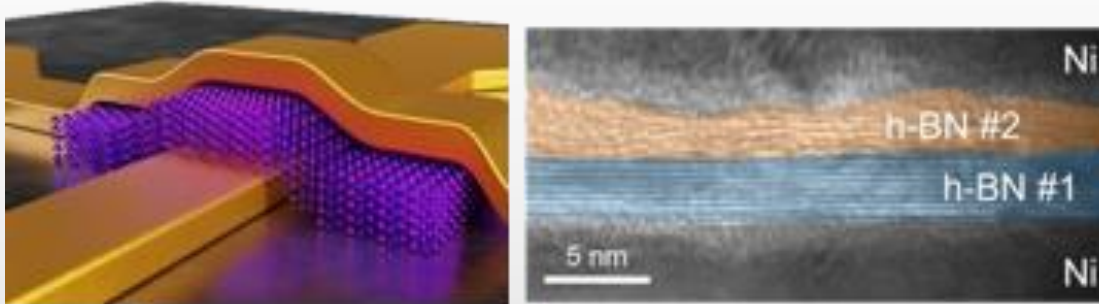
- Lateral Pd-MoS₂-Ag/Al memristors
- Variation of the gap size

- Forming-free operation for gaps < 2 μ m

Jimin Lee *et al.*, *IEEE EDTM 2025* (Poster WP-19)
Cruces *et al.*, *Small Science*, 2025

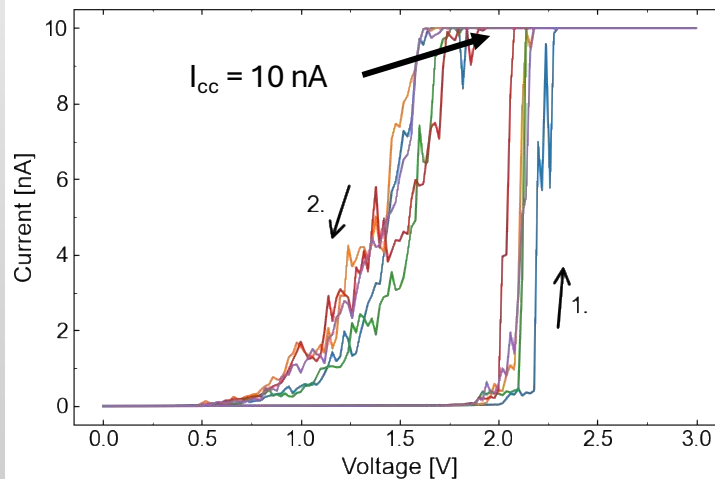


Threshold Resistive Switching in hexagonal Boron Nitride (h-BN)

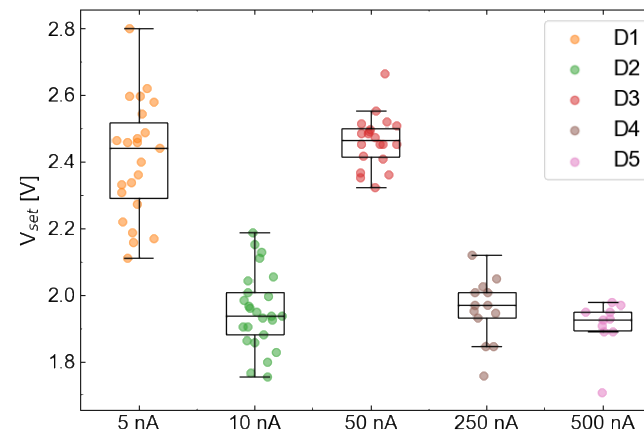


- Threshold RS with low currents in HRS
- DC endurance of ca. 600 cycles
- Mean $V_{\text{set}} = 1.96 \pm 0.10$ V

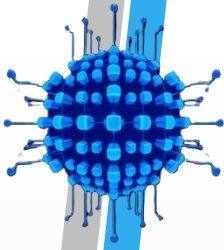
Threshold RS I-V curves



Device-to-device variability



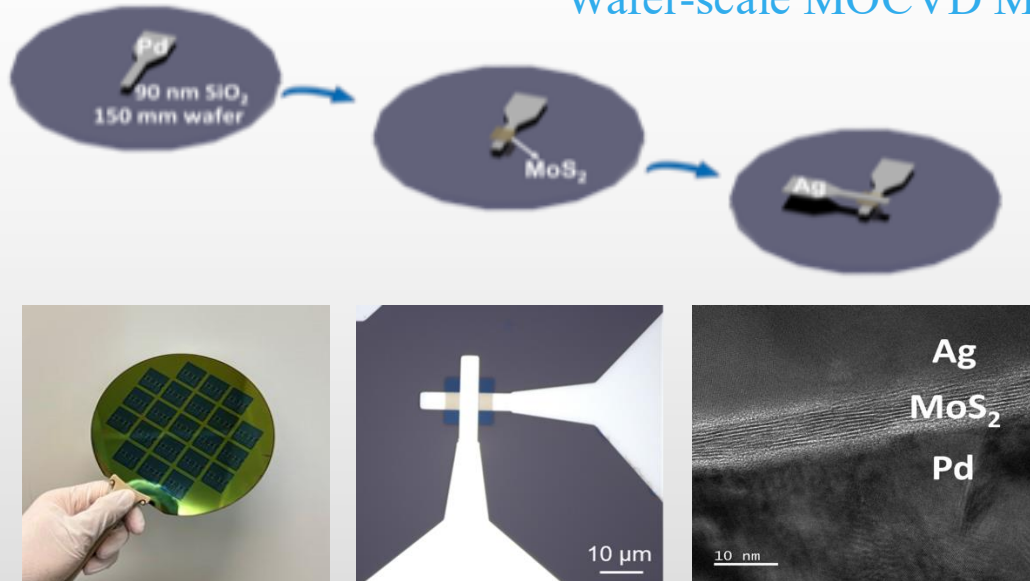
Völkel *et al.*, Adv. Funct. Mat. 2024
Völkel *et al.*, IEEE SNW, 2021



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Wafer-scale MOCVD MoS₂ Memristors

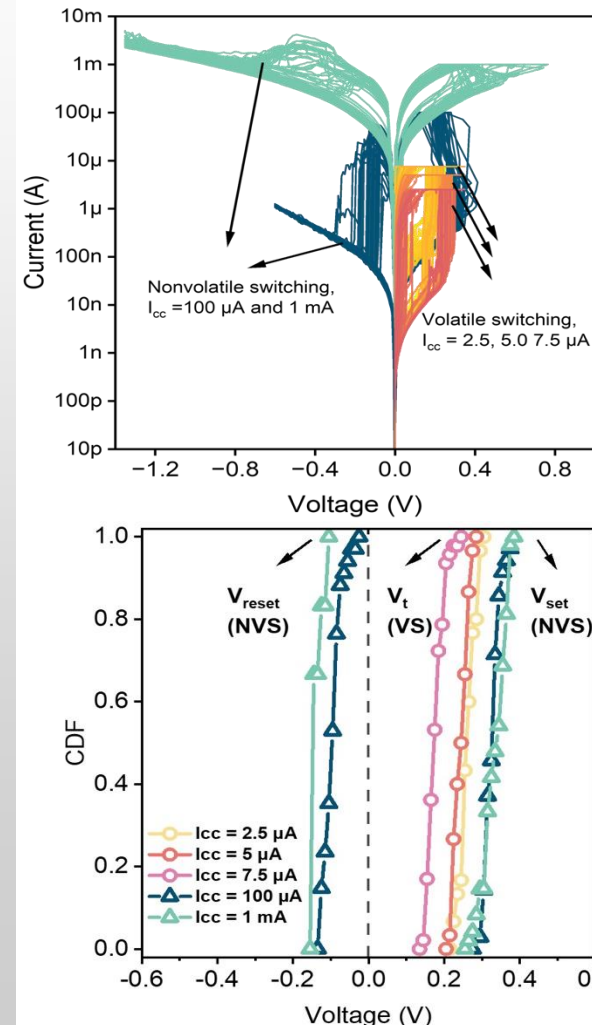


- Wafer-scale fabrication of MOCVD MoS₂-based memristors
- Back and top electrodes patterned via e-beam evaporator and lift-off
- Wet transferred MoS₂ patterned via RIE etching

Highlights



- Threshold and nonvolatile behavior depending on current compliance I_{CC}
- Two stable nonvolatile regimes
- Low voltage threshold, set and reset voltages within ± 1 V

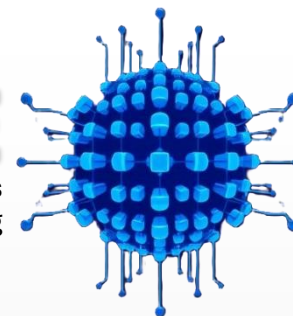


Fa *et al.*, MemriSys 2024



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Thank you



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