2025 International Semiconductor - June 16 2025, Jeju ICC

Researchers Forum

PROGRAM

| Purpose

· Semiconductors are vital to strategic sectors such as AI, quantum, and defense. To tackle high costs and complexity, international joint research is essential for reducing risks and driving sustainable innovation.

· Since the 2022 ROK-EU Digital Partnership, bilateral semiconductor R&D collaboration has expanded. This forum aims to share recent technology trends, present research outcomes, and explore future cooperation, including ROK-US collaboration and enhanced ties with the UK.

| Overview

Title	2025 International Semiconductor Researchers Forum
Date	June 16, 2025
Venue	Jeju International Convention Center (Jeju ICC)
Hosts	Ministry of Science and ICT(MSIT), National Research Foundation of Korea(NRF)
Organizers	KE-SRCC / KU-SRCC
Supporters	National NanoFab Center (NNFC)
Key Topics	· Presentations on international joint research outcomes and emerging technologie · Project-based presentations and networking sessions

| Forum Program

Pre-Forum

June 15, 2025

· Individual arrival and participation in GCIM2025 sessions*

* Note: Welcome Reception (6:00 PM at Ocean View Hall, 5F, Jeju ICC).

Main Forum

June 16, 2025

08:30~18:30

· Room 301, 3rd Floor, Jeju ICC

Post-Forum Activities

June 18, 2025

· National NanoFab Center(NNFC) Tour(June 18, 2025)

Main Forum (June 16, 2025)

Time	Program
08:30~09:00	Registration
Part 1	
09:00~09:10	Welcome Remarks Speaker **MSIT, Korea**
09:10~09:20	Congratulatory Speech Speaker **Rainer Wessely (EU Del. to RoK)**
09:20~09:30	International Collaboration Programs of Korea in Semiconductor R&D Speaker **Sang Wan Ryu (NRF)**
09:30~09:40	Horizon Europe Speaker **Ju Young Kim (EU Del. to RoK)**
09:40~09:55	The Chips Joint Undertaking and its role in the European semiconductor ecosystem Speaker **Jari Kinaret (Chips JU)**
09:55~10:05	ROK-EU SRCC Introduction Speaker **Seo Kyun Kim (KE-SRCC)**
10:05~10:20	Coffee Break
Part 2 (ROK-EU)	Chair: Francis Balestra
10:20~10:35	Current Progress in the Development of FeRAM-Based AI Accelerators Speaker **Dae Woong Kwon (Hanyang Univ.)**
10:35~10:50	Silicon compatible Hafnia-based ferroelectrics for neuromorphic computing technologies Speaker **Athanatos Dimoulas (NCSR Demokritos, GR)**
10:50~11:05	Neuromorphic Computing Systems for Heterogeneously-Integrated Silicon Photonics LiDAR Speaker **Jong Hyeok Yoon (DGIST)**
11:05~11:20	Neuromorphic Enhanced Heterogeneously Integrated FMCW LiDAR Speaker **Ruud Oldenbeuving (IMEC, NL)**
11:20~11:35	AI Compression and Hardware Acceleration for Edge AI Computing Speaker **Sung Ju Ryu (Sogang Univ.)**
11:35~11:50	EU-ROK collaborative project to enable energy efficient neuromorphic two-dimensional devices for edge computing Speaker **Dmitry Chigrin (AMO, DE)**
11:50~12:10	Development of AI Accelerators Leveraging Silicon Photonics Technology Speaker **Sang Yoon Han (DGIST)**
12:10~13:20	Lunch

Time	Program
Part 3 (ROK-EU)	Chair: Sang yoon Han
13:20~13:35	Pathfinding R&D to enable the transition from lab-to-fab Speaker **Inge Asselberghs (IMEC, BE)**
13:35~13:50	2D Semiconductor-Based Nanoelectronics: Advances in Materials, Processing, and Computing Speaker **Joon Ki Suh (UNIST)**
13:50~14:05	Power Device Speaker **Markus Pfeffe (Fraunhofer, DE)**
14:05~14:20	Sub-100 nm GaN HEMTs for W-band power amplifiier applications and beyond Speaker **Dae Hyun Kim (Kyungpook Nat'l Univ.)**
14:20~14:35	Heterogeneous integration for silicon photonics with micro-transfer printing Speaker **Emiel Dieussaert (GENT Univ., BE)**
14:35~14:50	Semiconductor epitaxy without chemical bonds on wafers for 3-dimensional vertical hetero-integration Speaker **Young Jun Hong (Sungkyunkwan Univ.)**
14:50~15:05	Horizon Europe ICOS (International Cooperation On Semiconductors) Speaker **Francis Balestra (Sinano Institute, FR)**
15:05~15:30	Coffee Break
Part 4 (ROK-US)	Chair: Young Jun Hong
15:30~15:40	ROK-US SRCC Introduction Speaker **Jie Hyun Lee (KU-SRCC)**
15:40~15:55	National Nanofab Center(NNFC) as a Service and Platform Technology Provider: Expanding International R&D Collaboration Speaker **Seok Jae Lee (NNFC)**
15:55~16:10	Secure and Probabilistic AI: Bayesian Neural Networks Enhanced by Gaussian Transistors Speaker **Ho Cheon Yoo (Hanyang Univ.)**
16:10~16:25	Particle Transfer-Based C4/Solder Ball Patterning for Vertically Integrated Array Implementation Speaker **Kang Il Seo (VEXAN Steel Co.)**
16:25~16:35	Coffee Break

Time	Program
Part 5 (ROK-UK)	
16:35~16:40	Welcome Remark
	Speaker **MSIT, Korea**
16:40~16:45	Congratulatory Speech
	Speaker **British Embassy Seoul**
16:45~17:00	To be Announced
	Speaker **Researcher from the UK**
17:00~17:15	Optically controlled polarization anisotropy in coupled quantum dots for single photon emission
	Speaker **Hee Dae Kim (Jeonbuk Nat'l Univ.)**
17:15~17:30	To be Announced
	Speaker **Researcher from the UK**
17:30~17:45	To be Announced
	Speaker **Researcher from the UK**
17:45~18:00	Realization of Blue-Emissive Perovskite Nanocrystals by Size Control and Post-Treatment of Short Ligand
	Speaker **Chang Lyoul Lee (GIST)**
18:00~18:15	To be Announced
	Speaker **Researcher from the UK**
18:15~18:30	To be Announced
	Speaker **Researcher from the UK**
Networking Reception & Dinner	

※ Poster presentations will be prepared for ROK-UK session.

Post-Forum Activities
National NanoFab Center (NNFC) Tour (June 18, 2025)

NNFC Tour Schedule(Draft)	
Time	Duration
09:25~10:35	Flight from Jeju to Cheongju(Individual reservation) * Jin Air(LJ402) : Depart at 9:25 AM, Arrive at 10:35 AM
11:00~12:00	Arrival at NNFC
12:00~13:00	Lunch
13:00~13:30	Opening Remarks by NNFC Director
13:30~15:00	NNFC Fab Tour
15:00~18:00	Transfer to Incheon Airport

※ Please note: Departure from Cheongju Airport to NNFC is scheduled for 11:00 AM.
Kindly reflect this in your individual flight reservation.

Part 1 Opening Session

• Welcome Remarks

| TBA

MSIT, REPUBLIC OF KOREA

• Congratulatory Speech

| Rainer Wessely

EU delegate to REPUBLIC OF KOREA

Dr. Rainer Wessely is a diplomat for the European Union. Since September 2024, he is posted as Digital and Research/Science Counsellor at the Delegation of the European Union to the Republic of Korea. From 2018 to 2024 he worked as Counsellor for Justice, Competition and Digital at the Delegation of the European Union to the United States in Washington, DC.Before this he served for four years as Assistant to Director General Johannes Laitenberger and Director General Alexander Italianer at DG Competition in Brussels. Rainer worked several years as a senior associate at Hogan Lovells and has conducted numerous cartel investigations, working in the Cartel Directorate of DG Competition for many years. He holds a PhD in international trade law and an LLM in European and international law.

• International Collaboration Programs of Korea in Semiconductor R&D

Semiconductor is one of the strongest industries in Korea. As the industry has grown, we have developed our R&D activities in both basic science and advanced production technologies. At present, we are seeking closer international R&D cooperation to catch up with the ongoing internalization of the semiconductor chip manufacturing process. In this regard, the Korean governments have established Korea-EU and Korea-NSF(US) programs on advanced semiconductor chip, processing, and packaging technologies. In addition, we have announced a call for Korean researchers to propose international collaborative research projects on semiconductors, open to counterparts from all countries. We believe that our efforts to promote multinational collaborative research will lead to a stronger bond between countries in the semiconductor chip production network.

| Sang Wan Ryu

National Research Foundation of Korea, REPUBLIC OF KOREA

Dr. Sang Wan Ryu is Director of the Division of Semiconductor & Display Technology at the National Research Foundation of Korea (NRF). He holds B.S., M.S., and Ph.D. degrees in physics from Seoul National University, with his doctoral work focusing on strained InGaAs(P)/InP materials and their application in optical communication laser diodes. Prior to joining NRF, he served as Professor of Physics at Chonnam National University since 2004 and worked as a Senior Researcher at ETRI. He also held a post as Research Associate at the University of Southern California. His expertise spans semiconductor materials, optoelectronic devices, and display technologies

• Horizon Europe

| Ju Young Kim

EU delegate to REPUBLIC OF KOREA

Ms. Ju Young KIM has been working for the EU Delegation to the Republic of Korea as a Policy Officer in Science, Technology, and Innovation since 2014. As a Korean agent of the Directorate-General Research & Innovation of the European Commission, she is in charge of the entire EU-RoK cooperation in science, technology, research, innovation, digital, and higher education at the Delegation.

Before joining the EU Delegation, she worked for the National Research Foundation of Korea (NRF) from 2008 to 2014. At the NRF, she dealt with international cooperation activities across nations and programmes, including the USA, China, Japan, and the EU. In particular, she supported the EU-RoK science and technology policies by coordinating several policy projects such as KONNECT, KESTCAP, KORRIDOR, and KORANET under the EU Research & Innovation Framework Programme 7 (EU FP7).

She holds a Bachelor's Degree in English from the Hanguk University of Foreign Studies and a Master's in International conference management from the University of Westminster, London, United Kingdom.

• The Chips Joint Undertaking and its role in the European semiconductor ecosyste

| Jari Kinaret

Chips JU, BELGIUM

Dr. Jari Kinaret was born in Finland and holds M.Sc. degrees in Theoretical Physics and Electrical Engineering from the University of Oulu in 1986 and 1987, respectively, and a Ph.D. in Physics from the Massachusetts Institute of Technology (MIT) in 1992. Prof. Kinaret has worked in various roles at research institutes and universities in Copenhagen, Denmark, and Gothenburg, Sweden.

From 2013 to 2023, he served as the Director of the Graphene Flagship, a one-billion-euro research project dedicated to exploring the potential of graphene. In October 2023, Prof. Jari Kinaret assumed the role of Executive Director at Chips Joint Undertaking(Chips JU), a European public-private partnership that supports research, development, innovation, and future manufacturing capacities in the European semiconductor ecosystem.

• ROK-EU SRCC Introduction

| Seo Gyun Kim

KE-SRCC / KFIA, REPUBLIC OF KOREA & BELGIUM

Dr. Seo Gyun Kim is the Director of the Korea-EU Semiconductor Collaboration Center (KE-SRCC) in Brussels and serves as Secretary General of the Korea Fabless Industry Association (KFIA). He also holds the role of Executive Director at the Korea System Semiconductor Cooperative Association. Prior to these roles, he was Executive Vice President and Head of R&D at Tmaxsoft Group and served nearly two decades at the Korea Evaluation Institute of Industrial Technology (KEIT) as Principal Research Fellow. He received his B.S., M.S., and Ph.D. degrees in Electronics Engineering from Chonnam National University. His career has focused on fostering global R&D collaboration, semiconductor industry policy, and innovation strategy.

Part 2 (ROK-EU) Joint Research Presentation 1

(Chair: Francis Balestra)

• Current Progress in the Development of FeRAM-Based AI Accelerators

This research project aims to address the growing demand for transformer-based AI models by leveraging FeRAM arrays based on 1T-nC (or 1T-nF) structured ferroelectric capacitors developed by our team. Key device characteristics such as latency, on/off ratio, and energy consumption, along with peripheral circuit parameters, are incorporated into a system-level architectural exploration platform. The goal is to improve performance and energy efficiency when running Vision Transformers using FeRAM arrays. In contrast to previous CIM (Compute-In-Memory) studies, this project applies more complex datasets (e.g., CIFAR-10, ImageNet) to enable accuracy and energy efficiency analysis at a commercialization-ready level. This progress report outlines the ongoing joint research efforts between Korea and the EU to achieve these goals.

| Dae Woong Kwon

Hanyang University, REPUBLIC OF KOREA

Dr. Dae Woong Kwon is an Associate Professor in the Department of Electrical Engineering at Hanyang University. He received his B.S. in Semiconductor Engineering from Kwangwoon University and M.S. and Ph.D. degrees in Electrical Engineering from Seoul National University, where his doctoral research focused on low-power tunneling FET biosensors for multiplexed sensing. His career includes academic roles at Inha University and postdoctoral research at UC Berkeley. He also has extensive industry experience as a senior engineer at Samsung Electronics and Intel's NVM Solutions Group. His expertise lies in neuromorphic devices, biosensors, and oxide semiconductor device technologies.

• Silicon compatible Hafnia-based ferroelectrics for neuromorphic computing technologies

An overview of the Si-compatible Hafnia-based ferroelectric technology will be presented emphasizing its importance for energy efficient in-memory and bioinspired neuromorphic computing. The pioneering contributions to the field by European and Korean institutions will also be reviewed. Subsequently, the Korea-EU joint project ViTFOX will be presented. In brief, the project targets the design and fabrication of the main components of a Vision Transformer, namely a Compute-in Memory demonstrator, a circuit level simulator and a hardware-software cooptimization platform with ferroelectric oxides. The platform will support two types of emerging memories, highdensity 3D FeRAM developed in Korea and epitaxial Ferroelectric Tunnel Junctions developed in EU, which will be presented in more detail.

| Athanasios Dimoulas

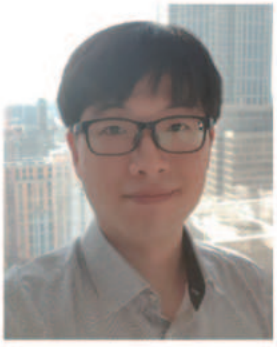
NCSR Demokritos, Athens, GREECE

Dr. Athanasios Dimoulas is Research Director at the National Center for Scientific Research DEMOKRITOS in Athens, Greece. He received his Ph.D. in Applied Physics from the University of Crete in 1991, with a dissertation on the MBE growth and thermal strain of GaAs on silicon. He has held prestigious international research positions, including Chair of Excellence at CEA/University of Grenoble-Alpes, visiting scientist at IBM Zurich, and research roles at CALTECH, University of Maryland, and University of Groningen. His expertise lies in advanced semiconductor materials and epitaxial growth technologies. Currently, he leads key research initiatives at NCSR Demokritos focusing on next-generation electronic materials and devices.

• Neuromorphic Computing Systems for Heterogeneously-Integrated Silicon Photonics LiDAR

Autonomous vehicles, encompassing unmanned aerial vehicles (UAVs) and unmanned aerial mobility (UAMs), necessitate robust object detection methodologies to facilitate reliable navigation systems. While Time-of-Flight (ToF) LiDAR modules are extensively utilized for object detection in autonomous vehicles, they encounter substantial limitations, including elevated costs, restricted detection angles, and susceptibility to interference from external light sources. Conversely, Frequency-Modulated Continuous Wave (FMCW) solid-state LiDAR modules offer broader detection angles, resilience to interference, and the capability to measure the velocity of nearby objects, rendering them a superior alternative.

In this presentation, I will introduce the KR-EU collaborative project to develop neuromorphic computing systems for heterogeneously-integrated silicon photonics LiDAR. Notably, I will emphasize the role of the Korean consortium, which comprises the following features: 1) The development of FeFET-based compute-in-memory (CIM) accelerators for energy-efficient processing, 2) The design of optimized AI network architectures tailored for real-time semantic segmentation tasks, and 3) The creation of wireline/wireless peripheral circuits to facilitate seamless intra- and inter-agent communication.



| Jong Hyeok Yoon

DGIST, REPUBLIC OF KOREA

Dr. Jong Hyeok Yoon is an Associate Professor in the Department of Electrical Engineering and Computer Science (EECS) at DGIST. He received his B.S., M.S., and Ph.D. degrees in Electrical Engineering from KAIST, graduating summa cum laude. His doctoral research focused on multi-standard Ethernet transceiver ICs with fully channel-independent operation. He previously conducted postdoctoral research at the Georgia Institute of Technology and has held faculty positions at DGIST since 2021. His work centers on high-speed integrated circuits and energy-efficient communication systems

• NEHIL: Neuromorphic Enhanced Heterogeneously Integrated FMCW LiDAR

With self-driving cars quickly emerging as commercial commodity, there is no doubt anymore: autonomous driving vehicles will be the future. This requires 3D sensing of the environment in high resolution, high speed and high accuracy, using complementary and/or redundant measurement methods. Fusing techniques such as radio detection and ranging (RADAR), light detection and ranging (LiDAR) and camera images, seems obvious to achieve this goal. However, the sheer amount of data generated by all of these techniques requires a significant advancement in Neuromorphic edge-computing (in more popular words: Artificial Intelligence), next generation frequency modulated continuous wave (FMCW) LiDAR on low-cost, low power consuming and light weight photonic integrated circuitry (PIC), that can beam-steer and detect without any moving parts, and the integration of electronic integrated circuits (EIC) to drive and read-out and combine all signals.

In the NEHIL project, Korean and European researchers (both academic and industrial) aim to combine Neuromorphic edge-computing with data from a PIC-based FMCW LiDAR using FeFET-based compute-in-memory (CIM) accelerators, to support hybrid SNN/ANN models for semantic segmentation. These systems aim to reduce power consumption and improve the efficiency of the LiDAR system and can be used in autonomous vehicles and other applications. The integration of CIM, neuromorphic computing, FMCW LiDAR and photonic reservoir computing technologies will enable high-resolution, low-power, and cost-effective solutions for real-time data processing and object recognition.

| Ruud Oldenbeuving

IMEC, Netherlands

Dr. Ruud Oldenbeuving is a Scientific Leader at imec with over 20 years of experience in laser development and more than 15 years in photonic integrated circuits (PICs). He was the first to design and realize a hybrid ultra-narrow linewidth laser combining InP and SiN, now an industry standard. Recognized as one of the Photonics 100 (2025)by Electro Optics, he is a thought leader consulted by global institutions. He has co-authored 80+ papers and holds multiple patents. Before imec, he worked at LioniX International and its spin-offs for 13 years.

• AI Compression and Hardware Acceleration for Edge AI Computing

In this presentation, Energize team will introduce research on AI compression and hardware acceleration methods for Edge AI computing. The presenter explains a selective skipping algorithm for model compression and a high-throughput network scheme to maximize the com puting speed on multi-PE arrays.

| Sung Ju Ryu

Sogang University, REPUBLIC OF KOREA

Dr. Sung Ju Ryu is an Assistant Professor in the Department of Electrical and Electronic Engineering at Sogang University. He earned his Ph.D. in Creative IT Engineering from POSTECH in 2021 and holds a B.S. in Electrical Engineering from Pusan National University. Before joining Sogang University, he served as Assistant Professor at Soongsil University and worked as a Staff Researcher at the Samsung Advanced Institute of Technology. His research interests include AI acceleration, edge computing, and system-level hardware design for efficient intelligence.

• ENERGIZE - EU-ROK collaborative project to enable energy efficient neuromorphic two-dimensional devices for edge computing

The ENERGIZE project aims to develop energy-efficient neuromorphic hardware based on wafer-scale two-dimensional materials (2DMs) for next-generation edge AI applications. By integrating innovations across the semiconductor value chain – from material synthesis and device fabrication to circuit design and system-level integration – ENERGIZE addresses the limitations of conventional CMOS technologies in meeting the power and performance requirements of modern artificial intelligence. The project focuses on 2DM-based two- and three-terminal memristive devices that support inmemory computing and biologically inspired synaptic behaviour. This presentation will highlight the interdisciplinary approach of ENERGIZE, which brings together leading European and Korean institutions in materials science, electronics, computer science and engineering. We will give an overview of the project's objectives and report on our recent progress.

| Dmitry Chigrin

AMO GmbH / RWTH Aachen University, GERMANY

Dr. Dmitry Chigrin is currently Scientific Adviser at AMO GmbH and Adjunct Professor (Privatdozent) at the Department of Physics, RWTH Aachen University. He received his Doctorate in Electrical Engineering from the University of Wuppertal in 2004, and completed his habilitation in Theoretical Physics at Friedrich-Schiller-University Jena in 2014 with research on plasmonic nano- and micro-structures. He previously served as Senior Researcher and Group Leader at RWTH Aachen University and led a research group at the University of Wuppertal. His work focuses on nanophotonics, plasmonics, and advanced electromagnetic structures, bridging theory and device-level applications.

• Development of AI Accelerators Leveraging Silicon Photonics Technology

The acceleration and energy efficiency of AI computation have emerged as key challenges in the design of next-generation computing systems. In this presentation, I will introduce research on photonic circuit-based AI accelerators, which integrate silicon photonics, IIIV compound semiconductors, and MEMS technologies as an alternative to overcome the limitations of electronic circuits in terms of computational density, power consumption, and thermal constraints.

| Sang Yoon Han

(DGIST, REPUBLIC OF KOREA

Dr. Sang Yoon Han is an Associate Professor in the Departments of Robotics & Mechatronics Engineering and Semiconductor Engineering at DGIST. He received his Ph.D. in Electrical Engineering and Computer Sciences from the University of California, Berkeley, and earned his B.S. in Electrical Engineering from Seoul National University, graduating summa cum laude. Prior to joining DGIST, he served as a postdoctoral researcher at KAIST, where he fulfilled Korea's mandatory military service through academic research. His research interests include silicon photonics, integrated systems for AI acceleration, and next-generation semiconductor technologies.

Part 3 (ROK-EU) Joint Research Presentation 2

(Chair: Sang yoon Han)

• Pathfinding R&D to enable the transition from lab-to-fab

Research results and project outcomes published in literature offer valuable insights which can drive future technologies. A key question is how to translate and verify these findings in an industry relevant fabrication environment. R&D Pilot line projects aim to bridge the gap between lab and industry. This report presents the approach followed by the 2D-PL and NanoIC pilot lines.

| Inge Asselberghs

IMEC, BELGIUM

Dr. Inge Asselberghs is Senior Manager at imec. She received the M.Sc. and Ph.D. degrees in chemistry from the University of Leuven, Leuven, Belgium. After a Post-Doctoral Fellowship in nonlinear optics, she joined imec in 2011, specializing in 2D-materials processing, device fabrication, and characterization. Her research interest covers new materials, process set-up, and integration pathfinding from the laboratory scale to fab infrastructure. Currently, she is the coordinator of the 2D-Pilot line and the NanoIC pilot line project.

• 2D Semiconductor-Based Nanoelectronics: Advances in Materials, Processing, and Computing

'Modern information technology accelerated data processing and storage, and scaled up their capacity since the introduction of integrated circuitry in the 1960s. Upon the technology-nodedriven miniaturization, we have witnessed that electronic device structure began to deviate from planar geometry and evolved into three-dimensional space, e.g., trigate FinFET and VNAND for better electrostatic control and massive data storage, respectively.

Following such device structural renovation, this talk will highlight how an emerging class of semiconductors, atomically-thin semiconductors, can be synergistically embedded to function as logic and nonvolatile memory operations in the More-Moore as well as in the More-than Moore domains. More importantly, as an integrated solution, I will introduce vapor-phase deposition (ALD and MOCVD) and a set of nanofabrication strategy tailored for target chalcogenide semiconductors and 3D device geometry. To be specific, I will initially address how our team approach to explore and solve fundamental scientific and engineering challenges in 3D adaptive MOCVD growth of 2D semiconductors and eventually monolithic integration of 2D vertical FETs in the complex device geometries.

Our recent works of hybrid-dual-gated electrochemical and multi-junction tunneling logic transistors will be followed to demonstrate field-controlled bimodal and steep-slope lowpower switching, respectively. In particular, the latter is enabled by phase-centric synthetic strategies where we achieve wafer-scale production of tin selenides (SnSe and SnSe2) in the 2D limit by utilizing a low-temperature MOCVD process. Next, I will present the wafer-scale growth of monoelemental 2D tellurium (Te) thin films using an annealing-free, low-temperature ALD process. As-deposited Te films exhibit exceptional homogeneity, precise layer controllability, and 100 % step coverage in high aspect ratio nanostructures.

Additionally, we showcase an ALD-Te-based selector device with fast switching time, selectivity and low Vth. Capable of low-temperature processing, I will conclude with the latest research progress toward BEOL-compatible neuromorphic hardware, all based on synthetic chalcogenide thin films.

| Joon Ki Suh

UNIST, REPUBLIC OF KOREA

Dr. Joon Ki Suh is an Associate Professor at the Department of Materials Science and Technology and the Graduate School of Semiconductor Materials and Devices Engineering at UNIST. He received his Ph.D. in Materials Science and Engineering from the University of California, Berkeley, and holds an M.S. from Stanford University and a B.S. from Yonsei University. Prior to his academic appointment, he conducted postdoctoral research at the University of Chicago and Cornell University. His research focuses on 2D materials, nanoelectronics, and semiconductor device integration, contributing to the advancement of nextgeneration semiconductor materials and fabrication technologies.

• Power Devices

The talk will present recent research activities of Fraunhofer IISB on Silicon Carbide (SiC) MOSFETs and provide an outlook on novel ultra-wide bandgap materials, such as Aluminum Nitride (AlN). Reducing resistive components is a primary measure for improving power switches. Recent architectural approaches toward low-resistivity SiC devices, including 3-dimensional channel arrangements and super-junction structures for high-blocking voltage and low-resistivity drift regions, will be discussed. The presentation will conclude with an outlook on material properties and related device architectures from an RTO perspective.

| Markus Pfeffer

Fraunhofer, GERMANY

Dr. Markus Pfeffer holds a diploma in Electrical Engineering and a PhD (Dr.-Ing.) with specialization in manufacturing optimization both from the University of Erlangen-Nuremberg. Since 2002 he has been working at Fraunhofer IISB in the Business Department Semiconductor Technology, where he is the fab manager of the Fraunhofer IISB Pi-Fab (SiC Processing and Prototype Fabrication) and he is in charge of quality and process control as well as founded research. He was/is involved in several national and international cooperative R&D projects in different functions.

• Sub-100 nm GaN HEMTs for W-band power amplifiier applications and beyond

GaN HEMTs have emerged as a key technology for high frequency and power applications due to their superior material properties such as extemely high 2-DEG concentration (n2-DEG) and breakdown field intensity [1-3]. One of the key challenges to achieve ultra high-frequency characteristics is a strict control of short-channel effects (SCEs), which considerably deteriorates the maximum oscillation frequency (fmax). This talk will summarize recent progress at KNU in our quest to map out the potential of AlxGa1-xN/GaN quantum-well (QW) HEMTs for W-band power-amplifier (PA) applications. In this talk, we report sub-100 nm Al0.4Ga0.6N/GaN HEMTs with a thin barrier design, yielding fmax = 490 GHz and BVDS = 30 V. To the best of our knowlegement, this is the first demonstration of GaN HEMTs that possess fmax > 400 GHz and BVDS > 30 V simultaneously.

| Dae Hyun Kim

Kyungpook National University, REPUBLIC OF KOREA

Dr. Dae Hyun Kim is a Professor at the School of Electronic and Electrical Engineering, Kyungpook National University. He holds a B.S. in Electronics Engineering from Kyungpook National University and earned his M.S. and Ph.D. degrees in Electrical Engineering from Seoul National University. His doctoral research focused on the fabrication and characterization of InGaAs/InAlAs nano HEMTs for high-speed integrated circuits. Prior to his current academic role, he held senior research positions at SEMATECH, Teledyne Scientific Company, and MIT, and served as a Postdoctoral Research Associate at Seoul National University. His expertise includes compound semiconductor devices, high-frequency MMICs, and advanced IC fabrication.

• Heterogeneous integration for silicon photonics with micro-transfer printing

Next-generation photonic integrated circuits require the heterogeneous integration of key components that cannot be readily realized in a CMOS environment, such as III-V semiconductor optical amplifiers and lasers, efficient electro-optic modulators, and optical isolators. Silicon and silicon nitride photonic platforms offer scalability and costeffectiveness but lack essential active functionalities. Micro-transfer printing provides a scalable, high-precision method to integrate these diverse materials and devices, enabling compact, high-performance photonic circuits. In this talk, we discuss the principles of micro-transfer printing, its advantages over conventional integration techniques, and its role in advancing applications in telecommunications, data centers, LiDAR, biomedical sensing, and quantum technologies.

| Emiel Dieussaert

Ghent University & IMEC, BELGIUM

In 2019, Emiel graduated from the Master in Engineering Physics at Ghent University. In his final Master year, he got introduced to world of integrated photonics and for his Master thesis he worked on onchip Raman spectroscopy at the Photonics Research Group with Prof. Roel Baets. After graduation, he decided to continue to work on sensing applications enabled by integrated photonics and he started his PhD in 2020 on silicon photonics-based Laser Doppler Vibrometry for non-contact photoacoustics at the Photonics Research Group of Ghent University and IMEC. This work has led to multiple journal publications and a patent. As from 2024, Emiel started working as business developer for the micro-transfer printing activities at Ghent-University and IMEC. Together with prof. Gunther Roelkens, he leads the business activities of Transverse, the wafer scale pilot line for micro-transfer printing. This pilot line supports companies worldwide in establishing micro-transfer printing as a key technique for advanced integration.

• Semiconductor epitaxy without chemical bonds onwafers for 3-dimensional vertical hetero-integration

"Epitaxy is a key technique for fabricating single-crystalline thin films on substrates via strong chemical bonding. These covalent bonds extend the crystal symmetry and orientation of the underlying wafer into the epitaxial layer, enabling high-performance semiconductor devices. However, the very nature of these strong bonds makes it difficult to separate the epitaxial layer from the substrate. Given that the epitaxial layer is typically only a few microns thick—compared to several hundred microns for the wafer—the substrate becomes a substantial waste of material and space in high-density microelectronic architectures. Moreover, while epitaxy excels in forming high-quality semiconductors, it poses challenges for heterogeneous integration, which is critical for multifunctional device systems.

In this talk, we introduce novel epitaxial growth strategies that avoid covalent bonding at the interface—namely, van der Waals epitaxy and remote epitaxy.

These methods offer promising pathways for the high-density integration of diverse semiconductor devices. As a demonstration, we present an ultrahigh-resolution full-color display based on a vertically stacked R/G/B pixel architecture.

Using non-covalent epitaxy, we grew red, green, and blue light-emitting diode (LED) epilayers that were subsequently delaminated from their native wafers via simple mechanical exfoliation.

These freestanding LED layers were then vertically stacked and patterned via photolithography to form pixel arrays. As a result, we achieved full-color displays with a pixel density of 5,100 pixels per inch (ppi). Additionally, we highlight the advantage of remote epitaxy in obtaining excellent crystal quality of the grown layers, further emphasizing its potential in advanced semiconductor integration.

| Young Joon Hong

Sungkyunkwan University, REPUBLIC OF KOREA

Dr. Young Joon Hong is a Professor in the Department of Nano Engineering and the Department of Display Engineering at Sungkyunkwan University, where he is also affiliated with the SKKU Advanced Institute of Nanotechnology. He earned his Ph.D. in Materials Science and Engineering from POSTECH and his B.S. from Korea University. Prior to joining SKKU, he served as a Professor at Sejong University for over a decade and worked as a Research Associate at the Research Center for Integrated Quantum Electronics at Hokkaido University in Japan. His research interests include 3D hetero-integration, advanced nanomaterials, and semiconductor display technologies.

• Horizon Europe ICOS (International Cooperation On Semiconductors)

This presentation will deal with the Horizon Europe ICOS project dedicated to International Cooperation On Semiconductors. International cooperation is key for speeding up technological innovation, reducing cost by avoiding duplicated research, boosting the resilience of the semiconductor value and supply chains, and is one of the objectives of the EU Chips Act. The objectives and first important ICOS results will be highlighted, including the analysis of the semiconductor economic and technological landscapes in Europe and leading semiconductor Countries, the identification of important technological areas for potential cooperation and the proposition of opportunities for bilateral or multilateral research collaborations, particularly in the areas of advanced functionalities and computing

| Francis Balestra

CROMA, France

Dr. Francis Balestra, CNRS Research Director at CROMA, is Director Emeritus of the European SiNANO Institute and President of IEEE Electron Device Society France, and has been Director of several Research labs. He coordinated many European Projects (ICOS, NEREID, NANOFUNCTION, NANOSIL, etc.) that have represented unprecedented collaborations in Europe in the field of Nanoelectronics. He founded and organized many international Conferences, and has co-authored more than 500 publications. He is member of several European Scientific Councils, of the Advisory Committees of International Journals and of the IRDS (International Roadmap for Devices and Systems) International Roadmap Committee as representative of Europe.

Part 4 - (ROK-US)

(Chair: Young Jun Hong)

• Introduction: Korea-US Semiconductor R&D Cooperation Center

The Korea-U.S. Semiconductor R&D Cooperation Center (KU-SRCC) was established as a strategic platform to advance collaborative research in the semiconductor sector between Korea and the United States. KU-SRCC facilitates joint R&D initiatives supported by the National Research Foundation of Korea (NRF), and fosters networking and exchanges among researchers and experts by strengthening partnerships across government, academia, and industry. By accelerating the development of advanced semiconductor technologies—including chip design, processing, and packaging, KUSRCC aims to enhance supply chain resilience and contribute to global technological collaboration.

| Jie Hyun Lee

ETRI US Center, USA / ETRI, REPUBLIC OF KOREA

Dr. Jie Hyun Lee is the General Director of the ETRI US Center in San Jose, California, and a Principal Researcher at the Electronics and Telecommunications Research Institute (ETRI) in Korea. She has been with ETRI since 2004 and previously served as a Visiting Researcher at Paderborn University in Germany. She received his Ph.D. in Electronics and Computer Engineering from Chungnam National University, where she worked on wavelength reuse schemes for RSOA-based WDM access networks. She also holds an M.S. in Electrical Engineering from KAIST, with research focused on ultrafast all-optical switching and wavelength conversion using nonlinear photonic waveguides. Her current research interests include advanced optical communication systems, WDM-PON architectures, and international R&D collaboration.

• National Nanofab Center (NNFC) as a Service and Platform Technology Provider

- Expanding International R&D Collaboration -

National NanoFab Center (NNFC) is the leading public organization providing semiconductor technology services in South Korea. Our mission is to offer technology platform services to industry, academia, and R&D institutes in the fields of silicon-based semiconductors, MEMS, bio-healthcare, metrology, and nano new materials.

Established in 2004 as an affiliated organization of the Korea Advanced Institute of Science and Technology (KAIST), NNFC has been committed to supporting domestic and international industries, academic institutions, and research organizations through its world-class infrastructure, based on 200 mm and 300 mm fabrication equipment.

To contribute to future technological advancements, NNFC actively collaborates with both domestic and international academia and research institutions to develop key technology platforms, including semiconductor-based solid-state batteries, nano-medical devices and silicon quantum device platforms.

Finally, NNFC continues to expand the shared use of its infrastructure with global partners, aiming to strengthen support for technology convergence and commercialization across its service domains.

| Seok Jae Lee

NNFC, REPUBLIC OF KOREA

Dr. Seok Jae Lee is currently Executive Vice President and Principal Researcher in the Division of Nano Convergence Technology Development at the National NanoFab Center (NNFC), South Korea. He received his Ph.D. in Chemical and Biomolecular Engineering from KAIST in 2004. His current research focuses on the development of semiconductor-based nanomedical, biosensor and biochip technologies. He has co-authored over 100 journal publications and holds more than 120 patents. He has received numerous national awards for his research achievements and has served as a committee member of NANO Korea, Korea BioChip Society.

• Secure and Probabilistic AI: Bayesian Neural Networks Enhanced by Gaussian Transistors

Gaussian distributions are fundamental to probabilistic models, yet their hardware realization remains elusive. Existing solutions based on heterojunction anti-ambipolar transistors suffer from structural asymmetry, inconsistent transport properties, and limited tunability. Here, we introduce a single-material, single-channel split-gate Gaussianmirroring transistor (SC-SMT) that generates highly symmetric, near-Gaussian transfer curves under reversal gate biasing. Independent gate control enables precise tuning of amplitude, mean, and standard deviation, achieving >99.99% cosine similarity with ideal Gaussian profiles. To validate functionality, we integrated the SC-SMT onto a printed circuit board with real-time current sensing and DAC-based gate control.

This system implements an analog Gaussian Naive Bayes classifier, distinguishing deepfake from authentic voices with 82% accuracy on the ASVspoof2019 dataset. Further, the device exhibits quadratic-order output scaling with dual-gate input, supporting analog vector-vector multiplication. We demonstrate its use in a memristor crossbar array for transformer attention scoring, eliminating the need for matrix projection.

These results establish the SC-SMT as a compact, tunable hardware primitive for realtime probabilistic inference and neuromorphic acceleration.

| Ho Cheon Yoo

Hanyang University, REPUBLIC OF KOREA

Dr. Ho Cheon Yoo is an Associate Professor in the Department of Electronic Engineering at Hanyang University. He earned his Ph.D. in IT Engineering from POSTECH, with a dissertation on split-gate ambipolar transistors, and holds a B.S. in Electronic Engineering from Hanyang University. Before joining Hanyang University in 2025, he served as Assistant and then Associate Professor at Gachon University. He also conducted postdoctoral research at Northwestern University and was a visiting researcher at Holst Centre in the Netherlands. His research spans emerging transistors, optoelectronic devices, AI hardware, security electronics, and advanced semiconductor packaging. He has received multiple honors including the Excellence in Research Award(Gachon University, 2022-2024), Researcher of the Month(2021), and the Korea Semiconductor Scholarship(KISA / Lam Research, 2013).

• Particle Transfer-Based Solder Ball Patterning for Vertically Integrated Array Implementation

The development of via-hole-less interconnection technology is important for the successful implementation of vertical integration technology of semiconductor devices, and this interconnection technology requires the introduction of micro-bump conductive ball array technology into RDL technology.

The research team of VEXAN Steel Co., Ltd. is developing this micro-bump conductive ball array bonding technology using micro-particle alignment and transfer technology.

In particular, the development of bump materials and bump formation technology according to the miniaturization of bump size is essential for the development of 3D packaging technology, and the micro-bump array technology of this research team is pursuing a 10μm pitch in the future, so it is considered to be suitable as a bonding solution for the next generation of 3D packaging.

| Kang Il Seo

VEXAN STEEL Co., Ltd., REPUBLIC OF KOREA

Dr. Kang Il Seo is Chief Technology Officer (CTO) at VEXAN STEEL Co., Ltd. He previously served as CTO at CLAP Co., Ltd., and CEO of WELLMER Co., Ltd. His industrial career spans over three decades, including senior R&D roles at 3M Korea and Samsung SDI.He holds a Ph.D. and M.S. in Chemical Engineering from KAIST, and a B.S. from Yonsei University. His doctoral research focused on the synthesis and electrical properties of PEDOT/PSSA conducting polymer complexes. His expertise includes advanced materials, polymer electronics, and corporate innovation leadership in the semiconductor and chemical industries.

Part 5 - (ROK-UK)

(Chair: Youngjun Hong)

• Optically controlled polarization anisotropy in coupled quantum dots for single photon emission

Recent advances in droplet epitaxy (DE) methods have enable the growth of diverse nanostructures including coupled quantum dots (CQDs). CQDs are regarded as crucial building block for the development of scalable quantum devices, as the coupling between adjacent quantum dots can be controlled both electrically and optically [1-4]. In such systems, the tunneling interaction is typically much weaker in laterally coupled QDs compared to vertically coupled ones, where wavefunction overlap is more likely to occur. Although tunneling-induced coupling is negligible due to the relatively large inter-dot distance in laterally configurations, excitons localized in the individual QDs can still interact through dipole-dipole coupling.

This dipole-dipole interaction is primarily mediated by two mecahnisms: Forster energy transfer (FRET) and the direct Coulomb interaction. Both mechanisms exhibit a ~1/R12 dependence on the inter-dot distance (~R12), yet their effectiveness is highly sensitive to the spatial configuration of the excitonic dipoles, particularly their orientation and charge distribution. Our findings suggest that excitons and biexctions in laterally coupled QDs exhibit controllable polarization properties, opening the possibility for tunable anisotropic emission through optical manipulation.

[1] K. M. Weiss et al., Phys. Rev. Lett. 109, 107401 (2012) / [2] P. M. Vora et al., Nat. Commun. 6, 7665 (2015)
[3] M. L. Kerfoot et al., Nat. Commun. 5, 3229 (2014) / [4] H. Thierschmann et al., Nat. Nanotechnol. 10, 854 (2015)

| Hee Dae Kim

Jeonbuk National University, REPUBLIC OF KOREA

Dr. Hee Dae Kim is an Associate Professor of Physics at Jeonbuk National University. He earned his Ph.D. in Physics from the University of Oxford and a B.Sc. in Physics from the University of Texas at Austin. He has held research and teaching positions at leading institutions including the University of Oxford (Research Associate/Lecturer), IFW-Dresden in Germany (Postdoctoral Researcher, independent position), Arizona State University (Research Professor), Hokkaido University in Japan (Assistant Professor), and Northeast Normal University in China (Distinguished Professor). He has also served as a Visiting Professor at Oxford. Research Interests: Optical spectroscopy of quantum dots, Surface plasmonbased photonic applications, Time-resolved quantum optical analysis

• Realization of Blue-Emissive Perovskite Nanocrystals by Size Control and Post-Treatment of Short Ligand

Halide perovskite nanocrystals (PNCs) have recently attracted lots of attention due to their excellent opto-electronic properties. Blue-emissive PNCs can be achieved via either size reduction or halide exchange. Low-temperature synthesis or ligand engineering is widely used to reduce the particle size of PNCs, leading to blue emission. However, these methods are limited by high defect density and broad FWHM, which causes low PLQY and structural degradation. In this work, the particle size of $CH_3NH_3PbBr_3$ NCs was reduced by controlling the interaction between ligands and anti-solvents with different dipole moments, enabling the fabrication of highly efficient blue-emissive PNCs. Additionally, halide exchange was employed to achieve blue-emitting PNCs, but high defect density was observed in the chlorine (Cl)-exchanged PNCs. To address this issue, a short ligand containing chlorine was applied, which suppressed defect formation and significantly improved the structural stability of the PNCs, resulting in blue emission at approximately 480 nm.

| Chang Lyoul Lee

GIST, REPUBLIC OF KOREA

Dr. Chang Lyoul Lee is the Head of the Advanced Photonics Research Institute (APRI) at the Gwangju Institute of Science and Technology (GIST), where he also serves as Director of R&D Coordination and a member of the Integrity Advisory Board. He received his Ph.D. in Materials Science and Engineering from GIST and has held visiting research positions at the University of Cambridge and Rice University. His research focuses on quantum dot-based optoelectronic devices, ultrafast optical spectroscopy, and organic/inorganic hybrid materials for light-emitting and photovoltaic applications. He has authored numerous high-impact publications and received multiple awards including the 2023 Distinguished Contribution to Science and Technology Award from the Ministry of Science and ICT.