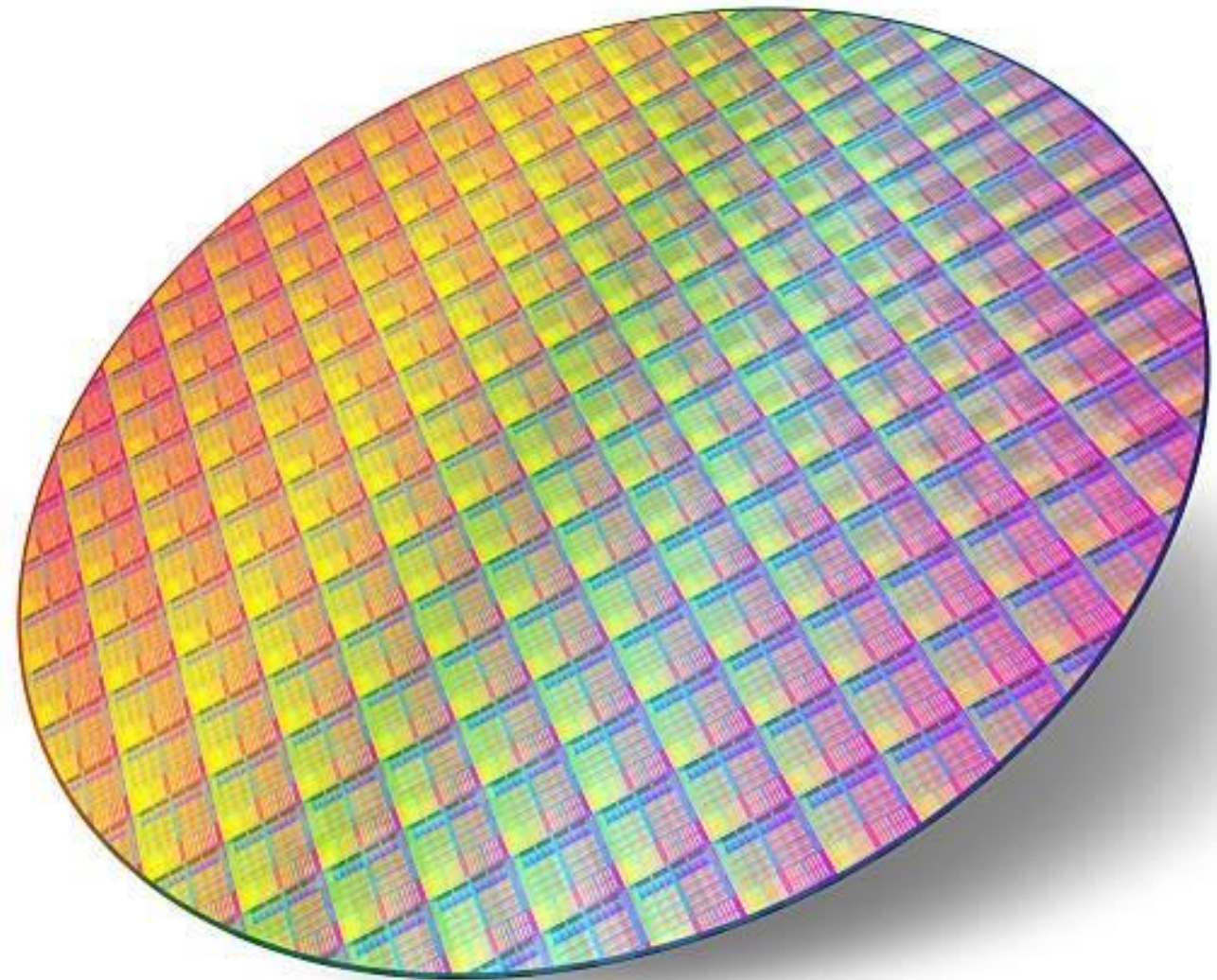




# Landscape of Indian Research and Development in Semiconductors

Sunita Verma,  
Group Co-ordinator, R&D Division,  
Ministry of Electronics and Information Technology,  
Government of India

# Catalyzing India's Electronics and Semiconductor Ecosystem



सत्यमेव जयते  
Ministry of Electronics  
& Information Technology  
Government of India



ELECTRONICS INDIA  
*Billion Needs Million Chips*



*Digital India*  
Power To Empower

# Vision for New India



Shri Narendra Modi  
Hon'ble Prime Minister of India

“

India is committed to become **world's reliable partner in global supply-chains**. This is the best time to invest in India.

”

“

India is making **policies keeping in mind the goals of next 25 years**. In this time period, the country has kept the goals of high growth and saturation of welfare and wellness.

”

‘State of World’ address World Economic Forum, 2022

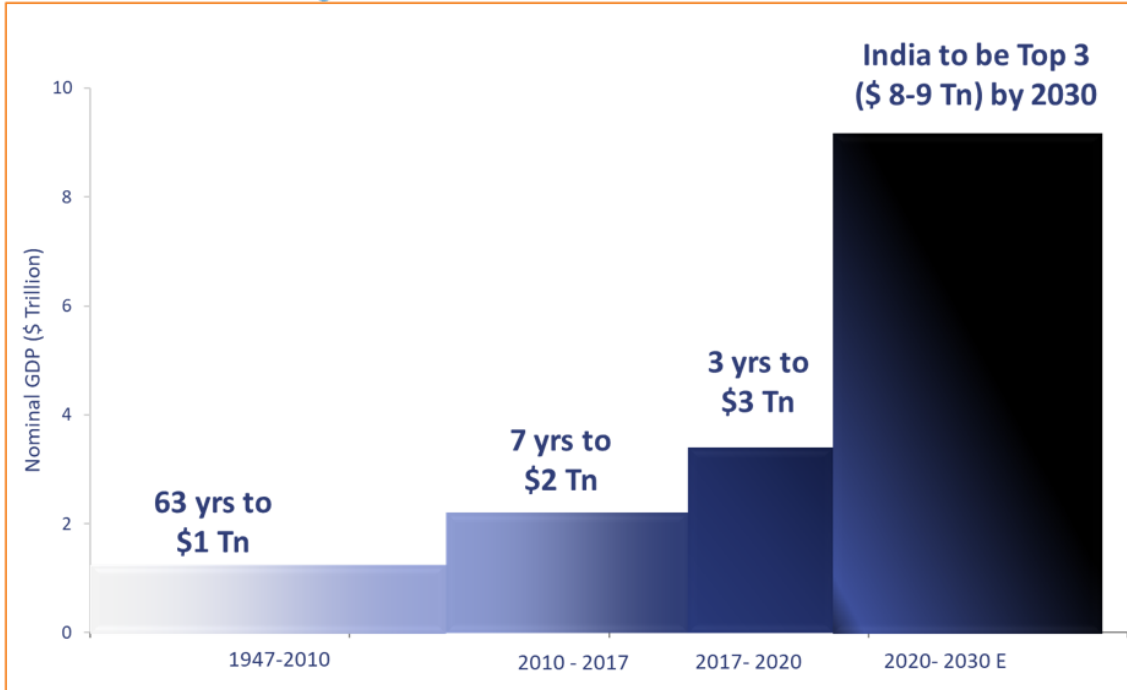
“

The role of the government should be like **“and gate”** instead of a **“not gate”**. While the industry works hard, **the government must work even harder**.

”

# World's 3<sup>rd</sup> Largest Economy by 2027\* - #IndiaTechade

1



2

### Advantage India

- #1 Fastest Growing G20 Economy
- #1 Global Fintech Adopter
- #2 Internet Users
- #3 Start-up Ecosystem

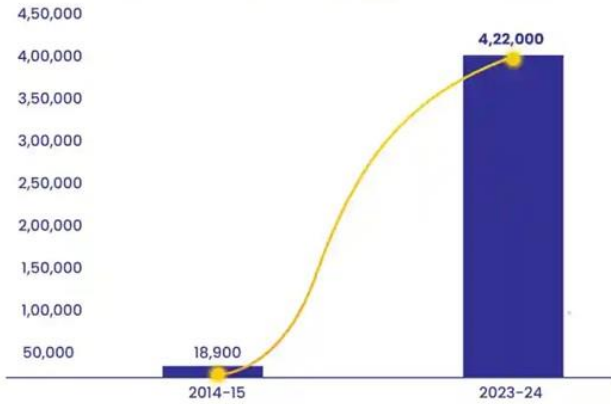


### Tech Start-up Ecosystem

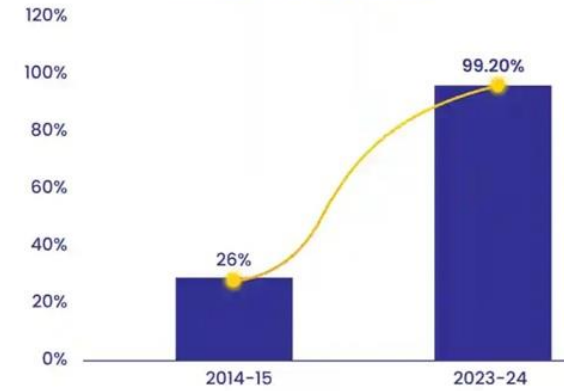
- >100,000 Registered Startups
- >25k Tech Startups
- >3000 leveraging deep tech including AI
- \$24 Bn+ Total equity investment received by Indian tech start-ups
- 115 Unicorns



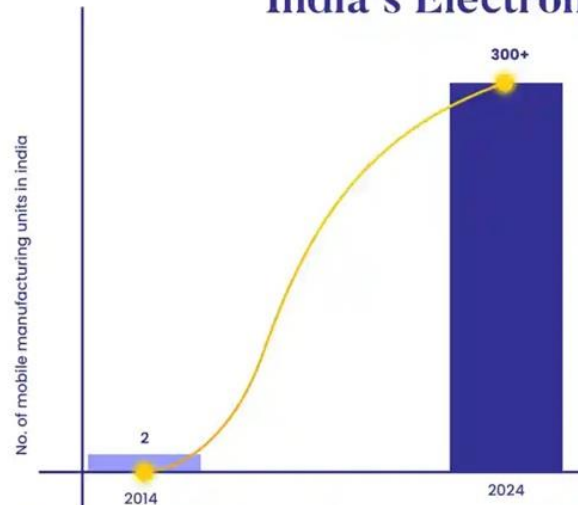
## Mobile Phone Manufacturing in India



## Made in India Mobile Phones Sold in India



## India's Electronics Manufacturing Boom



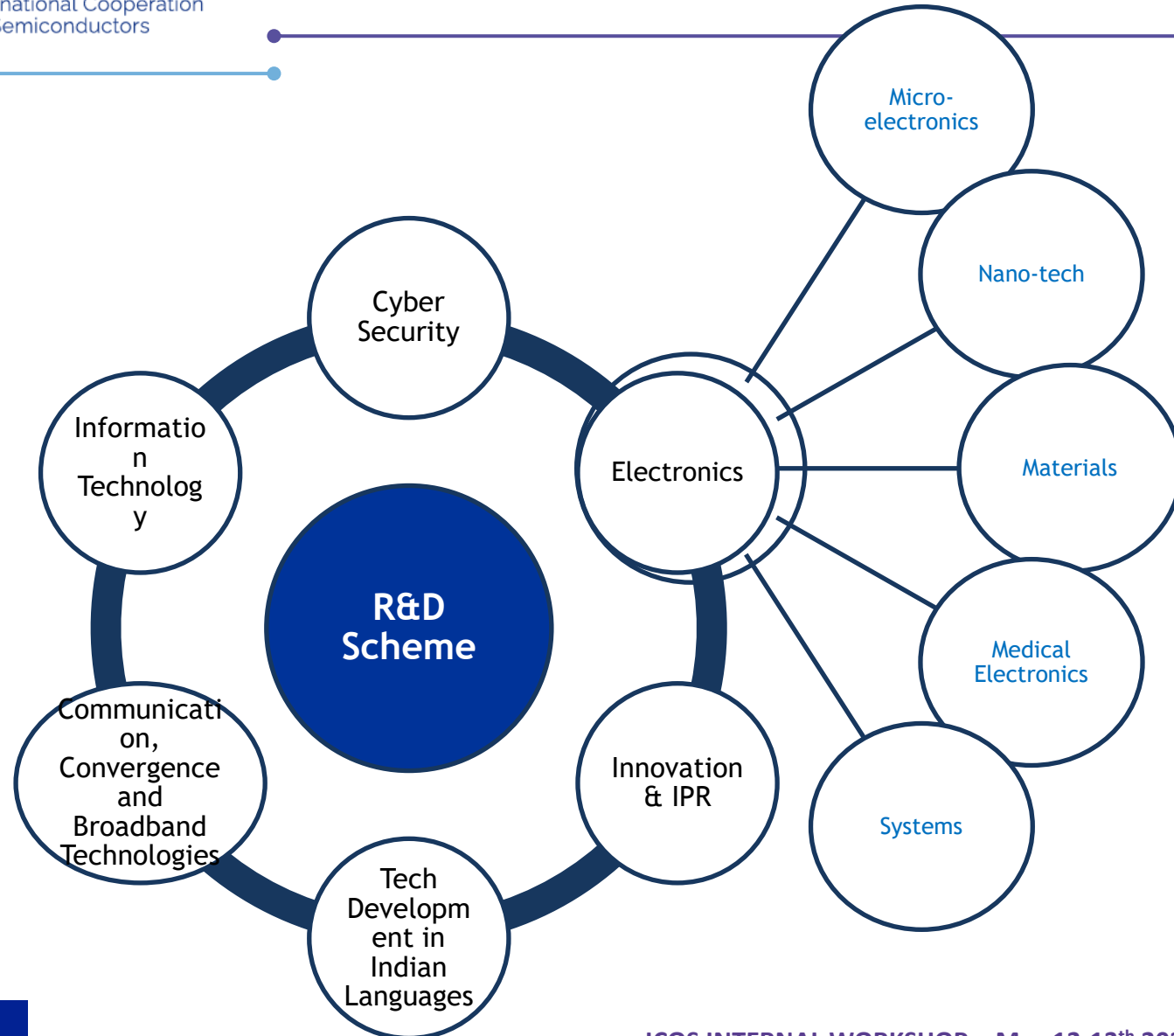
**325 million+**  
mobile phones being manufactured in India every year



**12 lakh** direct and indirect jobs created over the last decade

Source: PIB

# R&D at MeitY



The main objective is to:

- Create ecosystem for R&D
- Develop Indigenous technologies and IPs
- Generate skilled manpower
- Support startups

There are dedicated R&D societies like CDAC, C-MET, and SAMEER.

- Centres of Excellence have been established in the fields of
  - Semiconductors
  - ChipIn Centre
  - Nanoelectronics
  - Power Electronics
  - Artificial Intelligence
  - Photonics
  - Additive manufacturing
  - E-waste
  - Li-ion Batteries
  - Quantum Technologies
  - Cyber Security

The Ministry of Electronics and Information Technology (MeitY), Government of India, has established six Centers of Excellence (CoE) in Nanoelectronics across the country. These centers are part of MeitY's initiative to boost research and innovation in nanoelectronics, a key enabler for future technologies.



State of the art Centres of Excellence in Nanoelectronics established at various institutes

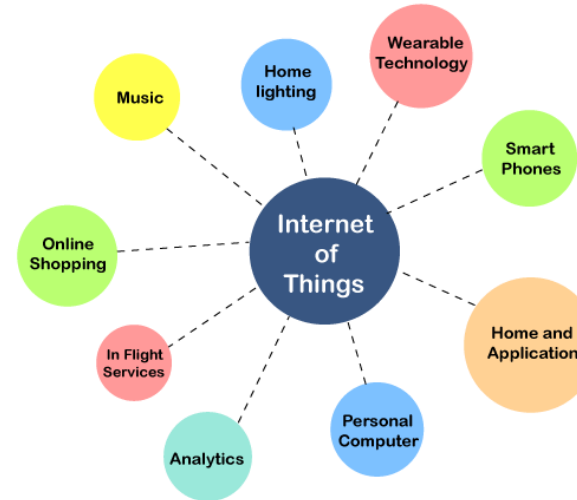
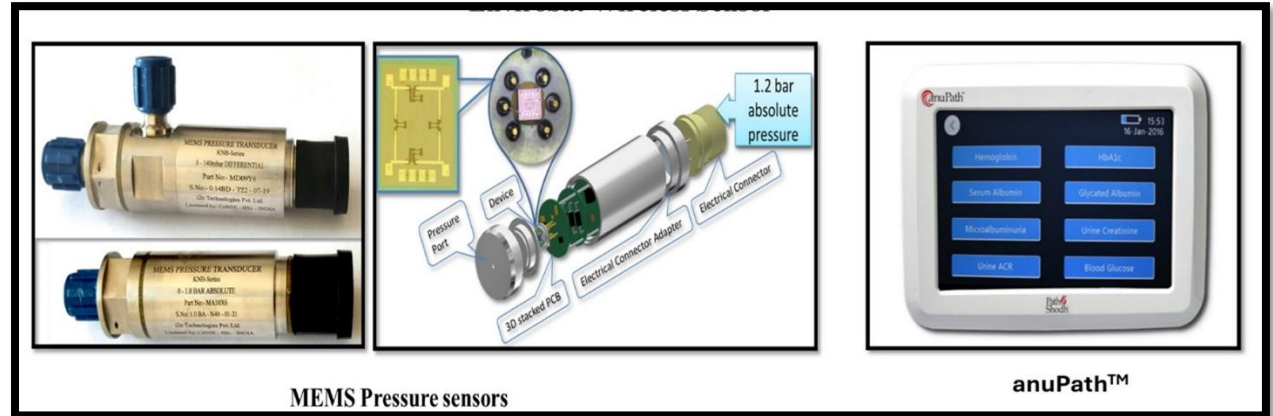
-  **IIT Delhi**
-  **IIT Bombay**
-  **IIT Kharagpur**
-  **IIT Guwahati**
-  **IIT Madras**
-  **IISc Bangalore**



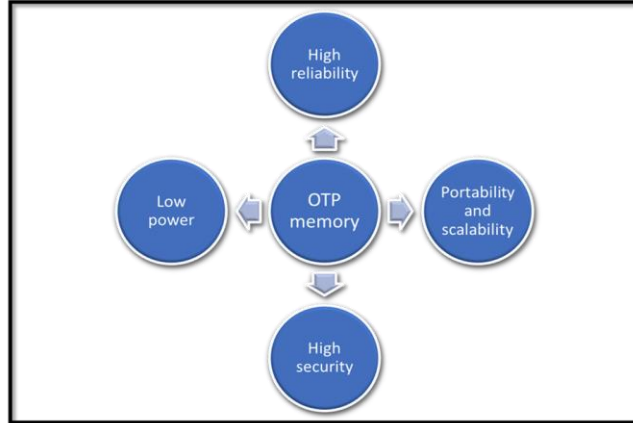
# IoT enabled MEMS Sensors

IoT enabled MEMS sensors for applications in various sectors:

- Healthcare
- Automotives
- Environmental Monitoring
- Safety and security



# Other developed technologies



OTP memory developed by IITB



1kW water cooled and 400W air cooled Fiber Lasers developed under Nnetra project



Flexible pouch type Li ion batteries and belt shaped Li-ion batteries for headphone and wrist watch developed by CMET



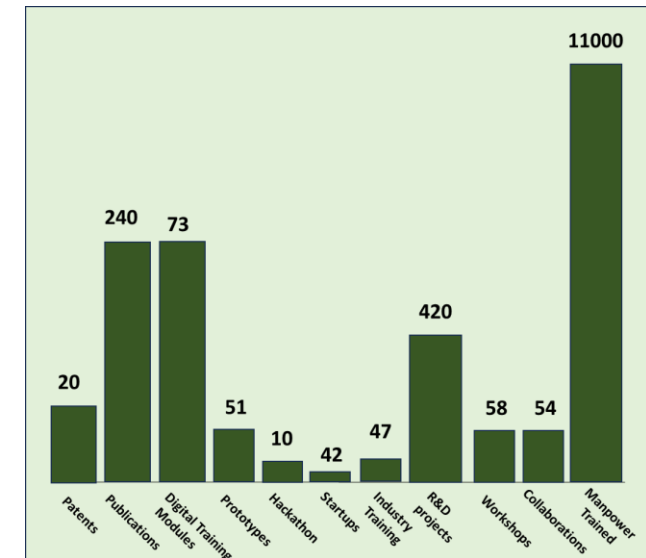
Air quality monitoring system deployed in Jayanagar & Hebbal- Bengaluru

- ❖ Launched in 2008
- ❖ Three phases: INUP-1 (2008-2014) , INUP-II (2014-2019) and INUP-i2i (2019-Present)
- ❖ At the CENs of IIT Bombay, IISc Bangalore, IIT Delhi, IIT Kharagpur, IIT Madras and IIT Guwahati



## Main objectives:

- To avail the cutting edge nanoelectronics facilities to researchers from academia, industry, and R&D labs
- Manpower skilling in the domain of nanoelectronics
- Mentorship of Tier-I and Tier-II academic institutions and startups



Major achievements under INUP-i2i

## Graphene centre in the country:

- **The India Innovation Centre for Graphene (IICG)** is a research center in Kerala that studies graphene and other 2D materials.
- **The India Graphene Engineering and Innovation Centre (IGEIC)** is a not-for-profit organization that aims to develop and commercialize graphene technology in India.
- **Centre for Materials for Electronics Technology (C-MET):** C-MET's R&D activities have been implemented in three laboratories i.e., Pune, Hyderabad and Thrissur.

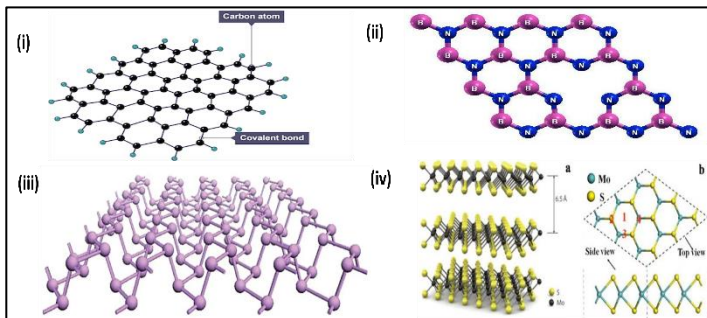
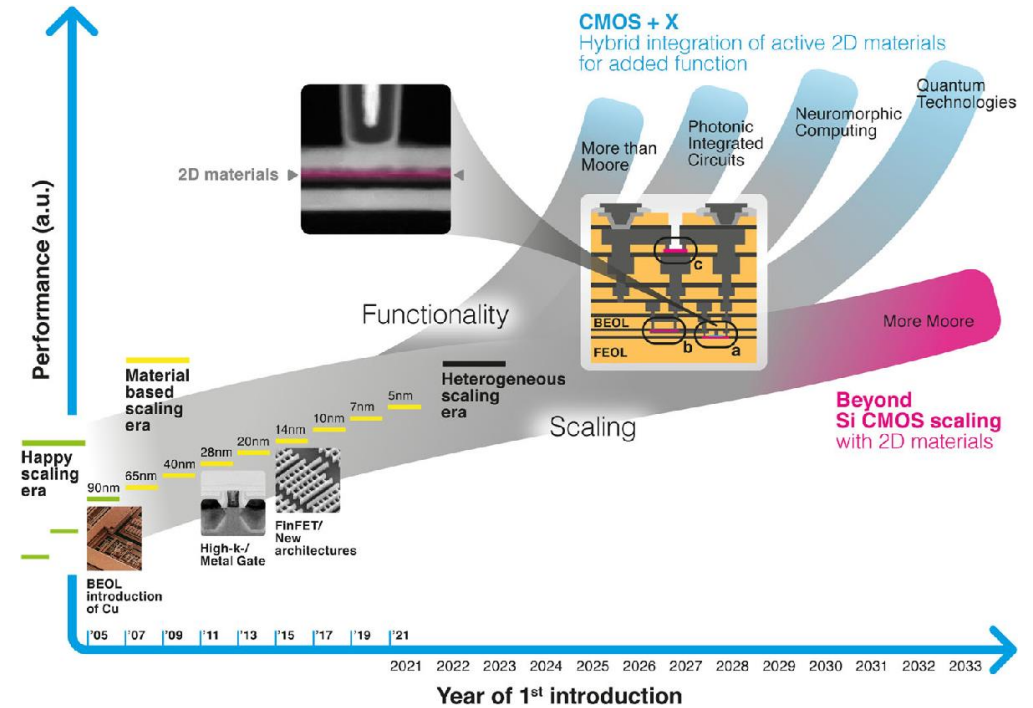


Figure. Structure of (i) Graphene (ii) h-BN (iii) Phosphorene and (iv) MoS<sub>2</sub> (Transition Metals Dichalcogenide)



**Figure:** The era of geometrical or Dennard scaling of silicon technology ended around the turn of the century (green lines, “happy scaling”)

# Neuromorphic Computing

Through the CoEs and infrastructure created, **research on neuromorphic computing**—which aims to mimic the architecture and functioning of the human brain using electronic systems—is being actively supported.

This includes:

- ❖ **Development of novel devices and materials for neuromorphic architectures.**
- ❖ **Circuit design and architecture for brain-inspired systems.**
- ❖ **AI hardware acceleration and energy-efficient computing.**

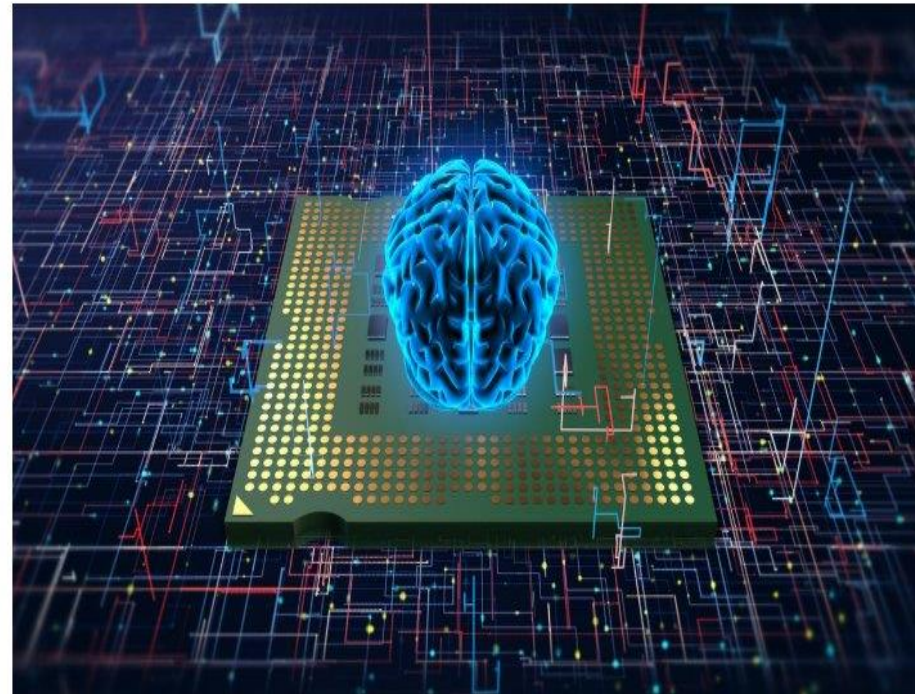


**IISc scientists develop brain-inspired analog computing platform capable of storing, processing data**



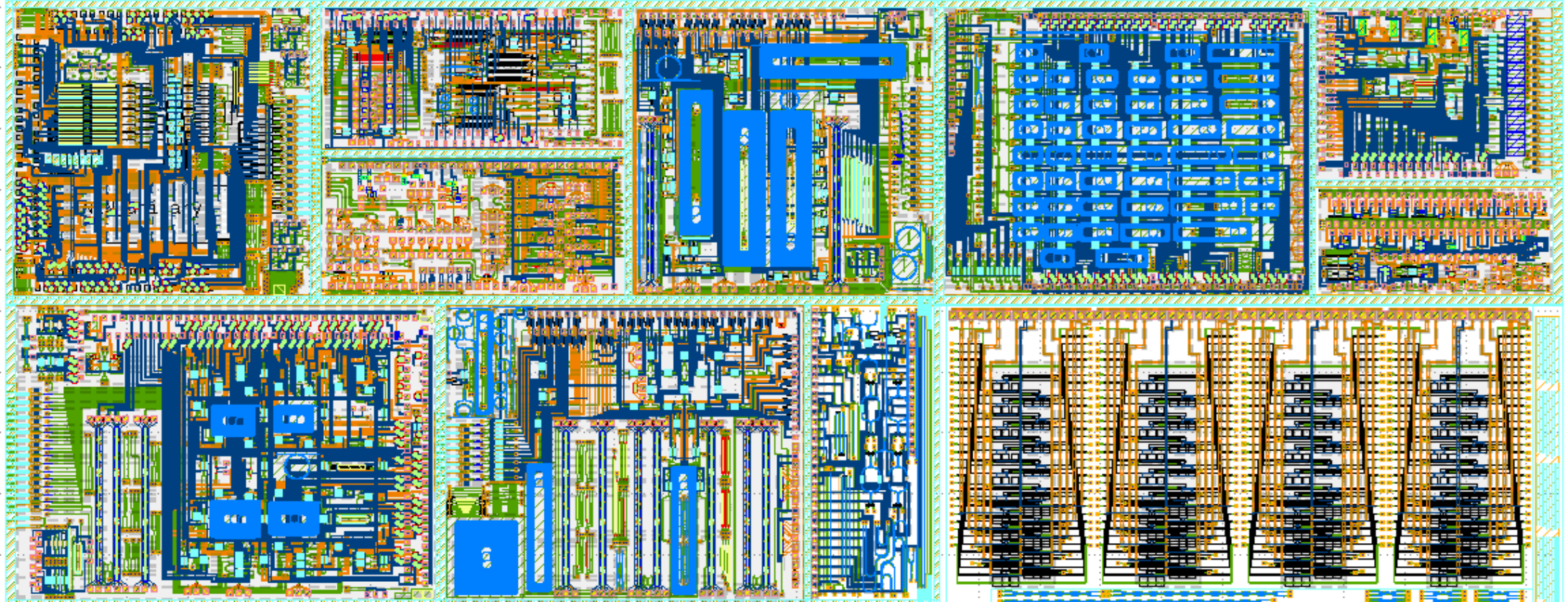
Updated - September 12, 2024 04:58 pm IST

PTI



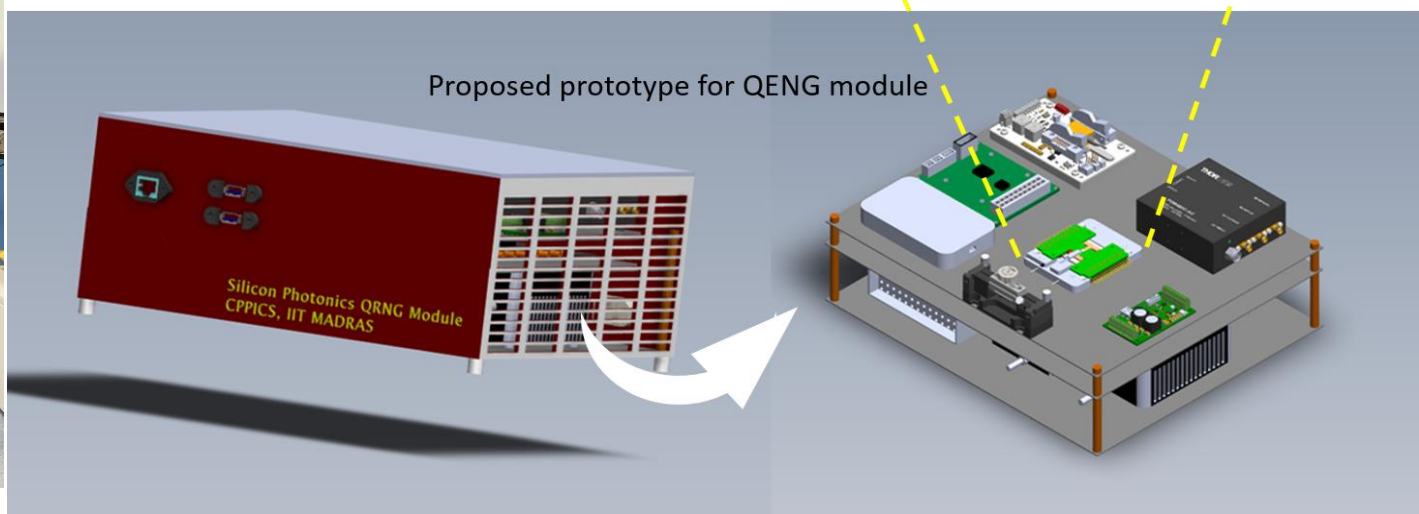
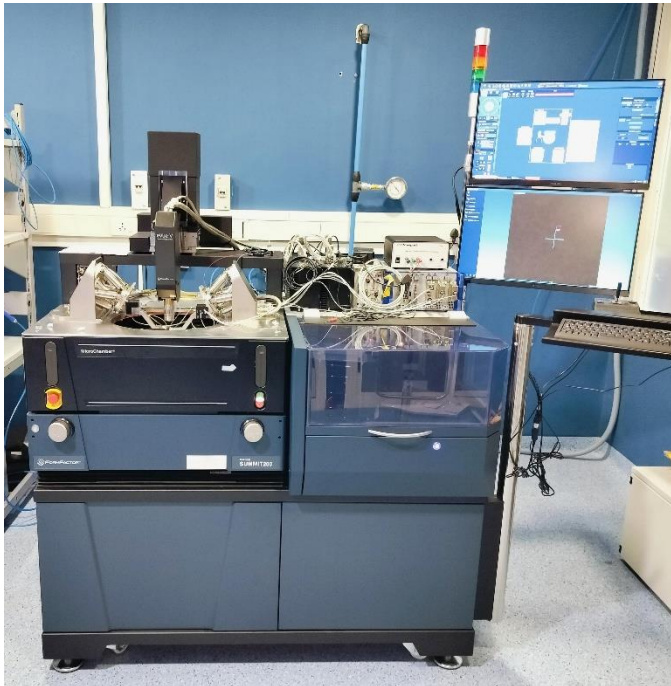
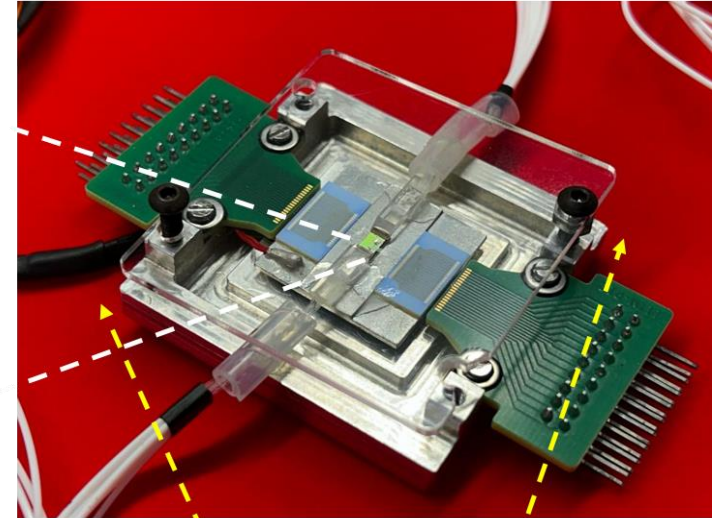
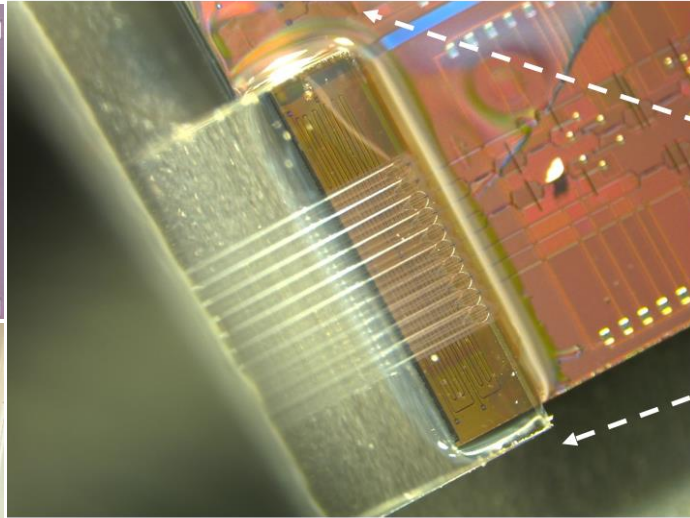
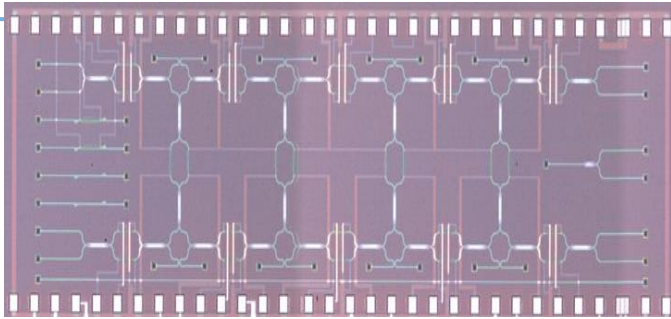
**Neuromorphic Molecular Computing: Nanomaterials to CMOS Chip to Enable AI on the Edge at IISc Bangalore**

Currently, major challenge we are trying to overcome is the fabrication of these memristor chip completely in India.



Various **programmable photonic integrated circuits** taped out for prototype development  
(Microwave Photonic Oscillator, Multiprotocol QKD Transceiver, Boson Sampling Processor) using our own  
propriety PDKs

# Technologies Developed Under CPPICS



MIL standard PIC packaging available

<b>Title</b>	Microprocessor Development Programme	
<b>Implementing Agencies</b>	C-DAC Trivandrum, IIT Madras and IIT Bombay	
<b>Objective</b>	Design, development and fabrication of a family of 32-bit/ 64-bit multi-core Open-source ISA based Microprocessors, reusable IP Cores and software tool-chain ecosystem	
<b>Outcomes</b>	C-DAC Trivandrum	Designed 32-bit/ 64-bit multi-core RISC-V ISA based <b>VEGA</b> Microprocessors and fabricated at 28nm-TSMC foundry, 130nm Silterra foundry and 180nm-SCL foundry
	IIT Madras	Designed 32-bit/ 64-bit multi-core RISC-V ISA based <b>SHAKTI</b> Microprocessors and fabricated at 22nm-Intel foundry and 180nm-SCL foundry
	IIT Bombay	Designed 32-bit/ 64-bit multi-core SPARC ISA based <b>AJIT</b> Microprocessors and fabricated at 180nm-SCL foundry

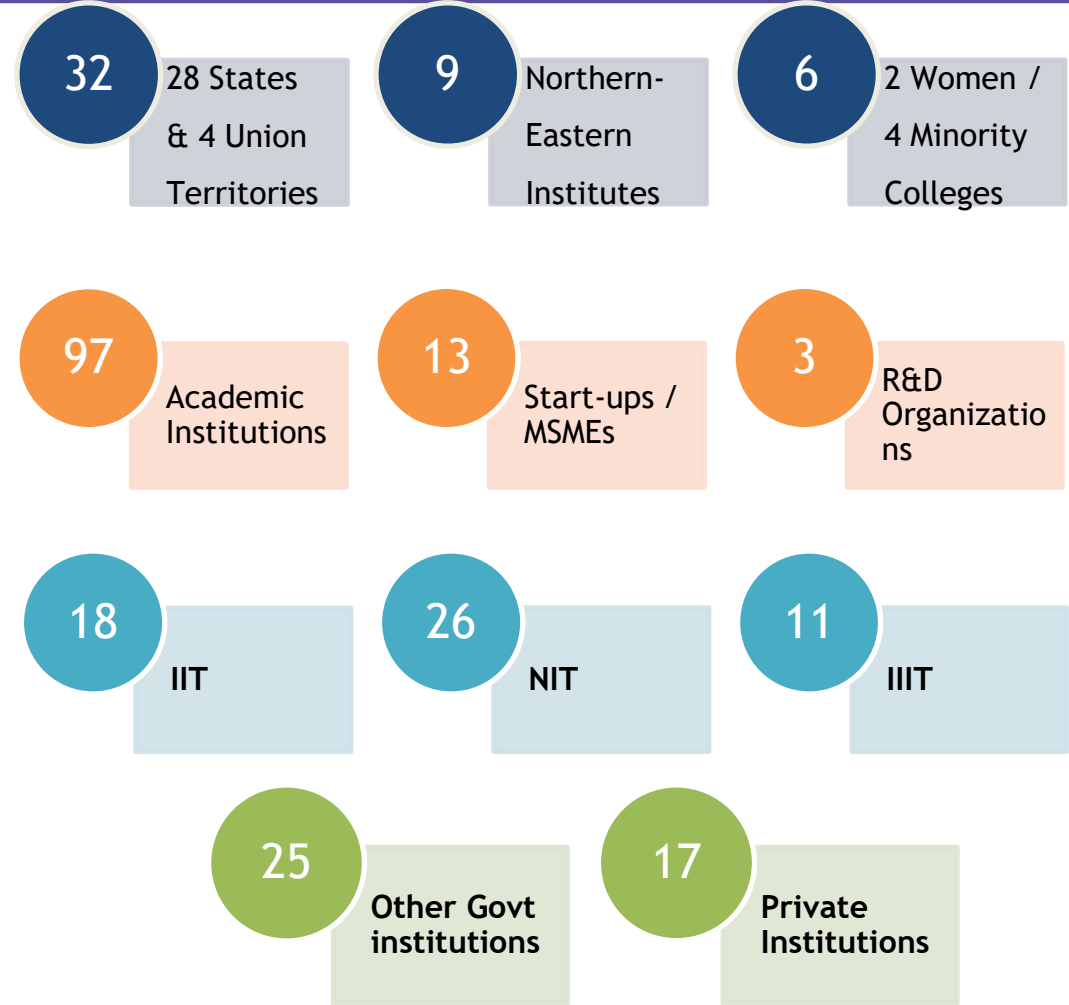
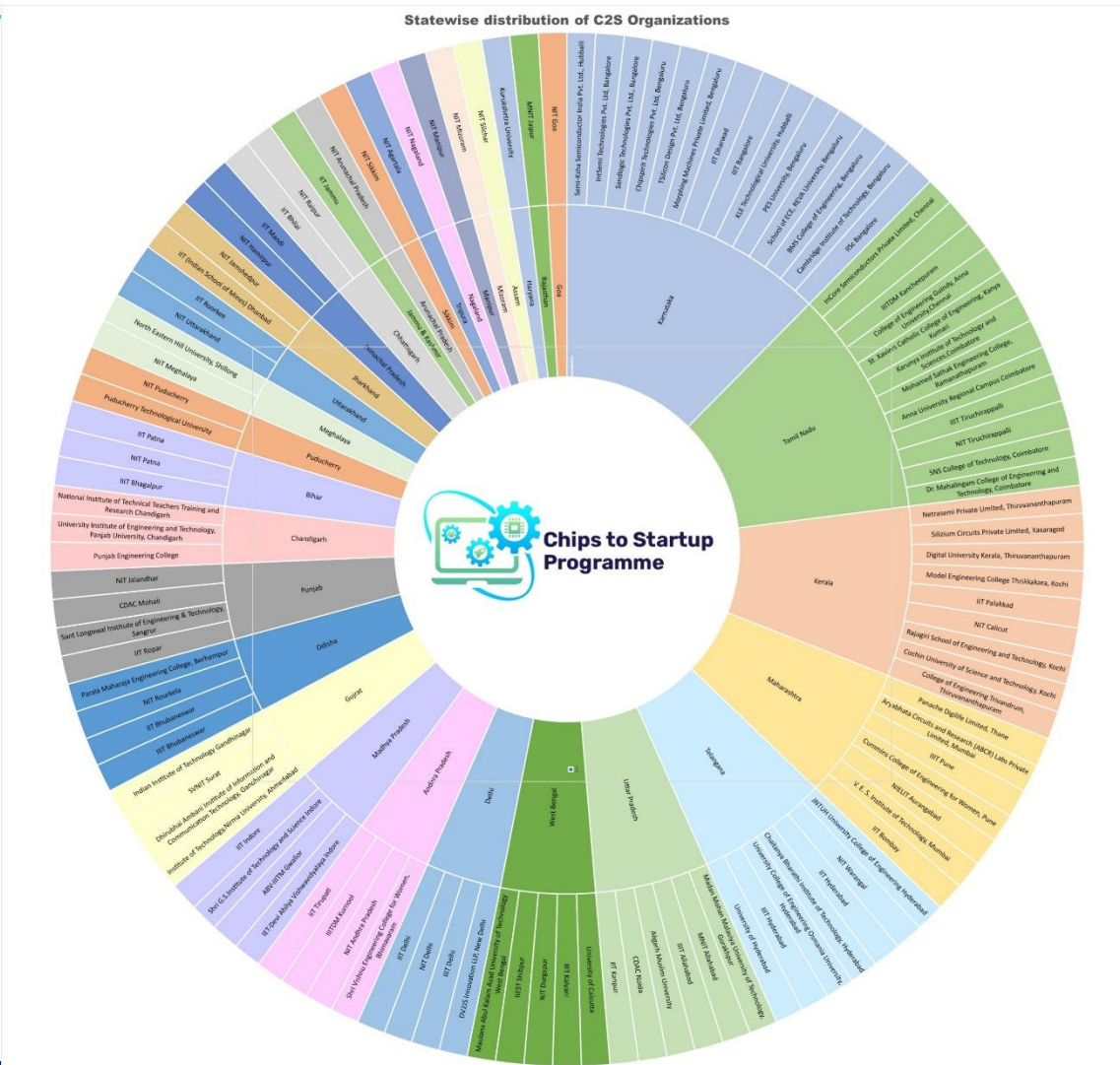
# Chips to Startup (C2S) Programme



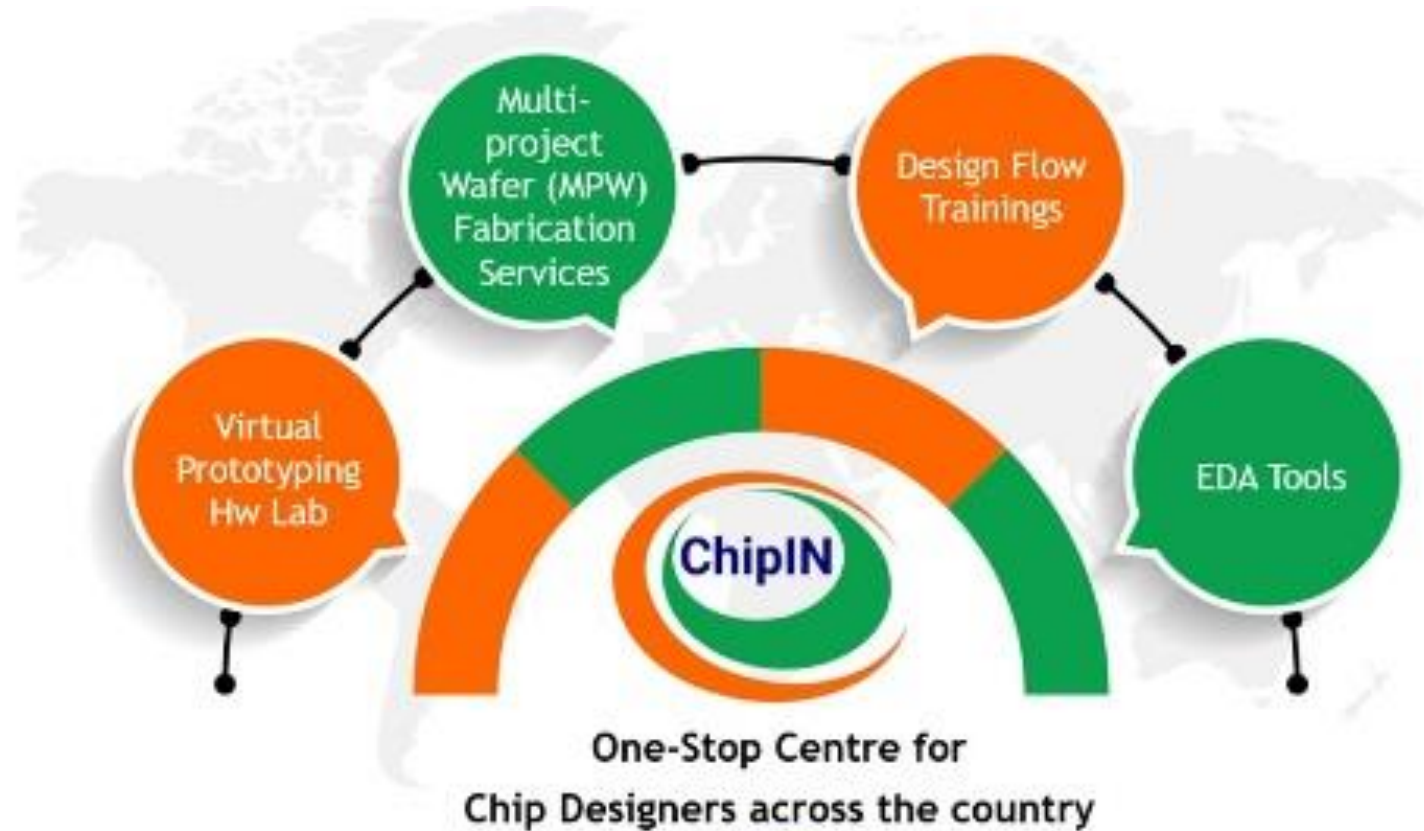
## Breakup of 85000 Manpower

Type-I Manpower (PhD)	300
Type-II Manpower (M. Tech in VLSI / Embedded System Design)	8500
Type-III Manpower (M. Tech in Computer / Communication / Electronic System / Equivalent with at least two VLSI courses / minor project in VLSI etc.)	11200
Type-IV Manpower (B. Tech with at least two VLSI Courses / minor project in VLSI)	65000

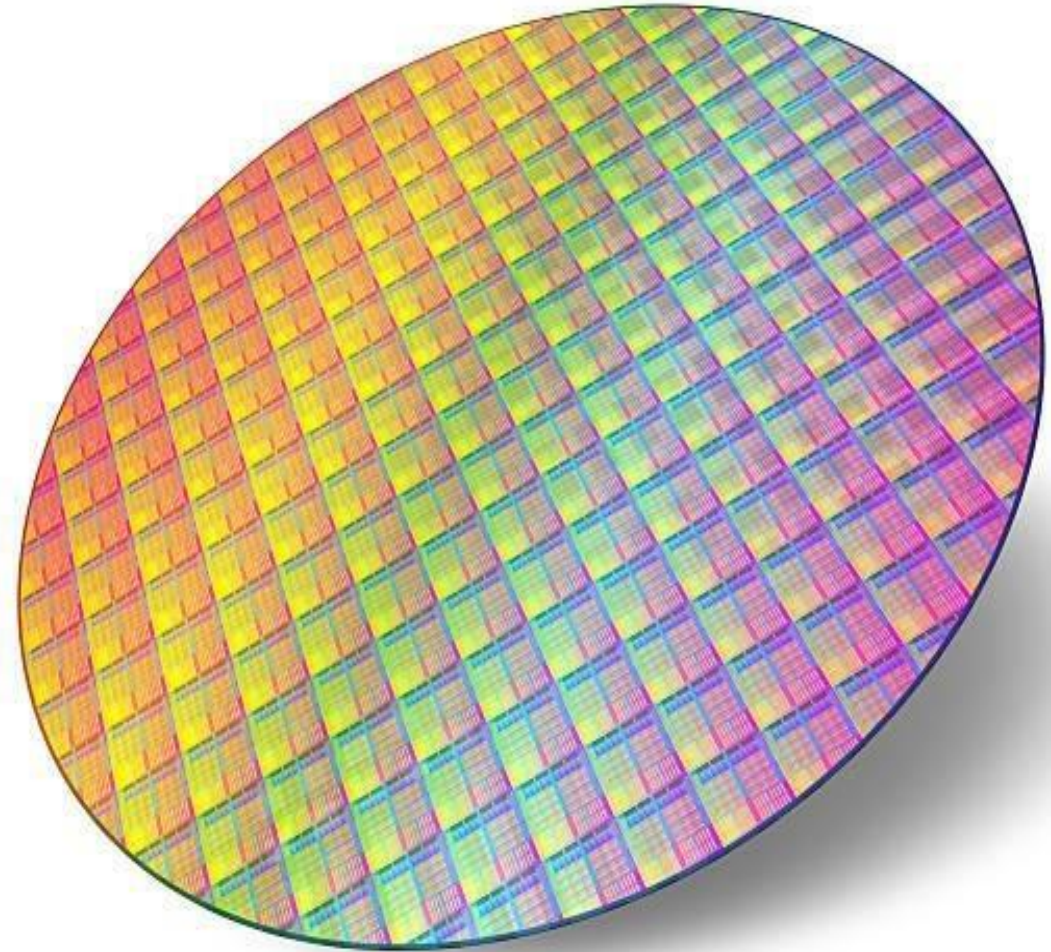
# List of 113 Institutions Getting Financial Support for implementing 65 R&D Projects under C2S Programme



# ChipIN Centre



<https://chips-dli.gov.in>



# Modified Design Linked Incentive (DLI) Scheme

*Design Semiconductor Chips in India, for the World !*



Ministry of Electronics & Information Technology  
Government of India



Start-ups

MSMEs

Domestic companies other than Start-ups/ MSMEs

## Eligibility of support components under the DLI Scheme

Categories of Support		Eligibility	
Design Infrastructure Support	<b>Infrastructure:</b> EDA Tools, IP Cores, MPW Prototyping, Post-Si Validation	Start-ups & MSMEs	
	<b>Design:</b> Milestones linked reimbursement of 50% of the eligible expenditure subject to a ceiling of 1.7 million USD	Start-ups & MSMEs	
Financial support	<b>Deployment:</b> Reimbursement of 6% to 4% of net sales over 5 years subject to a ceiling of 3.4 million USD per applicant	Threshold of Net sales	Incentive
		<b>Startups and MSMEs</b> 0.12 million USD from Year 1 to Year 5	Year 1 : 6% Year 2 : 6% Year 3 : 5%
		<b>Large Domestic companies</b> 0.59 million USD from Year 1 to Year 5	Year 4 : 5% Year 5 : 4%

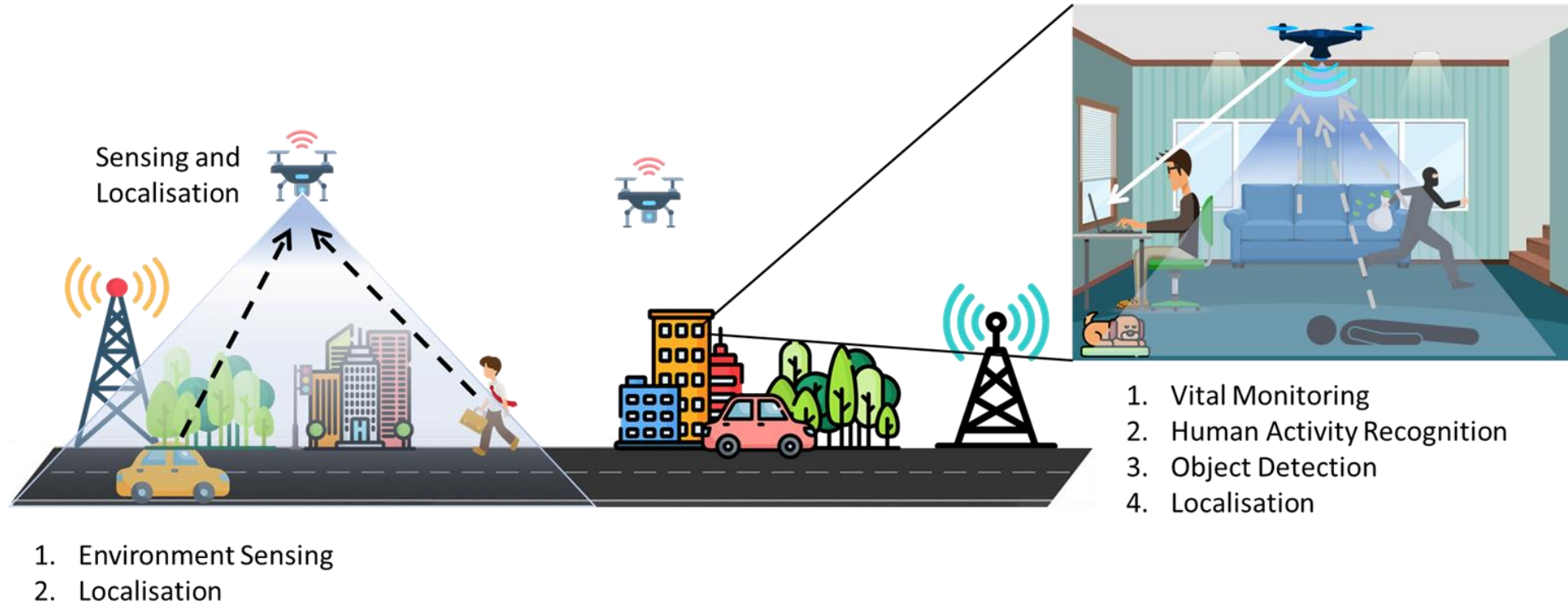
- **Objective:** Building a self-reliant processor ecosystem
- **Focus:** Indigenous development of advanced computing processors
- **Significance:** Strengthening India's technological sovereignty

- **Project:** AUM System-on-Chip (SoC)
- **Architecture:** Based on Arm architecture
- **Purpose:** Powering high-performance computing applications
- **Status:** Development initiated

## AUM Processor Technical Highlights

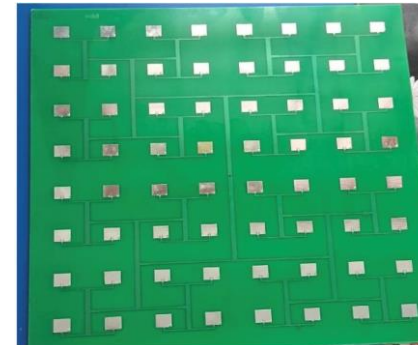
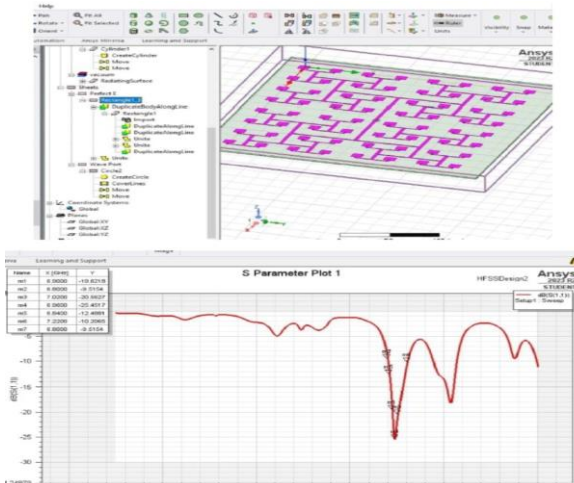
- **Cores:** 48 Cores per Chiplet, 96 Cores per Package (2 Chiplets); **Frequency:** 3.0 GHz (typical), 3.5+ GHz (turbo); **Memory:** 8-Channel DDR5-8800, 2 HBM3e Controllers (up to 144GB); **Bandwidth:** DDR: 563.2 GB/s, HBM3e: 4.916 TB/s; **Connectivity:** 64 PCIe Gen5/CXL 2.0 Lanes, UCIe D2D, CXL 2.0 C2C; **Compute:** ~5 TFLOPS (Double Precision)

# Integrated Sensing and Communication



## + Project Overview

This project develops a 6G NR modem prototype for the 6.425-7.125 GHz band in India, influences global 6G progress through contributions to ITU-R WP 5D and 3GPP 6G studies, and has already impacted the ITU-R WP 5D 6G Vision, Framework, and TPR.



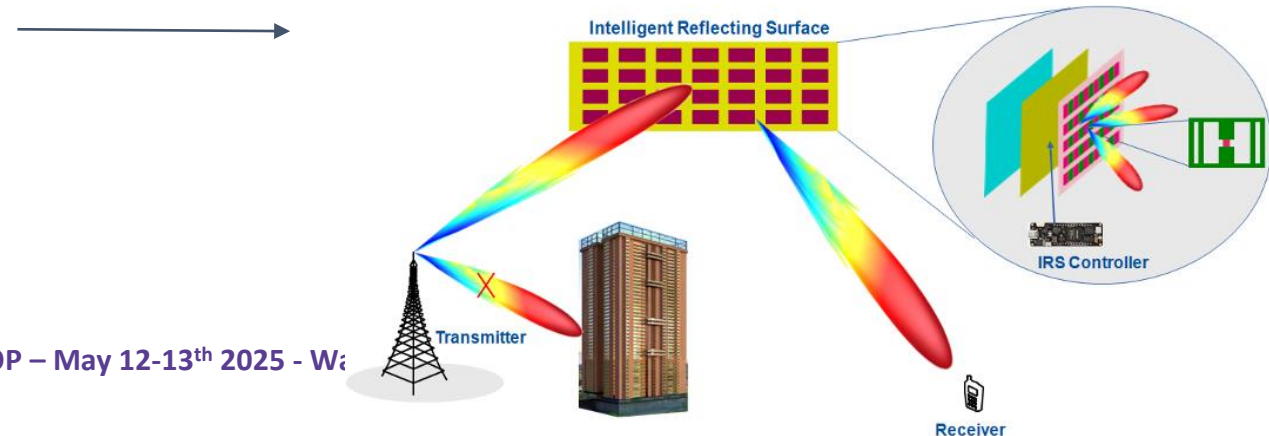
## + Project Overview

The project aims to develop and demonstrate a 140GHz 6G high-speed communication link, integrating transmitters, receivers, **Intelligent Reflecting Surfaces (IRS)**, and beamforming technologies.

## Deliverables of the project

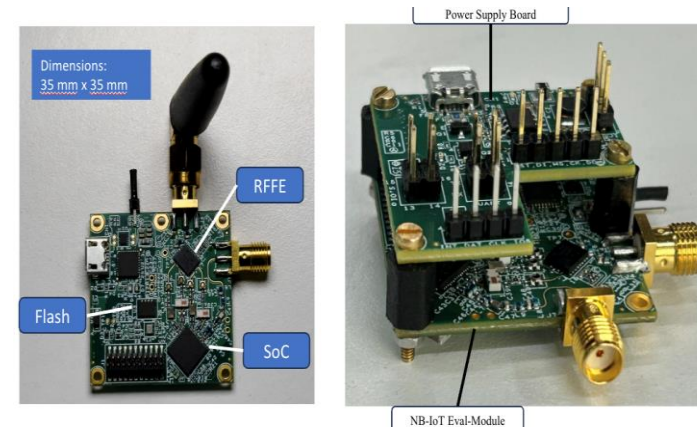
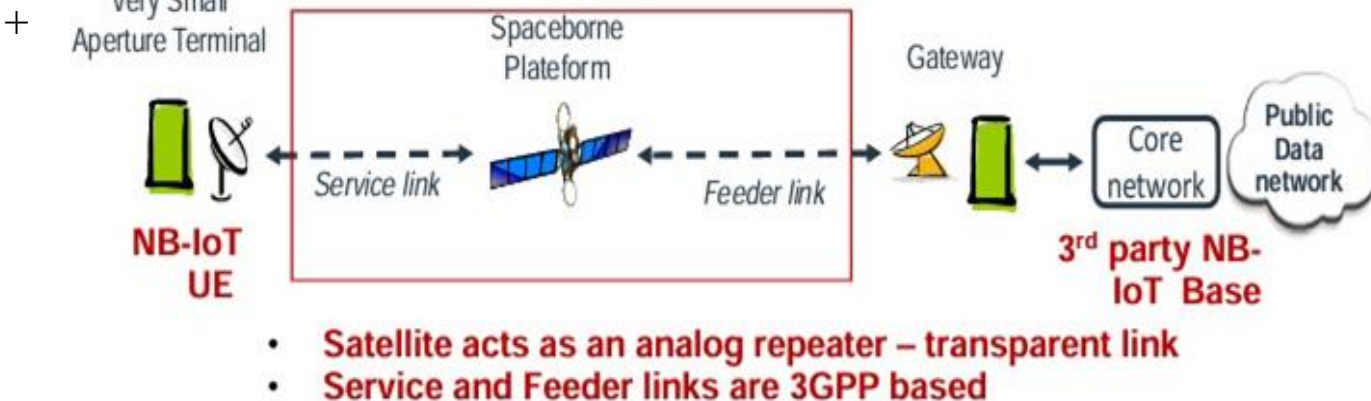
- 140GHz sub-THz communication link,
- IRS hardware with integrated antennas, and MMIC/RFIC transceivers.
- Sub-THz components, beamforming configurations, D-band antennas, and a digital baseband system.
- Contributions to global 6G standards through ITU forums, patents, and publications will support India's telecom ecosystem.

## + Proposed 6G IRS enabled Communication Link



## + Project Overview

- Significant advancements in Satcom and terrestrial communication convergence,
- Achieved key milestones such as developing 3GPP Rel-17 compliant Satcom IoT systems.
- Developed L-band NB-IoT SoC to support GEO satellites, which enables a plethora of low-bit rate satellite IoT applications.
- Contributed to the ITU WP 5D IMT-2030 Framework Document by integrating Satcom as a key interworking feature in IMT-2030



**Developed Link and System level simulators**

## RISC-V Based Processor Ecosystem

- **Scope:** Comprehensive processor development
  - Central Processing Units (CPUs)
  - General-Purpose Graphics Processing Units (GPGPUs)
  - AI/ML Accelerators
  - AI, data centers and consumer electronics chips
- **Architecture:** Open-source RISC-V architecture
- **Goal:** Versatile, scalable, and energy-efficient solutions

# Best fields for cooperation

- **Logic**

- MicroProcessor, GPU and AI/ML accelerator and In-memory computing

- **Mixed-signal processing**

- Wireless & RF SoC Technologies (i.e. RF front-end integration for 5G, Bluetooth, Wi-Fi, Mixed-signal support for software-defined radio (SDR), mmWave and sub-THz mixed-signal transceivers).

- **Powering**

- Power management ICs, IGBTs required for EVs, HPCs & Power Electronics systems.
- GaN and SiC based ICs and sub systems for e-mobility applications.
- SiC and GaN based converters/power electronics devices for energy systems.

- **Sensing**

- Sensor technologies for IoT, Advanced Manufacturing and Smart City applications.

- **Communicating**

- Integrated Sensing and Communication
- Next-G wireless network technology
- AI-native design in wireless communication

- **Photonics**

- Chip Interconnects
- Photonics Ics

## Logic

- **EDA & IP** - Entire VLSI design flow to be automated by developing Open-source EDA tools; Introducing innovation in CAD/ EDA tool design.
- **Chip Design**
  - India has made significant progress in establishing a CHIP design ecosystem to develop indigenous processors by initiating the development of RISC-V/ ARM based processors(VEGA & AUM Processors). Our goal is to achieve technological self-reliance in Compute and High-Performance Computing (HPC) by developing sovereign Exa-scale computing systems through collaborative co-development. To this end, we seek to explore partnerships between India and Europe, leveraging complementary capabilities to advance India's Exa-scale HPC development objectives.
  - Innovate in CPU, GPGPU and AI/ML accelerators
  - In-memory computing

## Sensing

- **System Design**
- **Manufacturing (front-end) Process Development:** Developing tools for optimizing fabrication processes such as lithography, etching, lift-off and materials deposition.
- **Manufacturing (back-end)**
- **Equipment & Tools (front-end)**
- **Equipment & Tools (back-end):** Equipment Design: Developing specialized equipment for assembly, sensor modification, packaging, and characterisation of sensor devices and systems

# Most challenging fields for cooperation

---

- HPC
- RISC-V based Processors, IPs and Software tool-chain Ecosystem
- Advanced Materials
- Scaling of technology for manufacturing of silicon photonics (48-180 nm node)
- Nanoelectronics
- Sensors
- Nueromorphic computing

To achieve technological self-reliance in High-Performance Computing (HPC) with sovereign Exa-scale systems via collaborative co-development, key Opportunities for International Cooperation (with Europe and beyond):

- Chip Design: Innovate in CPU, GPGPU and AI/ML accelerators, In-memory computing
- Design Tools & IP Cores: Enhance development capabilities
- Mixed-Signal & RF Transceiver Design: Advance communication technologies
- Power Supplies & Analog Electronics: Optimize performance and efficiency
- System Design & Manufacturing: Strengthen front-end and back-end processes.

- Sensor Manufacturing
- Component Manufacturing
- Neuromorphic Computing
- Communication
- Next-G wireless network technology
- High frequency system (HW/SW, Frequency Range 3, mm wave and sub-THz band)
- AI-native design in wireless communication



**THANK  
YOU**

This project has received funding from the European Union's Horizon Europe research and innovation programme under GA N° 101092562