ICOS International Cooperation On Semiconductors

WORKSHOP

Key Emerging Technologies for future Industrial Applications

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Landscape analysis of standards in semiconductor and chip

The first iteration

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Semiconductor standards

Why do we analyze?

- Growing importance of semiconductors for European industry and society
- Strengthen EU's position in global value chains in semiconductor: EU Chips Act
- Semiconductor standardization = Critical to ensure interoperability, efficiency and technical leadership

Objectives

- Identify and map the gaps in existing value chains potentially induced by a lack of international standards
  - provide a set of recommendations for standardization activities
- Identify needs of new standards for emerging technologies, for which value chains are under construction
  - provide specification of these needs and potential recommendations
- Recommendation on Standardisation (July 2025)
  - Now it is working in progress!

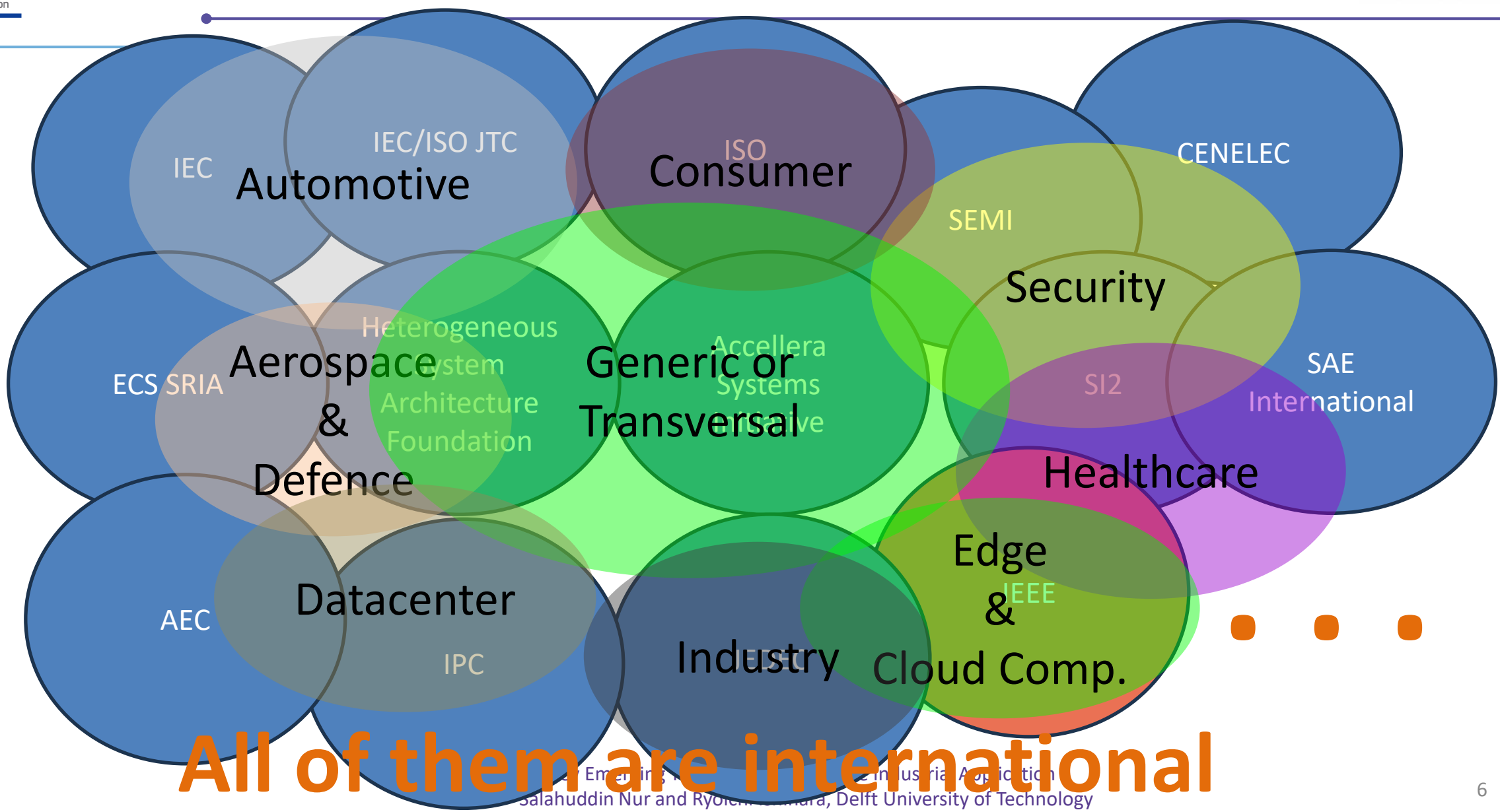
Approach

- List devices and process steps
  - Aeneas, input from ICOS WP3
- Form a technical working group (TWG)
  - ICOS, StandICT.eu and AllPROS.eu
- Identify standard development organizations (SDOs) and working groups
- List and classify the standards (~2500!) into types of devices, process steps and applications
- Analyse the statistics and identity and map the gaps

Original classifications

	Material	Equipment		IC Design			Front-End Fab.	Eng. Services	Software provider	Industrial tech.
Devices		Front-End Equipment & Services	Back-End Equipment & Services	EDA	IP Blocks	Whole IC				
AI				X	X	X			X	
Chiplets / Advanced packaging	X		X	X		X	X	X	X	
Energy efficiency and sustainability	X	X	X	X		X	X	X		X
Sub-5nm	X	X		X		X	X			
Advanced Litho.	X	X		X		X	X			
Quantum computing	X	X	X	X		X	X	X	X	X
Neuromorphic/ReRAM/AI chip	X			X	X	X	X			
Edge computing	X		X	X	X	X	X	X	X	X
Photonics	X		X	X	X	X	X	X	X	X
Cybersecurity										

SDOs Classifications: Applications



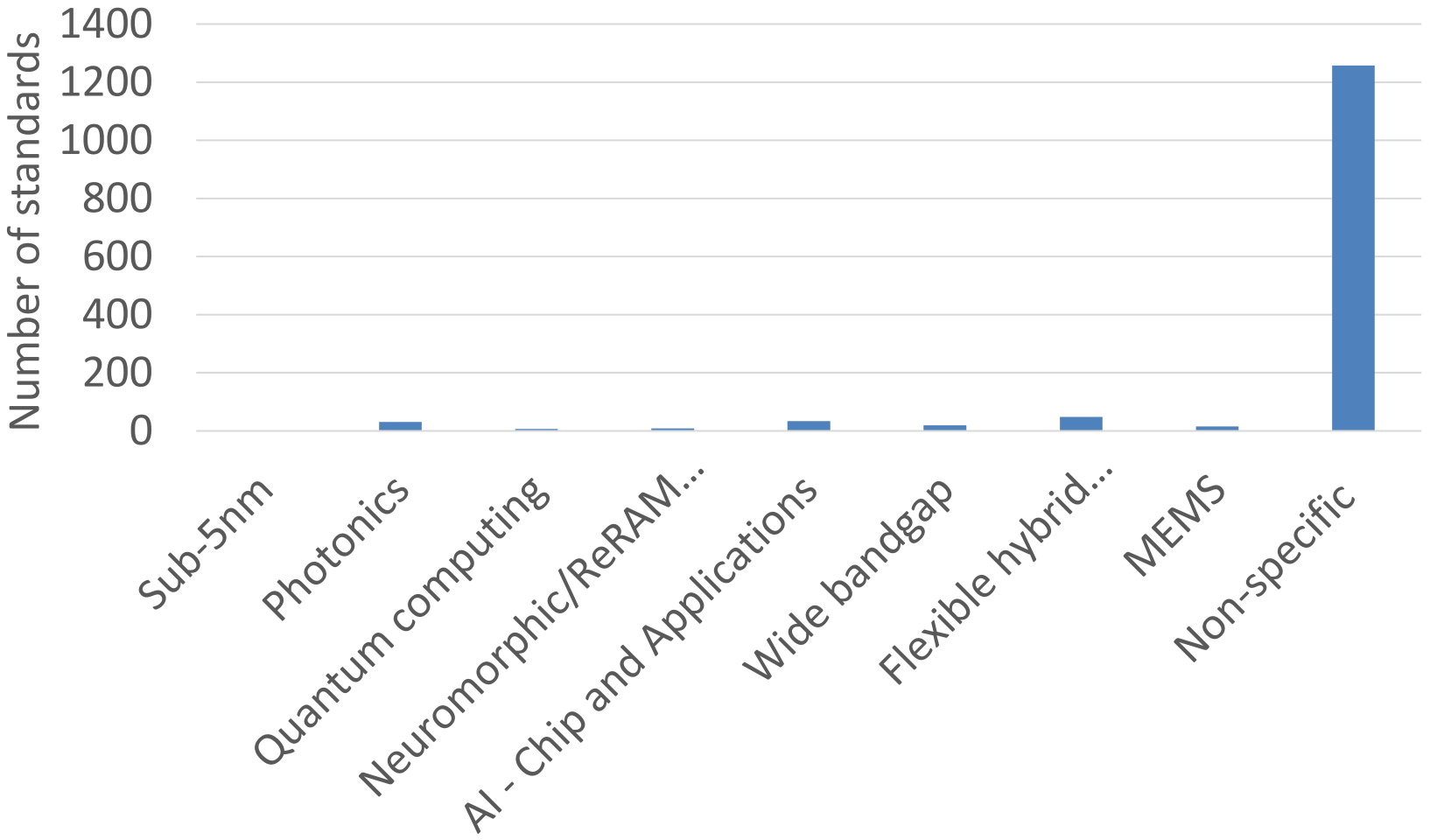
All of them are international

New Classifications

	Materials	Equipment Front-End and services	Equipment Back-End and services	IC Design EDA tools and services	IC Design Blocks	IC Design Whole IC	Front-End Fabrication
Sub-5nm							
Photonics							
Quantum computing							
Neuromorphic/ReRAM/AI Chip							
AI - Applications							
Edge & Cloud computing - Applications							
Wide bandgap							
Flexible hybrid electronics							
MEMS							
Generic							

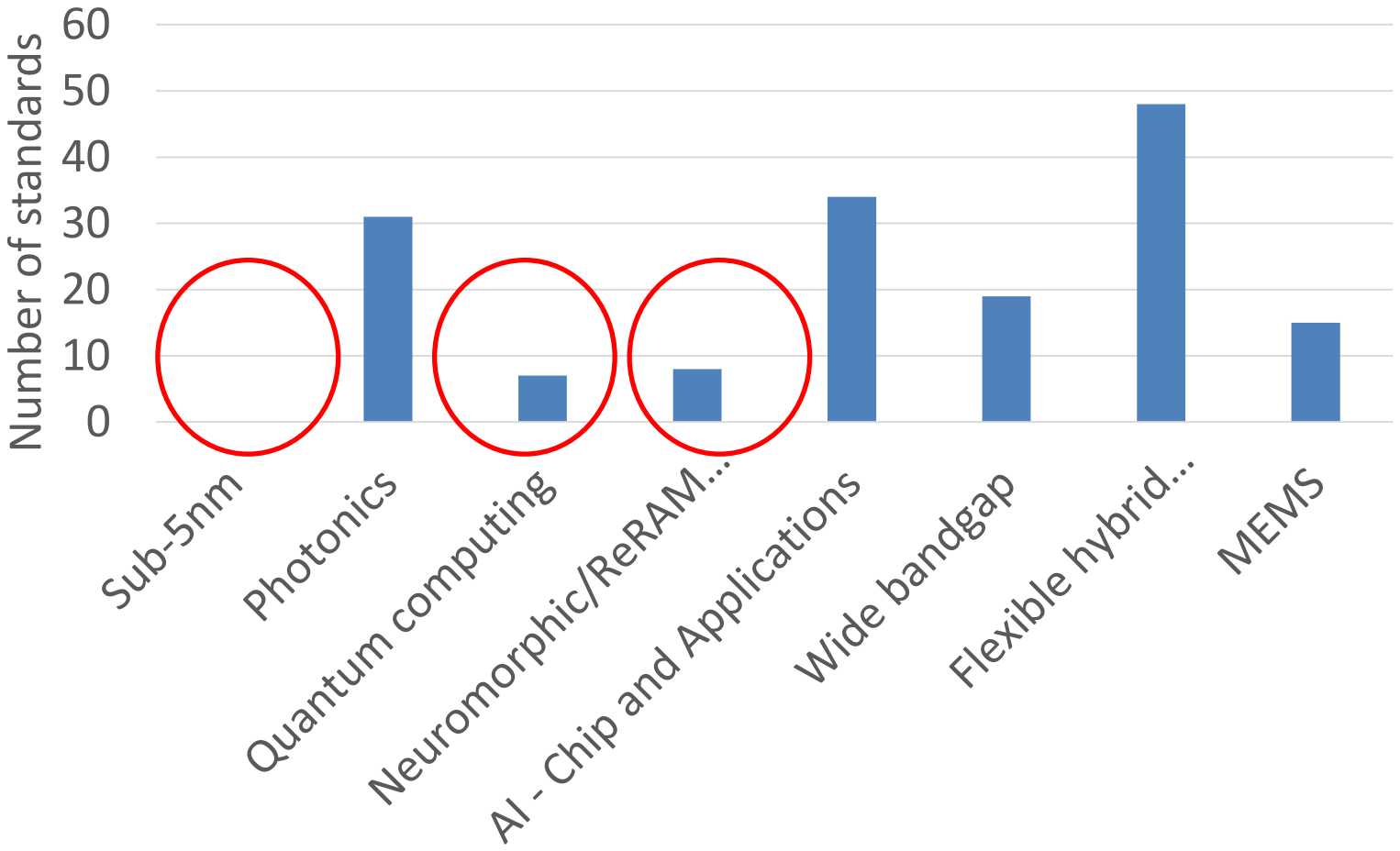
Advanced Lithography, Chiplets/advanced packaging and Energy efficiency & sustainability are included in the process steps

standardizations vs devices



standardizations vs devices

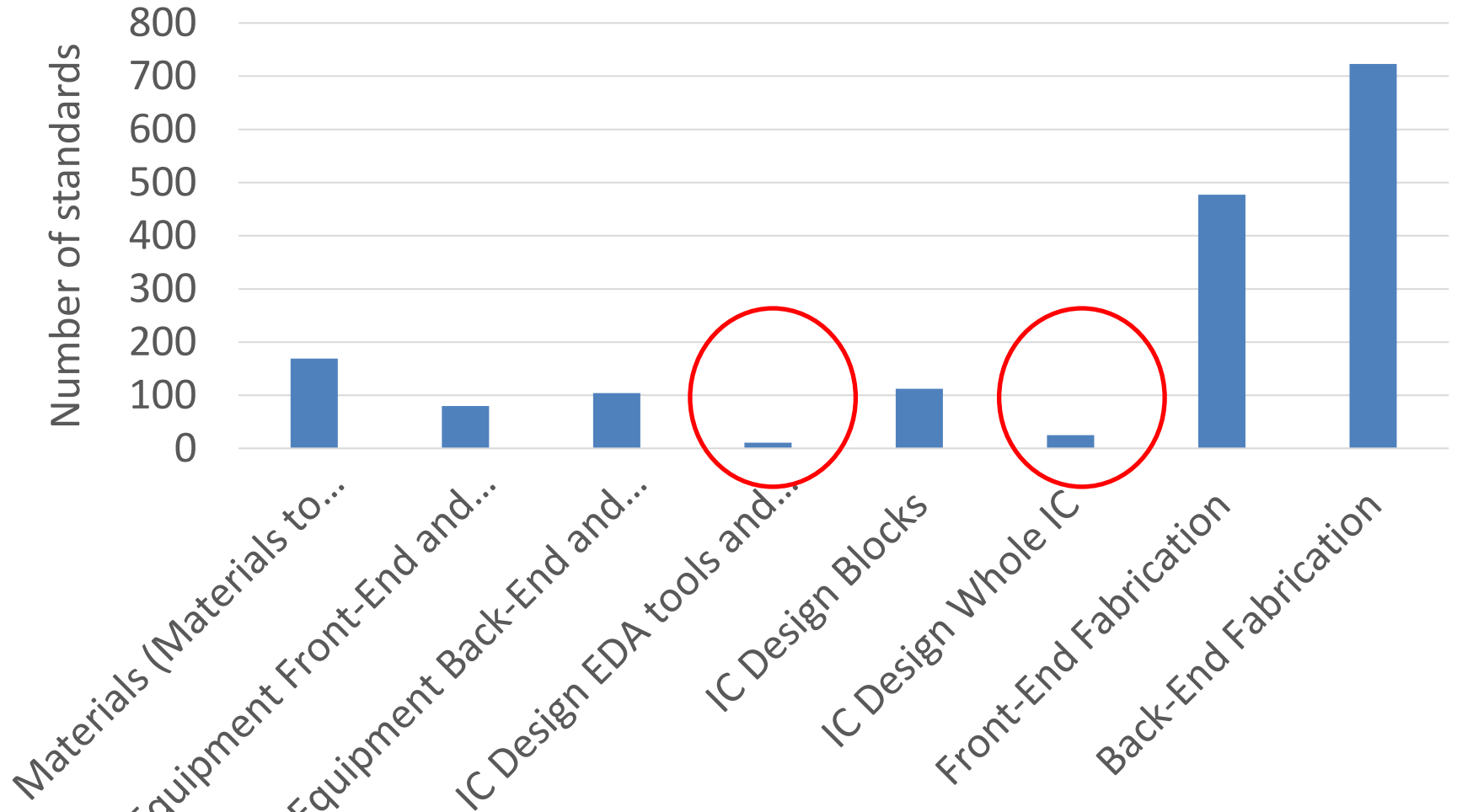
w.o. non-specific devices



Observation: Devices

- Moderately covered for photonics/AI/Flexible-hybrid electronics/Wide-bandgap/MEMs devices.
- Lack in emerging devices (sub-5nm, quantum, neuromorphic)
  - Did not analyze IEEE yet
  - Difficult to identify from abstract
    - Needs deep dive in Non-specific devices
  - SDOs not identified
  - Potentially the gap

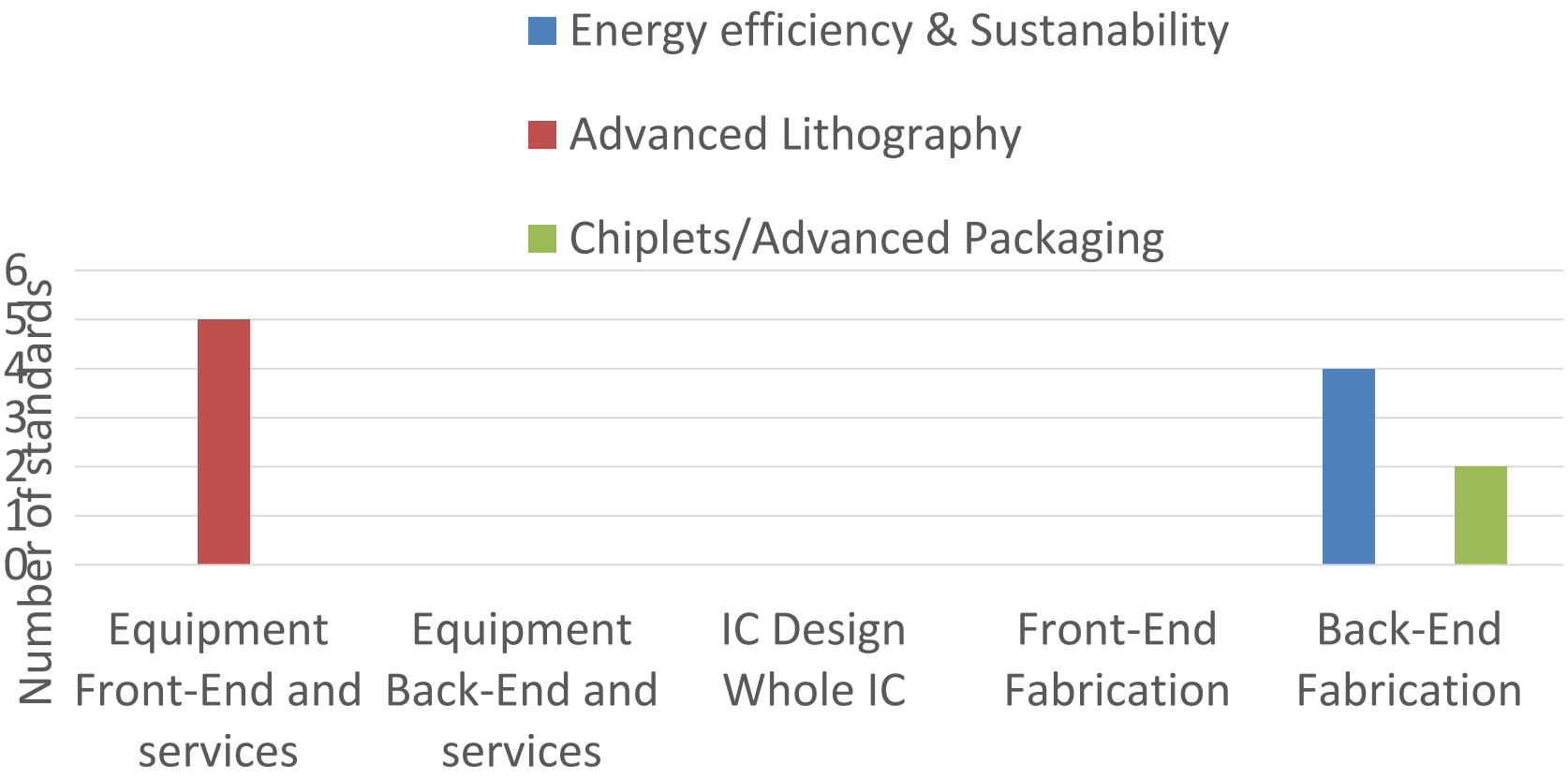
standardizations vs process steps



Observation: Process Steps

- Well covered for Front/backend fabrication
- Somewhat limited for Front/backend equipment
  - Difficult to distinguish between Equipment and Fabrication
- Very few for IC design tool and IC whole design
  - Did not analyze IEEE yet
  - Potentially the gap

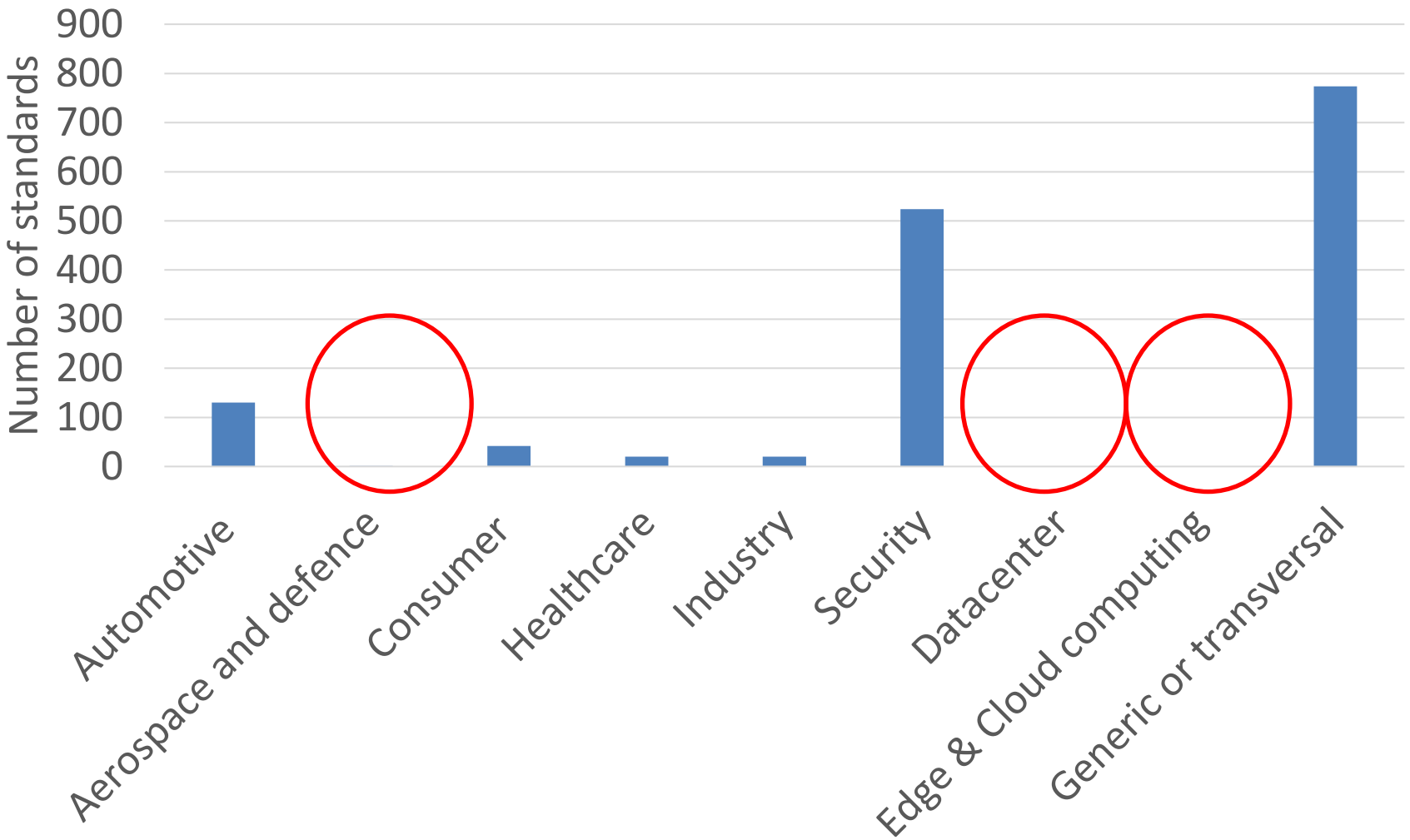
standardizations vs process steps for emerging technologies



Observation: Process steps for emerging technologies

- Very limited numbers of standardization for Energy efficiency & sustainability, Advanced lithography, and Chiplet/Advanced Packaging
  - No IEEE analysis yet
  - Missing SDOs
  - Hidden in the generic process steps
  - Potentially the gap

standardizations vs applications



Observation: Applications

- Well covered for Generic/Transversal and Security
- Limited for Automotive/Consumer/Health/Industry
  - Included in Generic/Tranversal
- None for Aerospace&Defense/Data center/Edge
  - No IEEE analysis yet
  - Included in Generic/Transversal

Conclusions

- The first round of semiconductor standardization landscape analysis has been performed.
- AI/Photonics/Flexible devices and Front/Backend fabrication process seem to be covered moderately well.
- Coverages in sub-5nm/quantum/neuromorphic devices, advanced litho./chiplet/energy efficiency and sustainability/advanced packaging, and IC design tool/whole design steps are very limited.
  - Hidden in IEEE standards and/or generic devices/process steps
  - Missing SDOs
  - Potentially the gaps

Outlook

- Find SDOs/WG for the emerging devices/process steps and potential national activities
  - Interview with experts
  - Organize a webinar
- 2nd iteration
  - Analyze the IEEE standards (~2500 entries)
  - Deep dive into Non-specific devices/process standards
  - Add new (sub) classifications, e.g., energy harvester
- Increase granularity of the analysis map (device vs. process steps) and identify the gaps
- Produce specifications and recommendations
- Finalize the report in July

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THANK YOU

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