Opportunities for international cooperation in the landscape of emerging (semiconductor) technologies

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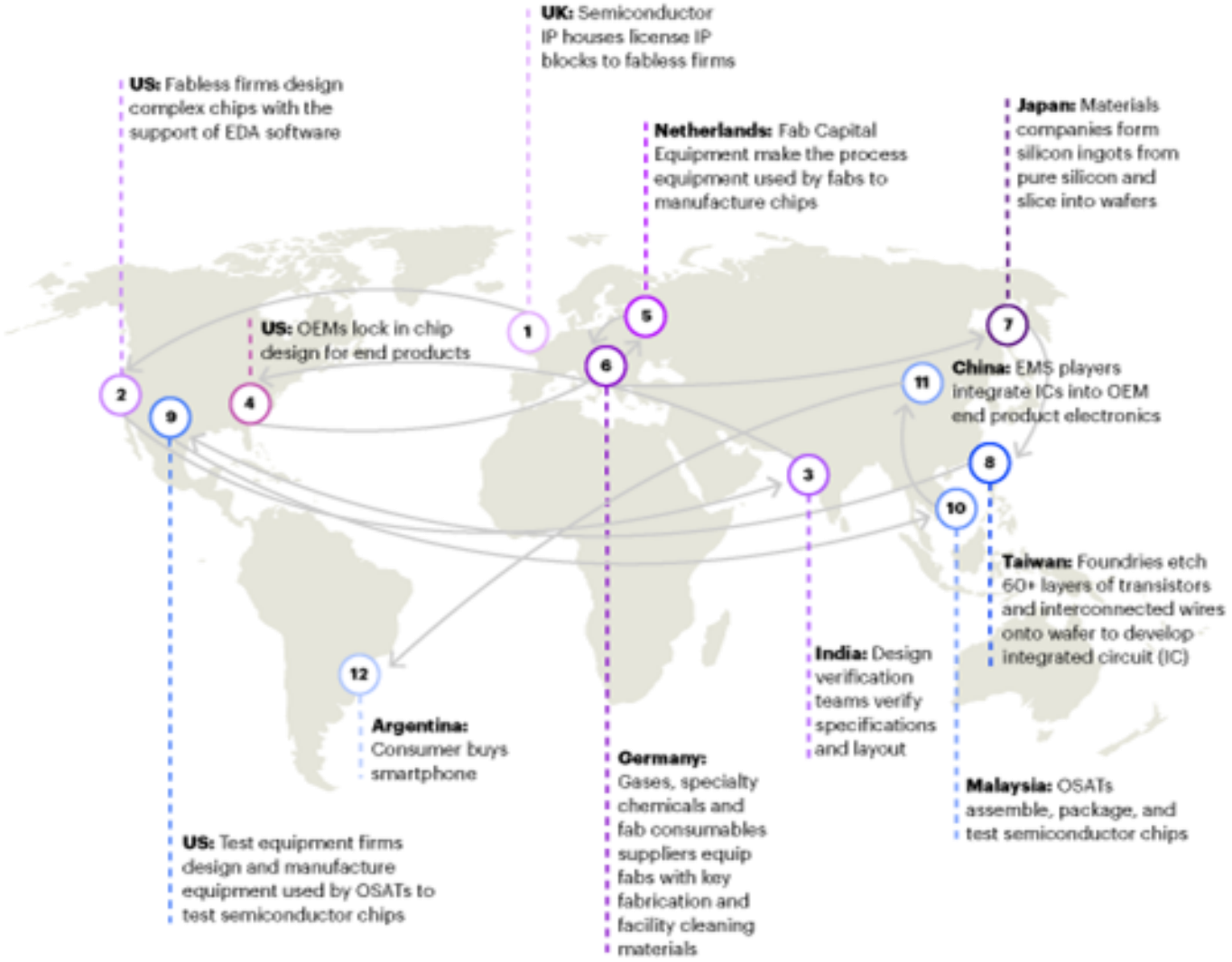
Motivation

Supply Chain Resilience

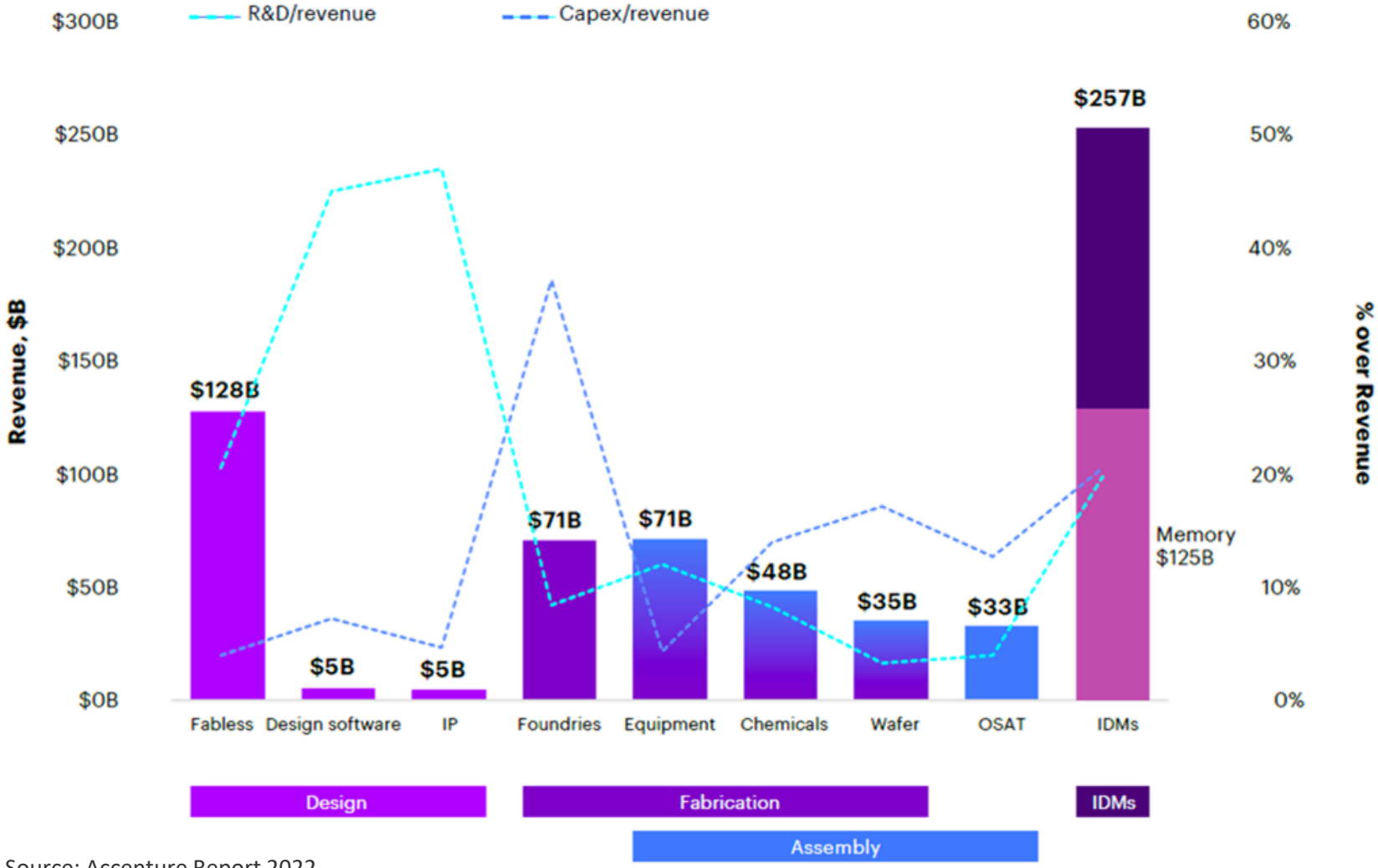
- Semiconductor manufacturing relies on a complex, geographically dispersed supply chain—no single country controls all stages (design, materials, fabrication, packaging)
- Bottlenecks or export restrictions in one country can disrupt the entire global tech ecosystem



Source: Accenture Report 2022

Safeguard Innovation

- High R&D costs and innovation complexity requiring billions of euros in R&D and infrastructure
- No single country can afford to go it alone indefinitely
- Shared research efforts and international talent exchange accelerate breakthroughs and reduce redundancy

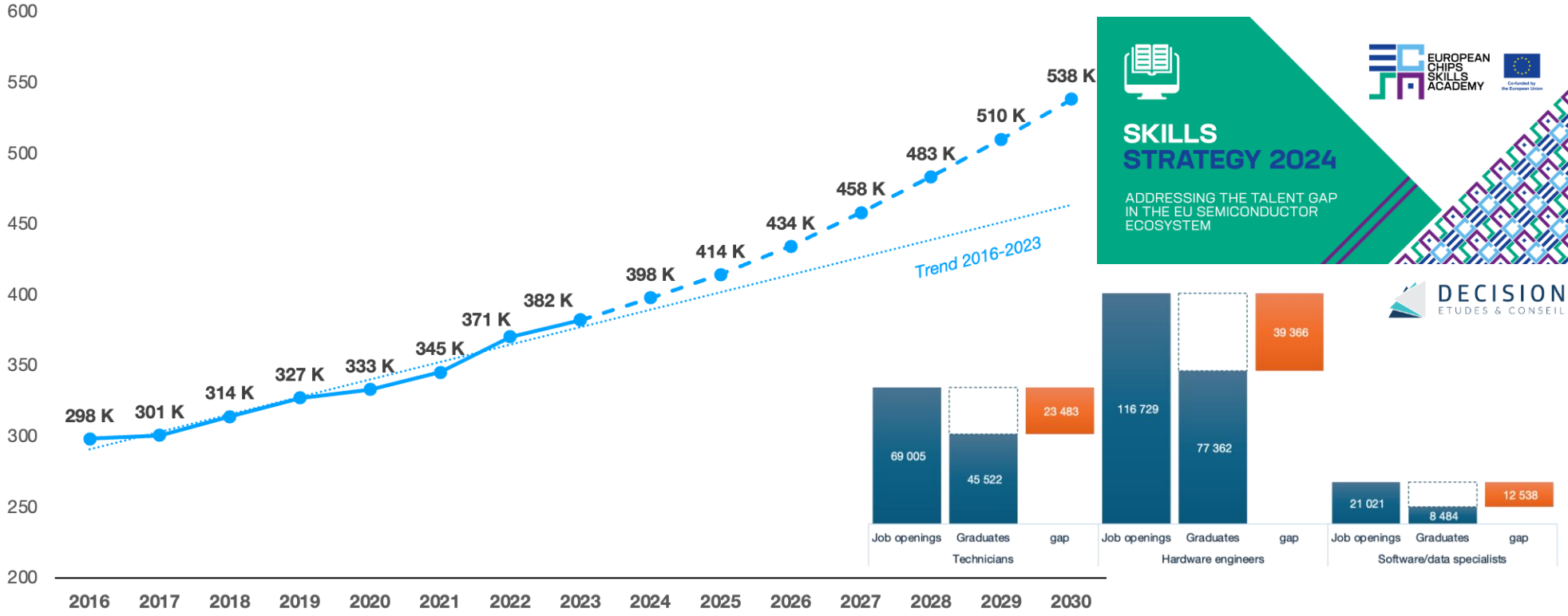


Source: Accenture Report 2022

Talent Development

- Chronic global shortage of semiconductor engineers, technicians, and researchers
- Cooperation through education, training programmes, and skilled worker mobility is essential to develop a future-ready workforce

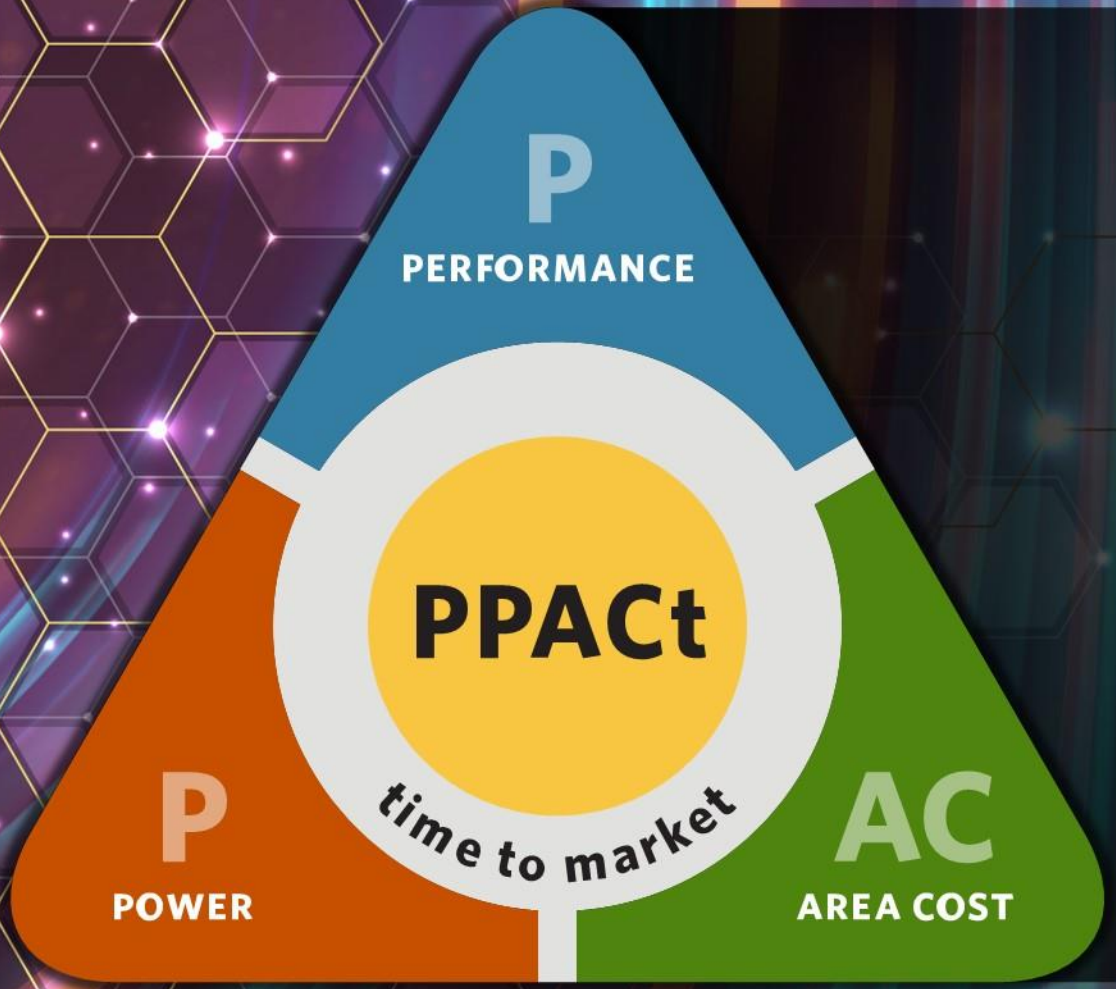
Workforce in the EU semiconductor industry



Long-term Sustainability

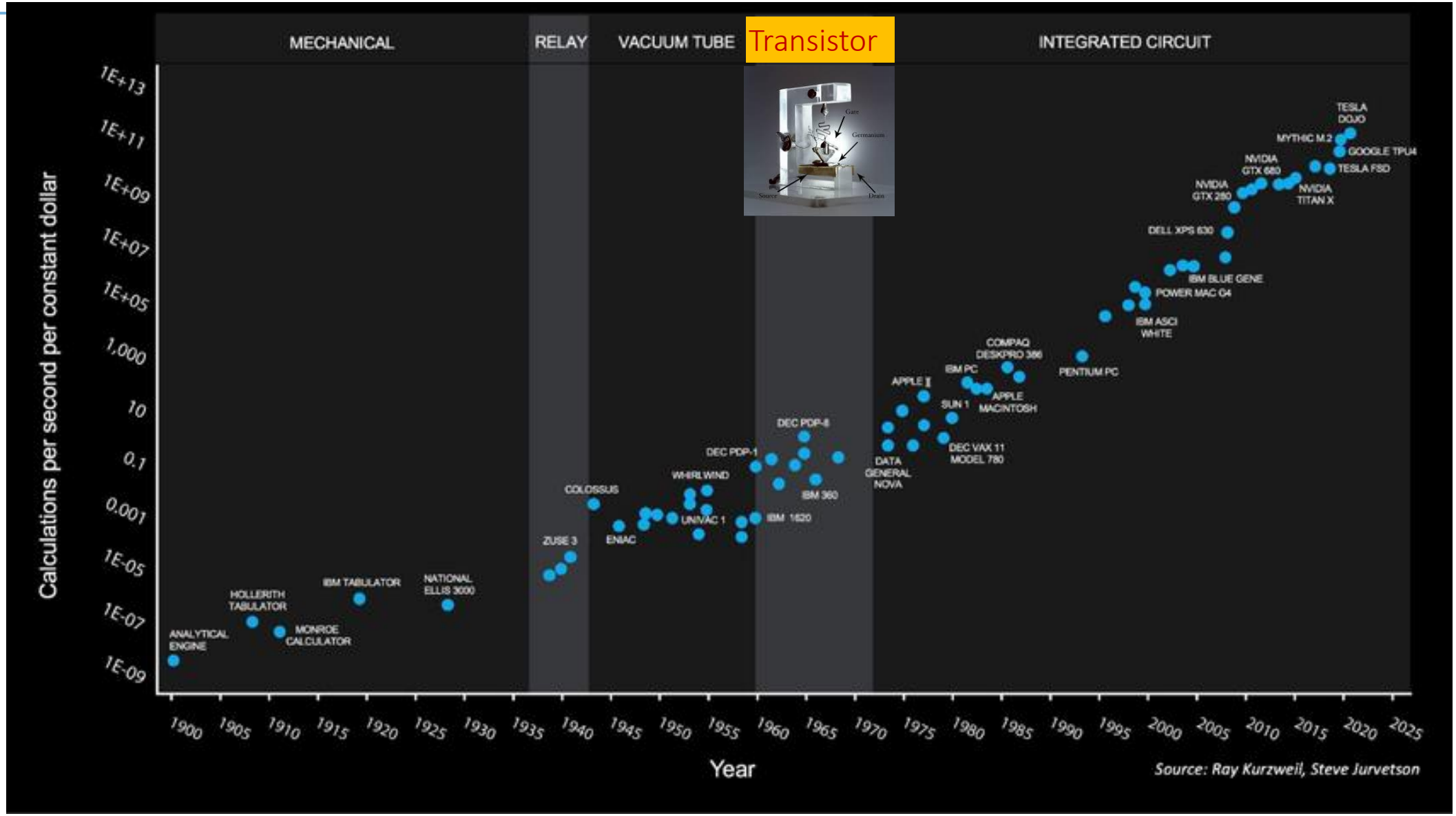
- International collaboration, including the definition of standards, ensures that innovations are interoperable and widely adoptable
- Shared sustainability goals and green manufacturing standards can reduce environmental impact—something no single country can solve in isolation.

The Landscape

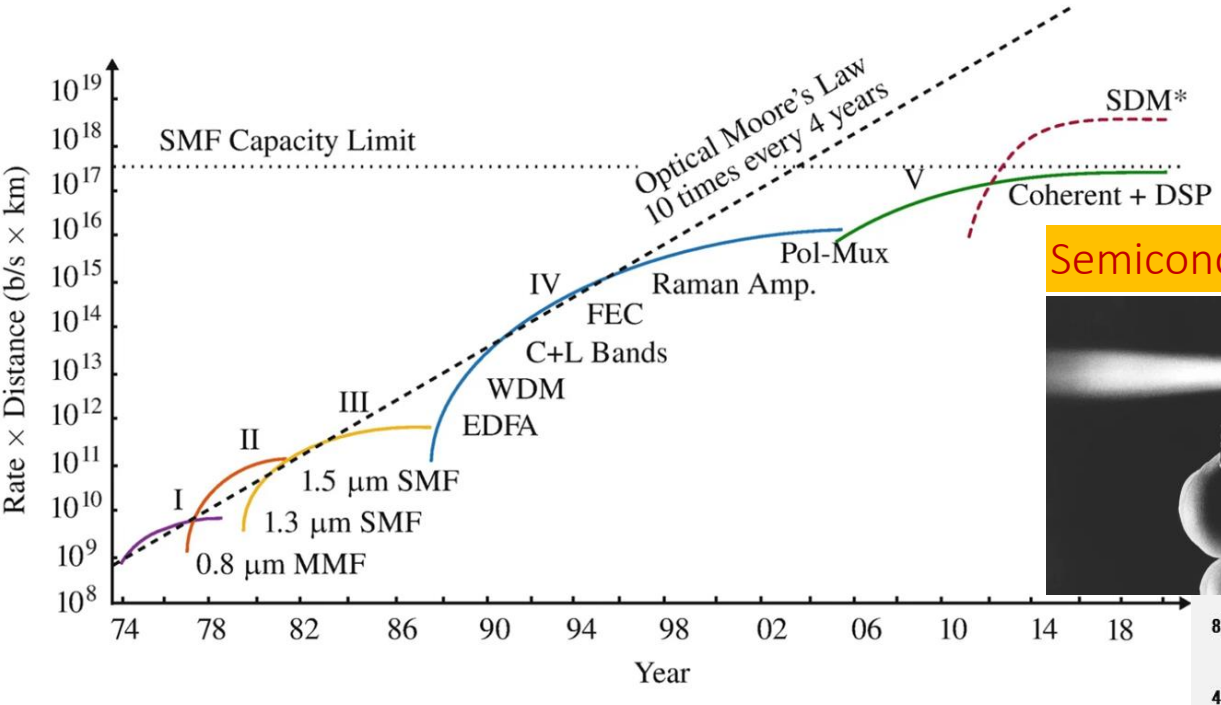


This is the **driving force** behind our industry's new playbook.

Ability to Process Data

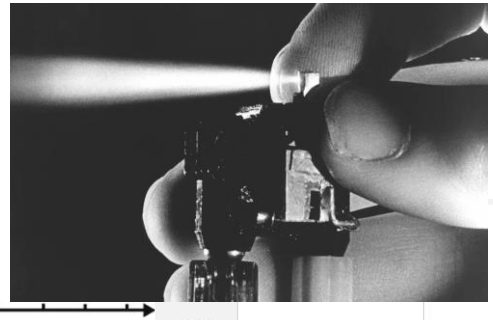


Ability to Transfer Data

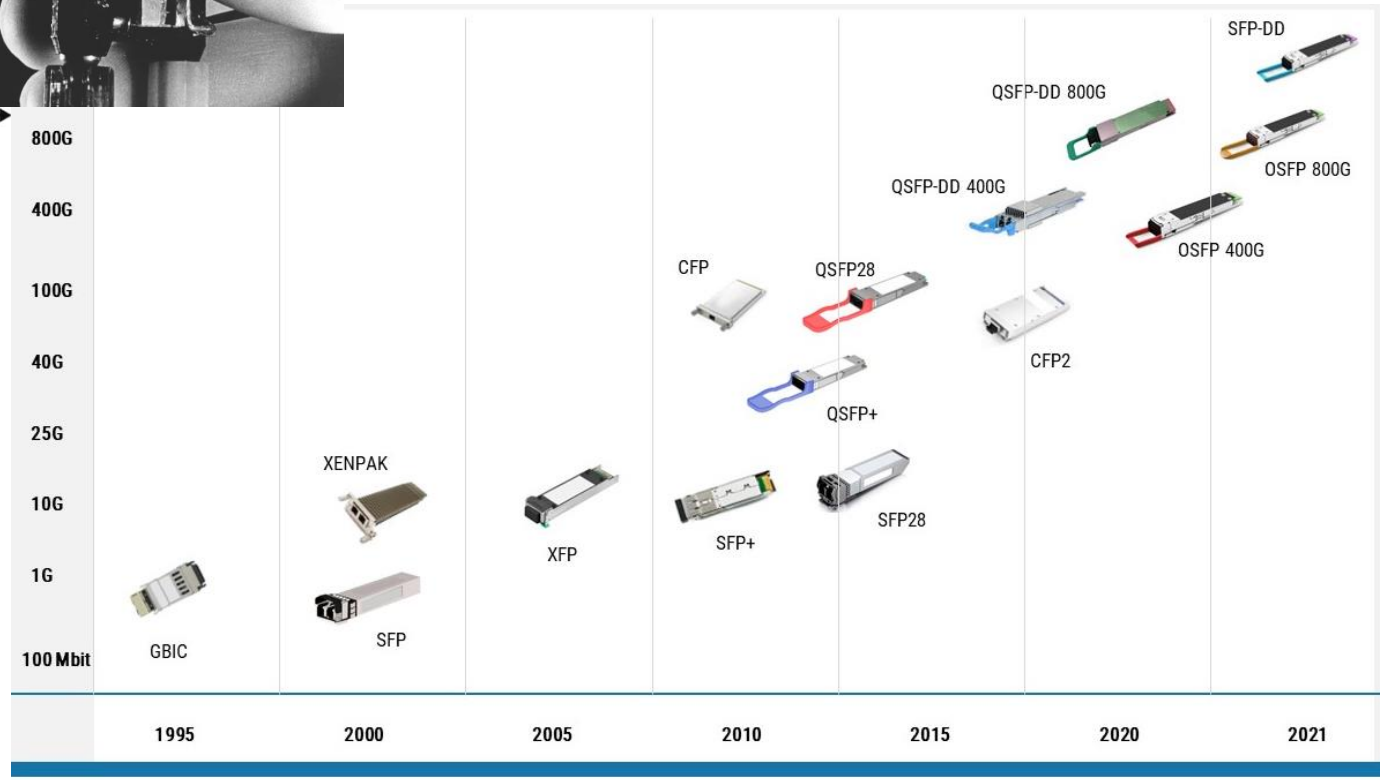


Optical Comms

Semiconductor Laser

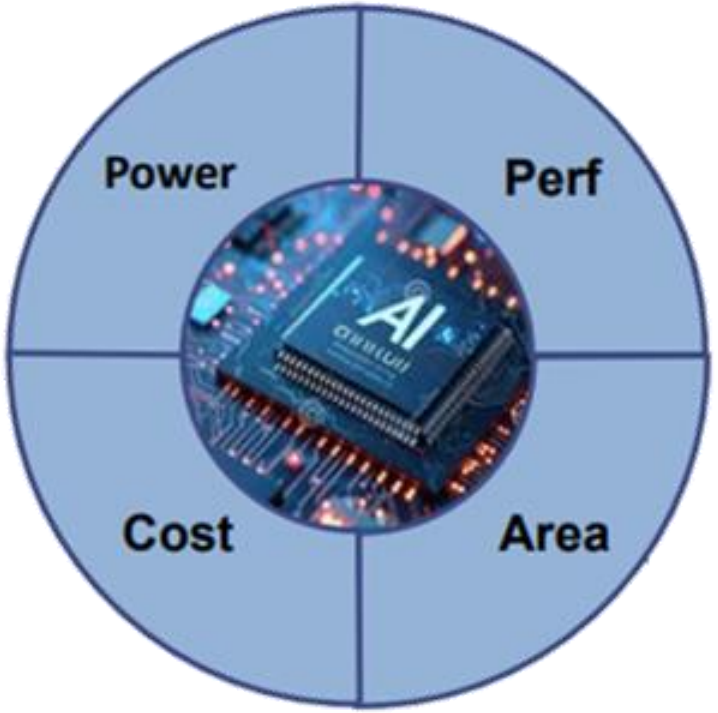


optical transceivers



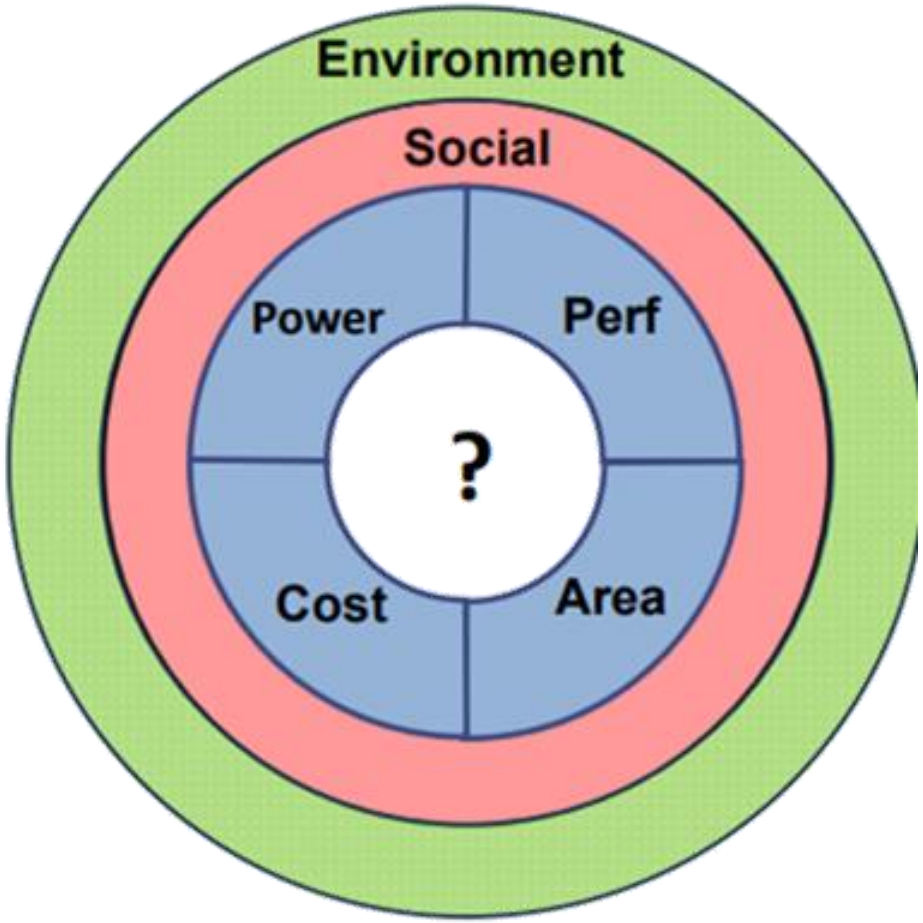
Beyond Performance-Power-Area-Cost

Today's Drivers
Performance & economy



PPAC

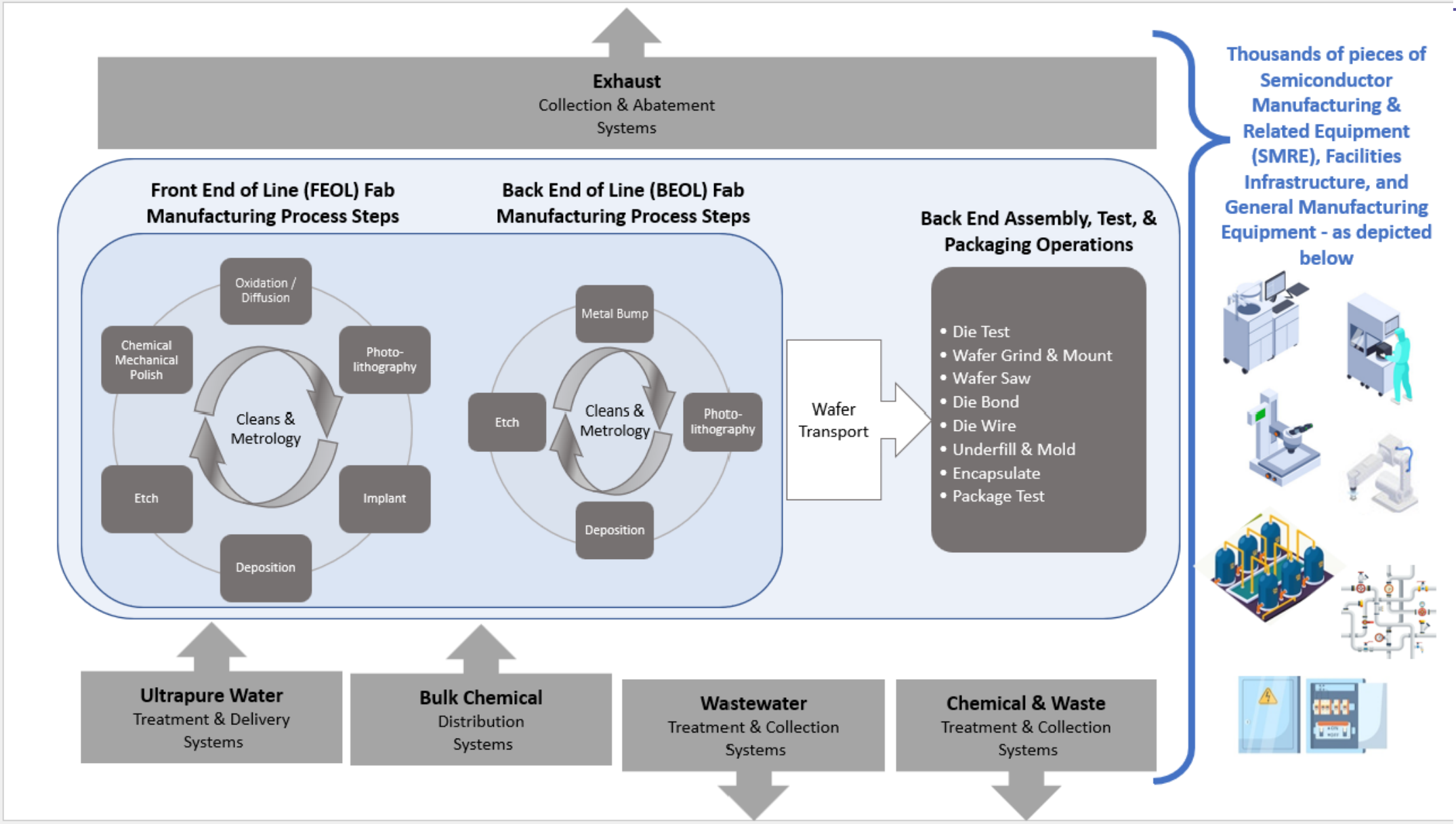
Tomorrow's Drivers?



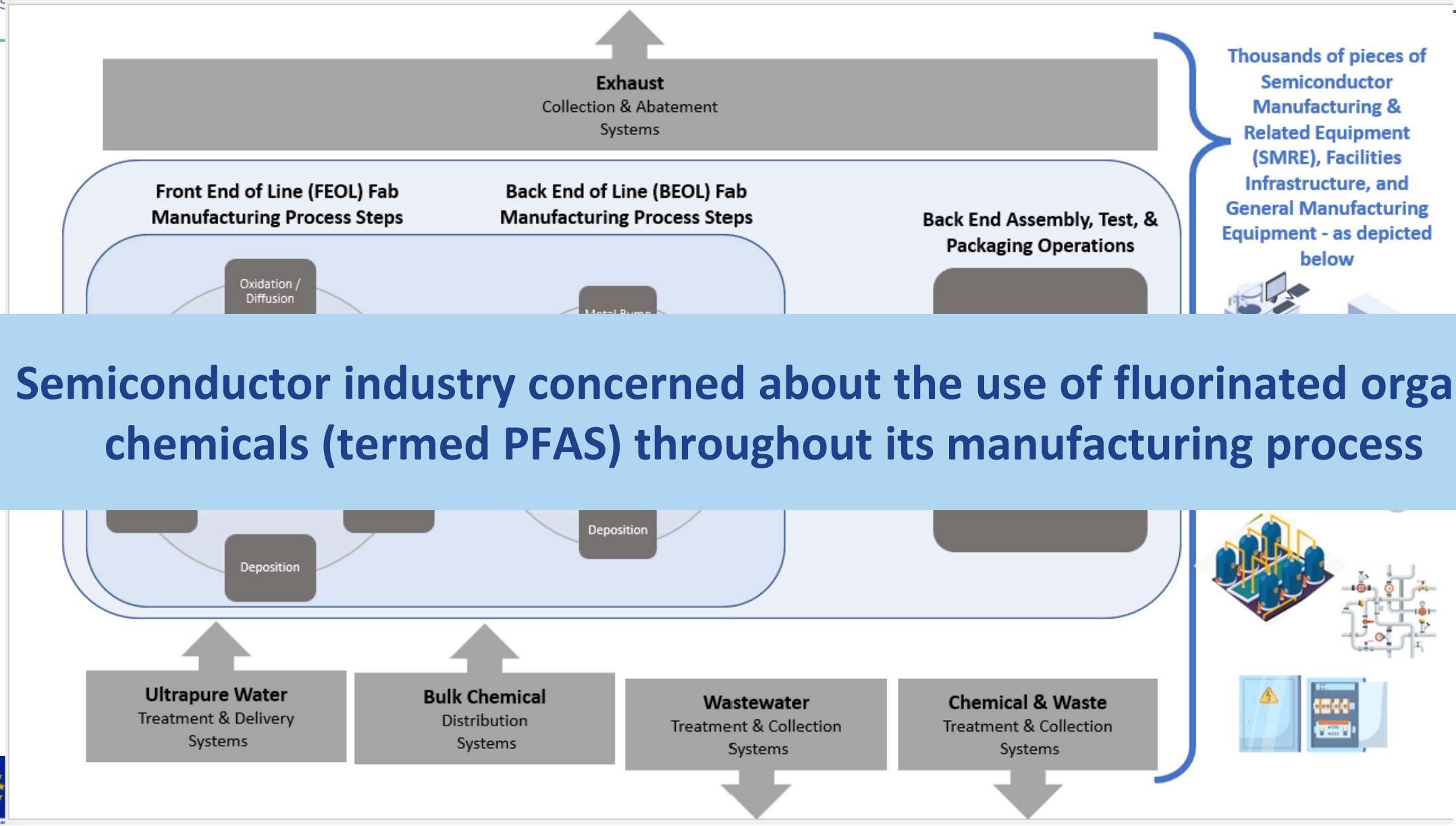
PPAC – E & S

Source: Jean-Pierre Raskin
(UCL, Université Catholique de Louvain)

Sustainability of semiconductor manufacturing

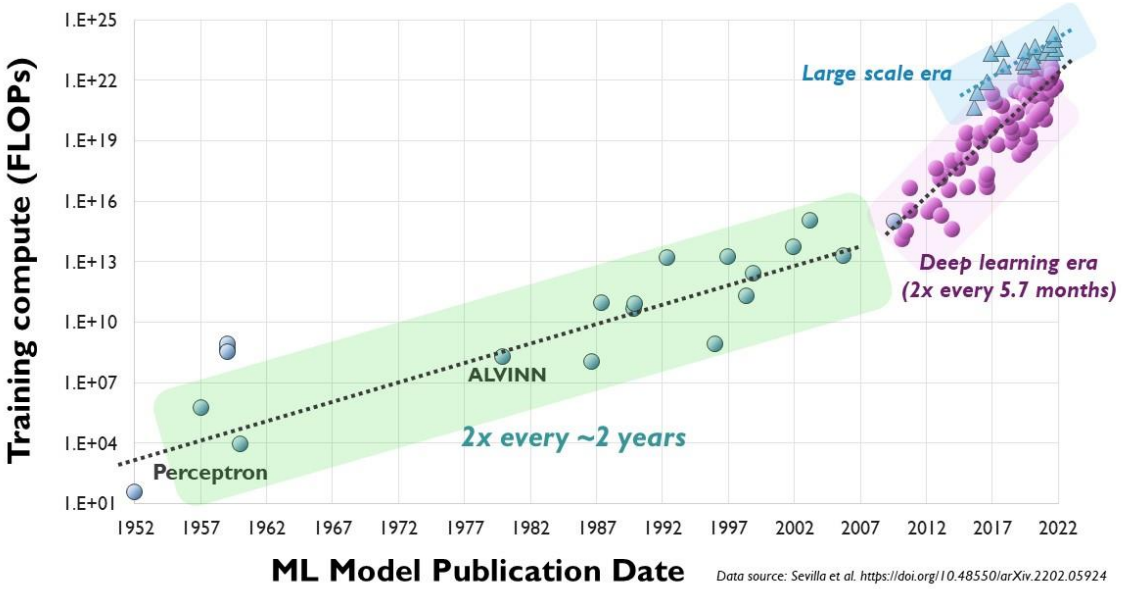


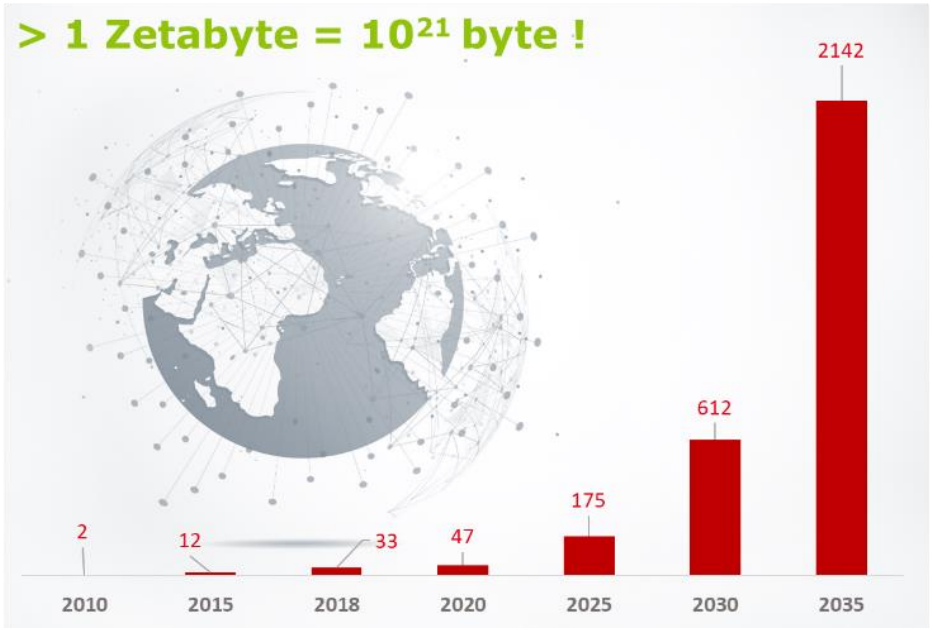
Sustainability of semiconductor manufacturing

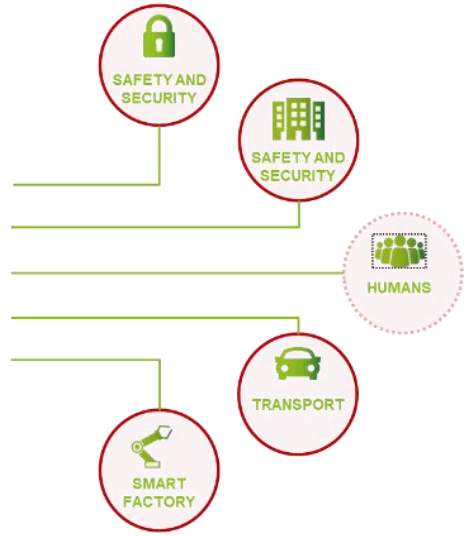


Semiconductor industry concerned about the use of fluorinated organic chemicals (termed PFAS) throughout its manufacturing process

Demand Pull for Information Processing

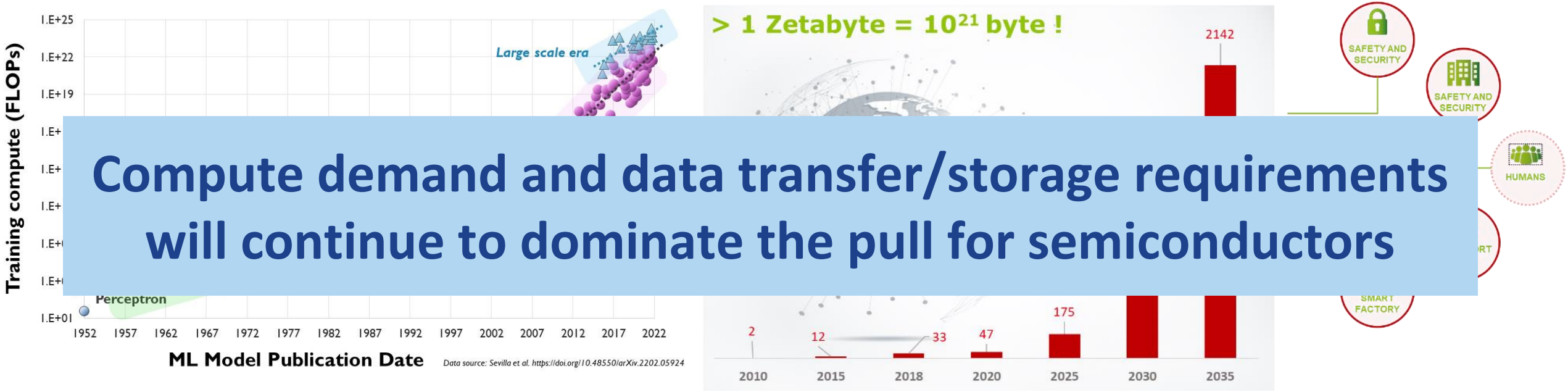






Source: Nadine Collaert (imec) & Olivier Faynot (CEA- leti)

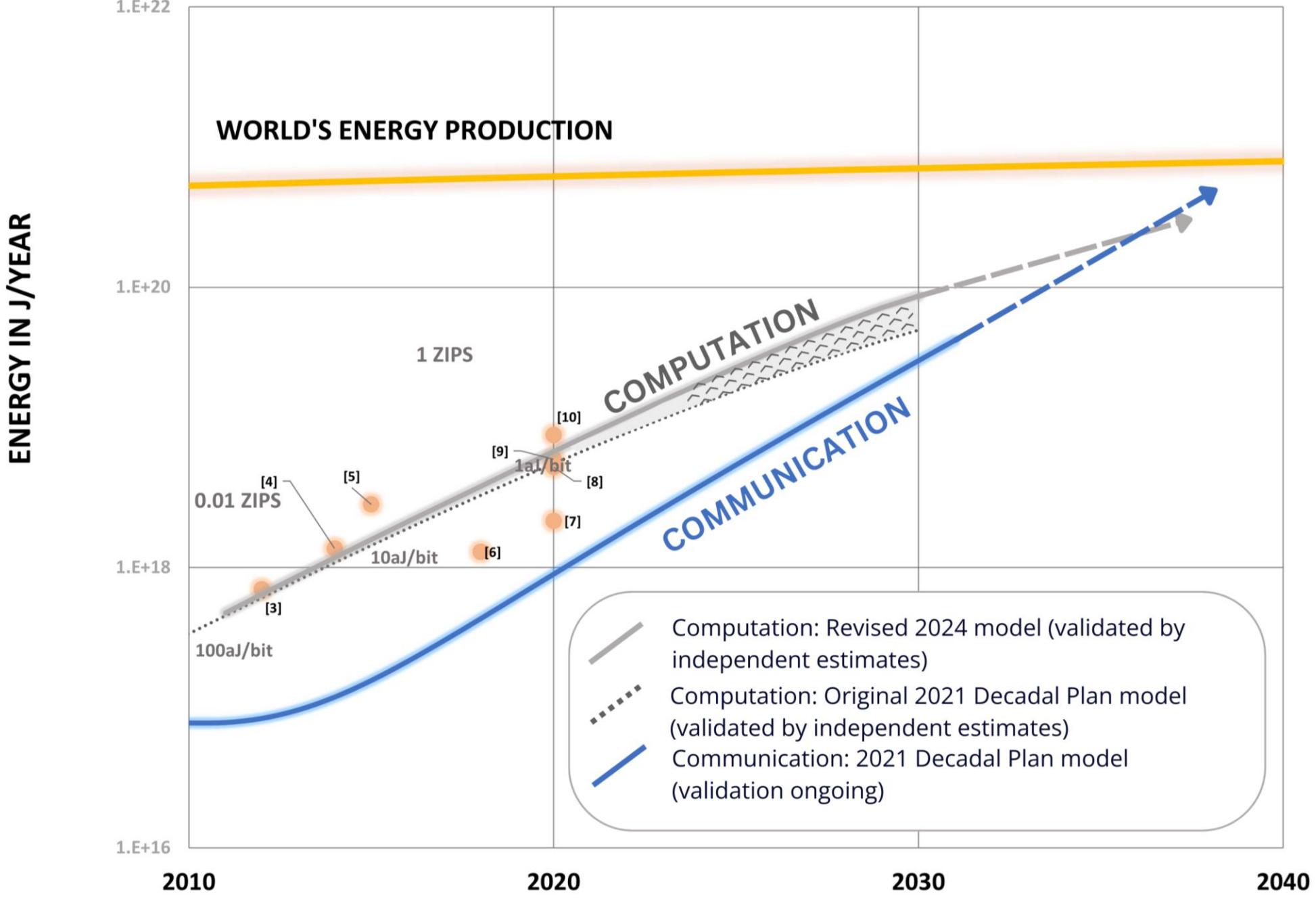
Demand Pull for Information Processing



Compute demand and data transfer/storage requirements will continue to dominate the pull for semiconductors

Source: Nadine Collaert (imec) & Olivier Faynot (CEA- leti)

ICOS
International Cooperation
On Semiconductors



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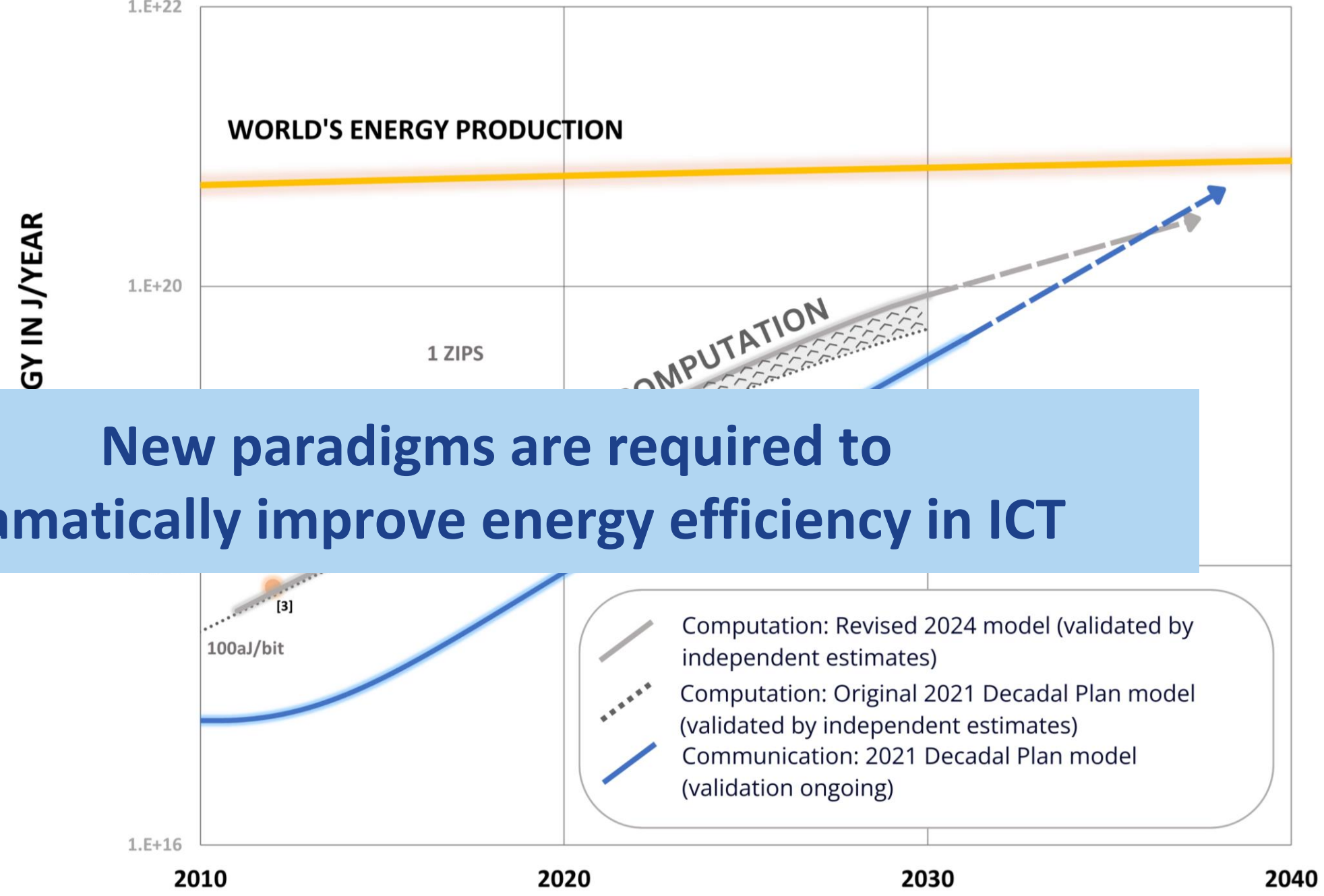


New paradigms are required to dramatically improve energy efficiency in ICT

From components to systems

World Electronic manufacturing value chain in 2023

Market service providers **61 177 B€**

Transportation, Health, Installation, Maintenance, Repair, etc.

Industrial equip. industries **1 547 B€**

Aero/Def/Secu Industries **1 439 B€**

Automotive Industry **1 971 B€**

Telecom operators, Internet, IT, Cloud, etc.

Total electronic systems **1 858 B€**

Embedded systems **902 B€**

Aerospace/Defense/Security **233 B€**

Industrial **329 B€**

Automotive **272 B€**

Health & Care **68 B€**

Stand-alone systems **956 B€**

Audio & Video **174 B€**

PCs **326 B€**

Home appliances **55 B€**

Telecoms **401 B€**

Electronic assembly **1 401 B€**

Electronic components **753 B€**

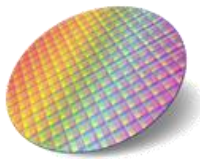
PCBs

Semiconductors

Passive & interconnect & Mechanical

Materials & tools **160 B€**

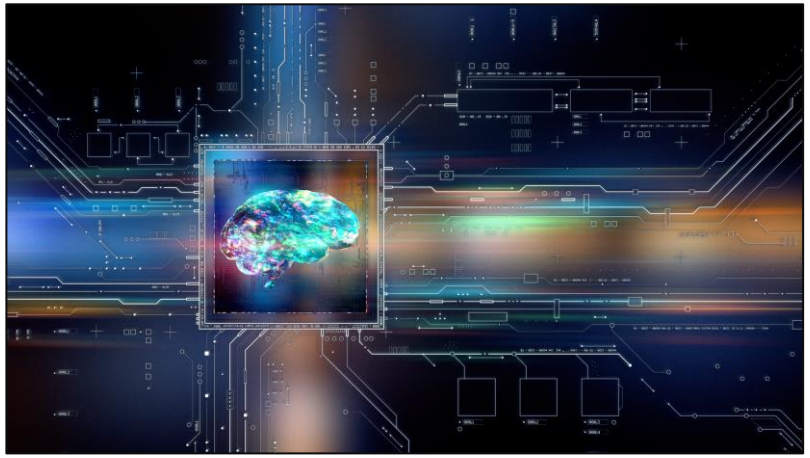
Source : DECISION Etudes & Conseil



	% EU27 / World
	17%
	11%
Stand-alone	4%
Embedded	19%
semiconductor technologies	
	7%
	7%
SC	10%
Other	3%
	19%

Diversity of Applications and Workloads

GPUs for Training



High throughput parallel compute
Very high memory bandwidth
Very high GPU-GPU bandwidth

AR/VR

Low power
Ultra low latency
High memory bandwidth
Small form factor

Autonomous driving

Multi-sensor fusion
Distributed real-time computation
Reliable and explainable AI

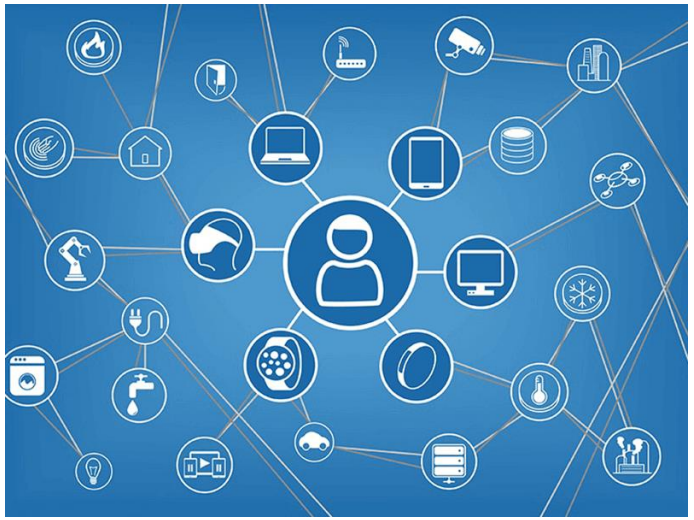
Source: Nadine Collaert (imec)

Diversity of Applications and Functionality

ubiquitous intelligence

Analog (real-time) measurements

Energy autonomy of devices



Ultra low latency

Secure and reliable data

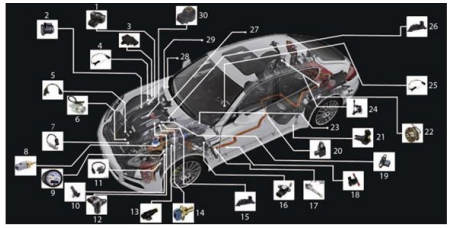
Fusion of sensor data
'Edge' data processing

Reliability and life-cycle

Cost/Economics

Environmental sustainability

Medical - Highly sterile

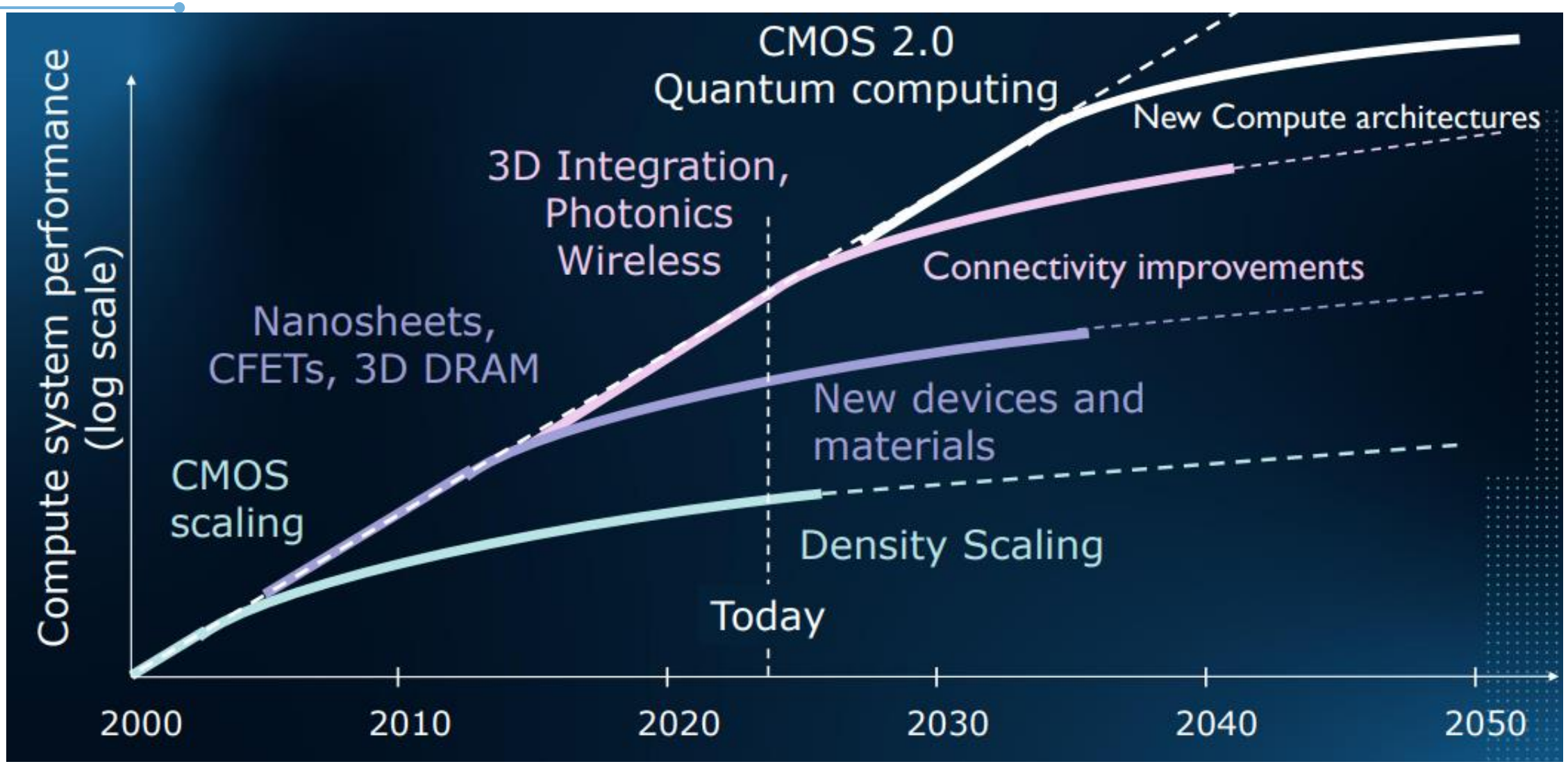


Automotive - Temperature

On-Farm - Fouling

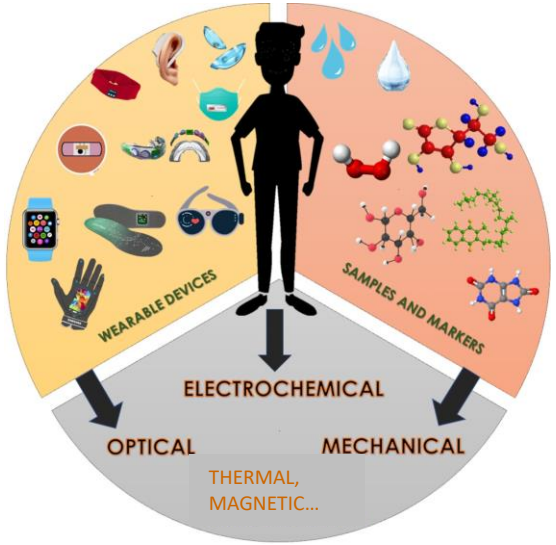
The key challenge in the development of smart systems is that a "**one size fits all" approach is not possible** due to the myriad of different deployment scenarios

Technology boosters for future compute

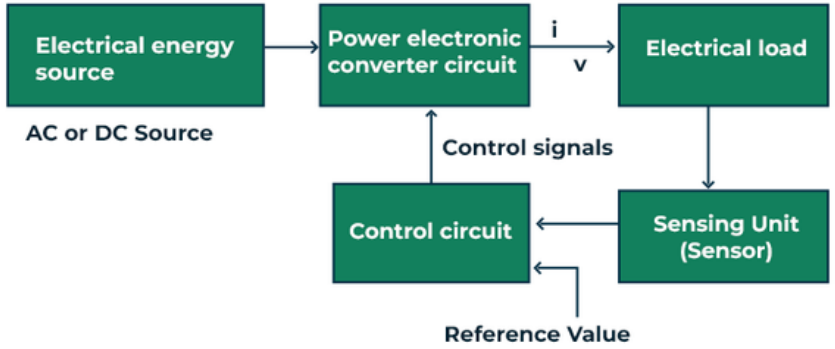


Devices for Advanced Functionality

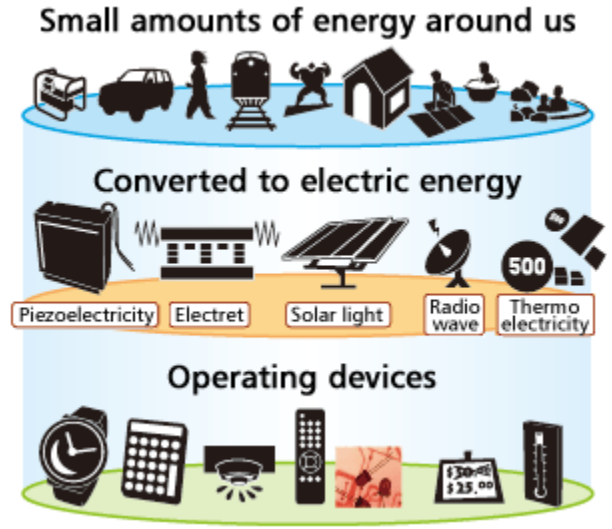
Sensors



Power Devices



Energy Harvesters



Collaboration Opportunities

How to collaborate

- Ambitious roadmapping
- Co-funded joint R&D and Innovation
- Talent Development and Education
- Joint ventures including Public-Private partnerships
- Standardisation and Regulation

What to collaborate on

Country	Key Benefit	Dependency Reduced On
US	IP tools, R&D, design frameworks	US toolchain dominance (mitigated via joint development)
Taiwan	Advanced logic chips	Asian-centred high-end production
Japan	Raw materials, equipment	Chinese material exports
South Korea	Memory & logic fab diversity	Korea-only supply vulnerabilities
India	Design, backend, scaling workforce	China/Asia-centric labour + design

A more detailed perspective

ICOS	Title	Recommendations for International Research Cooperation		
	Authors	Paolo Motto Ros, Danilo Demarchi, Nadine Collaert, Markus Pfeffer, Gustavo Ardila, Alan O'Riordan, Wim Bogaerts, Roel Baets and Georgios Fagas	Version	11

D3.3 Recommendations for International Research Cooperation

Project Number: 101092562

Project Acronym: ICOS

Project Title: International Cooperation On Semiconductors

Due date: 31/12/2024

Submission date: 21/02/2025

This project has received funding (2023 – 2025) from the European Union's Horizon Europe research and innovation programme under GA No 101092562.

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icos-semiconductors.eu

Collaboration Opportunities (Deep Dive into Technologies)

Logic

- AI-enhanced EDA tools for optimizing, verifying and predict logic designs across power, performance, area, cost, security and sustainability.
- Brain-inspired neuromorphic devices and architectures for edge computing systems, requiring low latency and high energy efficiency, including AI at the edge.
- High-bandwidth logic subsystems optimized for interconnects in network-on-chip architectures.
- Research and development of advanced transistor technologies and related manufacturing processes for future generation of FinFETs, nanosheets and CFET transistors for sub-3 nm nodes, with novel device geometries.
- Development of components enabling neuromorphic computing and quantum logic devices.
- New materials integration for alternative channel materials and added back-end-of-line (BEOL) functionality.
- Substrate thinning processes and back-side processing for new power and backside passive and active functionalization.
- Heterogeneous integration at the core of design and manufacturing processes for integrating logic cores with accelerators and memories, based on optimized IPs, and using chiplets and 2.5D/3D packaging.

Memory

- EDA solutions for emerging memory technologies, including reliability and performance modelling.
- IP design for novel memory hierarchies in data-centric computing, including persistent memory IPs for in-memory computing.
- Development of logic-in-memory designs to enable compute capabilities within memory chips.
- Designs for heterogeneous memory systems that optimize for workload-specific requirements (e.g., HPC, AI, IoT).
- System-level solutions for memory integrity verification and protection against data corruption and hacking, integrating advanced secure memory technologies for critical applications like autonomous vehicles and defence.
- Design and manufacturing of components for in-memory computing, including logic-in-memory approaches to reduce data movement and latency, exploring also FeRAM, MRAM, RRAM, phase-change memory and other storage-class memory solutions for hybrid memory/storage systems.
- Development of techniques for testing and mitigating failure mechanisms in stacked and hybrid memory architectures.

Mixed-Signal Processing

- Seamless integration of the analog and digital design and development.
- Heterogeneous simulation and modelling approaches at different levels, considering also IP libraries.
- Development of structural solutions for mitigating and preventing critical integration issues.
- Design for Testability.

Powering

- Tools and libraries that support the design of systems in the specific area of power devices and power harvesting, including Design for Testability (DFT) and Design for Manufacturability (DFM), yield management, reliability/fault tolerance and aging analysis, integration and interoperability.
- Methods and tools for integrating multiple components (e.g., passives) into a cohesive system for better performance and efficiency and for reducing the size of components while maintaining or improving performance.
- Equipment for quality control measures, ensuring that products meet industry standards and specifications and implementing real-time monitoring systems to track performance and detect issues in manufacturing equipment.
- Wide band gap (e.g., SiC, GaN) and ultrawide band gap materials (e.g., AlN, GaOx, diamond) for power devices.
- Focusing on energy harvesting:
  - Development of environmentally friendly materials for energy harvesters.
  - Develop comprehensive system design including all process aspects for increasing power generation efficiency.
  - A general limitation towards industrial adoption of Energy Harvesting is its reliance on environmental conditions. Developing Energy Harvesting combined with on-demand charging of the device could help solving this issue.

Sensing

- New approaches are required to facilitate integration of sensor performance into traditional simulation tools such as SPICE. This will enable seamless integration of the full sensor system.
- Key challenges remain around the need to calibrate individual sensors, ML methods at different levels are required to address these challenges.
- Scaling up sensor functionalisation and characterisation in-line with wafer-scale production.
- Developing of safe and sustainable and design fabrication, modification and characterisation.
- Advanced sustainable (bio)materials innovation and integration of in new, highly sensitive and more versatile sensors.

Communication

- ML-enabled tools for designing, optimizing, and integrating RF and mixed-signal circuits for 5G/6G applications, including system-level co-simulation of digital, analog, and RF components in heterogeneous systems.
- New materials for RF, mmWave and sub-THz devices, advanced dielectric materials and substrates for wireless/wireline applications and components.
- Innovations in the co-integration of passives with active components in heterogeneous systems, progress in antenna-on-chip and antenna-in-package technologies for high-frequency applications.
- Techniques to scale RF technologies alongside digital nodes while ensuring performance and reliability.

Photonics

- Tools for photonic active and passive circuit design and photonic-electronic codesign, layout, and simulation, including IP libraries and across multiple technology platforms.
- Heterogeneous and hybrid photonic-electronic integration platforms including multi-chip modules/chiplet integration, integration of light sources, back-end and front-end heterogeneous integration, optical fiber coupling and package design.
- Development of PDKs, ADKs etc. for rapid prototyping, bypassing long chip iteration cycles
- High-volume pure-play foundries for photonic integrated circuits, out-sources assembly and test providers (OSAT).