CEZAMAT, Warsaw - May 12-13th

ICOS Workshop

Key emerging technologies for future industrial applications

icos-semiconductors.eu

Programme

Day 1: May 12th afternoon

- **13:45 – 14:00 Welcome, Horizon Europe ICOS: EU and Non-EU Strengths, Weaknesses, Dependencies, Opportunities for International Collaboration – Francis Balestra (ICOS Coordinator)**

- **14:00 - 17:00 Interactive session: Turn risks into chances: closing gaps in the semiconductor value chain – Moderators: Melanie Hentsche, Sven Bökemeier, Monika Curto Fuentes (VDI VDE), Beth McEvoy (Future of UK Semiconductor R&D – *UKRT Grant*)**

Coffee Break 17:00 – 17:30

- ***17:30* – 19:00 Standardisation session. Working Group StandICT.eu / AllPros.eu / ICOS**

19:00 Networking Cocktail

Day 2: May 13th

- **8:45 – 12:00 EU International Cooperation on Semiconductors: Opportunities and Challenges – Chairs: Paolo Motto Ros, Danilo Demarchi (Politechnico di Torino), Giorgos Fagas (Tyndall National Institute)**

- 8:55 – 9:15 India and USA, Rakesh Kumar, Chair of IEEE Future Directions, DataPort, Past-chair IEEE Roadmaps
- 9:15 – 9:45 China and Singapore, Yong lIan, IEEE Division 1 Director, member of the IEEE Board of Directors
- 9:45 – 10:05 Taiwan, Dr. Tuo-Hung Hou, Director General of the Taiwan Semiconductor Research Institute (TSRI)

10:05 – 10:30 Coffee Break

- 10:30 – 10:50 India, Group Coordinator (R&D) at Ministry of Electronics & IT, Sunita Verma
- 10:50 – 11:10 South Korea, Myung Hoon Sunwoo, IEEE Circuits and Systems Society President
- 11:10 – 11:30 Japan, Hiroyuki Akinaga, University of Hokkaido / National Institute of

Advanced Industrial Science and Technology (AIST)

- 11:30 – 12:00 Panel of Experts

12:00 Lunch Break

- **14:00 – 14:45 International cooperation for a resilient Europe: priorities and opportunities – Mattias Verstuyft (ePIXfab)**

- **14:45 – 16:00 The emerging value chains according to the development of partnerships - Krzysztof Mieszkowski, (CEZAMAT WUT)**

16:00 – 16:30 Coffee Break

- **16:30 – 17:45 Panel Session “Potential international collaborations on emerging semiconductor technologies” Chair : Peter Ramm Fraunhofer EMFT**

- Hiroyuki Akinaga, from AIST and Hokkaido University, Japan
- Mustafa Badaroglu, Qualcomm, San Diego, USA
- Georgios Fagas, Tyndall, Cork, Ireland
- Dominique Noguet, CEA-Leti, France
- Mikael Ostling, KTH, Stockholm, Sweden
- N.N., ESMC, Amsterdam, Netherlands

18:00 Visit of CEZAMAT

19:30 Networking Dinner

Detailed Programme

Welcome Note - Horizon Europe ICOS: EU and Non-EU Strengths, Weaknesses, Dependencies, Opportunities for International Collaboration

Abstract:

The main objectives and outcomes of the Horizon Europe project ICOS dedicated to International Cooperation on Semiconductors will be presented. International cooperation is key for speeding up technological innovation, reducing cost by avoiding duplicated research, boosting the resilience of the semiconductor value and supply chains, and is one of the objectives of the EU Chips Act. The main ICOS results dealing with the analysis of the semiconductor economic and technological landscapes in Europe and leading semiconductor countries, as well as the identification of areas of potential cooperation on advanced functionalities and computing will be highlighted.

Speaker

Francis Balestra, CNRS Research Director at CROMA, is Director Emeritus of the European SINANO Institute and President of IEEE Electron Device Society France, and has been Director of several Research labs. He coordinated several European Projects (NEREID, NANOFUNCTION, NANOSIL, etc.) that have represented unprecedented collaborations in Europe in the field of Nanoelectronics, and is currently coordinator of the Horizon Europe ICOS project dedicated to International Cooperation on Semiconductors with leading semiconductor countries.

He founded and organized many international Conferences, and has co-authored more than 500 publications. He is member of several European Scientific Councils, of the Advisory Committees of International Journals and of the IRDS (International Roadmap for Devices and Systems) International Roadmap Committee, as representative of Europe.

Session 1 – Turn risks into chances: closing gaps in the semiconductor value chain

Abstract:

This session is co-organised with the project *Future of UK Semiconductor* R&D, funded as part of the UKRI grant and commissioned by DSIT.

International cooperation is a key objective of the ICOS project. By encouraging diverse perspectives, we can develop actionable strategies to achieve this goal. The interactive workshop will engage participants in group discussions to identify main gaps in the European semiconductor value chain and explore solutions to turn risks into opportunities. Through collaborative brainstorming and case studies, we will focus on measures needed in critical areas such as advanced materials, packaging technologies, design methods, and AI-driven innovations.

Join us to contribute your insights and shape the future of Europe's semiconductor industry!

Speakers:
Melanie Hentsche ; Sven Bokemeier ; Monika Curto Fuentes ; Beth McEvoy

Session 2 – Standardisation

Speakers:
Working group StandICT.eu / AllPros.eu / ICOS
Ryoishi Ishira
Salahuddin Nur

Abstract:
Coming Soon

Session 3 – EU International Cooperation on Semiconductors : Opportunites and Challenges

Abstract

The session aims to have contributions from non-EU leading experts about the strengths and weaknesses of seven countries (Japan, South Korea, USA, Singapore, Taiwan, India, China) in the semiconductor value chain and propose recommendations for international research cooperation.

Chairs:

Giorgos Fagas PhD MBA is Head of CMOS++ and EU Programmes at Tyndall, and member of Tyndall's Leadership Team. CMOS++ is a strategic programme addressing emerging materials, devices and architectures for next-generation information processing interfacing with CMOS and beyond. He is contributor to key international strategic R&I agendas incl. the ECS-SRIA and IRDS and has initiated several large-scale EU projects. He currently leads the EU-funded programmes for open access to infrastructure for early-stage research on nanoelectronics and semiconductor chips, respectively, ASCENT+ and INFRACHIP, and the ICOS project activity on Technology Scanning and Foresight. Giorgos holds prominent positions in various policy and industry groups including Director of the SiNANO Institute.

Danilo Demarchi is a full Professor at Politecnico di Torino, Department of Electronics and Telecommunications. Micro&Nano Electronics, Smart System Integration and IoTs for the AgriFood Value Chain and for BioMedical Devices. Author and co-author of 5 patents and more than 350 scientific publications in international journals and peer-reviewed conference proceedings. Leading the eLiONS Laboratory of Politecnico di Torino and coordinating the Italian Institute of Technology Microelectronics group at Politecnico di Torino (IIT@DET). Member of the IEEE Sensors Council and the BioCAS Technical Committee. Associate Editor of the IEEE Open Journal on Engineering in Medicine and Biology (OJ-EMB).Open Journal on Engineering in Medicine and Biology (OJ-EMB).

Paolo Motto Ros
Coming soon

International Talks:

- South Korea, Myung Hoon Sunwoo, IEEE Circuits and Systems Society President
- China and Singapore, Yong Ilan, IEEE Division 1 Director, member of the IEEE Board of Directors
- Japan, Hiroyuki Akinaga, University of Hokkaido / National Institute of Advanced Industrial Science and Technology (AIST)
- India and USA, Rakesh Kumar, Chair of IEEE Future Directions, DataPort, Past-chair IEEE Roadmaps
- Taiwan, Dr. Tuo-Hung Hou, Director General of the Taiwan Semiconductor Research Institute (TSRI)

Speakers:

Hiroyuki Akinaga (Senior Member, IEE) received the B.E., M.E., and Ph.D. degrees from the University of Tsukuba, Ibaraki, Japan, in 1987, 1989, and 1992, respectively. Currently, he is the Principal Research Manager, Device Technology Research Institute, National Institute of Advanced Industrial Science and Technology (AIST). He is co-leader of the Beyond CMOS Working Group (WG) at International Roadmap for Devices and Systems (IRDS), Japanese leader of the research field of energy harvesting at More-than-Moore WG, and a strategic committee member at WG of Environment, Health, Safety and Sustainability (ESHS). He has been serving as a convenor at International Electrotechnical Commission (IEC), TC113 (Nanotechnology for electrotechnical products and systems), WG7 (Reliability) and WG13 (Wafer-Scale System Integration). He is a fellow of Japan Society of Applied Physics. His current interests include nanoelectronics and open innovation platform

Coming soon

Session 4 – International cooperation for a resilient Europe: priorities and opportunities

Abstract:

We will present an analysis of the most urgent challenges facing the European semiconductor field and identify opportunities for international cooperation with other regions. This analysis is based on a survey polling experts in the field as well as previous work done in ICOS. We will finish by requesting feedback and opinions on this analysis from the audience

Mattias Verstuyft got his master thesis in theoretical physics at the University of Ghent in 2016, after which he did a PhD in silicon photonics at the Photonics Research Group in Ghent University under prof. Bart Kuyken. After managing several EU funded photonics projects with industrial and academic partners (through ActPhast and PhotonHub Europe), he started working as the technical coordinator of ePIXfab – the European silicon photonics alliance – where he handles day-to-day operations, coordinates trainings and other activities, and advocates on behalf of its members and the silicon photonics community at large.

Session 5 – The emerging value chains according to the development of partnerships

Abstract:
Coming soon

Krzysztof Mieszkowski is a researcher at the Centre for Advanced Materials and Technologies CEZAMAT at Warsaw University of Technology. He has almost 20 years of professional experience in the field of scientific research and development and higher education, including aspects of research and innovation policy. From 2012 to 2019, he worked at the European Commission's Joint Research Centre in Seville. As a member of the Smart Specialisation team, he was involved in promoting and implementing the concept of smart specialisation.
That time, he also dealt with the Key Enabling Technologies theme and in the activities of the Thematic Platform on Smart Specialisation for Industrial Modernisation. He used to be a member of working groups of the European Commission and the OECD.

Panel Session – International Cooperation (Chips Act related subjects)

Chair: Peter Ramm, Fraunhofer EMFT

Abstract:
The renowned panelists from universities, RTOs and industry will identify and discuss critical needs for future semiconductor technologies. The main goal is to identify emerging opportunities for international R&D initiatives/collaborations/partnerships – with the feedback of the audience.
Key technological challenges to be discussed are in the fields of More Moore, Beyond CMOS and More than Moore, as – but not limited to – CMOS scaling, advanced patterning technology, RF devices, memory, power devices, sensing technologies & MEMS, FDSOI, 2D materials, quantum computing, neuromorphic computing, heterogeneous integration, advanced packaging and microelectronics assembly.

Panelists:

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Giorgos Fagas PhD MBA is Head of CMOS++ and EU Programmes at Tyndall, and member of Tyndall's Leadership Team. CMOS++ is a strategic programme addressing emerging materials, devices and architectures for next-generation information processing interfacing with CMOS and beyond. He is contributor to key international strategic R&I agendas incl. the ECS-SRIA and IRDS and has initiated several large-scale EU projects. He currently leads the EU-funded programmes for open access to infrastructure for early-stage research on nanoelectronics and semiconductor chips, respectively, ASCENT+ and INFRACHIP, and the ICOS project activity on Technology Scanning and Foresight. Giorgos holds prominent positions in various policy and industry groups including Director of the SiNANO Institute.

Dominique NOGUET holds an engineering degree of the National Institute of Applied Sciences (INSA) in electrical engineering in 1992, an MSc in microelectronics in 1994, and a PhD from National Polytechnic Institute of Grenoble (INPG) in 1998. He started his carrier as an IC designer for telecommunication applications and then project manager in the same field. He led many projects at a national level (coordination of ANR projects) and in several European frameworks (FP5, FP6, FP7) in which he gained expertise and acknowledgement in the field of wireless design and cognitive radio (CR).

In this field, he has been a key member of several IEEE standard groups and was subsequently elevated to the grade of IEEE Senior Member for his contributions. In parallel he held managerial positions at CEA-Leti as lab manager and department manager. He was involved in ANR project selection committees and a reviewer of project proposals for the EU. In January 2023, he was appointed project manager for the ‘France 2030’ flagship project NextGen on FD-SOI advanced nodes and reports to Leti’s CEO since then. He is currently the project coordinator of the FAMES Pilot Line. Dominique has authored or co-authored ~100 scientific papers (several best paper awards), book chapters and holds 18 patents. He was a reviewer and a member of scientific committees of many conferences and a member of journal editorial boards. He was conference chair and TPC chair of several international conferences.

Mustafa Badaroglu works at Qualcomm with focus on technology ramp and architecture enhancements of AI chipsets, ultra-low voltage process and design methods and stacked memory technologies. Before joining Qualcomm, he previously worked at Huawei, imec, ON Semiconductor, and Tubitak Space. During his career he had various assignments for the execution and management of mobile and automotive chipset design from concept to initial ramp, process technology pathfinding, and system technology co-optimization. He holds a PhD in electrical engineering from the Catholic University of Leuven in Belgium

Mikael Östling received his MSc and the PhD degrees from Uppsala University, Sweden. He was deputy president of KTH between 2017-2022. His research interests are nanoscaled Si and Ge device technologies and emerging 2D materials, as well as device technology for wide bandgap semiconductors for high power/high temperature applications. He has supervised 47 PhD theses work and co-authored 500+ scientific papers published in international journals and conferences. Östling was an editor of the IEEE Electron Device Letters 2005-2014 and editor in chief of the IEEE J-EDS 2016-19. Östling is a Fellow of the IEEE.

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Chairman
IRDS International Roadmap for Devices and Systems

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