International Cooperation On Semiconductors

Recommendations for International Research Cooperation

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Executive Summary

The deliverable aims to evaluate the strengths and weaknesses of seven countries (Japan, South Korea, USA, Singapore, Taiwan, India, China) in the semiconductor value chain and propose recommendations for international research cooperation.

The first aim is to establish a comprehensive evaluation methodology by defining strengths/weaknesses and opportunities/challenges within the semiconductor value chain, ensuring all scenarios are non-overlapping and fully cover the ecosystem.

The second aim is a quantitative validation through expert surveys, providing insights into each country's positioning across defined axes. The analysis partitions the semiconductor field into categories like logic, memory, mixed-signal processing, and stages like chip design, manufacturing, and equipment tools.

Results of the analysis are recommendations and suggested topics for international research cooperation. These will be shared with international (EU and, most importantly, non-EU) experts, contributing to actionable insights for international research collaboration.

1 Overview

1.1 Purpose

The purpose of this deliverable is to present the work done towards identifying strengths and weaknesses of each country under consideration (Japan, South Korea, USA, Singapore, Taiwan, India, China), by leveraging insights from previous studies, knowledge from the consortium and partner network, desk research, and brainstorming sessions, and therefore to propose corresponding recommendations for international research cooperation.

- The first objective is to establish the investigation and evaluation methodology/ framework: strengths/weaknesses and opportunities/challenges should be clearly defined with respect to a specific context/aspect, with the set of all the scenarios not overlapping and covering the entire semiconductor value chain and ecosystem. The main objective of this activity is to obtain a qualitative evaluation of the scenario.
- The second objective is to quantitatively assess the key points previously identified by asking and collecting information from international (non-EU and working in the countries of interest) experts in the field so as to have the needed feedback and validate the proposed recommendations. The work is based on a survey to be sent to the experts; the obtained results

will give the quantitative indication of the different strengths and weaknesses of each country of interest.

2 First Objective: Investigation and Evaluation Methodology/ Framework

2.1 Proposed Approach

For the evaluation framework, two complementary perspectives have been taken into consideration:

- The *first one, "Across the value chain",* has the aim of grouping all the possible applications (from the research, design, development, and fabrication point of view, not from a final end-user/consumer one), independently of which segment of the value chain is mostly involved.
- The *second one, "Through the value chain",* has the aim of partitioning the value chain into subsets of homogeneous related activities, major research fields, or major steps/processes in the overall semiconductor industry, independently of the intended target application of the final product.

It is very clear that, since the goal is to evaluate the strengths and weaknesses of a country, considering only one of those approaches would not be enough to give a clear picture of the scenario according to the scope of the overall project. Indeed, it is better to consider them as complementary or, better, as two (somehow orthogonal) axes (even if categorical and not necessarily ordered), along which quantitatively estimate strengths and weaknesses.

As a result, the proposal for the partitioning of the semiconductor field has been the following:

- Across the value chain:
  - Logic
  - Memory
  - Mixed-signal processing
  - Powering
  - Sensing
  - Communicating
  - Photonics;

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- Through the value chain:
  - EDA & IP
  - Chip design
  - System design
  - Material integration
  - Components
  - Manufacturing (front-end)
  - Manufacturing (back-end)
  - Equipment & Tools (front-end)
  - Equipment & Tools (back-end).

Concurrently, an interesting exercise done (not with the full set of applications) has been to estimate quantitatively, for each country, each point “indexed” by the two previously defined axes. In order to understand and validate the effectiveness of the proposed methodology itself, we preferred to focus on the industry ecosystem initially; therefore, we did not consider, at this stage, RTOs and universities (whose impact on the overall ecosystem is more complex to evaluate). We therefore collected, analysed and ordered (according to the proposed framework), for each country, a fairly representative set of actors in the semiconductor field, and then scored the overall impact of the country (given the target application and the value chain segment) with values between 1 (very weak) and 5 (very strong/leading position), and -1 indicating the possibility of not having yet enough information in the related case.

Very preliminary results have been thus obtained and synthesized as a pair of two spider maps (for providing a better visual idea as well, other than quantitative information) for each country (see Figures 1–7), presented and discussed with the other partners and experts in the field involved in the project.

The selected target countries are:

- Japan
- South Korea
- USA
- Singapore
- Taiwan
- India
- China

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Japan

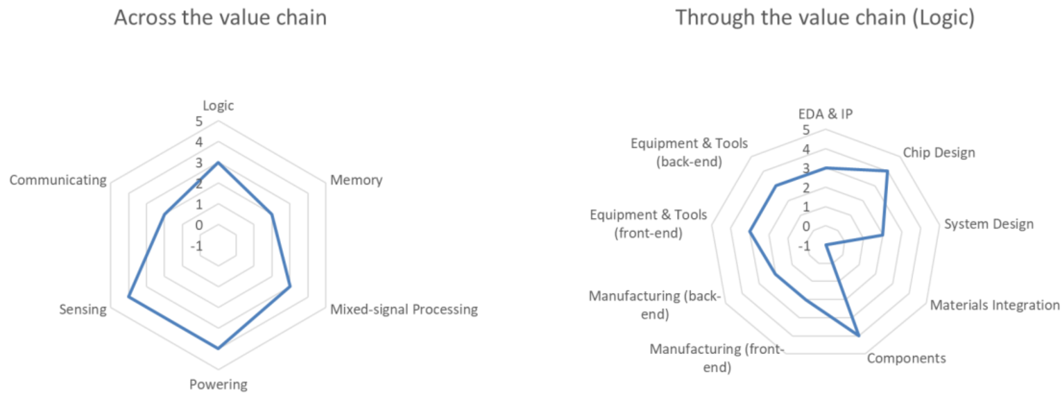

Figure 1 Japan strengths and weaknesses in the semiconductor industry — preliminary analysis.

South Korea

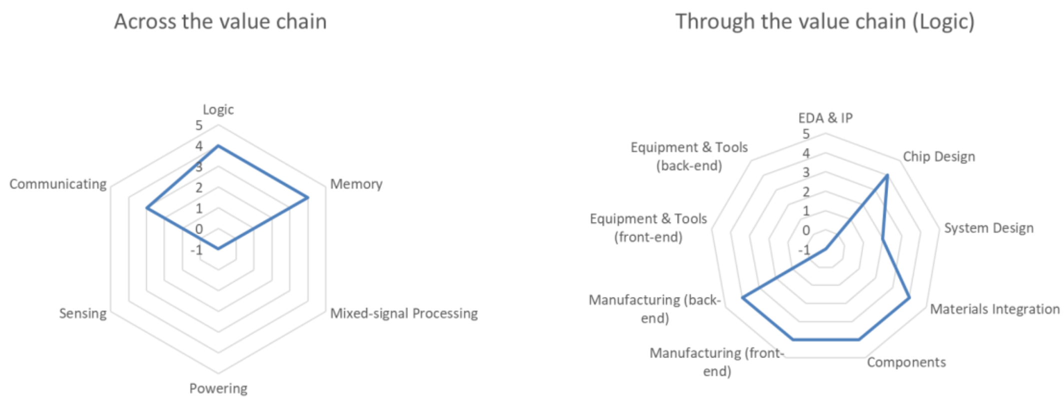

Figure 2 South Korea strengths and weaknesses in the semiconductor industry — preliminary analysis.

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USA

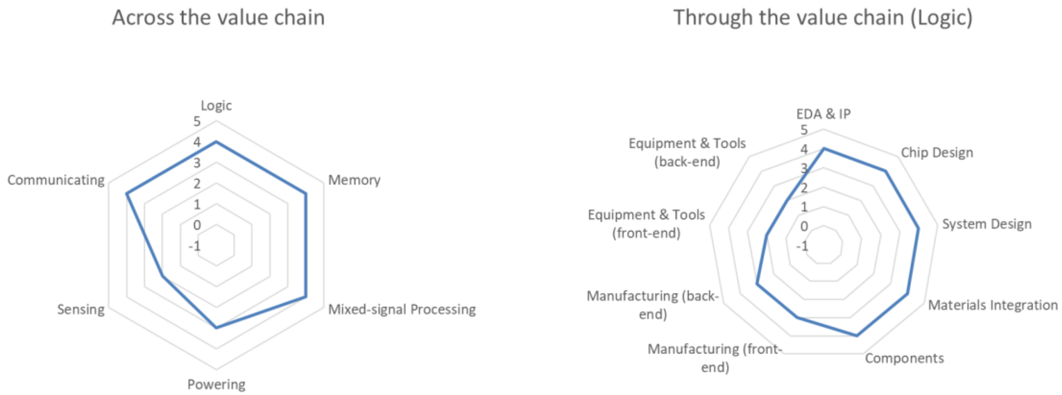

Figure 3 USA strengths and weaknesses in the semiconductor industry — preliminary analysis.

Singapore

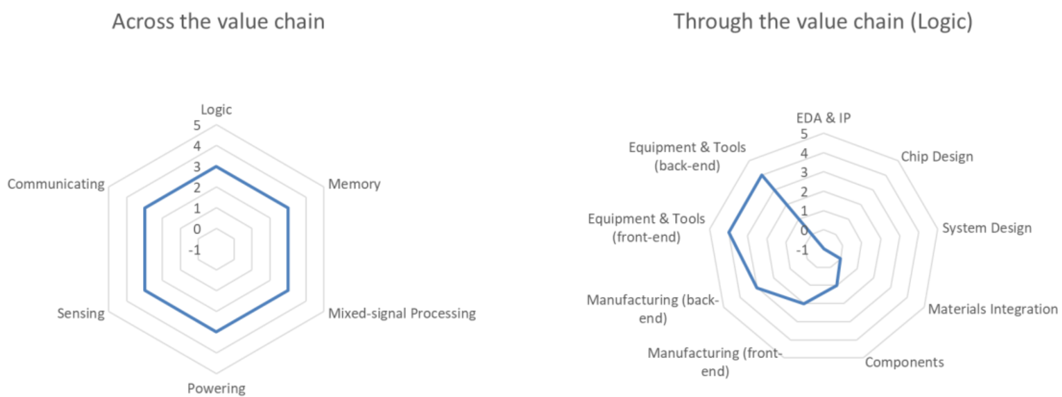

Figure 4 Singapore strengths and weaknesses in the semiconductor industry — preliminary analysis.

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Taiwan

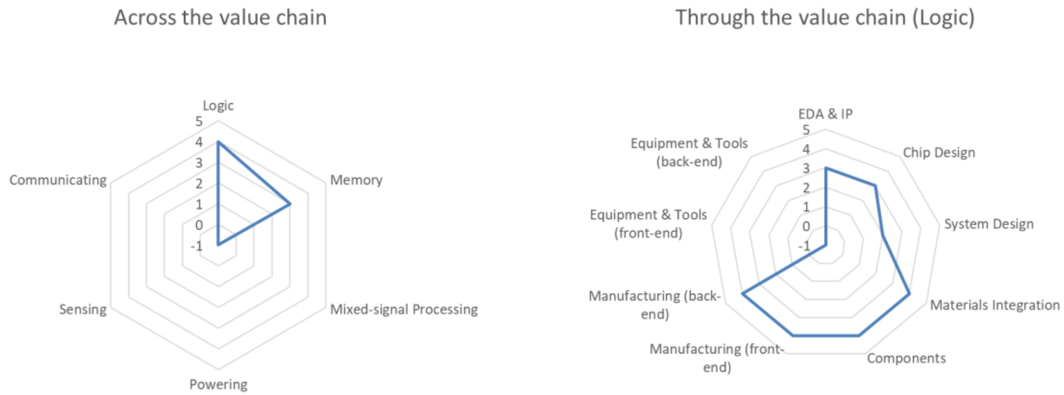

Figure 5 Taiwan strengths and weaknesses in the semiconductor industry — preliminary analysis.

India

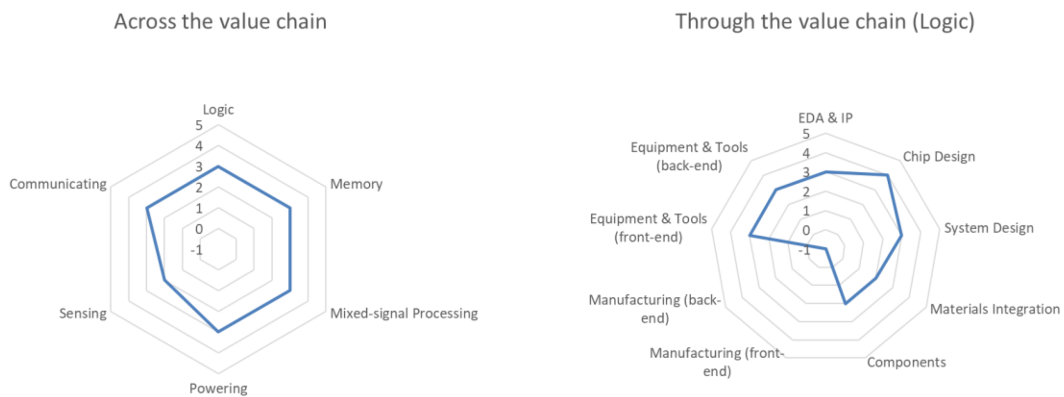

Figure 6 India strengths and weaknesses in the semiconductor industry — preliminary analysis.

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China

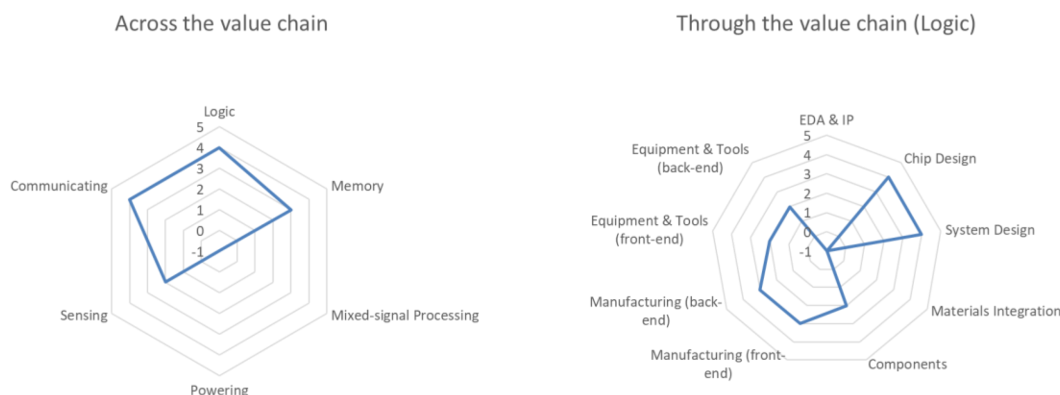

Figure 7 China strengths and weaknesses in the semiconductor industry — preliminary analysis.

3 Second Objective: Quantitatively Assess the Key Points about the International Research Cooperation Topics

The further important activity carried out as a part of the Task 3.3 has been first to detail, to map the research cooperation topics on the proposed framework, and then to design a questionnaire for non-EU experts (at the country level). The final goal will be to collect evaluations, feedback, and comments on the strengths and weaknesses, across and through the semiconductor value chain (as previously recommended and proposed), of each of the target countries. To this end, for each research field, for each segment of the value chain, specific research cooperation challenges and opportunities have been identified and proposed, asking to the recipients to score them depending on the specific country strength on the matter; the opportunity to suggest further cooperation points has been made available as well. In two cases (Powering and Communicating) further specific aspects of, or closely related to, the semiconductor value chain, Energy Storage Devices (solid state thin film solutions) and Equipment & Tools for test/metrology, respectively, have been deemed fundamental and therefore added to the survey. The target audience of the survey has been selected based on available contacts inside the consortium and partner network, renowned leading experts in the fields, available lists of established experts with roles and responsibilities in the related scientific communities, all operating in, or with a solid knowledge and experience about, one or more target countries.

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After brainstorming sessions, meetings, and revisions among the involved partners, the suggested international cooperation topics have been proposed and categorised in the following sections.

3.1 Logic

3.1.1 EDA & IP

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the EDA & IP segment of the semiconductor value chain for the Logic research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Development of AI-enhanced EDA tools for optimizing logic designs across power, performance, area, cost and sustainability (PPACE).
- Tools for advanced node design enablement (e.g., 3 nm and beyond), addressing challenges like variability, aging, and lithography limitations.
- Techniques for RTL-to-GDSII automation in increasingly complex designs.
- High-quality, scalable IPs for standard cells, memory compilers, and other foundational components.
- IPs optimized for heterogeneous integration in multi-die and chiplet-based solutions.
- Development of secure logic IPs with built-in cryptographic and anti-tampering capabilities.
- EDA solutions for comprehensive design-for-testability strategies in logic designs.
- Simulation and formal verification tools for error-free complex logic circuits at extreme scales.
- Leveraging machine learning for adaptive synthesis and layout generation in complex logic chips.
- AI-driven tools for predictive failure analysis during logic design and manufacturing.

3.1.2 Chip Design

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the Chip Design segment of the semiconductor value chain for the Logic research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Design of general-purpose processors, AI accelerators, and GPUs with cutting-edge performance.
- Techniques for optimizing pipeline depth, clock speeds, and instruction-level parallelism in logic chips.

- Development of ultra-low-power logic designs for mobile devices, IoT, and wearable applications.
- Techniques for dynamic voltage and frequency scaling and other power-saving mechanisms.
- Chip designs optimized for chiplet-based architectures, integrating logic with memory, analog, and other components.
- Architectures enabling co-packaged optics for high-bandwidth data transmission in logic-intensive applications.
- Logic designs featuring error correction codes and redundancy mechanisms for improved reliability.
- Designs focused on self-repairing logic circuits and real-time fault detection for mission-critical applications.

3.1.3 System Design

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the System Design segment of the semiconductor value chain for the Logic research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- System-level designs for multi-core processors, optimized for scalability and parallelism in high-performance computing.
- Architectures for edge computing systems, requiring low latency and high energy efficiency.
- System designs incorporating AI-optimized processors, such as TPUs and NPUs.
- Architectures for AI at the edge, leveraging compact and efficient logic designs.
- System-level designs focusing on energy-efficient data centers and cloud computing environments.
- High-bandwidth logic subsystems optimized for interconnects in network-on-chip architectures.
- System-level solutions for trusted execution environments and secure boot mechanisms in logic-centric systems.
- Integration of logic encryption techniques to protect intellectual property and user data.

3.1.4 Materials Integration

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the Materials Integration segment of the semiconductor value chain for the Logic research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

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- Research into new materials for transistor scaling (e.g., 2D materials, nanosheet and CFET compatible materials).
- Research into novel high-k dielectrics and metal gates for further scaling logic transistors.
- Innovations in contact materials and dielectrics for low-power logic devices.
- Integration of materials for heterogeneous 2D/3D logic systems.
- Techniques for integrating logic layers in monolithic 3D architectures (e.g. CFET), addressing thermal and interconnect challenges.
- Materials enabling vertical integration of logic chips with minimal performance degradation.
- Advanced thermal interface materials for efficient heat dissipation in high-density logic architectures.
- Stress-resilient materials for mechanical stability during manufacturing and operation of logic chips at advanced nodes.

3.1.5 Components

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the Components segment of the semiconductor value chain for the Logic research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Research and development of advanced transistor technologies such as FinFETs, nanosheets and CFET transistors for sub-3 nm nodes.
- Exploration of alternative materials for the channel (e.g. SiGe, 2D materials).
- Development of integrated passive components (e.g., capacitors, resistors, inductors) for System-on-Chip (SoC) and heterogeneous integration.
- R&D into passive components for power integrity and signal integrity in high-frequency and low-power logic circuits.
- Development of components enabling neuromorphic computing and quantum logic devices.
- R&D into materials and devices for beyond-CMOS technologies, including spintronics and carbon nanotubes.

3.1.6 Manufacturing (front-end)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the front-end Manufacturing segment of the semiconductor value chain for the Logic research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

This project has received funding (2023 – 2025) from the European Union’s Horizon Europe research and innovation programme under GA No 101092562.

- Development of advanced lithography techniques (e.g., EUV and beyond) to achieve feature sizes for sub-3nm nodes.
- R&D into process optimization for reducing variability and managing layout-dependent effects in advanced nodes.
- Implementation of high-k/metal gate materials and low-resistance interconnects for next-generation logic devices.
- Exploration of new doping techniques and materials for ultra-thin channel layers.
- Manufacturing processes for stacked nanosheet and CFET transistors and other novel device geometries.
- Techniques for addressing power-density challenges in high-performance computing logic chips.
- Substrate thinning processes and back-side processing for new power and backside passive and active functionalization.

3.1.7 Manufacturing (back-end)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the back-end Manufacturing segment of the semiconductor value chain for the Logic research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Manufacturing techniques for low-resistance, high-reliability interconnects at sub-3 nm nodes (e.g., alloys, alternative conductors).
- R&D into air-gap dielectric technologies to reduce RC parasitics.
- Processes for integrating logic cores with accelerators and memory using chiplets and 2.5D/3D packaging.
- High-precision assembly techniques for heterogeneous system integration.
- Back-end processes for integrating advanced thermal management materials, such as TIMs (Thermal Interface Materials).

3.1.8 Equipment & Tools (front-end)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the front-end Equipment & Tools segment of the semiconductor value chain for the Logic research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Development of advanced lithography tools (e.g., EUV lithography) and metrology equipment for sub-3 nm nodes.
- Innovations in defect detection and critical dimension measurement tools to ensure high yields in logic chip production.

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- Tools for electrical and thermal characterization of transistors at advanced nodes (e.g., FinFETs, nanosheets and CFET).
- Development of equipment for measuring variability in nanoscale devices and creating reliable early device models for design enablement.
- Equipment for deposition, etching, and doping processes for higher-mobility/alternative channel materials like SiGe and 2D materials.
- R&D into ALD and ALE tools for precise control of material layers in leading-edge process technologies.

3.1.9 Equipment & Tools (back-end)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the back-end Equipment & Tools segment of the semiconductor value chain for the Logic research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Tools for processing advanced materials, such as copper-alternative conductors and low-k dielectrics, to reduce interconnect resistance and capacitance.
- Development of high-precision equipment for TSV and micro-bump bonding in 3D integration of logic chips.
- Equipment for integrating logic cores with high-bandwidth memory or other accelerators in chiplet-based systems.
- R&D into advanced redistribution layer tools for improved signal and power integrity.

3.2 Memory

3.2.1 EDA & IP

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the EDA & IP segment of the semiconductor value chain for the Memory research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Development of EDA tools for modelling and simulation of 3D NAND and DRAM architectures at extreme scaling.
- Tools to address variability, defect tolerance, and yield optimization for high-density memory arrays.
- Custom EDA solutions for emerging memory technologies (e.g., MRAM, RRAM, PCM), including reliability and performance modelling.
- Creation of standardized memory controller IPs for heterogeneous architectures.
- IP design for novel memory hierarchies in data-centric computing, including persistent memory IPs for in-memory computing.

- Design methodologies for secure memory architectures, focusing on encryption and anti-tampering.
- Incorporation of machine learning models into EDA tools for predictive yield analysis and optimization in memory manufacturing.
- AI-based solutions for automated layout generation and verification of advanced memory designs.

3.2.2 Chip Design

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the Chip Design segment of the semiconductor value chain for the Memory research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Design of high-speed and high-capacity DRAM and NAND chips for next-generation computing systems.
- Architectures for improving latency, bandwidth, and energy efficiency in traditional memory systems.
- Chip designs leveraging emerging memory types (e.g., FeRAM, MRAM, RRAM, PCM) for specific applications like AI accelerators and edge computing.
- Design of hybrid memory/storage chips, combining traditional and non-volatile memory technologies to reduce data movement.
- Development of logic-in-memory designs to enable compute capabilities within memory chips.
- Architectures for monolithic 3D integration of memory and logic to achieve ultra-high-density and reduced latency.
- Memory chip designs with advanced error correction codes to improve reliability in scaled and stacked architectures.
- Circuit designs for mitigating soft errors, wear levelling, and endurance issues in emerging memory technologies.

3.2.3 System Design

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the System Design segment of the semiconductor value chain for the Memory research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- System-level architectures for tiered memory hierarchies, combining DRAM, NAND, and emerging memory technologies.
- Designs for heterogeneous memory systems that optimize for workload-specific requirements (e.g., HPC, AI, IoT).

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- Development of system-level designs for in-memory computing architectures, enabling data processing directly within memory.
- Architectures for accelerating AI/ML workloads through memory-optimized system designs.
- System designs focusing on reducing power consumption in memory subsystems for edge and mobile devices.
- HBM integration into chiplet-based systems for HPC and cloud applications.
- System-level solutions for memory integrity verification and protection against data corruption and hacking.
- Integration of advanced secure memory technologies for critical applications like autonomous vehicles and defence.

3.2.4 Materials Integration

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the Materials Integration segment of the semiconductor value chain for the Memory research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Research into new dielectric materials for improving capacitor scaling in DRAM technologies.
- Materials for achieving better endurance and retention in NAND flash memory.
- Integration of ferroelectric materials for FeRAM and hafnium-based oxides for non-volatile memories.
- Spintronic materials (e.g., magnetic tunnel junctions) for MRAM and resistive switching materials for RRAM.
- Development of phase-change materials for PCM with improved switching speeds and endurance.
- Materials research for enabling BEOL-compatible materials in monolithic 3D memory stacking.
- Techniques for integrating memory layers with logic in ultra-dense chip architectures.
- Integration of materials with improved thermal stability to handle heat dissipation in stacked and hybrid memory architectures.
- Research into stress-resilient materials for minimizing mechanical degradation in 3D NAND and other stacked memory solutions.

3.2.5 Components

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the Components segment of the semiconductor value chain for the Memory research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Research and development in DRAM and NAND technologies, focusing on scaling limits and improving energy efficiency.
- Exploration of high-density memory arrays and ultra-thin dielectric layers for advanced memory cells.
- Development of FeRAM, MRAM, and RRAM technologies for next-generation non-volatile memory.
- Exploration of phase-change memory and other storage-class memory solutions for hybrid memory/storage systems.
- Components for in-memory computing, including logic-in-memory approaches to reduce data movement and latency.
- R&D into hybrid memory technologies for monolithic 3D integration with logic.

3.2.6 Manufacturing (front-end)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the front-end Manufacturing segment of the semiconductor value chain for the Memory research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Techniques for manufacturing memory cells with ultra-high density and achieving vertical scaling in 3D NAND.
- Process development for scaling DRAM beyond traditional lithographic limits.
- Manufacturing techniques for integrating novel materials, such as ferroelectrics (FeRAM), spintronic materials (MRAM), and resistive materials (RRAM).
- Advanced deposition and etching methods for phase-change materials in PCM devices.
- Overcoming variability and defect challenges in extreme scaling of emerging memory technologies.
- R&D into uniformity and reliability improvements for wafer-scale memory production.

3.2.7 Manufacturing (back-end)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the back-end Manufacturing segment of the semiconductor value chain for the Memory research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Manufacturing processes for 3D NAND stacking and wafer-level bonding for DRAM and hybrid memory technologies.
- Integration of memory dies with logic chips in monolithic 3D architectures.
- Back-end processes for ultra-dense interconnects in memory modules (e.g., TSVs and micro-bump technologies).
- R&D into HBM interposer technologies.

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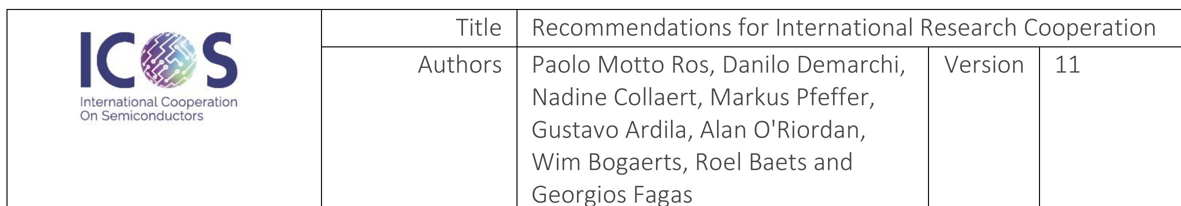

- Development of techniques for testing and mitigating failure mechanisms in stacked and hybrid memory architectures.
- Back-end processes for improving long-term reliability and minimizing thermal degradation.

3.2.8 Equipment & Tools (front-end)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the front-end Equipment & Tools segment of the semiconductor value chain for the Memory research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Development of EUV and multi-patterning tools for creating high-density memory arrays (e.g., NAND flash, DRAM).
- Tools for overcoming challenges in extreme scaling of memory cells (e.g., <10 nm features).
- Tools for precise deposition of materials used in ferroelectric FeRAM, MRAM, and RRAM.
- R&D into equipment for depositing and etching phase-change materials for non-volatile memory (e.g., PCM-based memory).
- Tools for evaluating read/write speeds, endurance, and retention of advanced memory devices under various operating conditions.
- Electrical characterization tools for studying variability in emerging memory types, such as MRAM and RRAM.

3.2.9 Equipment & Tools (back-end)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the back-end Equipment & Tools segment of the semiconductor value chain for the Memory research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Development of tools for high-precision wafer bonding and die stacking in 3D NAND flash and hybrid memory technologies.
- Equipment for integrating memory with logic in monolithic 3D architectures.
- R&D into tools for thermal management and reliability testing of stacked memory devices.
- Development of equipment for accelerated testing of memory endurance and failure mechanisms.
- Tools for creating high-density packaging solutions for HBM, including interposers and chiplets.
- Equipment for ultra-thin wafer handling and back-grinding to enable compact memory solutions.

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3.3 Mixed-Signal Processing

3.3.1 EDA & IP

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the EDA & IP segment of the semiconductor value chain for the Mixed-Signal Processing research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Research and development of early compact models for advanced/in-development nodes.
- Research and development of tools/libraries supporting the design of systems leveraging heterogeneous integration since the beginning of the design stages.
- Research and development of libraries and IPs of digitally-assisted analog circuits (e.g., with digital calibration), digital analog-like circuits (e.g., based on a standard cell design but with an analog behaviour).
- Research and development of advanced macro modelling techniques and tools leveraging data-driven/ML approaches for fast execution of comprehensive simulations of large/complex AMS designs.
- Research and development (including active support and promotion of new and emerging standard, open-source initiatives) of Hardware Description Languages (HDLs) and tools integrating different simulation approaches (e.g., event-driven and real-number simulators, numerical solvers) and targeting different levels of abstraction (e.g., behavioural, TLM- and RTL-like, transistor and/or physical levels).

3.3.2 Chip Design

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the Chip Design segment of the semiconductor value chain for the Mixed-Signal Processing research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Research and development of analog and mixed-signals circuits for leading edge process technologies.
- Research and development of digital wrapped or digitally-assisted analog circuits (e.g., with digital calibration), digital analog-like circuits (e.g., based on a standard cell design but with an analog behaviour).
- Research and development of low-power techniques targeting dynamic power management, for example leveraging dynamic voltage (or frequency) scaling, power gating.
- Research and development for Design for Testability (DfT) solutions for analog and mixed-signal ICs.

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3.3.3 System Design

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the System Design segment of the semiconductor value chain for the Mixed-Signal Processing research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Research and development of structural solutions for mitigating and preventing, at the system level, issues regarding power integrity, signal integrity, and performance degradation, especially in large digital designs combined with analog and mixed-signals sub-systems.
- Research and development of solutions for advanced packaging, multi-die (chiplet-based) solutions, and heterogeneous integration in general.
- Research and optimization in system-level optimization beyond PPAC (power, performance, area, cost), for example including R (robustness, reliability), T (temperature, thermal management), EDP (Energy-Delay product), Quality-energy trade-off.
- Research and development of constraints, requirements, and specifications bottom-up/top-down propagation methodologies, aiming at addressing the mutual impact between specific AMS circuit low-level design issues in leading edge process technologies and high-level, large and resource intensive, advanced applications such as AI/ML and quantum models and systems.
- Research and development of structural approaches for an effective and efficient implementation and integration of Design for Testability (DfT) solutions at the system level, in particular seamlessly extending digital solutions with advanced AMS features.

3.3.4 Materials Integration

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the Materials Integration segment of the semiconductor value chain for the Mixed-Signal Processing research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Research and development beyond Si-based devices, exploiting new materials (e.g., nanowires, carbon nanotubes, graphene, 2d materials in general) properties and their engineering/integration with Si-based devices and circuits.
- Research and development of materials for BEOL-compatible monolithic 3D integration of active and passive components.

3.3.5 Components

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the Components segment of the semiconductor value chain

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for the Mixed-Signal Processing research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Research and development of integrated passive devices on silicon substrate.
- Research and development of passive components for integration in advanced packaging and System-in-Package (SiP) solutions, multi-die (chiplet-based) solutions, heterogeneous integration in general.

3.3.6 Manufacturing (front-end)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the front-end Manufacturing segment of the semiconductor value chain for the Mixed-Signal Processing research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Research and development of techniques for better control/reduction of layout-dependent effects in leading edge process technologies.

3.3.7 Manufacturing (back-end)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the back-end Manufacturing segment of the semiconductor value chain for the Mixed-Signal Processing research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Research and development of techniques for better control/reduction of RC parasitics in leading edge process technologies.

3.3.8 Equipment & Tools (front-end)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the front-end Equipment & Tools segment of the semiconductor value chain for the Mixed-Signal Processing research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Research and development of equipment & tools for electrical characterization, aiming at developing reliable early models of devices and parasitics in leading edge process technologies.

3.3.9 Equipment & Tools (back-end)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the back-end Equipment & Tools segment of the semiconductor value chain for the Mixed-Signal Processing research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

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- Research and development of equipment & tools for electrical characterization, aiming at developing reliable early models of parasitics in leading edge process technologies.
- Research and development of equipment & tools for processing, and integrating in the BEOL processes, materials for BEOL-compatible monolithic 3D integration of components.

3.4 Powering

3.4.1 EDA & IP

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the EDA & IP segment of the semiconductor value chain for power devices and energy harvesting research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Research and development of tools and libraries that support the design of systems in the specific area of power devices and power harvesting, particularly aimed at improving:
    - Simulation Accuracy: Developing accurate models to predict device behaviour under various conditions.
    - Thermal Analysis: Creating tools for analysing heat dissipation and thermal management.
    - Process Variation: Addressing variations in manufacturing processes to ensure reliability.
    - Design Optimization: Implementing techniques to optimize layouts for performance and efficiency.
    - Integration with CAD Tools: Ensuring compatibility with existing Computer-Aided Design (CAD) tools for seamless workflows.
    - Design for Manufacturability (DFM): Making sure designs are practical and cost-effective for manufacturing.
    - Yield Prediction: Developing tools to predict and enhance yield rates in manufacturing.
    - Reliability Analysis: Conducting assessments of long-term performance and reliability of devices.

3.4.2 Chip Design

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the Chip Design segment of the semiconductor value chain for power devices and energy harvesting research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Design Automation: Developing tools for automating repetitive design tasks to improve efficiency.
- Simulation and Verification: Creating accurate simulation tools to verify functionality and performance of designs.
- Physical Design Tools: Implementing tools for layout design, including place and route processes.
- Power Analysis: Tools for analysing power consumption and optimizing for energy efficiency.
- Timing Analysis: Ensuring tools can check for timing violations and optimize clock distribution.
- Manufacturing Process Integration: Compatibility with specific manufacturing processes and technologies.
- Design for Testability (DFT): Implementing techniques to facilitate testing and debugging of chips.
- Yield Management: Tools to predict and improve yield in manufacturing processes.
- Reliability and Aging Analysis: Assessing long-term reliability and performance degradation of chips.
- Research and development, considering the development of circuits for power management in energy harvesting applications, of:
  - Strategies to reduce the overall device size and cost.
  - Efficient power management architectures fully integrated in a single chip.
  - Strategies to reduce the intrinsic power consumption.
  - Solutions allowing the miniaturization of the system embedding micro-magnetic components or power converters.
  - Strategies to reduce cold start and steady-state thresholds.
  - Strategies for the management of heterogeneous and/or multiple input energy transducers.
  - Integration of complex load management functions into the same silicon.

3.4.3 System design

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the System Design segment of the semiconductor value chain for power devices and energy harvesting research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Architecture Modelling: Developing tools for modelling system architectures to evaluate performance and scalability.

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- Design Specification: Creating frameworks for defining system requirements and specifications clearly.
- Simulation and Prototyping: Implementing tools for simulating system behaviour and creating prototypes for testing.
- Interface Design: Ensuring tools support the design of user interfaces and system interactions.
- Integration and Interoperability: Tools for ensuring seamless integration of different system components and interoperability.
- Performance Analysis: Developing tools to assess system performance under various conditions and workloads.
- Security Analysis: Implementing techniques to evaluate and enhance the security of system designs.
- Reliability and Fault Tolerance: Tools for assessing system reliability and incorporating fault tolerance mechanisms.
- Documentation and Compliance: Ensuring tools aid in generating documentation and compliance with industry standards.
- Research and development, considering the development of RF energy harvesting or wireless power transfer technologies, on:
    - Implementation of miniaturized energy stations to support the biasing of distributed sensors using RF energy.
    - Solutions to minimize the presence of RF power density in humanized environment and concentrating the power only where it is needed.
    - Solutions to increase device performance / efficiency.

3.4.4 Materials integration

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the Materials Integration segment of the semiconductor value chain for power devices and energy harvesting research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Material Selection: Developing tools for selecting appropriate materials based on electrical, thermal, and mechanical properties.
- Compatibility Assessment: Evaluating the compatibility of different materials to ensure reliable performance and integration.
- Synthesis and Fabrication Techniques: Implementing tools that support various synthesis and fabrication methods for materials.
- Characterization Methods: Developing techniques for characterizing the properties and performance of materials used in power devices.

- Thermal Management Solutions: Tools for integrating materials that enhance thermal management in energy harvesting devices.
- Reliability Testing: Assessing the long-term performance and reliability of materials under operational conditions.
- Recycling and Sustainability: Considering the lifecycle of materials and developing tools for recycling and sustainable practices.
- Multiscale Modelling: Implementing tools for modelling materials at different scales, from atomic to macroscopic levels.
- Cost-Effectiveness Analysis: Evaluating the cost-effectiveness of material choices in the context of manufacturing and performance.
- Research and development, considering the materials development for energy harvesting applications, of:
    - Non-toxic / abundant materials.
    - Materials from sustainable sources, easy to recycle, re-use, compost, re-purpose, etc.
    - Materials with added transparency and/or flexibility compatible with wearable applications.
    - Materials compatible with silicon technologies.
    - Processes or technologies to enhance materials properties and thus increase energy conversion efficiency.
    - Physical/chemical/electrical/electromechanical properties characterization techniques.

3.4.5 Components

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the Components segment of the semiconductor value chain for power devices and energy harvesting research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Performance Optimization: Implementing techniques to optimize the performance of components under various operating conditions.
- Integration Techniques: Tools for integrating multiple components into a cohesive system for better performance and efficiency.
- Testing and Validation: Developing methods for testing and validating component performance in real-world scenarios.
- Reliability Assessment: Tools for assessing the long-term reliability and durability of components under operational stresses.

- Miniaturization Techniques: Exploring methods for reducing the size of components while maintaining or improving performance.
- Power Management Solutions: Designing components that enhance power management capabilities in energy harvesting systems.
- Interfacing and Compatibility: Ensuring components are compatible with existing systems and can be easily interfaced with other devices.
- Cost Analysis: Evaluating the cost implications of component choices in the overall system design and manufacturing process.
- Research and development, considering the integration into energy harvesting devices, of:
    - Integration into devices being favourable to miniaturization, compatible with CMOS technologies and low cost.
    - Solutions to increase device performance / efficiency with a reduced surface and volume.
    - Solutions to increase the reliability of integrated systems.
    - Solutions for the integration into flexible substrates.
    - Transfer of solutions to industry, commercialisation of products.

3.4.6 Energy Storage Devices (solid state thin film solutions)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the development of energy storage devices (solid state thin film solutions), in particular regarding (but not limited to) the following challenges and opportunities:

- Research and development of solutions to increase the energy density and power at lower cost.
- Research and development of new materials for both electrodes and electrolyte with increased conductivities.
- Research and development of more sustainable active materials.
- Research and development of materials with added transparency and/or flexibility compatible with wearable applications.
- Research and development of options that can be processed on compostable substrates.

3.4.7 Manufacturing (front-end)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the front-end Manufacturing segment of the

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semiconductor value chain for power devices and energy harvesting research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Process Development: Developing tools for optimizing fabrication processes such as lithography, etching, and doping for specific materials used power device manufacturing.
- Material Handling: Implementing systems for effective handling and processing of raw materials to maintain quality.
- Yield Enhancement: Techniques for analysing and improving yield rates during the front-end manufacturing processes.
- Equipment Calibration: Tools for calibrating manufacturing equipment to ensure precision and consistency in production.
- Inline Monitoring: Developing systems for real-time monitoring of manufacturing processes to detect and address issues promptly.
- Design for Manufacturability (DFM): Ensuring designs are optimized for easy and efficient manufacturing.
- Cleanroom Protocols: Implementing tools for maintaining cleanliness and contamination control in manufacturing environments.
- Data Management: Systems for managing and analysing manufacturing data to inform process improvements and decision-making.
- Integration with Back-End Processes: Ensuring smooth transitions and compatibility between front-end and back-end manufacturing processes.

3.4.8 Manufacturing (back-end)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the back-end Manufacturing segment of the semiconductor value chain for power devices and energy harvesting research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Assembly Techniques: Developing tools for efficient assembly processes, including die bonding and wire bonding.
- Packaging Solutions: Implementing designs for reliable and effective packaging of devices to ensure performance and protection.
- Testing and Quality Control: Tools for conducting thorough testing and quality assurance of finished products to meet specifications.
- Thermal Management: Solutions for integrating thermal management systems into packaging to enhance device performance.
- Reliability Testing: Assessing long-term reliability and durability of packaged devices under various environmental conditions.

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- Supply Chain Management: Tools for managing the supply chain effectively to ensure timely availability of components and materials.
- Automation and Robotics: Incorporating automation and robotic solutions to streamline back-end processes and reduce labor costs.
- Process Optimization: Techniques for optimizing back-end manufacturing processes to improve efficiency and reduce waste.
- Sustainability Practices: Developing methods for reducing environmental impact through sustainable practices in back-end manufacturing.

3.4.9 Equipment & Tools (front-end)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the front-end Equipment & Tools segment of the semiconductor value chain for power devices and energy harvesting research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Equipment Integration: Developing systems that facilitate seamless integration of various front-end manufacturing equipment for streamlined workflows.
- Standardization and Modularity: Implementing standardized and modular designs to allow easy upgrades and replacements of equipment components.
- Automated Control Systems: Creating advanced automation systems that enhance precision and efficiency in front-end manufacturing processes.
- Real-Time Monitoring: Tools for real-time monitoring and data collection to ensure optimal equipment performance and process control.
- Maintenance and Support: Developing systems for predictive maintenance and support to minimize equipment downtime and extend lifespan.
- Data Analytics: Utilizing data analytics tools to optimize equipment performance and improve manufacturing outcomes based on historical data.
- User Interface Design: Creating intuitive user interfaces for equipment operation and monitoring to enhance usability and reduce operator error.
- Energy Efficiency: Designing equipment that prioritizes energy efficiency and minimizes waste in the manufacturing process.
- Safety and Compliance: Ensuring all front-end equipment meets safety standards and regulatory compliance for safe operation in manufacturing environments.

3.4.10 Equipment & Tools (back-end)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the back-end Equipment & Tools segment of the

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semiconductor value chain for power devices and energy harvesting research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Equipment Design: Developing specialized equipment for assembly, packaging, and testing of power devices and energy harvesting systems.
- Automation Systems: Implementing automation solutions to enhance efficiency and precision in back-end processes.
- Reliability Testing Equipment: Tools for conducting reliability tests, including thermal cycling and mechanical stress testing.
- Quality Assurance Systems: Equipment for quality control measures, ensuring that products meet industry standards and specifications.
- Material Handling Systems: Developing systems for the efficient handling and transport of materials and components within back-end processes.
- Process Monitoring Tools: Implementing real-time monitoring systems to track performance and detect issues in manufacturing equipment.
- Maintenance Solutions: Tools and protocols for maintaining back-end equipment to ensure optimal performance and minimize downtime.
- Integration Capabilities: Ensuring back-end equipment can seamlessly integrate with front-end processes and existing manufacturing systems.
- Data Analytics: Utilizing data analytics tools to gather insights from equipment performance and improve manufacturing processes.

3.5 Sensing

3.5.1 EDA & IP

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the EDA & IP segment of the semiconductor value chain for the Sensing research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Development of AI-enhanced EDA tools for optimizing sensor designs across, sensitivity performance, area, cost and sustainability.
- IP blocks that offer pre-designed modules that can be easily integrated into new designs, saving time and resources.
- IP blocks/modules that can be customized to meet specific design requirements to reduce cos and accelerate time to market.
- IP blocks/modules that enable simulation reducing the risk of design errors.
- Development of secure logic IPs with built-in cryptographic and anti-tampering capabilities.

- IPs optimized for heterogeneous integration in multi-die and chiplet-based solutions.
- IP blocks/modules on post fabrication simulation of real environmental deployment characterisation.
- IP blocks/modules are designed to work seamlessly with leading EDA tools, ensuring smooth integration.
- EDA solutions for comprehensive design-for-testability strategies in single or multimodal sensor designs.
- AI-driven tools for predictive failure analysis during sensor design and manufacturing.
- Ensuring signal integrity vital for sensor performance, e.g., HyperLynx.
- Power Analysis and Optimization.
- EDA tools can handle designs of varying complexities, from simple sensors to complex systems-on-chip (SoCs).
- Leveraging machine learning for adaptive manufacturing, layout generation and subsequent creation of global calibration curves to address fabrication variations.

3.5.2 Chip Design

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the Chip Design for the Sensing segment of the semiconductor value chain, in particular regarding (but not limited to) the following challenges and opportunities:

- Design of high-speed and high sensitivity sensor chips for next-generation computing systems.
- Advanced Simulation and Modelling tools for or analog, digital, and mixed-signal designs.
- Architectures for improving latency, bandwidth, and energy efficiency in sensor systems.
- Chip designs leveraging power management with integrated microcontrollers.
- Architectures for AI at the edge, leveraging compact and efficient logic designs.
- Circuit designs for mitigating soft errors, wear levelling, redundancy and endurance issues in emerging sensor technologies.
- Development of ultra-low-power logic designs for mobile devices, IoT, and wearable applications.
- Chip designs optimized for chiplet-based architectures, integrating logic with memory, analog, and other components.

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3.5.3 System Design

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the System Design segment of the semiconductor value chain for the Sensing research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Design Specification: Developing tools for modelling system architectures to evaluate performance and scalability.
- Design Specification: Creating frameworks for defining system requirements and specifications clearly. Analog, digital and mixed signal designs.
- Simulation and Prototyping: Implementing tools for simulating system behaviour and creating prototypes for testing.
- Interface Design: Ensuring tools support the design of user interfaces and system interactions.
- Integration and Interoperability: Tools for ensuring seamless integration of different system components and interoperability.
- Performance Analysis: Developing tools to assess system performance under various conditions and workloads.
- Security Analysis: Implementing techniques to evaluate and enhance the security of system designs.
- Reliability and Fault Tolerance: Tools for assessing system reliability and incorporating fault tolerance mechanisms.
- Documentation and Compliance: Ensuring tools aid in generating documentation and compliance with industry standards.

3.5.4 Materials Integration

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the Materials Integration segment of the semiconductor value chain for the Sensing research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Material Selection: Developing tools for selecting appropriate materials based on electrical, thermal, mechanical properties, chemical covalent and site selective attachment, target chemical selectivity and sensitivity.
- Compatibility Assessment: Evaluating the compatibility of different materials to ensure reliable performance and integration.
- Synthesis and Fabrication Techniques: Implementing tools that support various synthesis and fabrication methods for materials.

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- Characterization Methods: Developing techniques at small to ultra small areas (25 µm^2 and beyond) for characterizing the properties and performance of materials used e.g., exp, ATR-FTIR, µ-Raman, NMR
- Reliability Testing: Assessing the long-term performance and reliability of materials under operational conditions
- Recycling and Sustainability: Considering the lifecycle of materials and developing tools for recycling and sustainable practices from cradle to grave.
- Multiscale Modelling: Implementing tools for modelling materials at different scales, from atomic to macroscopic levels.
- Cost-Effectiveness Analysis: Evaluating the cost-effectiveness of material choices in the context of manufacturing and performance.

3.5.5 Components

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the Components segment of the semiconductor value chain for the Sensing research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Performance Optimization: Implementing techniques to optimize the performance of components under various operating conditions.
- Integration Techniques: Tools for integrating multiple components into a cohesive system for better performance and efficiency.
- Testing and Validation: Developing methods for testing and validating component performance in real-world scenarios under simulated real word conditions.
- Reliability Assessment: Tools for assessing the long-term reliability and durability of components under operational stresses.
- Miniaturization Techniques: Exploring methods for reducing the size of components while maintaining and/or improving performance while increasing sustainability
- Interfacing and Compatibility: Ensuring components are compatible with existing systems and can be easily interfaced with other devices.
- Integration: Ensuring components that be interconnected with existing systems
- Cost Analysis: Evaluating the cost implications of component choices in the overall system design and manufacturing process.

3.5.6 Manufacturing (front-end)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the front-end Manufacturing segment of the

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semiconductor value chain for the Sensing research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Process Development: Developing tools for optimizing fabrication processes such as lithography, etching, lift-off and materials deposition.
- Material Handling: Implementing systems for effective handling and processing of raw materials to maintain quality.
- Yield Enhancement: Techniques for analysing and improving yield rates during the front-end manufacturing processes.
- Equipment Calibration: Tools for calibrating manufacturing equipment to ensure precision and consistency in production.
- Inline Monitoring: Developing systems for real-time monitoring of manufacturing processes to detect and address issues promptly. AI/ML techniques to optimise manufacturing processes.
- Design for Manufacturability (DFM): Ensuring designs are optimized for easy and efficient manufacturing.
- Cleanroom Protocols: Implementing tools for maintaining cleanliness and contamination control in manufacturing environments while also allowing for non-conventional materials integration.
- Data Management: Systems for managing and analysing manufacturing data to inform process improvements and decision-making.
- Integration with Back-End Processes: Ensuring smooth transitions and compatibility between front-end and back-end manufacturing processes.

3.5.7 Manufacturing (back-end)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the back-end Manufacturing segment of the semiconductor value chain for the Sensing research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Assembly Techniques: Developing tools for efficient assembly processes, including traditional die bonding and wire bonding and non-traditional electrical pinouts for connection with USB or HDMI connectors.
- Packaging Solutions: Implementing designs for reliable and effective packaging of devices to ensure performance and protection. Develop packaging is sufficient for hostile deployments for examples, soil, rivers, etc.
- Testing and Quality Control: Tools for conducting thorough testing and quality assurance of finished products to meet specifications.

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- Reliability Testing: Assessing long-term reliability and durability of packaged devices under various environmental conditions.
- Supply Chain Management: Tools for managing the supply chain effectively to ensure timely availability of components and materials.
- Automation and Robotics: Incorporating automation and robotic solutions to streamline back-end processes, reduce labour costs and increase reproducibility of deposited materials.
- Process Optimization: Techniques for optimizing back-end manufacturing processes to improve efficiency and reduce waste.
- Sustainability Practices: Developing methods for reducing environmental impact through sustainable practices in back-end manufacturing.

3.5.8 Equipment & Tools (front-end)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the front-end Equipment & Tools segment of the semiconductor value chain for the Sensing research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Equipment Integration: Developing systems that facilitate seamless integration of various front-end manufacturing equipment for streamlined workflows.
- Standardization and Modularity: Implementing standardized and modular designs to allow easy upgrades and replacements of equipment components.
- Automated Control Systems: Creating advanced automation systems that enhance precision and efficiency in front-end manufacturing processes.
- Real-Time Monitoring: Tools for real-time monitoring and data collection to ensure optimal equipment performance and process control.
- Maintenance and Support: Developing systems for predictive maintenance and support to minimize equipment downtime and extend lifespan.
- Data Analytics: Utilizing data analytics tools to optimize equipment performance and improve manufacturing outcomes based on historical data.
- User Interface Design: Creating intuitive user interfaces for modular equipment operation and monitoring to enhance usability and reduce operator error.
- Energy Efficiency: Designing equipment that prioritizes energy efficiency and minimizes waste in the manufacturing process.
- Safety and Compliance: Ensuring all front-end equipment meets safety standards and regulatory compliance for safe operation in manufacturing environments.

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3.5.9 Equipment & Tools (back-end)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the back-end Equipment & Tools segment of the semiconductor value chain for the Sensing research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Equipment Design: Developing specialized equipment for assembly, sensor modification, packaging, and characterisation of sensor devices and systems.
- Automation Systems: Implementing automation solutions to enhance efficiency and precision in back-end processes.
- Reliability Testing Equipment: Tools for conducting reliability tests, including thermal cycling, mechanical stress testing operation under in-operando conditions.
- Quality Assurance Systems: Equipment for quality control measures, ensuring that products meet industry standards and specifications.
- Material Handling Systems: Developing systems for the efficient handling and transport of materials and components within back-end processes.
- Process Monitoring Tools: Implementing real-time monitoring systems to track performance and detect issues in manufacturing equipment.
- Maintenance Solutions: Tools and protocols for maintaining back-end equipment to ensure optimal performance and minimize downtime.
- Integration Capabilities: Ensuring back-end equipment can seamlessly integrate with front-end processes and existing manufacturing systems.
- Data Analytics: Utilizing data analytics tools to gather insights from equipment performance and improve manufacturing processes.

3.6 Communicating

3.6.1 EDA & IP

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the EDA & IP segment of the semiconductor value chain for the Communicating research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Design tools for RF circuits, including power amplifiers, low-noise amplifiers, and transceivers.
- Libraries and IPs optimized for high-speed wireline communication circuits (e.g., SerDes, PHYs for PCIe, USB).
- ML-enabled tools for designing and optimizing RF and mixed-signal circuits for 5G/6G applications.

- Tools supporting system-level co-simulation of digital, analog, and RF components in heterogeneous systems.

3.6.2 Chip Design

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the Chip Design segment of the semiconductor value chain for the Communicating research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- RF front-end designs for 5G/6G, including beamforming and mmWave transceivers.
- Mixed-signal chips for wireline communications (e.g., high-speed SerDes, ADC/DACs for optical communication).
- Low-power techniques for wireless IoT devices and sensor networks.
- Integration of communication subsystems in advanced SoCs for AI/ML and edge computing applications.

3.6.3 System Design

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the System Design segment of the semiconductor value chain for the Communicating research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Development of advanced antenna systems and RF beamforming architectures.
- Integration of communication subsystems into heterogeneous architectures, including chiplet-based designs.
- System-level power and thermal optimization for high-data-rate communication systems.
- Development of advanced packaging solutions (e.g., fan-out wafer-level packaging) for high-frequency systems.

3.6.4 Materials Integration

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the Materials Integration segment of the semiconductor value chain for the Communicating research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- New materials for RF, mmWave and sub-THz devices, including GaN, GaAs, InP, and 2D materials.
- Materials enabling low-loss interconnects for high-frequency signals in advanced packaging.
- Advanced dielectric materials for wireless/wireline applications.

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- (Engineered) substrates for RF components.

3.6.5 Components

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the Components segment of the semiconductor value chain for the Communicating research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- RF compound semiconductor devices and components.
- Development of IPDs (inductors, capacitors, filters) on silicon substrates tailored for wireless communication technologies, with a focus on performance and miniaturization.
- Research into high-Q factor passive components for RF applications to enhance efficiency in wireless communication systems.
- Development of passive components suitable for integration into advanced packaging solutions, including SIP and chiplet-based solutions for 5G/6G and IoT devices.
- Innovations in the co-integration of passives with active components in heterogeneous systems to optimize signal integrity and minimize parasitics.
- R&D on novel materials and processes to improve thermal management and power efficiency of communication modules in SiP and 3D IC designs.
- Progress in antenna-on-chip and antenna-in-package technologies for high-frequency applications, such as mmWave and (sub-)THz bands.
- R&D into reconfigurable antennas for advanced wireless communication systems.

3.6.6 Manufacturing (front-end)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the front-end Manufacturing segment of the semiconductor value chain for the Communicating research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Research into tailored process technologies for RF and analog components, such as silicon germanium (SiGe), RF CMOS, compound semiconductors like GaN, GaAs, InP, enabling low-noise amplifiers, power amplifiers, switches, filters etc. for communication systems.
- Techniques to scale RF technologies alongside digital nodes while ensuring performance and reliability.

3.6.7 Manufacturing (back-end)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the back-end Manufacturing segment of the semiconductor

value chain for the Communicating research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Development of interconnect technologies optimized for RF performance, including low-loss transmission lines for mmWave and terahertz communications.
- R&D on 3D integration for communication components to improve bandwidth and reduce latency.

3.6.8 Equipment & Tools for test/metrology

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering Equipment & Tools for test/metrology segment of the semiconductor value chain for the Communicating research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Development of tools for accurate RF device characterization at high frequencies (mmWave, sub-THz), enabling better device modelling and design optimization.
- Innovations in equipment for testing high-performance RF transistors and circuits under in-operando conditions.
- Development of tools for measuring parasitics in advanced packaging solutions, such as SiP and chiplets, at mmWave and (sub-)THz frequencies.
- Innovations in characterization tools to measure signal integrity and thermal performance in communication modules.

3.6.9 Equipment & Tools (front-end)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the Equipment & Tools for front-end processing segment of the semiconductor value chain for the Communicating research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- R&D into deposition, etching, and annealing tools optimized for Si-based RF technologies.
- Equipment for enabling and upscaling compound semiconductor technologies like, e.g., MOCVD.

3.6.10 Equipment & Tools (back-end)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the Equipment & Tools for back-end processing for the Communicating segment of the semiconductor value chain for the Communicating research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Equipment for ultra-fine pitch bonding and redistribution layer fabrication for SiP and chiplet-based communication systems.
- Tools for embedding antennas and passive components into advanced packages for wireless communication.
- R&D into equipment for back-end-of-line (BEOL) processes integrating BEOL-compatible monolithic 3D components, such as RF filters and MEMS for communication systems.
- Development of tools for precise deposition and integration of new materials, such as low-loss dielectrics, for RF and high-frequency communication chips.

3.7 Photonics

3.7.1 EDA & IP

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the EDA & IP segment of the semiconductor value chain for the Photonics research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Photonic circuit design and layout software tools (EDA for photonics).
- Photonic-Electronic codesign capabilities (both for low-speed signals and RF).
- Photonic building block design and physical simulation capabilities.
- IP libraries and providers for photonic integrated circuits.

3.7.2 Chip Design

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the Chip Design segment of the semiconductor value chain for the Photonics research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Photonic passive chip design expertise.
- Photonic active chip design expertise (including design for heterogeneously integrated chips and high-speed transceiver design).
- Design houses or independent design service providers/consultants for photonic integrated circuits, especially across multiple technology platforms.

3.7.3 System Design

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the System Design segment of the semiconductor value

chain for the Photonics research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Optical fiber coupling and package design.
- Photonic/electronic partitioning.
- Multi-chip modules/chiplet technologies for photonic-electronic integration.

3.7.4 Materials Integration

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the Materials Integration segment of the semiconductor value chain for the Photonics research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Hybrid integration of (packaged) light sources on (silicon/silicon nitride) photonic integrated circuits.
- Heterogeneous Integration of optical gain materials on (silicon/silicon nitride) photonic integrated circuits.
- Integration of electro-optic materials for high-speed modulation.

3.7.5 Components

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the Components segment of the semiconductor value chain for the Photonics research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Semiconductor lasers and light sources.
- High-speed modulators (O-band, C-band), transmitters.
- High-speed photodetectors / receivers.
- Low-loss optical waveguide and high-quality passive components (e.g., WDM filters, spectrometers, sensor readout components).

3.7.6 Manufacturing (front-end)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the front-end Manufacturing segment of the semiconductor value chain for the Photonics research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Low-volume and prototyping capabilities for silicon photonic integrated circuits:
  - Silicon Photonics;
  - Compound Semiconductors (III-V) – GaAs, InP;

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  - Silicon Nitride Photonics;
  - Thin-film Lithium Niobate.
- High-volume pure-play foundries for photonic integrated circuits: mainstream (65 nm – 130 nm node equivalent).
- High-volume pure-play foundries for photonic integrated circuits: top-tier (32 nm – 45 nm node equivalent).
- Monolithic photonic-electronic integration platforms.
- Front-end heterogeneous integration on silicon.

3.7.7 Manufacturing (back-end)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the back-end Manufacturing segment of the semiconductor value chain for the Photonics research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Back-end heterogeneous integration (low volume resp. high volume).
- Prototyping and development for new photonic packages.
- Low-volume out-sources assembly and test providers (OSAT).
- High-volume out-sources assembly and test providers (OSAT).

3.7.8 Equipment & Tools (front-end)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the front-end Equipment & Tools segment of the semiconductor value chain for the Photonics research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- R&D into deposition and processing of photonic-oriented materials (e.g. BTO, ...).
- Equipment for enabling and upscaling compound semiconductor technologies for active photonic circuits.
- Equipment for front-end heterogeneous integration (bonding).

3.7.9 Equipment & Tools (back-end)

Suggested international cooperation topics, used as a reference for rating the overall strength of each target country, considering the back-end Equipment & Tools segment of the semiconductor value chain for the Photonics research/application field, in particular regarding (but not limited to) the following challenges and opportunities:

- Equipment for back-end integration of functional materials, light sources, ... (transfer printing...).

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- Equipment for large-scale and cost-effective optical packaging (fiber attach).

4 Conclusions

In this deliverable, the activities undertaken to produce the recommendations for the International Research Cooperation were presented.

The two objectives of the work have been described:

1. The first is to establish the investigation and evaluation methodology/framework by strengths/weaknesses and opportunities/challenges with respect to a specific context/aspect for obtaining a qualitative evaluation of the scenario.
2. The second is to quantitatively assess the key points previously identified by asking for and collecting information from international experts to obtain a quantitative indication of the different strengths and weaknesses of each country of interest.

In the preliminary analysis and internal discussions among experts and partners involved in the project, some suggested topics for international cooperation have emerged as the possible most promising or attractive ones. In particular, grouped by the research/application field:

- Logic
    - AI-enhanced EDA tools for optimizing, verifying and predict logic designs across power, performance, area, cost, security and sustainability.
    - Brain-inspired neuromorphic devices and architectures for edge computing systems, requiring low latency and high energy efficiency, including AI at the edge.
    - High-bandwidth logic subsystems optimized for interconnects in network-on-chip architectures.
    - Research and development of advanced transistor technologies and related manufacturing processes for future generation of FinFETs, nanosheets and CFET transistors for sub-3 nm nodes, with novel device geometries.
    - Development of components enabling neuromorphic computing and quantum logic devices.
    - New materials integration for alternative channel materials and added back-end-of-line (BEOL) functionality.
    - Substrate thinning processes and back-side processing for new power and backside passive and active functionalization.

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  - Heterogeneous integration at the core of design and manufacturing processes for integrating logic cores with accelerators and memories, based on optimized IPs, and using chiplets and 2.5D/3D packaging.
- Memory
  - EDA solutions for emerging memory technologies, including reliability and performance modelling.
  - IP design for novel memory hierarchies in data-centric computing, including persistent memory IPs for in-memory computing.
  - Development of logic-in-memory designs to enable compute capabilities within memory chips.
  - Designs for heterogeneous memory systems that optimize for workload-specific requirements (e.g., HPC, AI, IoT).
  - System-level solutions for memory integrity verification and protection against data corruption and hacking, integrating advanced secure memory technologies for critical applications like autonomous vehicles and defence.
  - Design and manufacturing of components for in-memory computing, including logic-in-memory approaches to reduce data movement and latency, exploring also FeRAM, MRAM, RRAM, phase-change memory and other storage-class memory solutions for hybrid memory/storage systems.
  - Development of techniques for testing and mitigating failure mechanisms in stacked and hybrid memory architectures.
- Mixed-signal processing:
  - Seamless integration of the analog and digital design and development.
  - Heterogeneous simulation and modelling approaches at different levels, considering also IP libraries.
  - Development of structural solutions for mitigating and preventing critical integration issues.
  - Design for Testability.
- Powering
  - Tools and libraries that support the design of systems in the specific area of power devices and power harvesting, including Design for Testability (DFT) and Design for Manufacturability (DFM), yield management, reliability/fault tolerance and aging analysis, integration and interoperability.
  - Methods and tools for integrating multiple components (e.g., passives) into a cohesive system for better performance and efficiency and for reducing the size of components while maintaining or improving performance.

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- Equipment for quality control measures, ensuring that products meet industry standards and specifications and implementing real-time monitoring systems to track performance and detect issues in manufacturing equipment.
- Wide band gap (e.g., SiC, GaN) and ultrawide band gap materials (e.g., AlN, GaOx, diamond) for power devices.
- Focusing on energy harvesting:
  - Development of environmentally friendly materials for energy harvesters.
  - Develop comprehensive system design including all process aspects for increasing power generation efficiency.
  - A general limitation towards industrial adoption of Energy Harvesting is its reliance on environmental conditions. Developing Energy Harvesting combined with on-demand charging of the device could help solving this issue.

- Sensing
  - New approaches are required to facilitate integration of sensor performance into traditional simulation tools such as SPICE. This will enable seamless integration of the full sensor system.
  - Key challenges remain around the need to calibrate individual sensors, ML methods at different levels are required to address these challenges.
  - Scaling up sensor functionalisation and characterisation in-line with wafer-scale production.
  - Developing of safe and sustainable and design fabrication, modification and characterisation.
  - Advanced sustainable (bio)materials innovation and integration of in new, highly sensitive and more versatile sensors.
- Communicating
  - ML-enabled tools for designing, optimizing, and integrating RF and mixed-signal circuits for 5G/6G applications, including system-level co-simulation of digital, analog, and RF components in heterogeneous systems.
  - New materials for RF, mmWave and sub-THz devices, advanced dielectric materials and substrates for wireless/wireline applications and components.
  - Innovations in the co-integration of passives with active components in heterogeneous systems, progress in antenna-on-chip and antenna-in-package technologies for high-frequency applications.
  - Techniques to scale RF technologies alongside digital nodes while ensuring performance and reliability.
- Photonics

- Tools for photonic active and passive circuit design and photonic-electronic codesign, layout, and simulation, including IP libraries and across multiple technology platforms.
- Heterogeneous and hybrid photonic-electronic integration platforms including multi-chip modules/chiplet integration, integration of light sources, back-end and front-end heterogeneous integration, optical fiber coupling and package design.
- Development of PDKs, ADKs etc. for rapid prototyping, bypassing long chip iteration cycles
- High-volume pure-play foundries for photonic integrated circuits, out-sources assembly and test providers (OSAT).

The prepared survey will be shared with the selected experts in the next period, feedback will be collected and analysed, and the final results will be reported in the Deliverable D3.4 “Updates on future emerging technologies and recommendations”.

@ICOS_horizon ICOS - International Cooperation On Semiconductors

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