PROGRAMME

1st DAY

Morning

Welcome Coffee and Pastries

OPENING AND POLICY SESSION *(Chair: Elles Van de Ven)*

- 08h45 – **Welcome note** – Mr. Sagar Sharma, CoS, ISM, In-person
- 08h55 – **Welcome Note** – Pierre Chastanet - Head of the Unit of C.3 Microelectronics and Photonics - European Commission
- 09h05 – 09h35 – **Industry Participants introduction/ presentation** - India – Mr. Rajesh Nair, Tata Electronics; Mr. Raghu Panicker, Kaynes
- 09h05 – 09h35 – **Industry Participants introduction/ presentation** – EU - Christofer Frieling – SEMI Europe

SESSION 1 – Heterogeneous Integration & Packaging *(Chair: Francis Balestra)*

- 09h35 – **High-speed interconnects for advanced computing and communication: Evolution, Challenges, and what lies ahead?** - Prof. Rohit Y Sharma - IIT Ropar
- 10h00 – **How 3D integration can help the emergence of Power efficient innovative architectures?** - Olivier Faynot, CEA-Leti
- 10h25 – **Heterogenous integration -Enabling systems beyond Moore's Law** - Andreas Middendorf - Fraunhofer IZM

Coffee Break 10h50

SESSION 2 – More than Moore Functionalities *(Chair: Francis Balestra)*

- 11h20 – **Silicon Photonics Technology at CoE-CPPICS, IIT Madras** - Prof. Bijoy Krishna Das, IIT Madras
- 11h45 – **GaN Technology for Power Electronics Applications** – Urmimala Chatterjee, imec
- 12h10 – **Semi-conductor Laboratory : Capabilities Overview** - Dr. Kamaljeet Singh, DG, SCL
- 12h35 – **Silicon Photonics: review of the main EU and international activities and technologies** - Roel Baets, Ugent

Lunch Break 13h00

Afternoon

SESSION 3 – Sustainable Manufacturing and Materials *(Chair: Giorgos Fagas)*

14h20 - **Bio-based materials and processes for pcbs: an example of pathway for sustainable micro-nanoelectronics?** – Pascal Xavier, Université Grenoble Alpes

14h55 - **Advanced Materials for next-generation Semiconductor technology** - Rajeev Ahuja, IIT Ropar

15h20 - **Towards Sustainable electronic** – Olivier Faynot, CEA-Leti

15h45 - **Sustainability in information and communication technologies** – Jean-Pierre Raskin, UCLouvain

Coffee Break 16h10

SESSION 4 – IC & System Design *(Chair: Giorgos Fagas)*

16h40 - **IC and System Design - The quantum way** – V.Kamakoti Veezhinathan, IIT Madras

17h05 - **AI-enabled smart and secure electronic systems design and Indigenous Electronic Design Automation Tools for VIKSHIT BHARAT 2047 –** Gaurav Trivedi, IIT Guwahati

17h30 - **The Open-Source PULP Platform for tinyML Heterogeneous Hardware Acceleration –** Francesco Conti, Unibo

17h55 - **Digital system design at IIT Bombay** – Madhav P. Desai, IIT Bombay

FINAL SESSION

18h20 - **Closing remarks -** Elles Van de Ven, European Commission DG Connect

Cocktail Dinner 18h30

ABSTRACTS AND SPEAKERS

OPENING AND POLICY SESSION

Sagar Sharma is a trained engineer but a social scientist at heart. He is the Chief of Staff at the India Semiconductor Mission and is committed to strengthening Electronics System Design and Manufacturing in India. He played a key role in getting four semiconductor manufacturing facilities with the total investment of over USD 17 Bn, conceptualizing the strategy and policy for the Semicon India Program for the development of semiconductor and Display manufacturing ecosystem and setting up the India Semiconductor Mission which got approved by the Union Cabinet, Government of India in Dec 2021.

He has garnered rich experience while attempting to solve challenges in multiple domains, ranging from engineering to the education sector. In his previous assignment at the ministry of education, Sagar researched and analysed various policies (including National Education Policy 2020), schemes, and statutes to suggest possible policy-level interventions for better outcomes and service delivery. He has worked with TCS innovations lab, Bangalore, and NCETIS, Mumbai. Sagar is an alumnus of IIT Bombay and believes in diversifying science and has worked extensively to promote scientific temper, STEM skills, and hands-on skills by co-founding a non-profit, VigyanShaala International.

Pierre CHASTANET is Head of the Unit of C.3 Microelectronics and Photonics at the European Commission, where he manages the development of European semiconductor policy and the implementation of the European Chips Act.
Mr. Chastanet has been working for over 17 years in the European Commission, supervising different digital policies in the areas of cloud, data flows, software, cybersecurity, privacy, green ICT, and telecom innovation.
Prior to that, Mr. Chastanet gained more than 10 years of ICT experience, mostly in various IT management positions in a large multinational company.
He graduated from Telecom ParisTech, the Free University of Brussels, and the London School of Economics and Political Science. He also earned a Leadership Executive Certificate from Harvard Kennedy School of Government.

Raj Nair is the Senior Vice President and Head of Fab Technology Development at Tata Electronics (since September 2024). Prior to that he was Vice President for Power Products at GlobalFoundries (2018-2024) and was head of the Technology Development group in Singapore (2013-2018). Raj's team was responsible for development of several of the Power and Non-Volatile technologies currently in volume production at GF. Raj has over 30 years of Operations and R&D experience in the semiconductor and advanced battery industries. Before joining GlobalFoundries in 2013, Raj held executive positions at Johnson Controls, Maxim, Motorola and On

Semiconductor. At Johnson Controls he was the Vice President for Advanced Manufacturing and Quality. Raj is a pioneer in the development of SmartPower integrated circuit technologies. Raj has an MSEE degree from NTU, an MS ChE from Syracuse University and a B.Tech degree from IIT Bombay. Raj has been awarded eight patents and has authored multiple publications in the semiconductor domain.

Raghu Panicker is the CEO of Kaynes SemiCon. He is an Electronics and Communication engineer, self-motivated and business professional with over 32 years of experience across industries, cross cultures in various roles & responsibilities and multi-geographic locations.

Raghu started his career from Semiconductor Complex Ltd., (SCL, a govt Fab) in 1991 for 10 years as R&D engineer. Then as Country Manager for Mentor Graphics (now Siemens EDA) for 20 years. Before Kaynes, Raghu was with Tessolve Semiconductor for 2 years running the APAC business.

Christofer Frieling is Director for Advocacy and Public Policy at the SEMI Europe Brussels Office. He oversees SEMI Europe's advocacy work in Brussels as well as SEMI's engagement in EU funded projects. Christopher has a background in EU affairs, innovation, and tech policy. Prior to SEMI he worked at the Brussels office of Fraunhofer in several roles including most recently as Senior Advisor. Christopher holds an MSc in Economics of Science and Innovation from the Barcelona Graduate School of Economics and a Bachelor of Business Administration.

SESSION 1 – HETEROGENEOUS INTEGRATION & PACKAGING

- **High-speed interconnects for advanced computing and communication: Evolution, Challenges, and what lies ahead?**
  Rohit Sharma, IIT Ropar

Advance computing and high-speed wireless communication have necessitated heterogeneously integrated packages and systems that can meet the higher throughput and lower energy budget requirements. Significantly reduced line width and pitch of on-chip interconnects have resulted in size effects such as surface and grain boundary scatterings in conventional Cu interconnects. This significantly degrades the electrical performance of interconnects and aggravates thermal impact that leads to reliability concerns.

Carbon and other 2D materials such as graphene and carbon nanotubes, and their nanocomposites are potential materials to replace on-chip Cu interconnects. Among them, nanoscale graphene ribbons with widths of a few nanometers are promising candidates to address the scaling issue of Cu interconnects owing to their outstanding electrical and thermal properties and chemical reliability. In this webinar, we understand the prospects of Cu-graphene hybrid heterostructures for BEOL compatible high-performance interconnects. We aim to understand the complexities involved in mainstreaming this potential technology and what lies ahead in terms of potential benefits of hybrid nanoscale interconnects. We take the help of several case studies to highlight the benefits of Cu-graphene hybrid interconnects for applications in next-generation packages and systems.

Rohit Sharma is a Professor in the Department of Electrical Engineering at IIT Ropar.

His primary research expertise includes, but are not limited, to the following areas: modeling and design of high-speed on-chip and chip-to-chip interconnects; electrical-Thermal co-design of electronic packages and nanoscale systems; application of machine learning in design and analysis of interconnects and packages; design and optimization of Graphene-based and 2D materials-based nanoelectronics.

He is an associate editor to the IEEE Transactions on Components, Packaging and Manufacturing Technology. He is a Program Committee member of all major IEEE packaging conferences (ECTC, EPEPS, EDAPS and SPI). He has authored more than 100 papers in leading conferences and journals including multiple best paper awards.

He has also been a visiting professor at the Packaging Research Center at Georgia Tech and a research professor at Penn State University in the past.

He holds the PhD degree in Electronics and Communication from Jaypee University of Information Technology, India.

- **How 3D integration can help the emergence of Power efficient innovative architectures?**

  Olivier Faynot, CEA LETI

World's digitalization induces a tremendous increase of data generation, close to 500 Zetabyte by 2030. This data deluge leads to a dramatic increase of energy consumption, not sustainable on a medium term. Technological breakthrough must be developed in order to significantly improve (by a factor of 1000) the Power efficiency of electronic.

This paper will detail all the ongoing developments in 3D integration that will enable the emergence of new type of circuits architectures, with improvement of the Power efficiency. 3D technologies technological toolbox will be detailed, with Wafer to Wafer or Die to Wafer approaches.

New specific architectures will also be presented during that talk.

Olivier Faynot received his Ph.D. degree from the Institut National Polytechnique de Grenoble in 1995. He joined CEA-LETI in 1995. Since 2019, he is managing the whole Silicon Component division at CEA-LETI. He is author and co-author of more than 300 scientific publications in journals and international conferences, and was successively in the committees of the main international Semiconductors conferences like IEDM, the symposium on VLSI Technology, the IEEE International SOI conference, the EUROSOI network, SSDM conference and the International S3S conference. He received the 'Général Férié' award in 2012 and the 'Electron d'Or' award with CEA-Leti, ST Microelectronics and SOITEC in 2017.

- **Heterogenous integration -Enabling systems beyond Moore's Law**

  Andreas Middendorf, Fraunhofer IZM

Heterogenous integration brings together the world of semiconductors with advanced packaging technologies (e. g. for pcb) and enables by these systems that overcome Moore's Law. The presentation shows realized examples based on available technologies in industry as well as from Fraunhofer IZM and other FMD-institutes.

According to the demands from different application fields like automotive, medical, food or automation in combination with e. g. AI or HPC possible challenges were discussed. The collaboration with partners from EU and India might be very fruitful, especially taking into account the strong position of India in software and design. Let`s bring together the skills from EU and India.

Dr.-Ing. **Andreas Middendorf** works as a business developer in the Business Development Team of the Fraunhofer Institute for Reliability and Microintegration (IZM). He was working as a scientist in the department Environmental and Reliability Engineering of the Fraunhofer Institute for Reliability and Microintegration (IZM) and of the Technical University Berlin since May 1995. He was responsible for the development and implementation of methods and demonstrators for the estimation of lifetime for electronic appliances. Further on he is investigating technological aspects that combine the electronics design with environmental engineering techniques. This includes environmental assessments through LCA and through other methods, especially for Eco-Design, the evaluation of recycling attributes, the development of databases and software as well as environmental oriented product evaluation. He carried out courses on EcoDesign for electronic companies, holds four patents and has coordinated several cooperative research projects in Germany and Europe.

SESSION 2 – MORE THAN MOORE FUNCTIONALITIES

- **Silicon Photonics Technology at CoE-CPPICS, IIT Madras**
  Bijoy Krishna Das, IIT Madras

Owing to the success of high-speed silicon photonic transceivers for data centres, demand for similar products in several other fields such as 5G/6G, quantum photonic applications, etc. has emerged during recent years. In this talk, we will discuss about the present state-of-the-art technology and some recent progress in this direction carried out at the Silicon Photonics CoE-CPPICS, IIT Madras.

Bijoy Krishna Das obtained his master's degree in solid-state physics from Vidyasagar University, Midnapore, India (in 1996) and Ph.D. degree (Dr.rer.nat) in integrated optics from the University of Paderborn, Germany (in April 2003). Prior to his Ph.D. research in Germany, Dr. Das started his research career in the area of integrated optics at the Microelectronics Centre, IIT Kharagpur for three years (January 1996 – December 1998). His postdoctoral research was carried out in three different countries First, he was an FRC Postdoctoral Fellow in the Graduate School of Engineering, Osaka University, Osaka, Japan (2004-2005). Later, he joined as a postdoctoral researcher in the Center for Optical Technologies, Lehigh University, Bethlehem, PA, USA. In April 2005, he re-joined the Integrated Optics Group at the University of Paderborn as Wissenschaftlicher Mitarbeiter and continued his research on integrated nonear optical devices. He also worked for a while at Laboratoire Aime Cotton, CNRS, Orsay, France. Since August 2006, Dr. Das has been associated with the Dept. of Electrical Engineering, IIT Madras, where he is presently holding a full Professor position. At IIT Madras, Prof. Das has founded the Silicon Photonics Centre of Excellence: Centre for Programmable Photonic Integrated Circuits and Systems (CoE-CPPICS) for which he is fully dedicated for establishing state-of-the-art silicon photonics research ecosystem following product research development and manufacturing (PRDM) model.

GaN Technology for Power Electronics Applications

Urmimala Chatterjee, imec

GaN technology can drive the high frequency operation for power circuits beyond today's limit that facilitates to build a smaller, lighter and more cost-effective solution compared to its other silicon alternatives. This talk will give you a brief of IMEC's different GaN technology platforms for the discrete power devices. Besides this will also cover the aspects of monolithic integration in this technology. In order to fully utilize the fast-switching capability of GaN technology, monolithically integrated GaN power IC is beneficial. For instance, integration helps to reduce the gate ringing, switching loss which in-turn makes a smooth highly efficient circuit.

Urmimala Chatterjee received her bachelor's degree from WBUT, India and master's degree from NTU-TUM, Munich. After that she pursued her PhD in ESAT, KU Leuven on power converter design for Before joining IMEC, she worked a few years in TAS, Belgium on discrete circuit design for space electronics. Presently in IMEC she is working in GaN power electronics, mainly responsible for GaN IC activities and device design.

Semi-conductor Laboratory : Capabilities Overview

Dr. Kamaljeet Singh, DG, SCL

The talk reveals the journey of SCL show causing capabilities developed in the various domain of semiconductor chain. The present capabilities in terms of packaging and integration of processes are presented such as MCM, SiP etc. Various products covering wide spectrum from analog, digital, RF, sensors, detectors with high reliability features are presented.

The presentation covers sensors which needs specific packaging apart from the compound semiconductor related development at SCL.

Dr. Kamaljeet Singh M. Tech, Ph. D, joined ISRO in 1999 and entrusted with the design of RF receiver for satellites. He was deputed to Semi-Conductor Laboratory where he got trained in thin film and re-initiated MEMS activities. He was instrumental in the initiation of MEMS sensors development and its productionization along with re-establishment of 6" MEMS fabline at SCL. He worked in various capacities after joining back ISRO in 2016 dealing with multiple space craft projects. As Group Director of HMC & Indigenization group he was responsible for the development and delivery of HMCs and MIC/MMIC circuits for various missions apart from indigenization of components through industry

interface. He joined as Director General Semi-Conductor Laboratory in December 2023.

He is Fellow of IETE, Fellow of Punjab Academy of sciences, Life member of ASI & IMAPS and Senior member of IEEE. He has 2 patents and published more than 200 technical articles in various journals/conferences. His main area of interest are in RF & Microelectronics. He is the recipient of young scientist awards from INAE, IETE & ISRO. He has written various technical books: RF principle and its application in RF-MEMS switch (2018), Si-RF technology (2019), Sensors based on IC techniques and its applications (2021), Interdigital Capacitors (2020) and Microstrip multipliers (2021) etc.

- **Silicon Photonics: review of the main EU and international activities and technolgies**
  Roel Baets, UGent

Silicon photonics is a technology that benefits from the existing CMOS infrastructure to manufacture compact and densely integrated photonic ICs at low cost. Today, this technology provides solutions for high-speed connectivity ranging from a few meters to hundreds of kilometres. Millions of modules are in operation, and there is a growing demand due to increased demand for connectivity. In parallel, silicon photonics applications in markets for medical diagnostics, high-performance computing, quantum processing, agri-food, and autonomous driving are gaining traction and maturity. Cost, scalability, miniaturization, and competitive performance are some drivers that make silicon photonics a relevant technology for applications in these markets. This diversification of applications requires the retrofitting of the technology to meet new demands. There are several dimensions of this evolution and will discuss some of the most prominent aspects in this talk. For the last several years, Europe has been in a leading position in R&D for photonic integration in general and in silicon photonics in particular. In the second part of my talk, I will position Europe vis-à-vis the other regions and review the main EU and international silicon photonics activities and technologies.

Roel Baets is a full professor at Ghent University (UGent) and is also associated with IMEC, both in Belgium. He received MSc degrees from UGent and Stanford University and a PhD degree from UGent. Since 1989 he has been a professor in the Faculty of Engineering and Architecture of UGent where he founded the Photonics Research Group. Roel has led major research projects in silicon photonics in Europe and founded ePIXfab in 2006, the globally first Multi-Project-Wafer service for silicon photonics (now European Silicon Photonics Alliance). Roel is a Fellow of IEEE, of European Optical Society (EOS) and of Optica. He has been a recipient of the 2011 MOC award, of the 2018 PIC-International Lifetime Achievement Award, of the 2020 OSA-IEEE John Tyndall award and of the 2023 IEEE Photonics Award.

SESSION 3 – SUSTAINABLE MANUFACTURING AND MATERIALS

Bio-based materials and processes for pcbs: an example of pathway for sustainable micro-nanoelectronics?

Pascal Xavier, Technology University Institute of Grenoble

After a brief introduction to the global context and related challenges, some promising and original technological avenues in the field of printed circuits will be described, from the point of view of materials, manufacturing and recycling processes.
The obtained results could pave the way towards greater sustainability in the micro and nanoelectronics sector.

Pascal XAVIER, received the Ph. D. degree in Physics from the University of Grenoble, France, in 1994. He was also graduated from Grenoble INP in electrical engineering in 1988. From 1994 to 2003, in the CNRS, his research interests were dealing with numerical methods for the analysis of coupled thermo-electromagnetics problems and design of microsensors in the fields of microwaves.

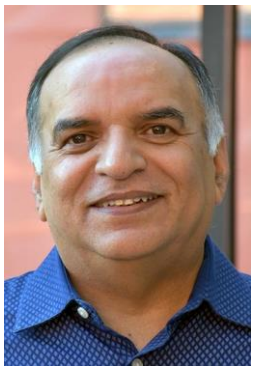
He joined the Centre for Radiofrequencies, Optics and Microelectronics of the Alps (CROMA) of Grenoble in 2003 where he is currently team leader and coordinator of a Horizon Europe EIC Pathfinder Challenges project on responsible electronics. His research interests include design, realization and test of sustainable microwave devices and sensors for environmental applications, bioelectromagnetism and characterization of complex materials.

He is Full Professor in the Department of Electrical Engineering, Technology University Institute of Grenoble (UGA), involved in teaching of Electronics and Physics.

Advanced Materials for next-generation Semiconductor technology

Rajeev Ahuja, Indian Institute of Technology Ropar, Rupnagar, Punjab, India

The evolution of semiconductor technology, particularly Silicon (Si) technology, has been a critical driver for the technological advancements that we see around us. Going further, conventional bulk semiconductor technologies like Silicon find it challenging to meet future technology requirements. Therefore, the end of Moore's law and the emergence of beyond-Si electronics, optoelectronics, and quantum technologies are well-accepted directions of the last 15 years and so. Among various emerging technologies, 2-Dimensional (2D) semiconductors promise to offer new opportunities in semiconductor technology. The purpose of this talk is to provide an overview of the most recent studies in the area of materials science with focus on Semiconductor technology.



Prof. Rajeev Ahuja is a professor of computational Materials science at Uppsala University, Sweden. Currently, he is serving as the Director of Indian Institute of Technology (IIT) Ropar, India. He was also holding the additional charge of director of IIT Guwahati, India from Nov. 2023 to May 2024. He is one of the most highly cited researchers as well as top 5 materials scientist in Sweden and India. He has done his Ph.D. from IIT Roorkee in India in 1992. Same year, he joined Uppsala University, Sweden as postdoctoral fellow. He became Professor in 2007 at Uppsala University, Sweden. His main area of interest is materials science with focus on energy such Batteries, Hydrogen Storage & production, sensors as well high-pressure physics.

He has published 1150 scientific papers in peer reviewed journals H-Index of 104, i-10 index 806 & no. of citations more than 50000. Prof. Ahuja has supervised 30 PhD students, more than 35 post-docs. He has recently elected as the Fellow of the Royal Society of Chemistry (F-RSC), UK, and as an APS Fellow by the American Physical Society (APS), USA. He serves on the advisory board of the Journal of Materials Chemistry A and Materials Advances from the Royal Society of Chemistry. Additionally, he is the Associate Editor of Nano Energy.

Prof Ahuja has received several prestigious awards, including the Beller Lectureship at the APS March Meeting in 2017, the Wallmark Prize in 2011 from the Royal Swedish Academy of Sciences (KVA), and the Eder Lilly & Sven Thureus Prize, as well as the Benzelius Prize from the Swedish Royal Society of Sciences (KVS). He is an elected member of the Swedish Royal Society of Sciences (KVS). Prof Ahuja has been awarded Best Alumnus award from IIT Roorkee, India for excellence in research for 2021.

Towards Sustainable electronic

Olivier Faynot, CEA-Leti

Challenges of Sustainability will be reviewed and opportunities will also be detailed.

Electricity and water consumption, wastes, recycling, CO2 emission, PFAS material, rare earth materials are the main challenges that Semiconductor industry is facing today.

The presentation will detail the on-going actions that are pursued to solve all those issues and enable a more sustainable electronic.

Sustainability in information and communication technologies

Jean-Pierre Raskin, Louvain School of Engineering

In the talk, we will lift the veil on the invisibles of the digital world. Based on the assessed impacts of ICT, we will question the merits of certain technological choices made in the name of the transition. A holistic, transdisciplinary and pragmatic approach must be put in place in order to think, design and innovate within the constraints of our ecosystem limits. Concrete examples of current research will be shared, such as a critical look at the deployment of connected objects, the eco-design of sensors, a reflection on the pursuit of Moore's law and its environmental consequences, and the strategies to minimize e-waste.

Jean-Pierre Raskin is full professor at the Ecole Polytechnique de Louvain, UCLouvain, Belgium. His research interests are the modeling, wideband characterization and fabrication of advanced SOI MOSFETs and high-frequency integrated circuits, as well as micro and nanofabrication of MEMS / NEMS sensors and actuators, including the extraction of intrinsic material properties at nanometer scale. He is involved in the development of a more sustainable electronics. He has been managing a Chair in eco-innovation at CEA-Leti since January 2024.

He has been IEEE Fellow since 2014. He received the Médaille BLONDEL 2015, the SOI Consortium Award 2016, the European SEMI Award 2017, the Médaille AMPERE 2019, the Georges Vanderlinden Prize 2021 and the IET Achievement Medal in Electronics 2022, in recognition in his vision and pioneering work for RF SOI. He is author or co-author of more than 400 scientific journal articles.

He has been elected member of the Royal Academy of Belgium in 2023.

SESSION 4 – IC & System Design

IC and System Design - The quantum way

V. Kamakoti Veezhinathan, IIT Madras

IC and System Design have evolved based on two critical empirical laws [Moore's and Rent's law]. ICs are fundamentally semiconductor based. A transistor is the fundamental device on which ICs are built. cmos based transistors scaling [shrinking in size] has resulted in billions of transistors in a present-day ICS. EDA was the prime and major enabler of both IC design and IC based System Design. EDA algorithms are NP hard. NP hard are better solved by ML methods. ML methods help immensely both in design automation and manufacturing process optimisation [yield].ML methods aren't efficient to solve analog and RF design. They are more skill based like an art. Beyond ML methods we have quantum Computing but realizing a quantum computer is yet to fructify. It means we need to have utility qcomp. With that utility qcomp and ML we can solve more problem space. Till then ML will help. We will have situation where EDA will help design qcomp and qcomp will help execute EDA algorithm. But for that to happen, a utility qcomp from point of view of EDA, IC and System Design complexity have to be re-defined and thus achieved.

Prof. **Kamakoti Veezhinathan** received his M.S. and Ph.D. degrees in Computer Science and Engineering from IIT Madras. He joined the faculty of IIT Madras in 2001 and took over as its Director in January 2022.

He specializes in the area of Computer Architecture, Information Security and VLSI Design. He heads the Microprocessor Development Program and the Information Security Education and Awareness Program at IIT Madras funded by the Ministry of Electronics and Information Technology, Government of India. He is member of the National Security Advisory Board. He was also the Chairman of the Artificial Intelligence Task Force constituted by the Ministry of Commerce and Industry, Government of India. He is appointed as member of the institute body of AIIMS, Madurai. At IIT Madras, he has served as the Chairman, JEE and as Associate Dean, Industrial Consultancy and Sponsored Research.

He has over 150 publications in International Journals and Conferences, guided many research scholars for their PhD and Master of Science (By research) program. He has coordinated and successfully delivered close to 50 projects from Industry and Government R&D establishments. He serves in the Technology committees of the National Stock Exchange and Reserve Bank of India.

Dr. Kamakoti is the recipient of DRDO Academic Excellence Award, Indian Electronics and Semiconductor Association Techno Visionary Award, 'Abdul Kalam Technology Innovation National Fellowship', ACCS Life-time Achievement Award, IBM Faculty Award and VASVIK Industrial Research award.

- **AI-enabled smart and secure electronic systems design and Indigenous Electronic Design Automation Tools for VIKSHIT BHARAT 2047**

  Gaurav Trivedi, IIT Guwahati

Self-reliance is the key to unimaginable success, and India is poised to achieve it by 2047 through VIKSHIT BHARAT 2047 mission. Semiconductors and ESDM have become prominent in all domains, and most products around us incorporate electronics subsystems. Therefore, creating a complete ecosystem for ESDM is imperative, and the role of the semiconductor chip design and manufacturing ecosystem becomes pivotal. Developing Indigenous electronic design automation is critical in designing ICs and enabling anybody to innovate and create electronic systems cheaply. This talk summarizes the ongoing activities in chip design, electronic design automation, and advanced workforce development needed to achieve the goal.

Dr Gaurav Trivedi is a faculty member of the Electronics and Electrical Engineering Department at IIT Guwahati. He received an MTech (Microelectronics) and PhD in Electrical Engineering from the Indian Institute of Technology Bombay, India, in 2000 and 2007. Dr Gaurav Trivedi is the principal investigator of Daksh Gurukul, a joint skill development programme of IIT Guwahati, NSDC, and MSDE. He is also the Principal Investigator of the Electronics & ICT Academy, and Nine Labs funded by MeitY. Dr. Trivedi has 08 Indian Patents, 07 Book and Book Chapter Publications, and more than 150 peer-reviewed journal and conference articles. He has received 06 best paper awards in peer-reviewed international conferences. He has been a Visiting faculty/ Expert in 10 national and international institutes. Under his supervision, 21 PhD students, 75 MTech students and over 90 BTech students have graduated, and over 25 PhD and 10 MTech students are enrolled in different projects at IIT Guwahati. Under his guidance, E&ICT Academy IIT Guwahati has completed 400+ advanced skilling courses, including VLSI, AI/ML, Security, Semiconductor Technology,

Embedded Systems, etc., and trained over 25,000 faculty members, students, industry professionals and government officials in the last seven years. Dr. Gaurav Trivedi was the General Chair of VLSI Design 2021 and served on various international conference committees. He chairs the Board of Studies of Electronics and Communication Engineering at Assam Science and Technical University. He actively set up Northeast's first supercomputer, PARAM-ISHAN, and established the High-Performance Computing and FPGA Lab at IIT Guwahati. He is actively involved in designing an AI Accelerator, Quantum Secure Cryptography Engine, Smart Secure Camera and Neuromorphic computing-based ML systems. his research interests are in Electronic Design Automation (VLSI CAD), Digital Design, Neuromorphic Computing, Embedded Systems, Hardware Security, Hardware Machine Learning Architectures, and Smart Agriculture.

The Open-Source PULP Platform for tinyML Heterogeneous Hardware Acceleration

Francesco Conti, Unibo

In the last few years, our perception of what constitutes a "tinyML device" has shifted from simple microcontrollers to complex heterogeneous SoCs suited to execute DNNs directly at the extreme edge in real time and at minimal power cost. These devices provide ultra-low latency and high energy efficiency necessary to meet the constraints of advanced use cases that cannot be satisfied by cloud solutions. However, how can tinyML hardware keep up with the evolution of the AI landscape, continuously pushing towards much larger and more complex models? The costs to develop new accelerators and Neural Processing Units for each evolutive step in AI are hard to sustain. A possible way forward is given by the open-source model for digital hardware, popularized by RISC-V: multiple actors – both academic and industrial – collaborate on the development of digital technology that can benefit all parties. In this presentation, I discuss a 10+-year "quest" to push the performance and energy efficiency of tinyML further and further by exploiting a fully open-source model based on the PULP Platform initiative. I show how the open-source cooperative model makes it possible to combine different ideas and contributions in a technologically portable way, acting as an innovation catalyst and enabling the fast pace of evolution required to keep up with new ideas in AI within a tiny power budget.

Francesco Conti received his Ph.D. degree in electronic engineering from the University of Bologna, Italy, in 2016. He is currently a Tenure-Track Assistant Professor with the DEI Department at the University of Bologna. He has also served as a consultant on hardware acceleration for AI for GreenWaves Technologies, Grenoble from 2020 to 2024. From 2016 to 2020, he held a research grant with the University of Bologna and a position as a Post-Doctoral Researcher with ETH Zürich. His research is centered on hardware acceleration in ultra-low power and highly energy-efficient platforms, with a particular focus on System-on-Chips for Artificial Intelligence applications. His research work has resulted in more than 100 publications in international conferences and journals and was awarded

several times, including the 2020 IEEE Transactions on Circuits and Systems I: Regular Papers Darlington Best Paper Award.

Digital system design at IIT Bombay

Madhav P. Desai, IIT Bombay

In this talk, I will describe our research in to tools and system realizations. The focus of the tools related work is to establish an algorithm to System-on-chip flow for the rapid realization of custom optimized embedded systems. Using these tools, we have designed several complex systems ranging from processors to a GPS/IRNSS receiver SOC. Currently, we are working in the area of secure processor realizations and high-performance embedded systems.

Madhav P. Desai received his B.Tech. (Electrical Engineering) degrees from the Indian Institute of Technology Bombay, and a Ph.D. (Electrical Engineering) degree from the University of Illinois (Urbana-Champaign). He is currently a Professor (Electrical Engineering) at the Indian Institute of Technology Bombay (in Mumbai, India). His areas of interest are in VLSI Design, Circuits and Systems, and VLSI CAD tools. Prior to joining IIT-Bombay as a faculty member, he was part of the semiconductor engineering group at Digital Equipment Corporation, Hudson MA (USA). He is also a director in Powai Labs Tech. pvt.ltd., a company which was incubated at IIT-Bombay. His work includes :

- The development of the AJIT micro-processor, a flexible and scalable processor which has been proven in Silicon.
- The development of the AHIR-V2 algorithm to hardware compiler toolset which maps algorithms described in high level languages (C, Python) to hardware and systems-on-chip.
- The development of a 3D capacitance extractor.
- Static timing analysis of digital circuits using accurate, embedded SPICE models.

He is currently working in the area of secure digital systems and high performance embedded computing.

FINAL SESSION – CLOSING REMARKS

Elles van de Ven is Policy Officer within the Unit "Microelectronics and Photonics" at the European Commission, Directorate General for Communications Networks, Content & Technology. She received a LL.M. from the Amsterdam Law School of the University of Amsterdam, specialising in European Competition Law and Regulation. After her studies, Elles worked for the Ministry of Economic Affairs and Climate Policy of the Netherlands, playing a key role in Dutch semiconductor policy initiatives. In the European Commission, she works on

implementation of the European Chips Act, economic security and international cooperation.

CHAIRS

Giorgos Fagas PhD MBA is Head of CMOS++ and EU Programmes at Tyndall, and member of Tyndall's Leadership Team. CMOS++ is a strategic programme addressing emerging materials, devices and architectures for next-generation information processing interfacing with CMOS and beyond. He is contributor to key international strategic R&I agendas incl. the ECS-SRIA and IRDS and has initiated several large-scale EU projects. He currently leads the EU-funded programmes for open access to infrastructure for early-stage research on nanoelectronics and semiconductor chips, respectively, ASCENT+ and INFRACHIP, and the ICOS project activity on Technology Scanning and Foresight. Giorgos holds prominent positions in various policy and industry groups including Director of the SiNANO Institute.

Francis Balestra, CNRS Research Director at CROMA, is Director Emeritus of the European SINANO Institute and President of IEEE Electron Device Society France, and has been Director of several Research labs. He coordinated several European Projects (NEREID, NANOFUNCTION, NANOSIL, etc.) that have represented unprecedented collaborations in Europe in the field of Nanoelectronics, and is currently coordinator of the Horizon Europe ICOS project dedicated to International Cooperation on Semiconductors with leading semiconductor countries. He founded and organized many international Conferences, and has co-authored more than 500 publications. He is member of several European Scientific Councils, of the Advisory Committees of International Journals and of the IRDS (International Roadmap for Devices and Systems) International Roadmap Committee, as representative of Europe.