IC and System Design

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Process Nodes	Year
20 µm	1968
10 µm	1971
6 µm	1974
3 µm	1977
1.5 µm	1981
1 µm	1984
800 nm	1987
600 nm	1990
350 nm	1993
250 nm	1996
180 nm	1999
130 nm	2001

Process Nodes	Year
90 nm	2003
65 nm	2005
45 nm	2007
32 nm	2009
28 nm	2010
22 nm	2012
14 nm	2014
10 nm	2016
7 nm	2018
5 nm	2020
3 nm	2022
2 nm	Beyond 2025 ?

What does this table indicate to us?

➡ **MOSFET Scaling and Process Nodes over the years**

Moore's Law

Rent's rule

Why doubt at all?

ICS are Typical Semiconductor devices

- Processors,
- Microcontrollers,
- Memory Chips (NAND flash and DRAM)

➡ **All most all ICS are typically CMOS Devices**

What's EDA?

CMOS Based Mostly

Semi-Conductor Manufacturing

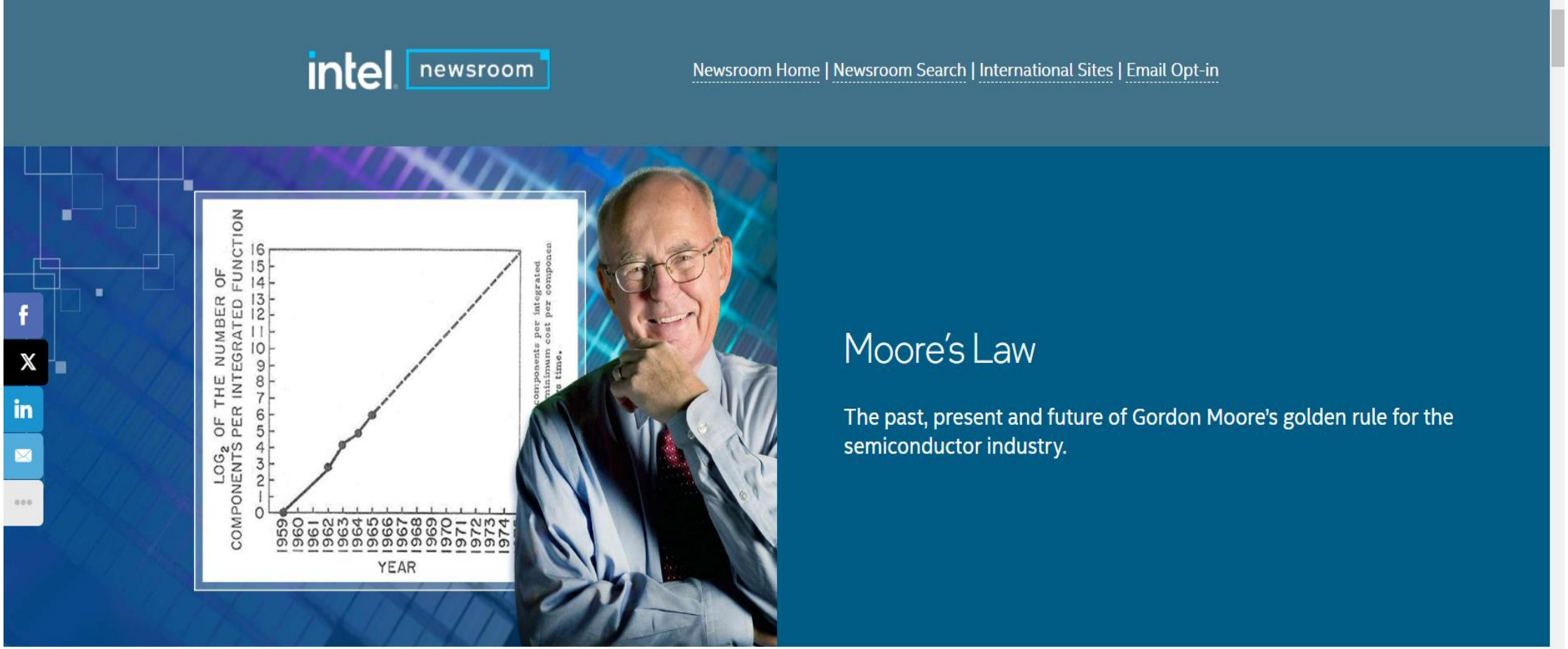
Metrology

ASIC, SOC, FPGA, CPLDs, Memories..

Electrical, Electronics, Mechanical, Computer Science, Industrial, Material Sciences, Chemicals …

Analog/Digital/Mixed Signal/RF High Speed/Power Aware/Low Power
Consumer Electronics, Automotive Aerospace Safety Critical
Medical, Industrial, Instrumentation, Power Systems
IOT, CPS, Edge Devices, Embedded Systems, Transducers
PCS, Servers, GPGPUS, HPC, FPGA Boards
Mobile, Telecom Networking, Satellite Communication, Positioning Systems
Software, Simulation, Emulation, Modeling, Verification, Validation, Testing

Integrated Chips System Design



Ref : https://www.intel.com/content/www/us/en/newsroom/resources/moores-law.html#gs.fnxl6a

Summing UP →

All Electronic Devices and ICs

ICS are typically Semiconductor Devices

Rent's Rule
Coincidence or the Result of the Design Process?

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The design process for VLSI systems requires several iterations of the physical design cycle. After a partitioning of the circuit and a floorplanning step, the circuit components are placed. The wires between the components are then routed taking the placement into account. A bad placement cannot be solved by a good routing. Therefore, the information obtained during routing generally leads to a new placement step to improve the placement results. A new routing is then performed and so on.

In order to fasten the iteration process and to improve the placement and routing results, it is mandatory to efficiently use estimates of area, wire length, etc. Three kinds of estimates are used: a priori, on line, and a posteriori estimates [1, 2]. The first kind estimates circuit parameters before any of the layout steps (floorplanning, placement, or routing) is performed. On line estimates are obtained during the layout process and are based on the information that results from the layout process itself. A posteriori estimates are obtained after a complete layout step and present the layout results.

A priori estimates need basic information on the circuit to be designed, on the architecture in which it is to be designed, and on the layout process that performs the implementation of the circuit into the architecture [3, 4]. In this position statement, we consider the circuit information.

Apart from the number of gates (or blocks) in the circuit, its number of in- and outputs, its number of nets and number of pins, the most important information is the notion of interconnection complexity of the circuits netlist.

The interconnection complexity information is provided by Rent's rule [5]

$$P = T_b\, B^r$$

where B is the number of gates (blocks) in the circuit, P is the number of pins, and T_b is the average number of terminals per gate (block). The exponent r is called the Rent exponent and is a measure for the interconnection complexity of the circuit. The problem is: "can we rely on the Rent exponent to make a priori estimations?" To answer this question, we have to ask ourselves some related questions:

Ref : https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=3c51d041b2cefe4b5ae7df7ec1ec6ade93bb6b05

This relates to the number of I/Os required for a block containing a given number of computing elements

GlobalFoundries Stops All 7nm Development: Opts To Focus on Specialized Processes

127 Comments

by Anton Shilov & Ian Cutress on August 27, 2018 4:01 PM EST

Posted in Semiconductors CPUs AMD GlobalFoundries 7nm 7LP

7LP CANNED DUE TO STRATEGY SHIFT

For most of our lives, the idea that computers and technology would get better, faster, and cheaper every year was as assured as the sun rising every morning. The story "GlobalFoundries Halts 7-nm Chip Development," in *IEEE Spectrum*, doesn't sound like the end of that era, but for you and anyone who uses an electronic device, it most certainly is.

Technology innovation is going to take a different direction.

GlobalFoundries was one of the three companies that made the most advanced silicon chips for other companies, such as AMD, IBM, Broadcom, Qualcomm, STM and the Department of Defense.) The other foundries are Samsung in South Korea and TSMC in Taiwan. Now there are only two pursuing the leading edge. (Intel too is pursuing these advanced chips, but its business making chips for other companies is relatively small.)

This is a big deal.

Ref https://www.anandtech.com/show/13277/globalfoundries-stops-all-7nm-development

Ref https://spectrum.ieee.org/what-globalfoundries-retreat-really-means

- System-Level Electronics Design
- Chip-Level Electronics Design
- Embedded Design
- System Modelling
- Std Cell Libraries
- I.S.A design [Open-Source vs Proprietary]
- I/O and Peripherals [Opensource vs Proprietary]
- SOC inter and Intra connects [Open-Source vs Proprietary]
- Packaging
- Reliability and Quality
- Timing
- Functionality
- Synthesis
- Verification and Validation
- Yield Analysis
- Simulation and Emulation, Modelling
- Power Electronics
- PCB Designing
- RF, Analog, Mixed Signal Modelling, Simulations
- ….

Enter EDA

There are 1000s of books and articles written, lectures delivered

Definition

Electronic Design Automation, or EDA, is a market segment consisting of software, hardware, and services with the collective goal of assisting in the definition, planning, design, implementation, verification, and subsequent manufacturing of semiconductor devices, or chips. Regarding the manufacturing of these devices, the primary providers of this service are semiconductor foundries, or fabs. These highly complex and costly facilities are either owned and operated by large, vertically integrated semiconductor companies or operated as independent, "pure-play" manufacturing service providers. This latter category has become the dominate business model.

Why is EDA Important?

Semiconductor chips are incredibly complex. State-of-the-art devices can contain over one billion circuit elements. All of these elements can interact with each other in subtle ways, and variation in the manufacturing process can introduce more subtle interactions and changes in behavior.

There is simply no way to manage this level of complexity without sophisticated automation, and EDA provides this critical technology. Without it, it would be impossible to design and manufacture today's semiconductor devices.

It is also worth noting that the cost of an error in a manufactured chip can be catastrophic. Chips errors cannot be "patched." The entire chip must be re-designed and re-manufactured. The time and cost of this process is often too long and too expensive, resulting in a failure of the entire project. So, the complexity to design chips is high and the need to do it flawlessly is also required.

Without EDA tools, these challenges cannot be met.

Ref : https://www.synopsys.com/glossary/what-is-electronic-design-automation.html

What does EDA mean to A Theoretical Computer Scientist

IC designs are NP-hard.

- The complexity of Integrated Circuits (IC) has increased exponentially, posing challenges to circuit design's scalability and reliability.
- EDA algorithms and software must be more effective and efficient to handle a large search space with low runtime.
- Many problems in EDA, are placement and wiring or scheduling.
- Simulation, Emulation, and Modeling are Complex and Resource Intensive

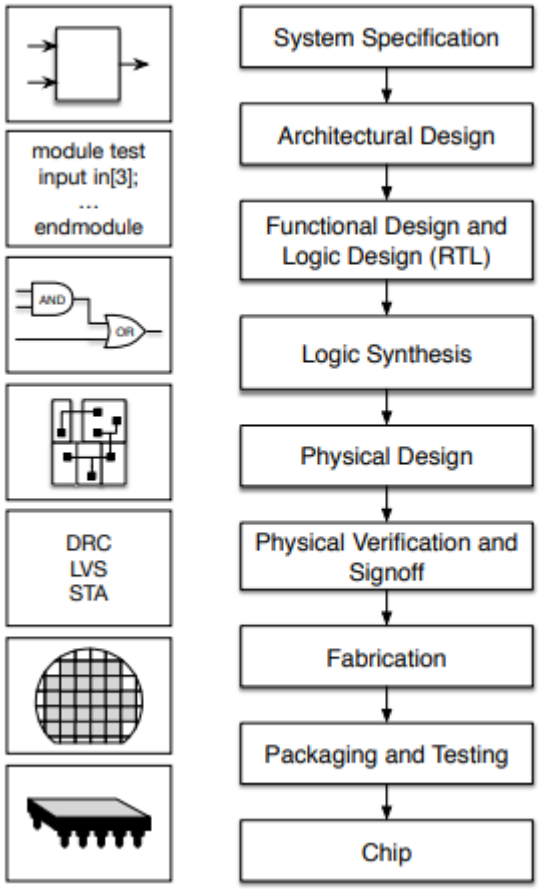
Without EDA, Moore's law would have remained applicable to ONLY satisfy curiosity.

The world wouldn't have had a single billion- -million or even a 1000s transistor chip.

Without EDA, systems could not have been designed, modelled, simulated, debugged, or tested.

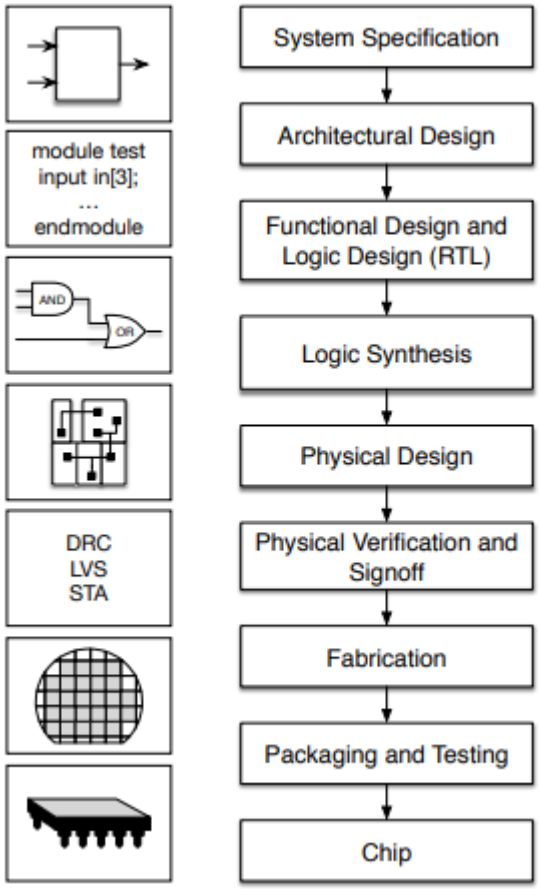
Modern Day Computer-Aided Design Tools aids all System Design

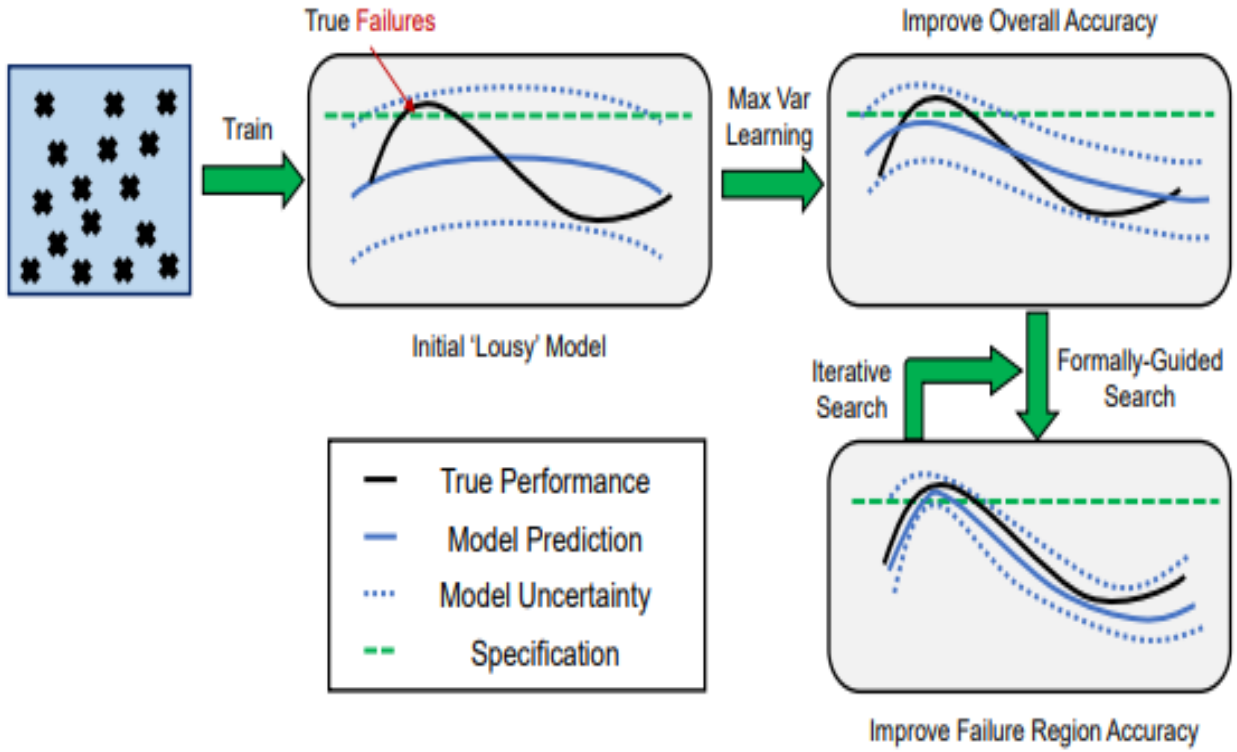
Enter ML Methods



Optimization Idea	Task	ML Algorithm
Test Set Redundancy Reduction	Digital Design	Statistical Model
		Search Methods
		Rule Learning
		CNN, SVM, et al.
		GCN
	Analog/RF Design	KNN, ONN
		Regression
	Semiconductor Technology	CNN
Test Complexity Reduction	Digital Design	SVM, MLP, CNN, et al.
	Analog/RF Design	ONN
		Active Learning

Ref : https://arxiv.org/pdf/2102.03357





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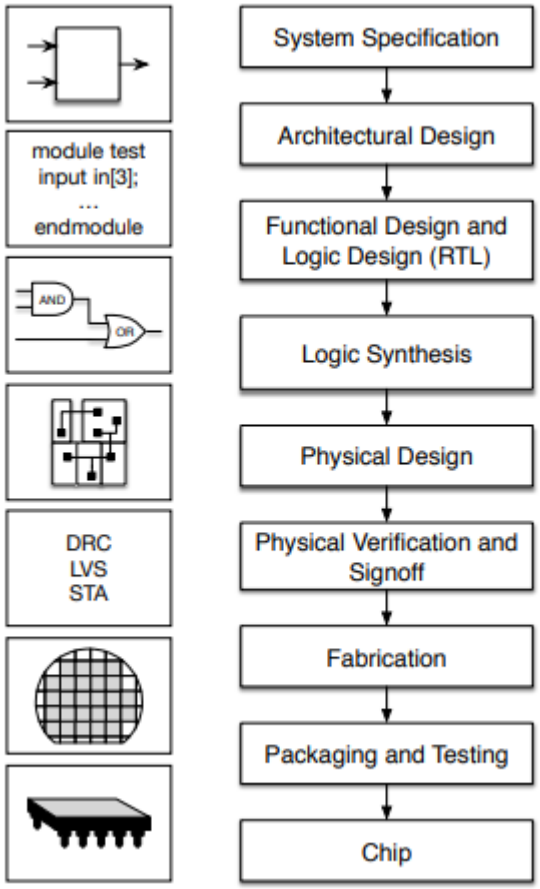


ML Functionality	Task / Design Stage	ML Algorithm	Input	Output
Decision making in traditional methods	HLS Design space exploration	Decision Tree, quadratic regression, etc.	Hardware directives (pragmas) in HLS design	Quality of hyper-parameters, e.g., initial state, termination conditions
	Logic synthesis	DNN	RTL descriptions	Choice of the workflow and optimizer
	Mask synthesis	CNN	Layout images	Choice of optimization methods
Performance prediction	Analog topology design	CNN, Fuzzy logic, etc.	Analog specifications	Best topology selection
	HLS	Linear Regression, SVM, Random Forest, XGBoost, etc.	HLS Report, workload characteristics, hardware characteristics	Resource usage, timing, etc.
	Placement and routing	SVM, CNN, GAN, MARS, Random Forest etc.	Features from netlist or layout image	Wire-length, routing congestion, etc.
	Physical implementation (lithography hotspot detection, IR drop prediction, power estimation, etc.)	SVM, CNN, XGBoost, GAN, etc.	RTL and gate-level descriptions, technology libraries, physical implementation configurations	Existence of lithography hotspots, IR drop, path delay variation, etc
	Verification	KNN, Ontogenic Neural Network (ONN), GCN, rule learning, SVM, CNN	Subset of test specifications or low-cost specifications	boolean pass/fail prediction
	Device sizing	ANN	Device parameter	Possibility of constraint satisfaction

Ref : https://arxiv.org/pdf/2102.03357

- Could we do Analog/RF testing/Physical design, with their performance tied to machine learning models or an ML and Classical Methods ensemble?
- How would this meet the industrial needs?
- How to trust ML methods?
- Do we have enough trust in classical EDA?

Night Marish? Or Exciting Opportunities?

EDA for QComp

QComp for EDA

- Limitations of Semi-Conductor Process Nodes?
- FIN FET and Tunneling effect and other Quantum Effects
- Which QUBIT Manufacturing for Utility QComps?

Enter Quantum Computing

Information is processed based on Binary Logic - BITS	Information processed] – based on Logical of Quantum Mechanics - QUBIT
Logic elements that operate with N distinct states	Logic elements that operate with N states with different probability amplitudes simultaneously
Computational Power is based on the number of distinct states.	Computational Power is based on a linear combination of probability amplitude states.

Based on Binary States

Algorithms

Parallel Operations

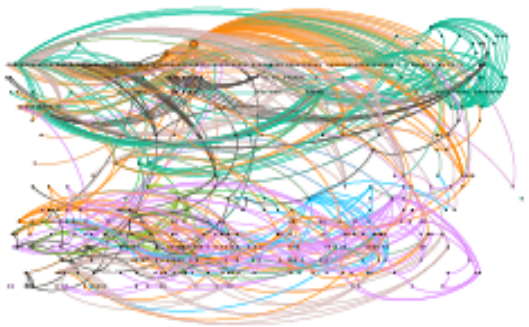
CMOS Based Transistors

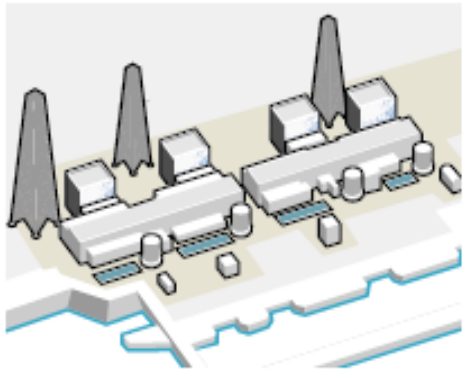
Super Position → The Basis

Interference → Quantum Algorithms

Entanglement → To be Harnessed

Super Conducting, Cold atoms, NV Centre, Photons..





complex problem
unreacheable in human time for classical computing

much faster resolution
than classical computing and useful task with input data

doing something useful
and quantum circuit hard to simulate classically

energy, cost, weight
better with quantum computing

aka « **quantum supremacy** »
or « **quantum primacy** »

aka « **quantum advantage** »
and « **quantum utility** »

« **quantum utility** »

IBM

aka « **quantum energy advantage** »

#QEI
the quantum energy initiative

sometimes used as synonyms...

Figure 788: trying to define quantum supremacy (or primacy) and quantum advantage. (cc) Olivier Ezratty, 2022-2024.

- From the viewpoint of a C.S and a Policy advocate, I believe
  - Utility of a QCOMP comes when we can't solve a classical problem with HP
  - When we have an industry-compatible manufacturing process for QUBIT Implementation
  - When the Energy, Power, and Operating Cost of QComp is better than the present HPCs
  - When QCOMPS are "Trustable"

- Till then?
  - Accelerate adoption of ML /Data Sciences methods in EDA and SemiCon Processes
  - As strong cases of utility QCOMP dawn, integrate ML and QCOMP
  - That time may not be far away though

Thankyou

Any Questions?