AI-ENABLED SMART AND SECURE ELECTRONIC SYSTEMS DESIGN AND INDIGENOUS ELECTRONIC DESIGN AUTOMATION TOOLS FOR VIKSHIT BHARAT 2047

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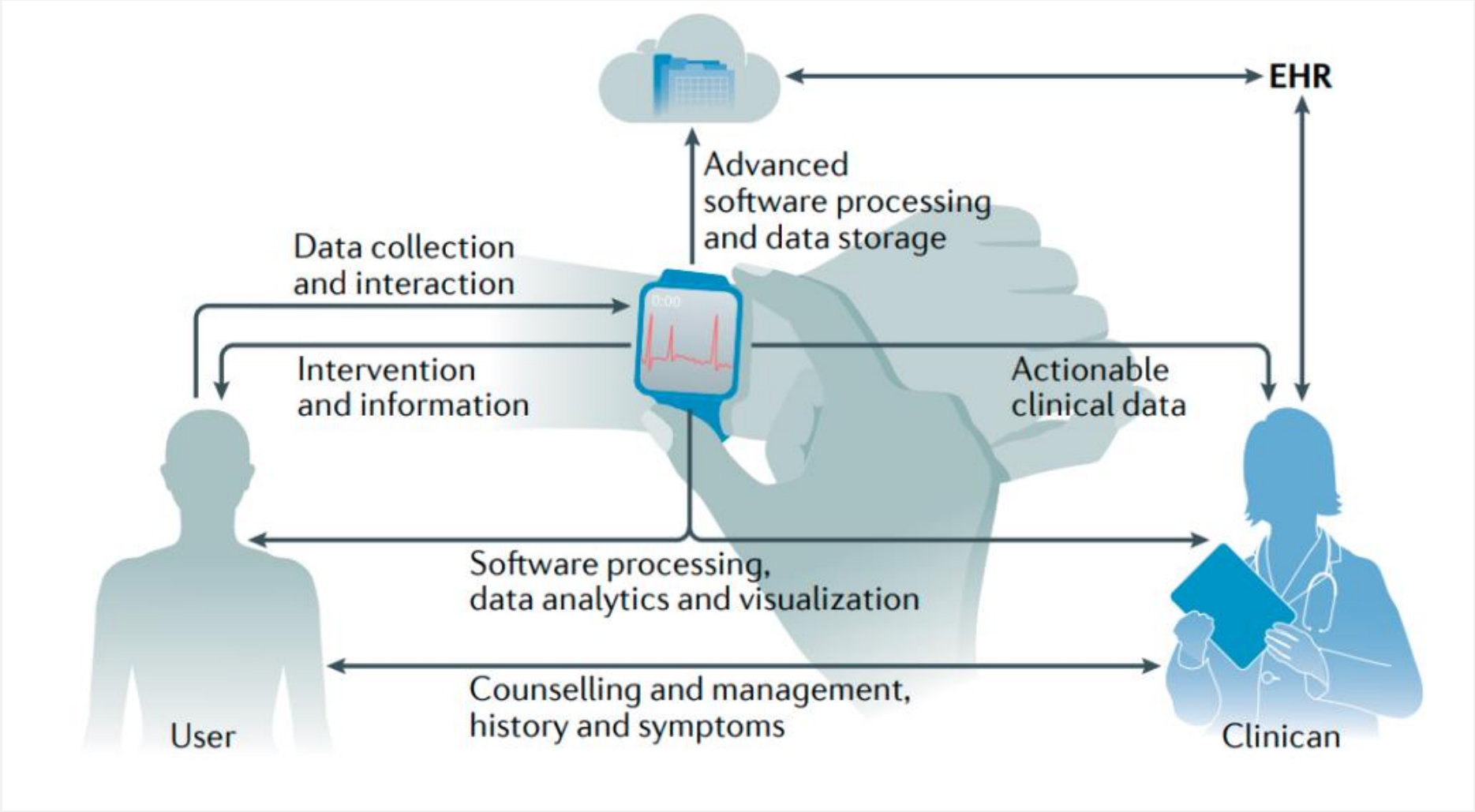
OUTLINE

- **Design**
  - Wearable Healthcare Devices
  - Post Quantum Cryptography Coprocessor
  - Secure AI SoC
  - Neuromorphic Computing Core
  - Roadmap
- **Electronic Design Automation (EDA)**
  - Analog/RF Circuit Simulator
  - TCAD Simulator
  - Floorplanning, Placement and Routing Engine
  - Power Analyzer
  - Roadmap
- **Advanced ESDM Workforce Development**
  - Roadmap

WEARABLE HEALTHCARE DEVICES



https://www.researchgate.net/publication/349774075_Smart_wearable_devices_in_cardiovascular_care_where_we_are_and_how_to_move_forward/figures?lo=1

WEARABLE HEALTHCARE DEVICES

Benefits of Wearable Technology

IT ALLOW MEDICAL FACILITIES TO STAY CONNECTED TO PATIENTS

IT ALLOWS USERS TO GAIN BETTER VISIBILITY INTO THEIR HEALTH STATUS

ENABLES BETTER AND ON-TIME TREATMENT, IMPROVING QUALITY OF LIFE.

LOWERS OPERATIONAL COSTS AND REDUCE NUMBER OF VISITS TO HOSPITALS

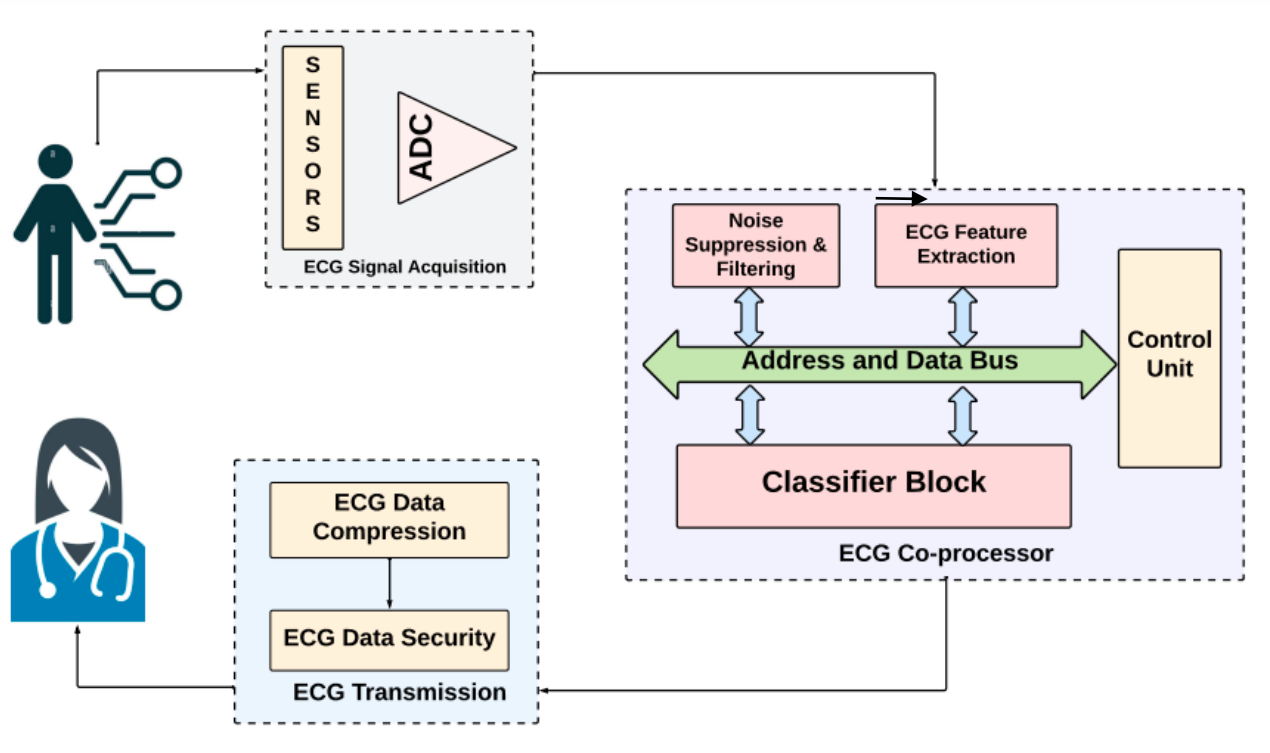
WEARABLE HEALTHCARE DEVICES

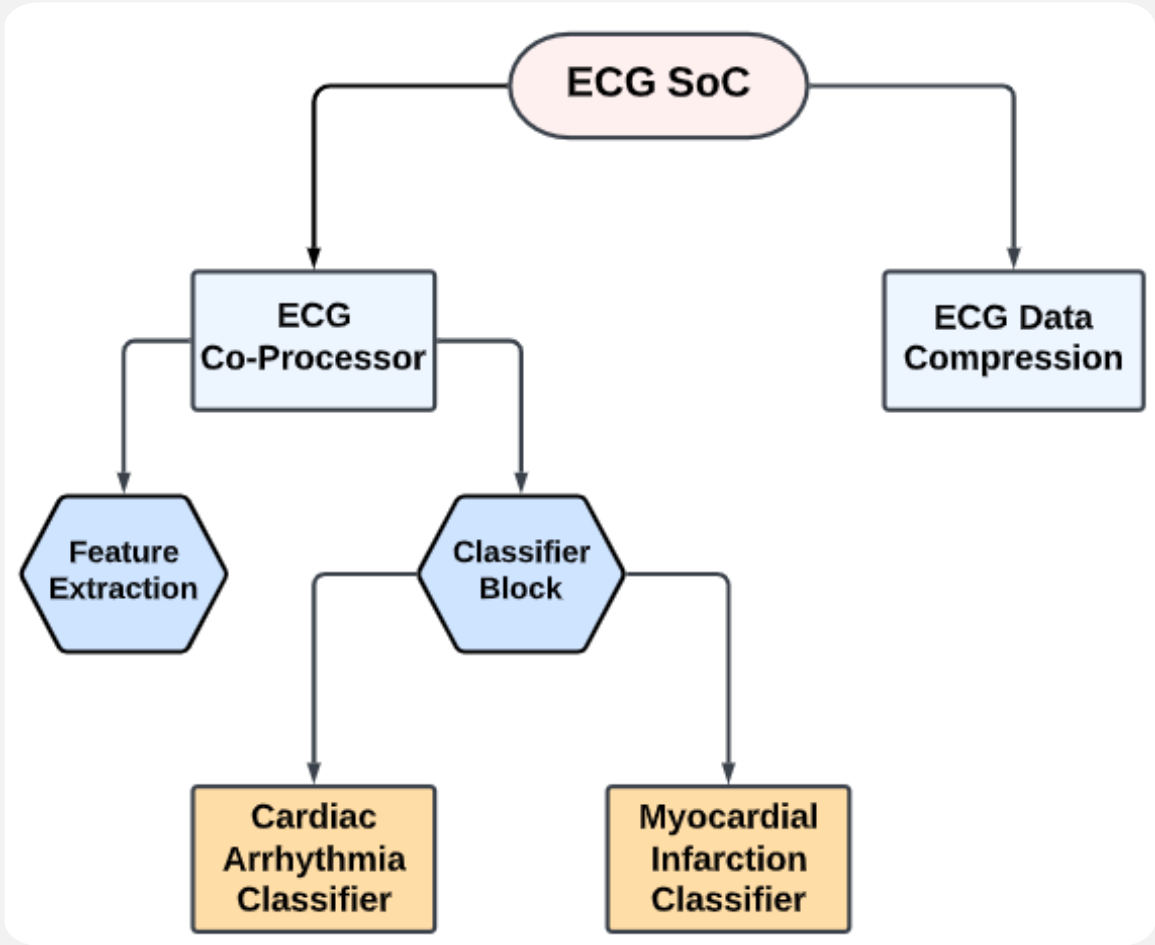
CHALLENGES FACED BY WEARABLES

- Availability of Medical Data
- Small Size and Wearability
- Battery Life
- Data Transmission of extensive medical data
- Data Security

WEARABLE HEALTHCARE DEVICES

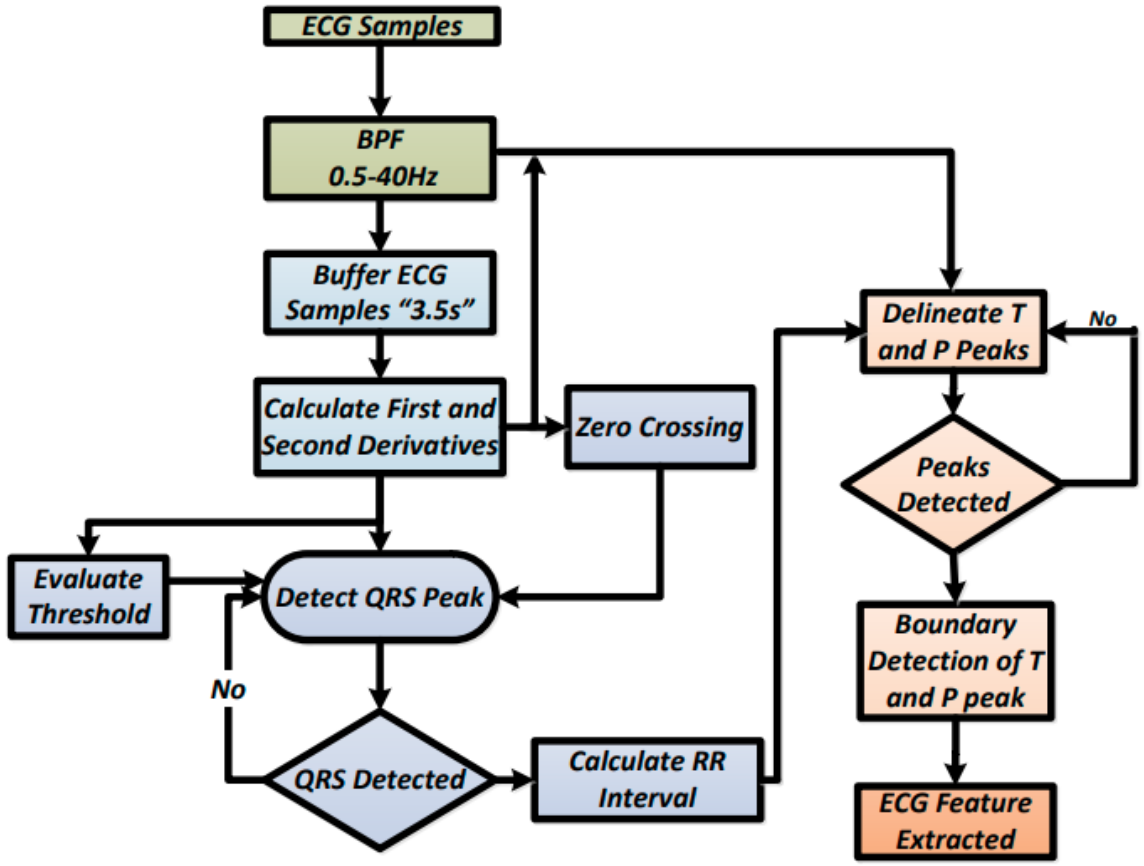
CONVENTIONAL ECG SOC FLOW





- Cardiovascular Disease Detection and Prediction
  - Detect different types of cardiac arrhythmia
  - Predict ventricular arrhythmia before its occurrence
  - Detect severity stages of Myocardial Infarction
- Multi-Lead ECG data compression

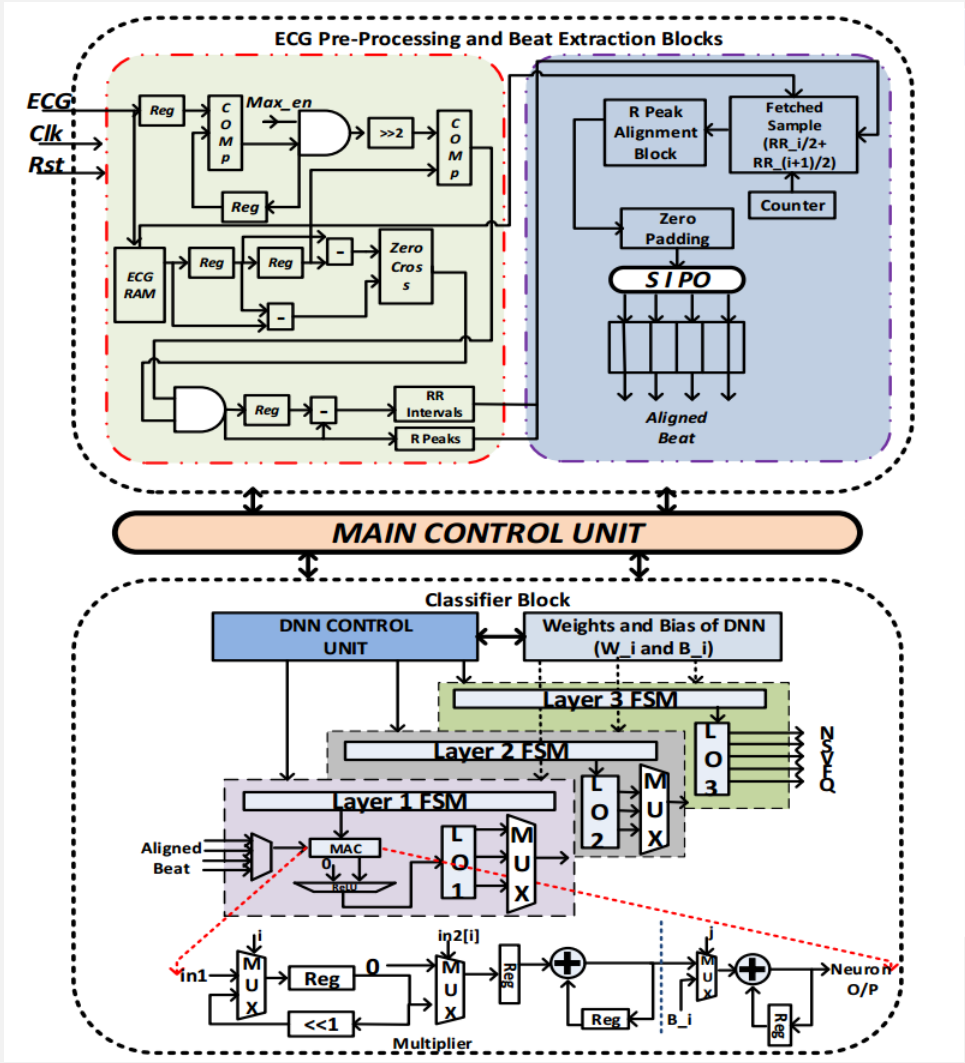
WEARABLE HEALTHCARE DEVICES



Parameter	[15]	[16]	[17]	[18]	Proposed
Technology	180nm	180nm	180nm	180nm	180nm
Frequency	1 MHz	1 MHz	NA	0.12 KHz	1 MHz
Supply Voltage	1.8V	1.2V	1.0V	1.2V	1.98V
ECG Features	P-QRS-T	P-QRS-T	QRS	QRS	P-QRS-T
Power	9.47µW	32µW	0.410µW	5.97µW	7.38µW

ECG FEATURE EXTRACTION ARCHITECTURE

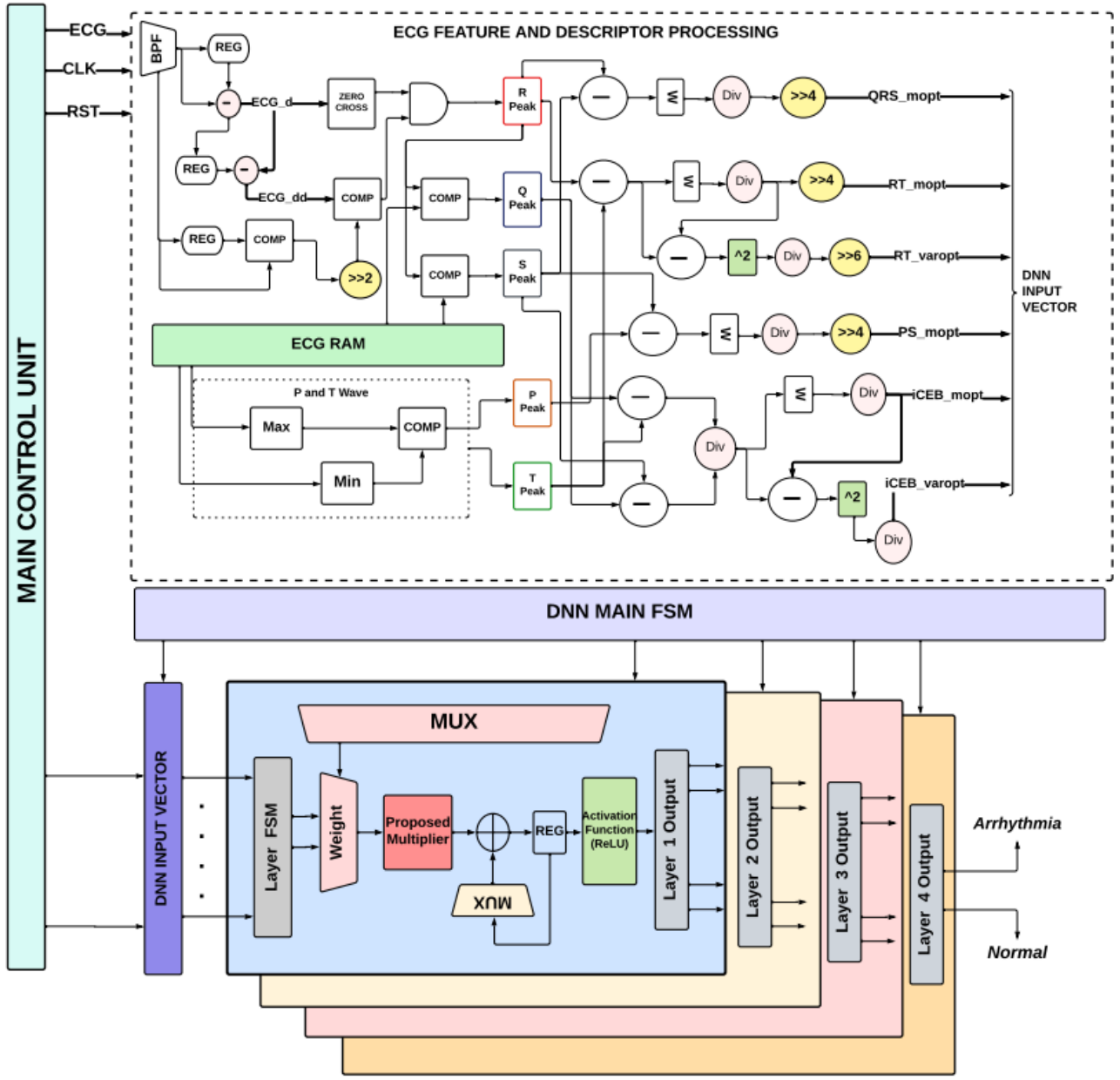
WEARABLE HEALTHCARE DEVICES



Parameter	[19]	[20]	[21]	[22]	Proposed
Technology	180nm	65nm	40nm	40nm	180nm
Frequency (Hz)	10k-25M	10k	1M	10k	12k
Supply Voltage	1.8	1	1	1.1	1.98
Power (W)	13.34µ	2.78µ	14.14m	3.76µ	8.75µ
Area (mm^2)	0.9250	0.112	0.135	0.12	1.32
Model	ANN	Naive Bayes	SVM	WLC+SVM	DNN
Evaluation Scheme	Patient Specific (PS)	Class Oriented (CO)	Subject Oriented (SO)	Class Oriented (CO)	Subject Oriented (SO)
Overall Accuracy(%)	99.39	86	88.06	98.2	91.6
Number of Classes	5	2	3	2	5

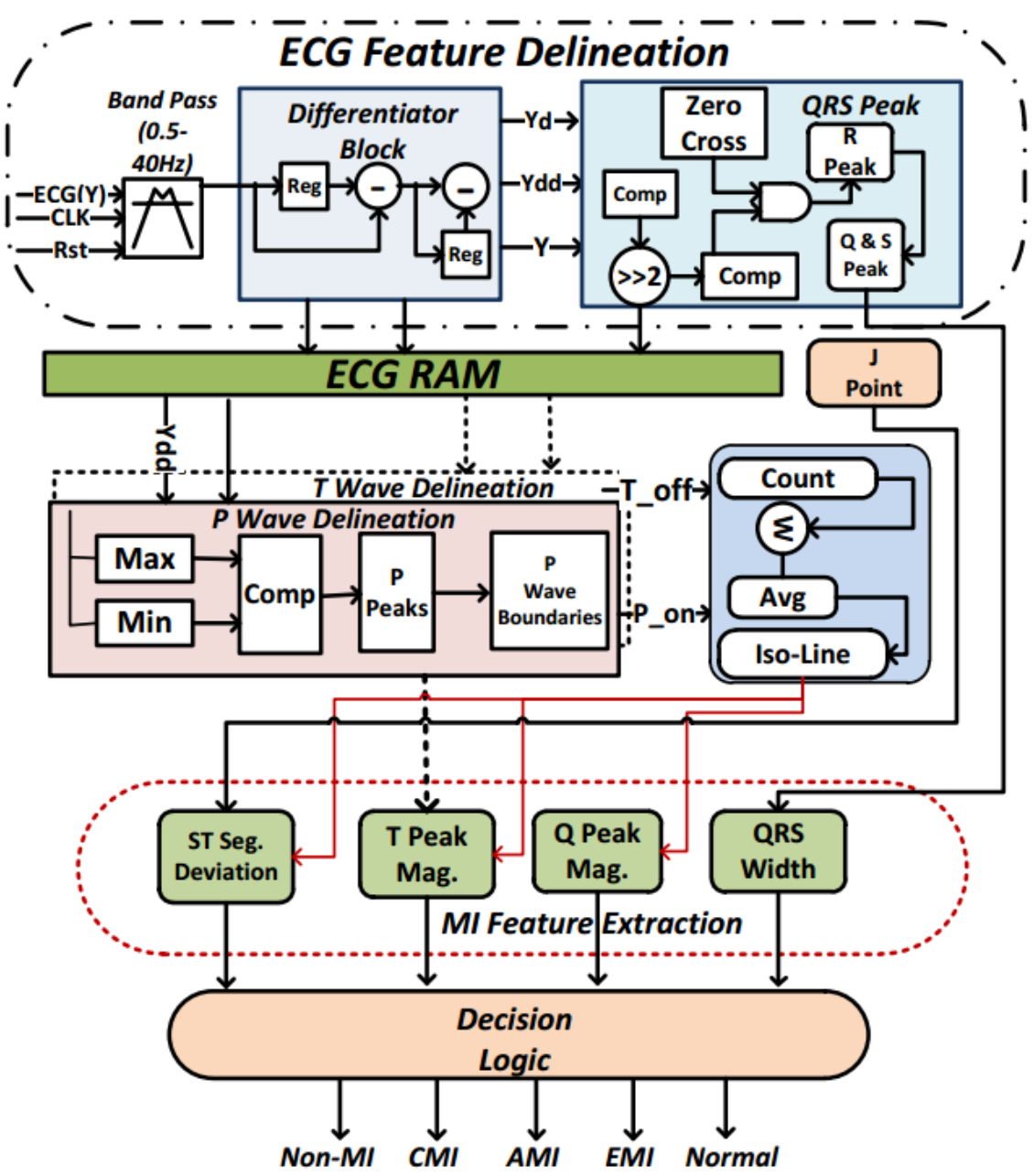
CLASSIFICATION OF FIVE TYPES OF CARDIAC ARRHYTHMIA

EARLY DETECTION OF VENTRICULAR ARRHYTHMIA



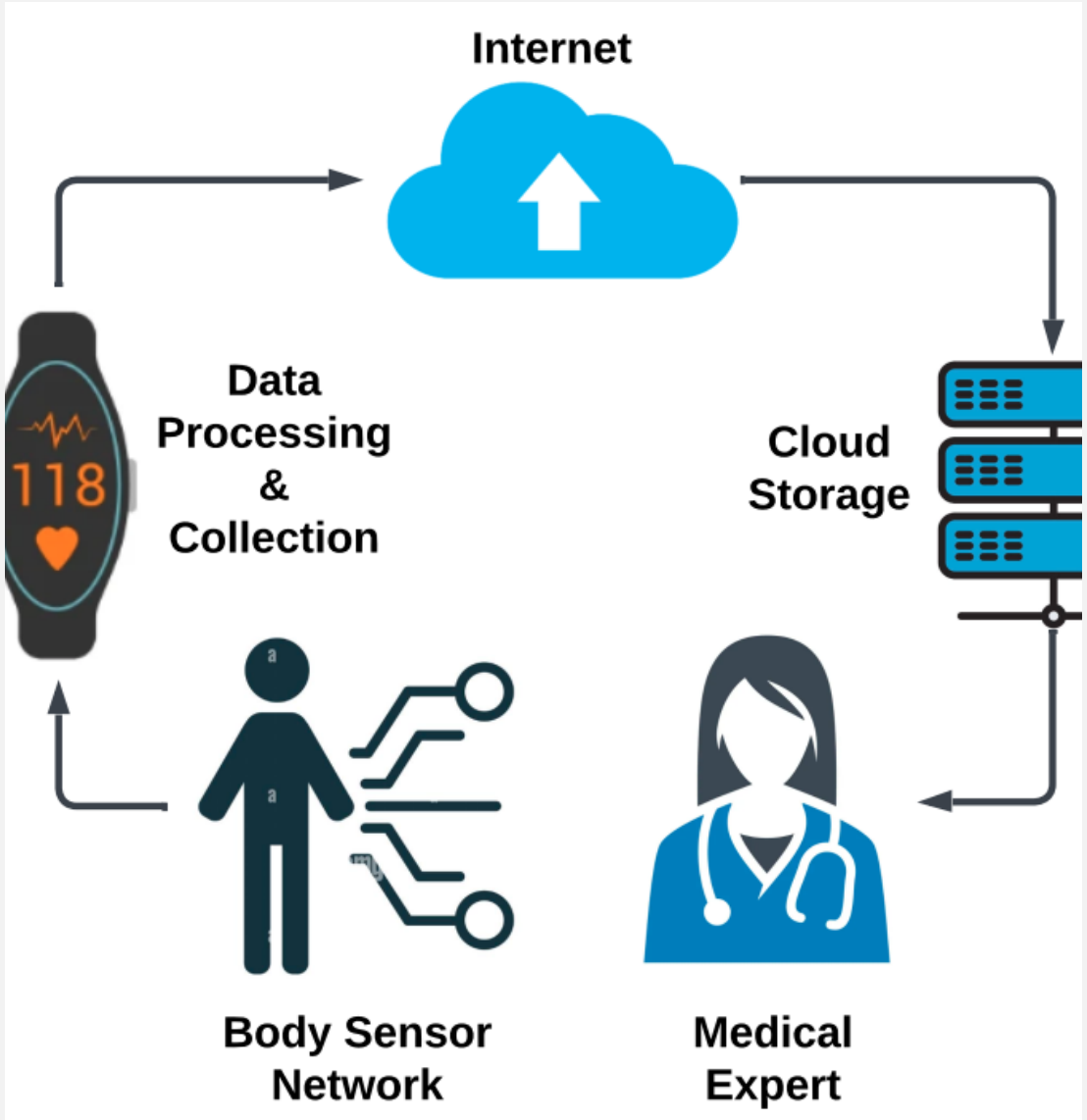
Parameter	[19]	[22]	[23]	[24]	[20]	Proposed
Approach	Detection	Detection	Detection	Prediction	Prediction	Prediction
Database	MIT-BIH	MIT-BIH	MIT-BIH	NSRDB, VFDB	MIT-BIH NSRDB	MIT-BIH
Classifier	ANN	SVM	Threshold Based	Decision Trees	Bayes Naive	DNN
Accuracy	99.68%	98.3%	97.02%	NA	86%	91.61%
Sensitivity	NA	NA	94.64%	95%	NA	91.94%
Specificity	NA	NA	99.41%	90%	NA	91.42%
Platform	ASIC	ASIC	ASIC	Software	ASIC	ASIC
Technology Node	180nm	40nm	180nm	NA	65nm	180nm
Voltage (V)	1.8	1.1	1.8	NA	1V	1.98V
Frequency (Hz)	25M	10k	1k	NA	10k	12.5kHz
Area (mm^2)	0.9246	0.12	NA	NA	0.112	1.8
Power (W)	13.34µ	3.76µ	5.04µ	NA	2.78µ	4.69µ

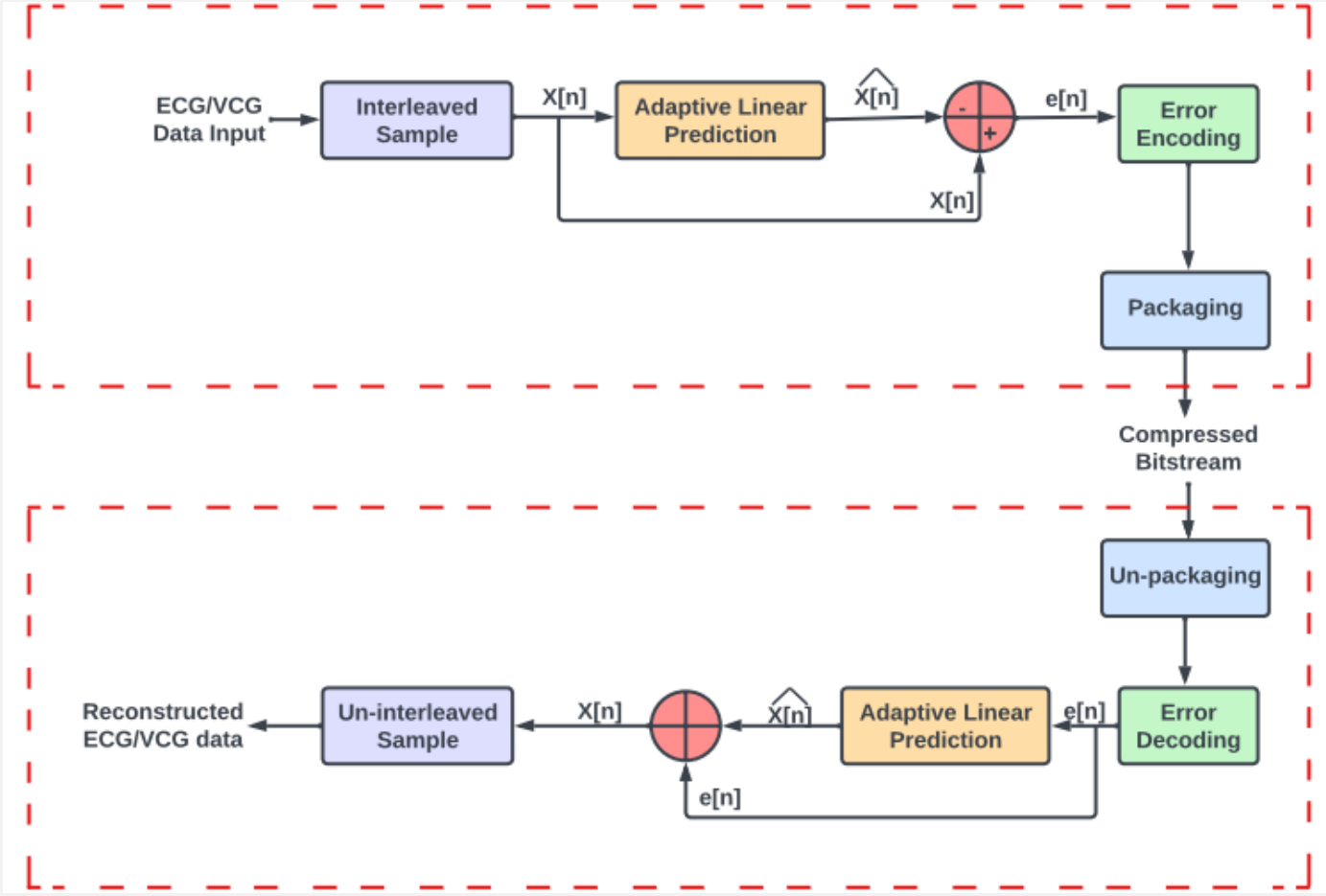
CLASSIFICATION OF STAGES OF MYOCARDIAL INFARCTION



Parameter	[25]	[26]	[27]	[28]	[29]	Proposed
Platform	Software	Software	Software	Software	ASIC	ASIC
Database	PTB, PTB-XL	PTB	PTB	STAFF III	Long Term ST	PTB, STAFF III, PTB-XL
Classes	2	2	2	2	2	5
Sensitivity(%)	91.59	99.97	85.33	83.3	96.43	EMI=84.42 AMI=85.6 CMI=80.2 Non-MI=88.22 Normal=92.46
Specificity(%)	85.89	99.54	84.09	91.7	96.88	EMI=97.3 AMI=96.7 CMI=97 Non-MI=95 Normal=96.3
Voltage (V)	NA	NA	NA	NA	1.8	1.98
Frequency (Hz)	250-1000	250	250	1000	250	8
Area (mm^2)	NA	NA	NA	NA	0.137	1.38
Power (W)	NA	NA	NA	NA	0.274u	5.12u

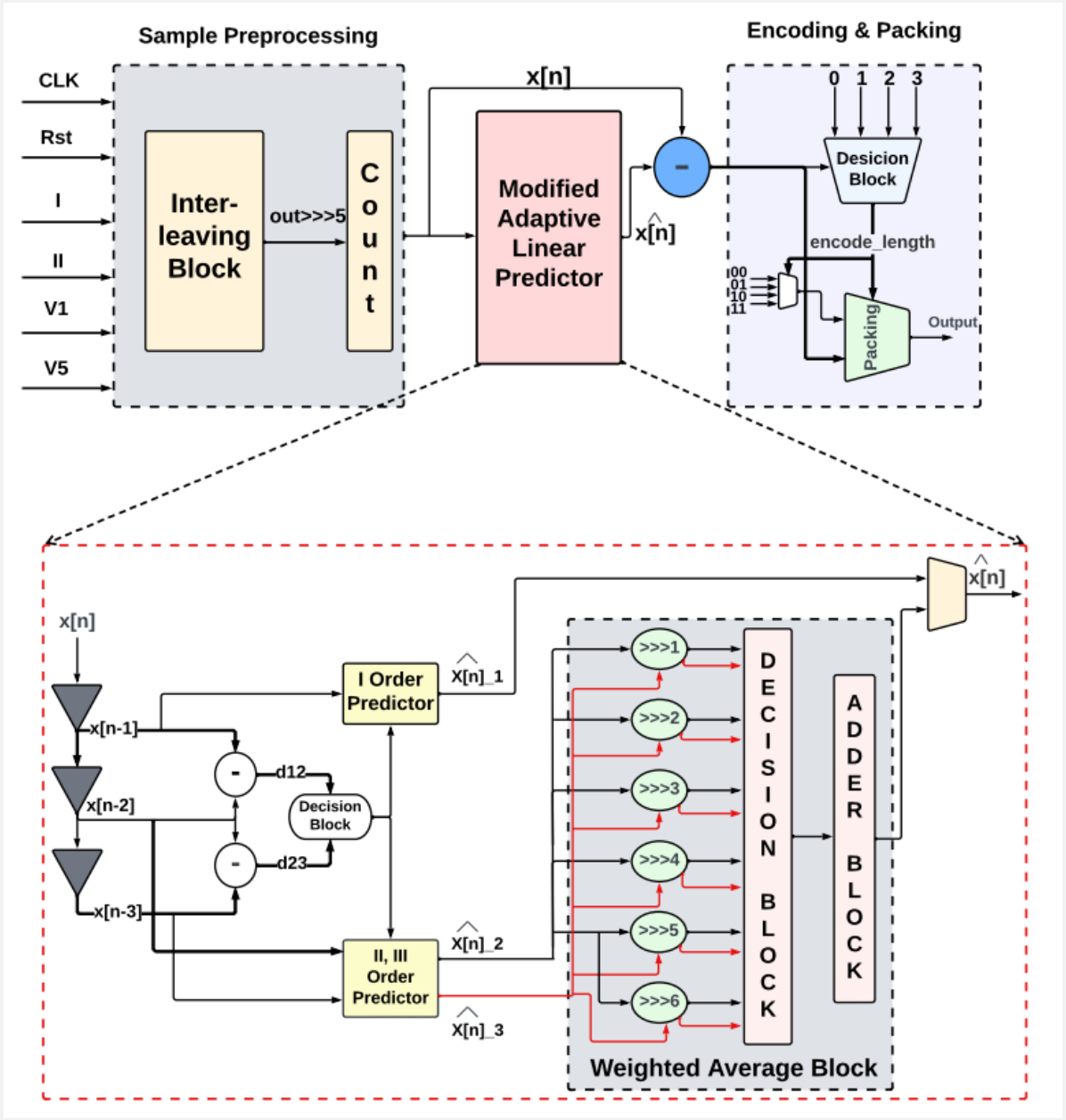
ECG DATA COMPRESSION

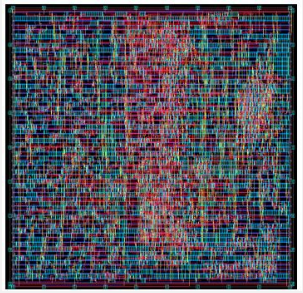




A GENERIC ECG DATA COMPRESSION SYSTEM

ECG DATA COMPRESSION

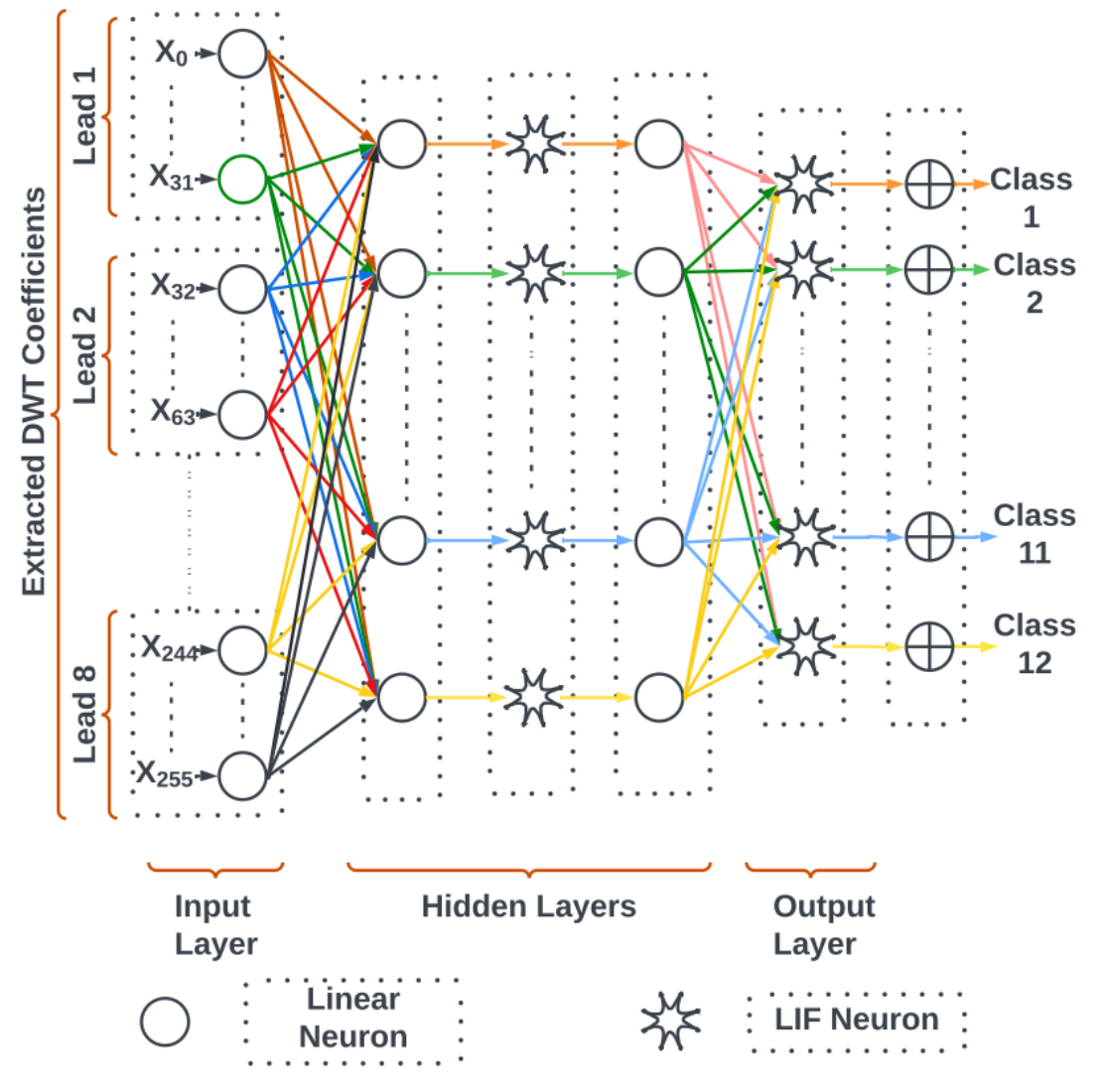




- Design Metrics:
  - **Area: 0.0831 mm^2**
  - **Voltage: 1.98V**
  - **Frequency: 36kHz**
  - **Power:2.102uW**
- Compression Ratio= 3.857

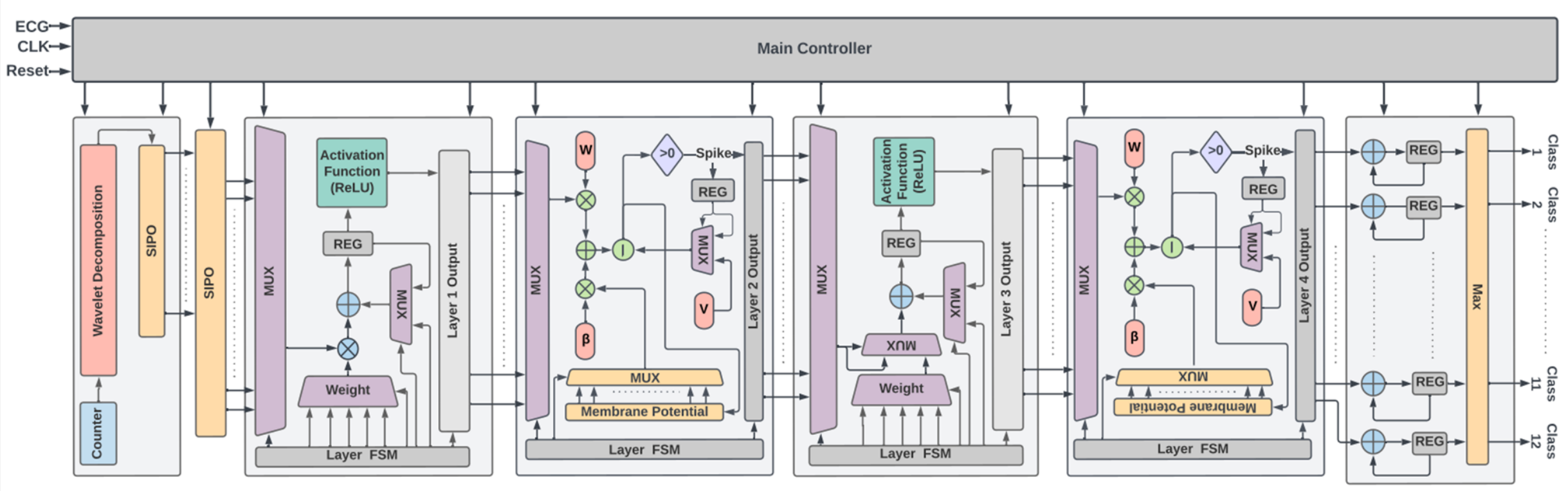
Parameter	[30]	[31]	[32]	Proposed	
Signals	ECG	ECG	ECG	ECG	
#Leads	4	1	2	4	
Function	Compression	Compression	Compression	Compression	Decompression
Type	Lossless	Lossless	Lossless	Lossless	
Database	PTB-DB	MIT-BIH	PTB-DB	PTB-DB	
Technology(nm)	180	90	180	180	
CR	4.067	2.91		3.86	
Voltage(V)	1	1.2	1.8	1.8	
Frequency(Hz)	1k	100M	16M	36k	
Area(mm^2)	16.4	0.0051	-	0.0813	0.0801
Gate Count	475.9k	0.4k	9.5k	2442	2412
Power Consumption(uW)	69.18	18.78	12.7	2.102	1.913

AN SNN INSPIRED AREA AND POWER EFFICIENT VLSI ARCHITECTURE OF MYOCARDIAL INFARCTION CLASSIFIER FOR WEARABLE DEVICES



Proposed Architecture

AN SNN INSPIRED AREA AND POWER EFFICIENT VLSI ARCHITECTURE OF MYOCARDIAL INFARCTION CLASSIFIER FOR WEARABLE DEVICES



Proposed Architecture

AN SNN INSPIRED AREA AND POWER EFFICIENT VLSI ARCHITECTURE OF MYOCARDIAL INFARCTION CLASSIFIER FOR WEARABLE DEVICES

Work / Parameter	[16]	[17]	[18]	[19]	[20]	[21]	[22]	[23]	[24]	[25]	[26]	Proposed Work
Features Used	Multi lead raw ECG	Multilead Fourier-Bessel Series expansion based empirical wavelet transform	Raw ECG	22 features extracted using variational mode decomposition (VMD)	Spectral and Phase coherence indices	T wave amplitude, Q wave amplitude and ST deviation	Raw ECG	Multi-lead raw ECG	Time domain Features extracted from DWT of ECG	Raw ECG	Multivariate variational mode decomposition of VCG	DWT
Classifier	GRU	CNN	Stacked Sparse Autoencoder and TreeBagger	KNN	SVM	KNN	CNN	CNN	CNN	CNN+RNN	CNN	SNN
ECG Sample Window	1 HB	1 HB	1 HB	3 and 11 HB	650 Samples	1 HB	651 Samples	651 Samples	5 sec	512 Samples	651 Samples	650 Samples
Leads	8 leads	12 leads	Lead II	Lead 7	12 leads	12 leads	Lead II	12 leads	12 leads	Lead I	3 VCG leads	8 leads
No. of Classes	5+HC	6+HC	11+HC	11	6	10+HC	1+HC	10+HC	6+HC	1+HC+Noisy+ Other	6+HC	11+HC
Implementation Platform	Software	Software	Software	Software	Software	Software	Software	Software	Software	Software	Software	ASIC
Sensitivity	99.80*	NA	99.95	99.76	97.9	98.67*	95.49	NA	98.14	92.4	NA	99.49
Specificity	99.96*	NA	99.87	99.96	98.78	98.71*	94.19	NA	99.4	97.7	NA	99.94
Accuracy	99.84	99.84	98.88	99.75	98.85	98.8	95.22	99.78	98.22	97.2	99.86	99.9
F1-Score	NA	99.7	NA	NA	NA	NA	NA	NA	NA	94.6	NA	99.31
Technology Node	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	180 nm
VDD	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	1.98 V
Operating Frequency	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	250 KHz
Area(mm^2)	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	1.69
Power (μW)	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	NA	268.9

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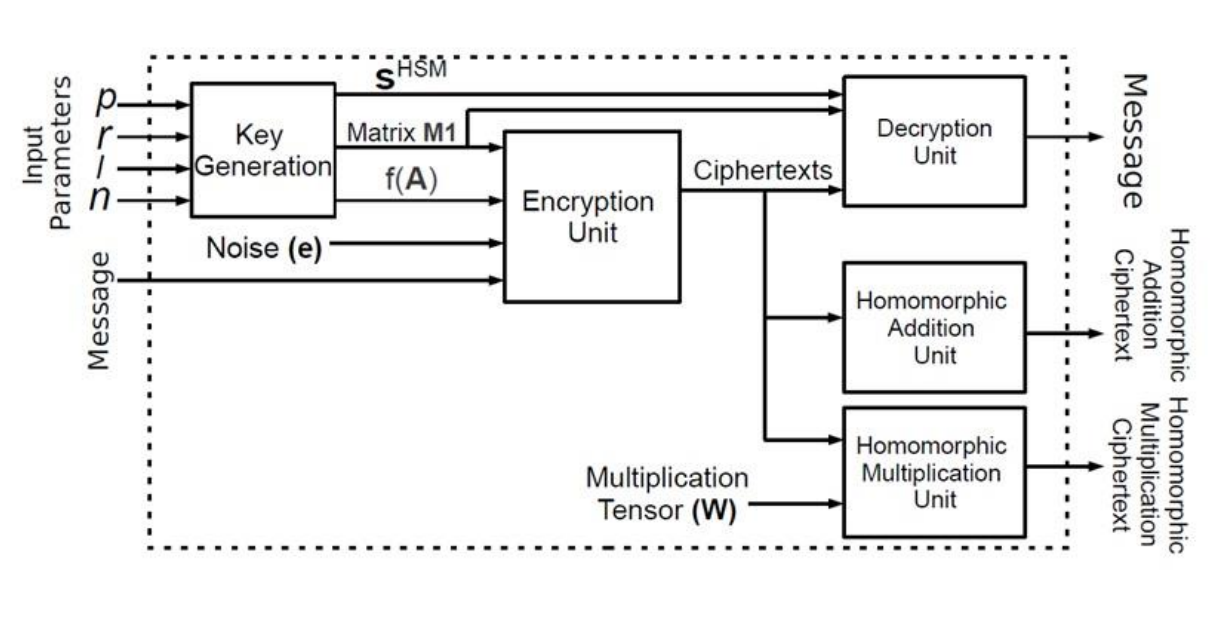
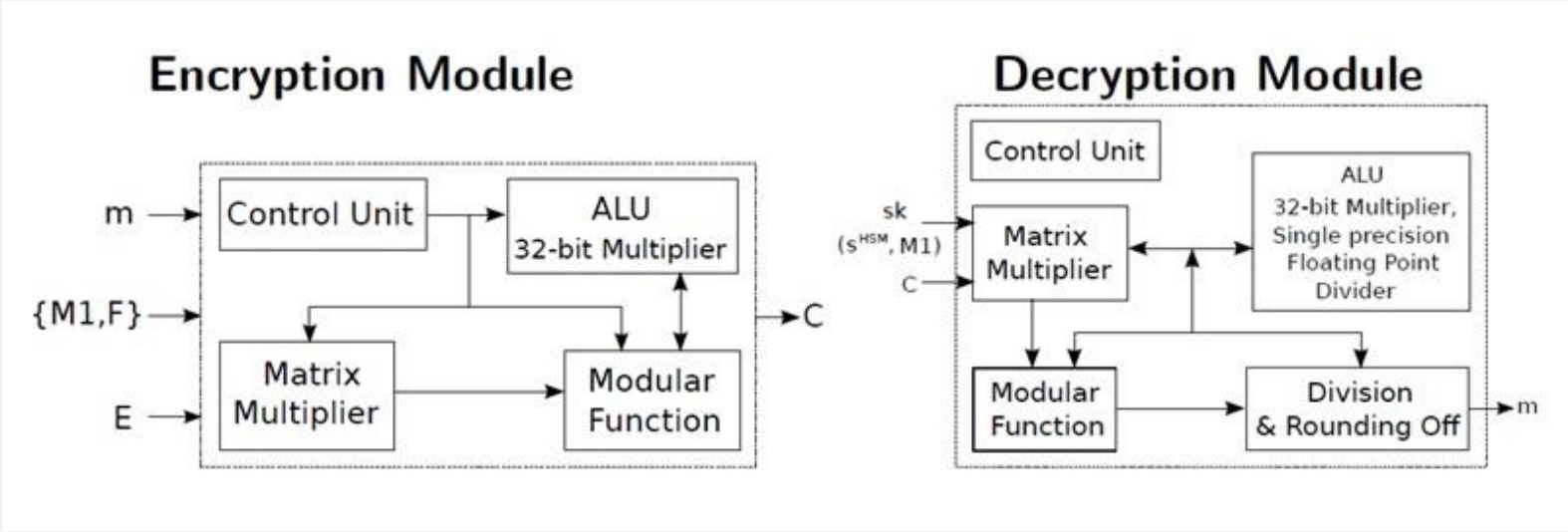


Basic block diagram of our LWE FHE (Jointly with Prof. Srinivasan Krishnaswamy)



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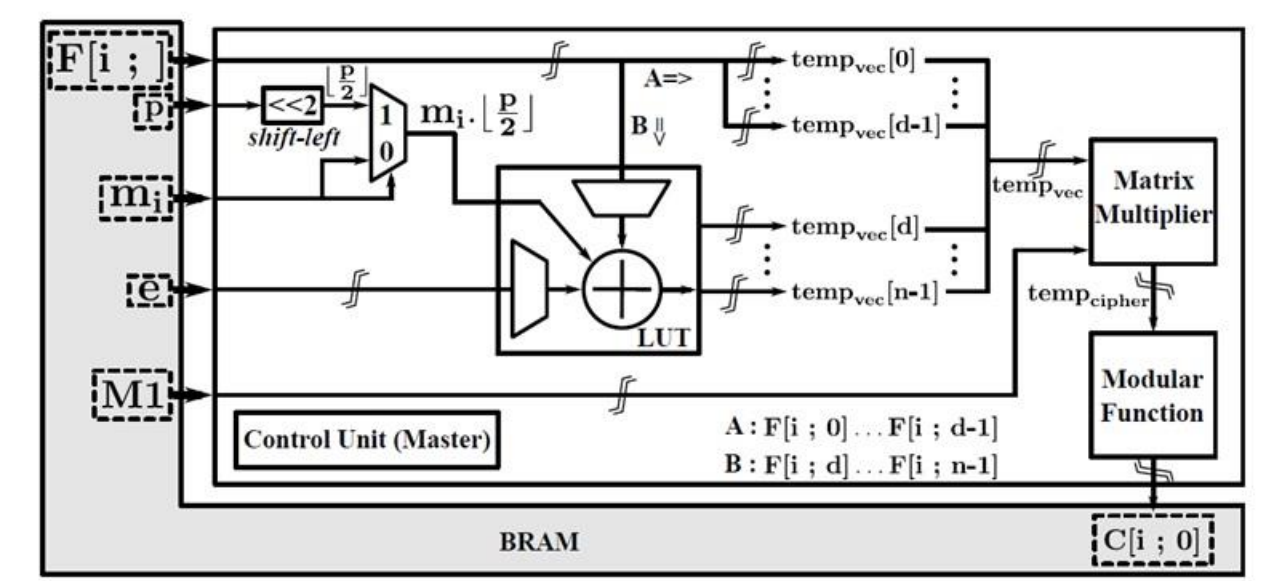
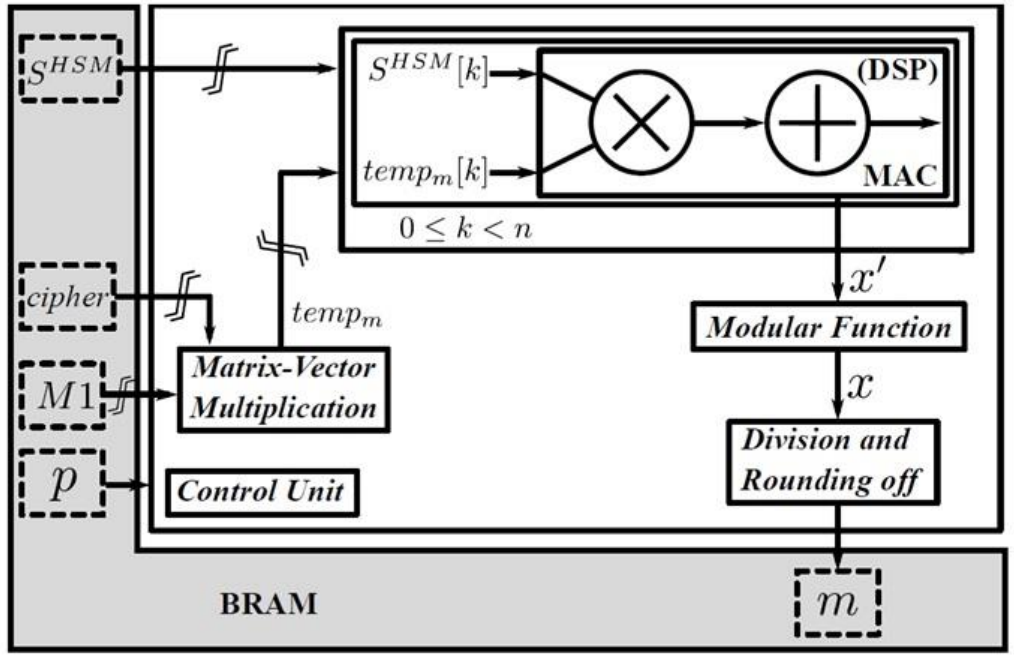


Hardware Architecture of LWE FHE Encryption Module



Hardware Architecture of LWE FHE Decryption Module

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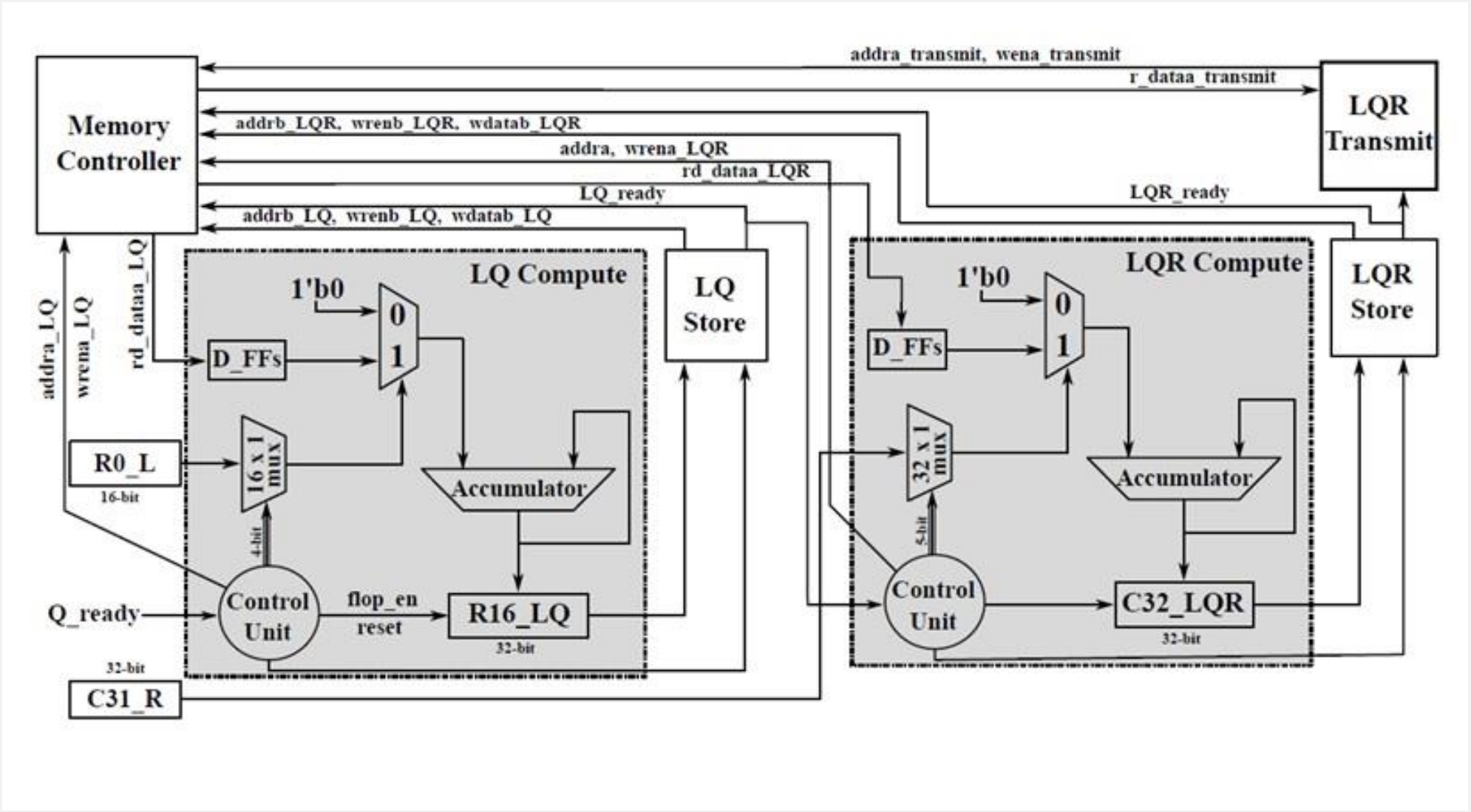

Lightweight LWE based FHE Decryption Module

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Work	Scheme	Platform	Operation	LUT/REG/DSP/BRAM	Utilization	Clock (MHz)	CC	Delay	(Mbps)*
Proposed Variant 1	RLWE PHE	Zedboard	Encryption	7622/7058/3/13.5	1.43 X	50	344	6.88μs	5.814
			Decryption	6940/7865/3/12.5			809	16.18μs	2.472
			Recryption	938/365/-/-			142	2.84μs	14.084
		Virtex-7	Encryption	7821/7159/3/14	1.47 X	200	330	1.65μs	24.242
			Decryption	7114/8085/3/15			876	4.38μs	9.132
			Recryption	980/396/-/-			144	0.72μs	55.556
Proposed Variant 2	Lightweight LWE PHE	Zedboard	Encryption	5489/5281/3/5	X	50	72	1.44μs	177.778
			Decryption	4621/5514/-/7			48	0.96μs	266.667
			Recryption	375/190/-/2			11	0.22μs	1163.636
		Virtex-7	Encryption	5519/5298/3/6	≈X	200	70	0.35μs	731.429
			Decryption	4762/5510/-/8			45	0.225μs	1137.778
			Recryption	379/192/-/3			10	0.055μs	4654.545
[24]	BGV RLWE Non-pipelined	Virtex-7 UltraScale	En/Decryption	~	~	150	~	14.54μs	237.69
			Recryption					0.85μs	4065.88
	BGV RLWE pipelined	Virtex-7 UltraScale	En/Decryption	527493/133813/165/23.5	52.71 X	150	~	6.84μs	505.26
			Recryption	381068/89849/120/16				0.85μs	4065.88
[25]	FV RLWE	Virtex-6	Recryption	72613/63086/250/84	6.33 X	100	~	50ms	804.78
[26]	GH FHE	TSMC 90-nm	Encryption	~	~	666	12M	18.1ms	~
			Decryption				10.7M	16.1ms	
			Recryption				2000M	3.1s	
[27]	Iterative FV	Virtex-7	Encryption	77K/~/952/325.5	3.64 X	200	~	1.4μs	2.72
			Decryption					1.24μs	3.08
			Recryption					0.96μs	3.97
	Four-Step FV	Virtex-7	Encryption	67K/~/599/129	3.15 X	200	~	1.8μs	2.12
			Decryption					1.8μs	2.12
			Recryption					1.4μs	2.73
[28]	GH-FHE	Virtex-7	En/Decryption	153771/68467/672/~	10.37 X	~	~	11ms	~

"~" and "–" denote "Data not specified" and "Resource not utilized", respectively; "*" (Degree of Polynomial × No. of bits) / Speed, where "Speed" is the time taken to produce an output after input is loaded in FPGA memory for computations.

Comparison With Lattice FHE Hardware Accelerators

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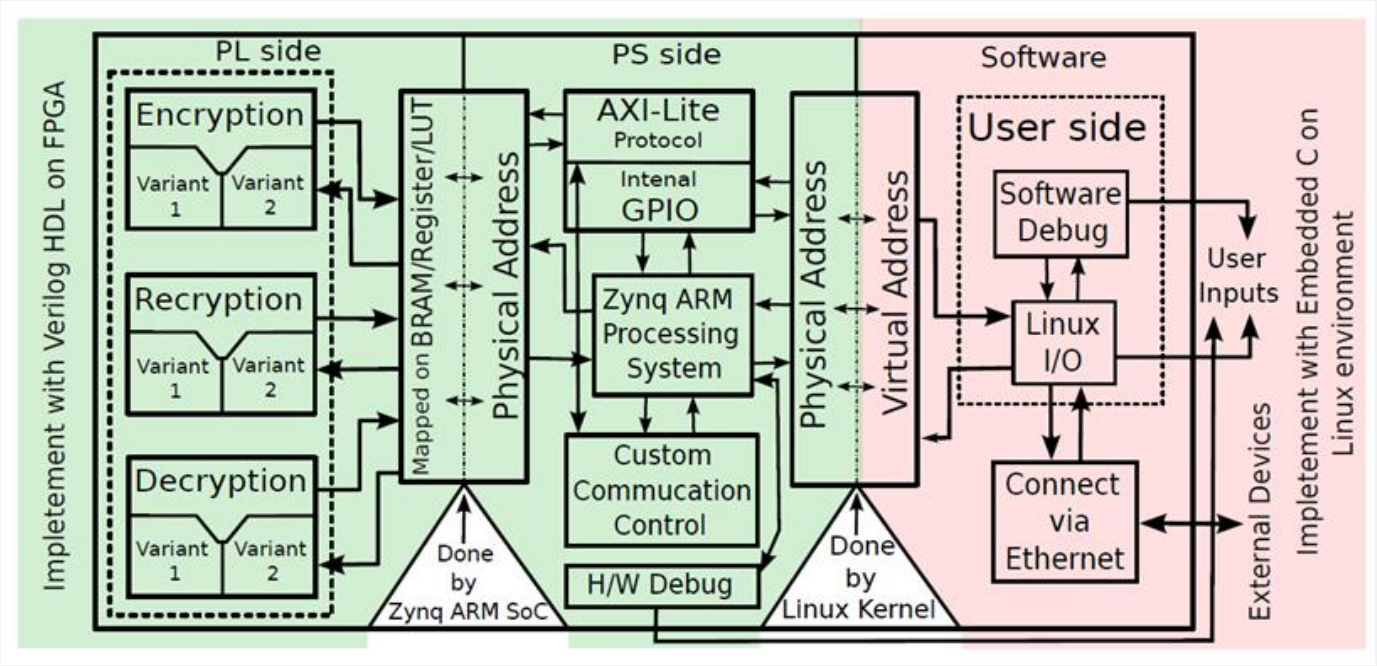

Hardware Accelerator and SoC Integration

Scheme (Software used)	Op.	Avg. Software Timings	Hardware Timings		Speed-up	
			ZedBoard (50MHz)	Virtex-7 (200MHz)	ZedBoard (50MHz)	Virtex-7 (200MHz)
RLWE (SageMath)	Encrypt	563.62 μs	6.88 μs	1.65 μs	81.92 $\times$	341.59 $\times$
	Decrypt	882.16 μs	16.18 μs	4.38 μs	54.52 $\times$	204.41 $\times$
	Recrypt	149.18 μs	2.84 μs	0.72 μs	52.53 $\times$	207.19 $\times$
Lightweight LWE (MATLAB)	Encrypt	535.00 μs	1.44 μs	0.35 μs	371.53 $\times$	1528.57 $\times$
	Decrypt	148.40 μs	0.96 μs	0.225 μs	154.58 $\times$	659.56 $\times$
	Recrypt	61.30 μs	0.22 μs	0.055 μs	278.63 $\times$	1114.55 $\times$

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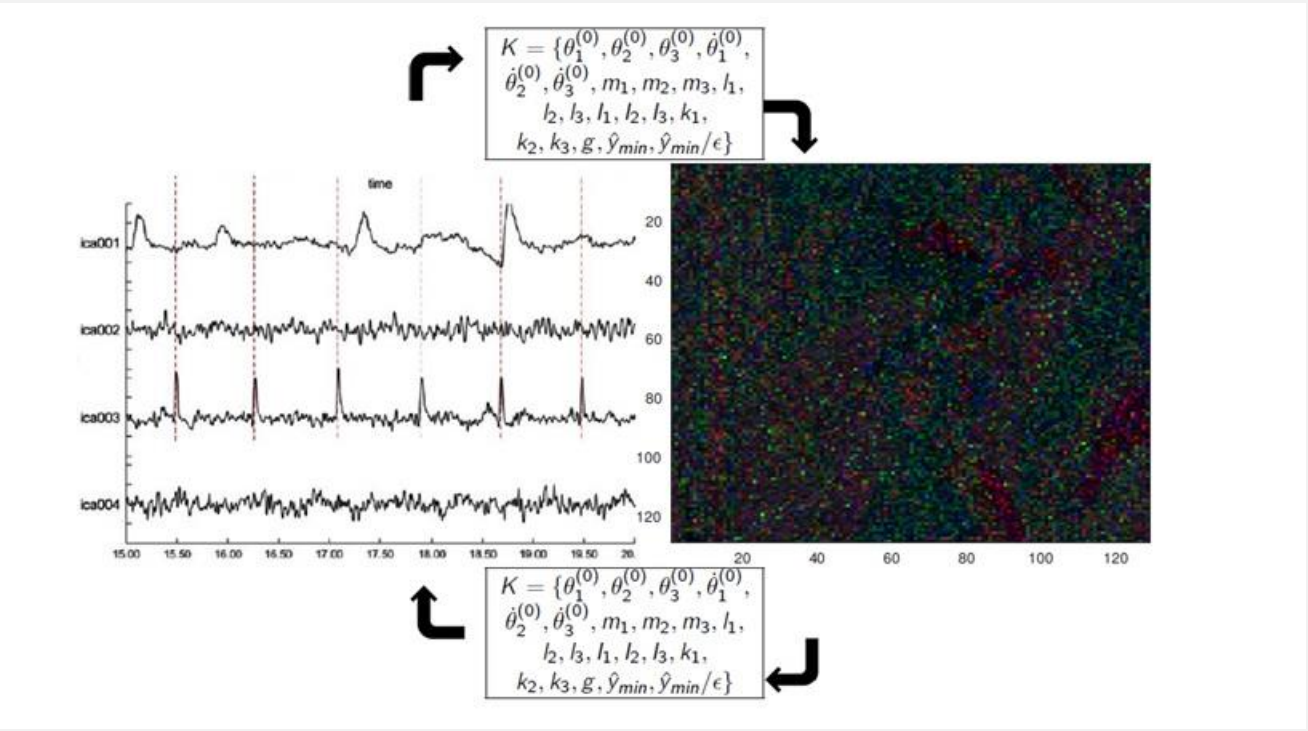
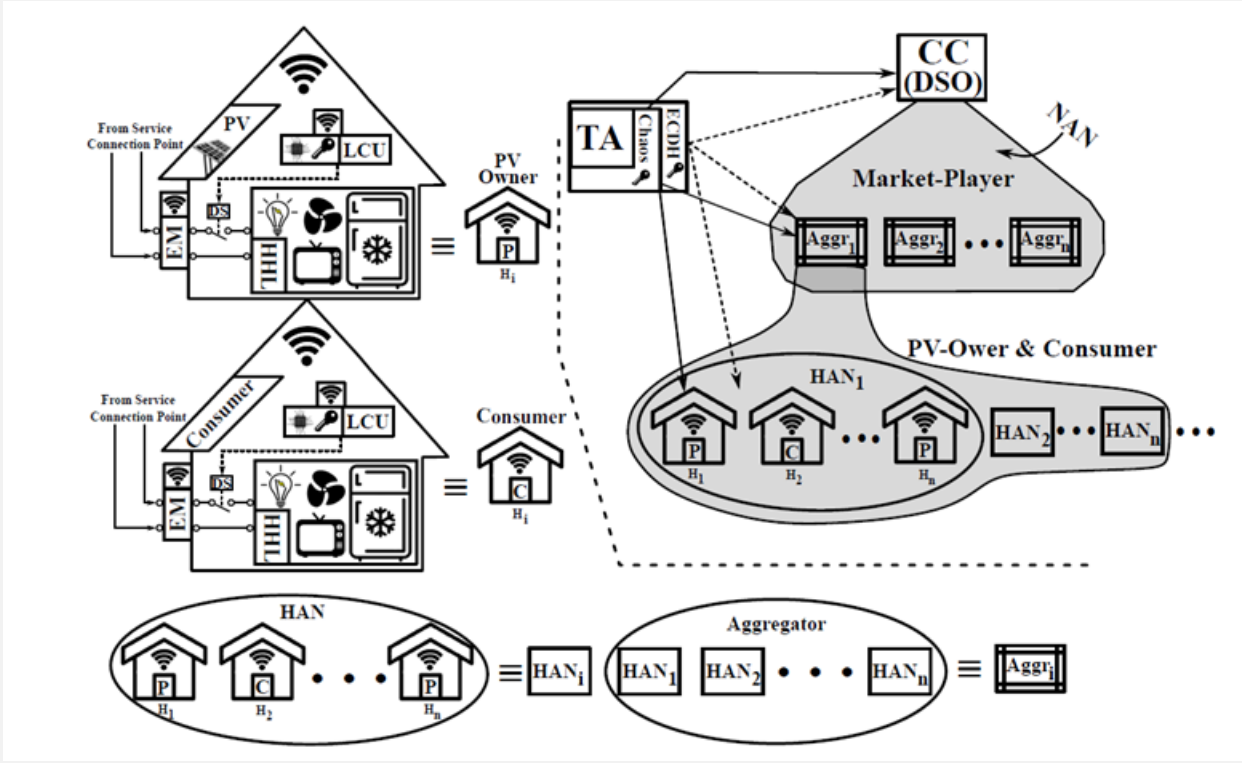


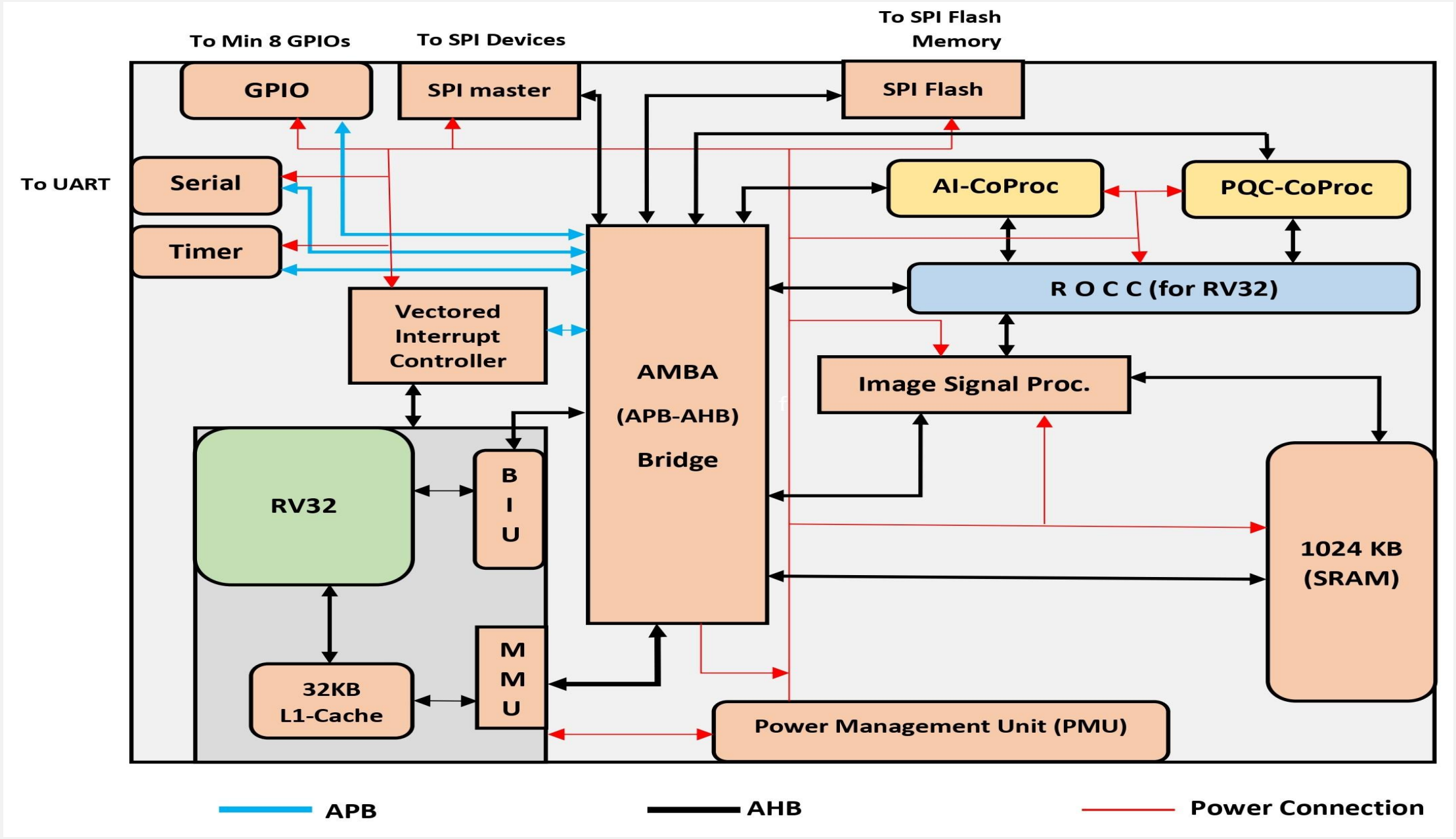
Biomedical data security



Secure Smart-grid Hierarchical Architecture

Indian Patent Filed

SECURE AI SOC INDIRA©/INDRA ©TOP LEVEL ARCHITECTURE



SECURE AI SOC IMPLEMENTATION PLAN

Approach 1

Designing our own RV-32 and using ROCC for integrating AI/ML co-processor as shown in top level architecture.

- Processor in development stage.
- Development time is more as we have to design, integrate, test and verify.

Approach 2

Using AJIT/SHAKTI/VEGA Processor and integrate AI/ML Processor using memory map method.

- Verified indigenous processor cores will be used.
- Development time is less that approach1 as we only need to integrate and verify.

Approach 3

Using ARM Cortex-M33 IP for integrating AI/ML co-processor.

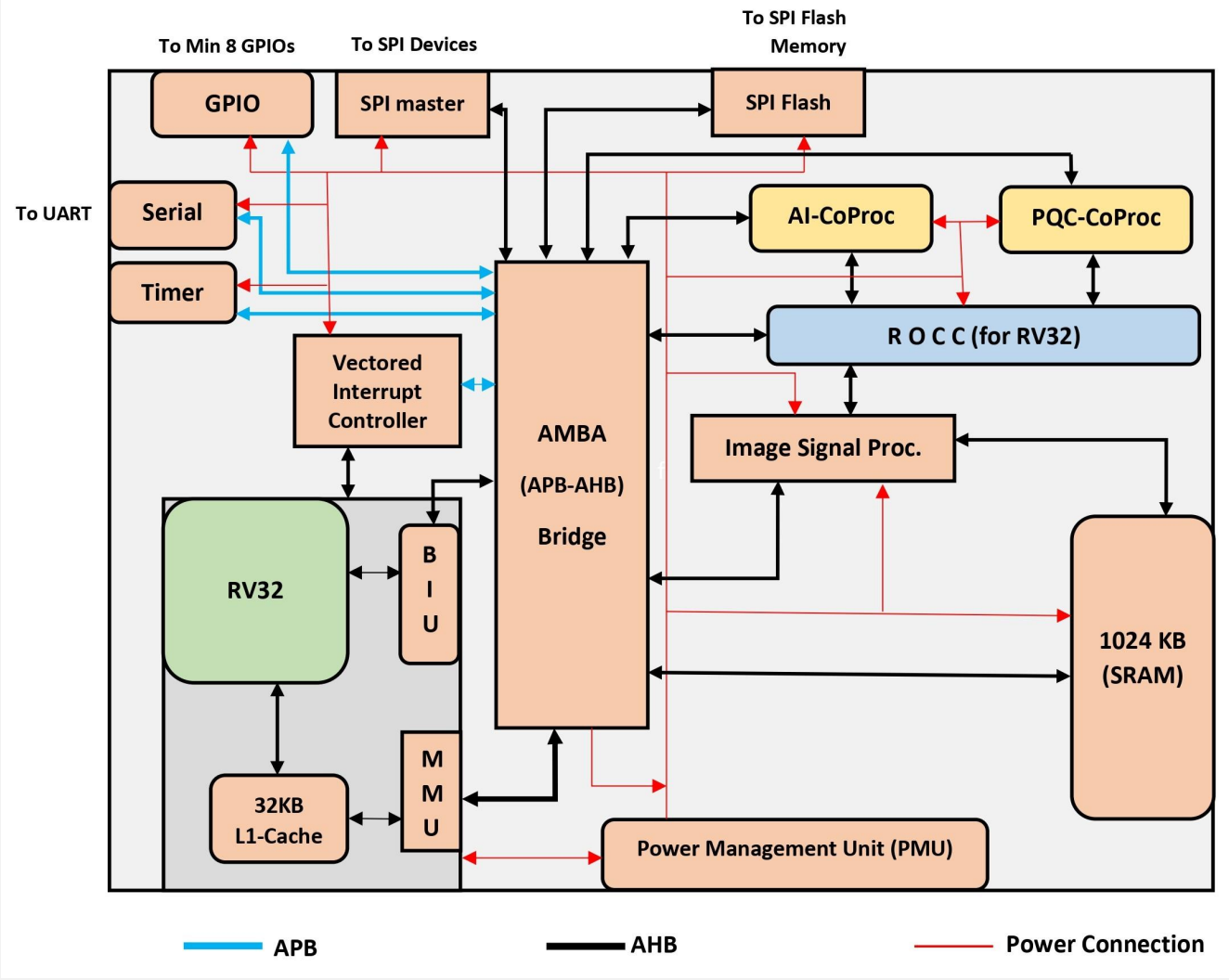
- Integrating AI/ML processor and testing will take time.
- Development time will be less as all verification flow and Backend flow is provided by ARM

RV-32 APPROACH

RV-32 will serve as main processor.

ROCC will be used as bridge for communication between main processor and AI/ML co-processor

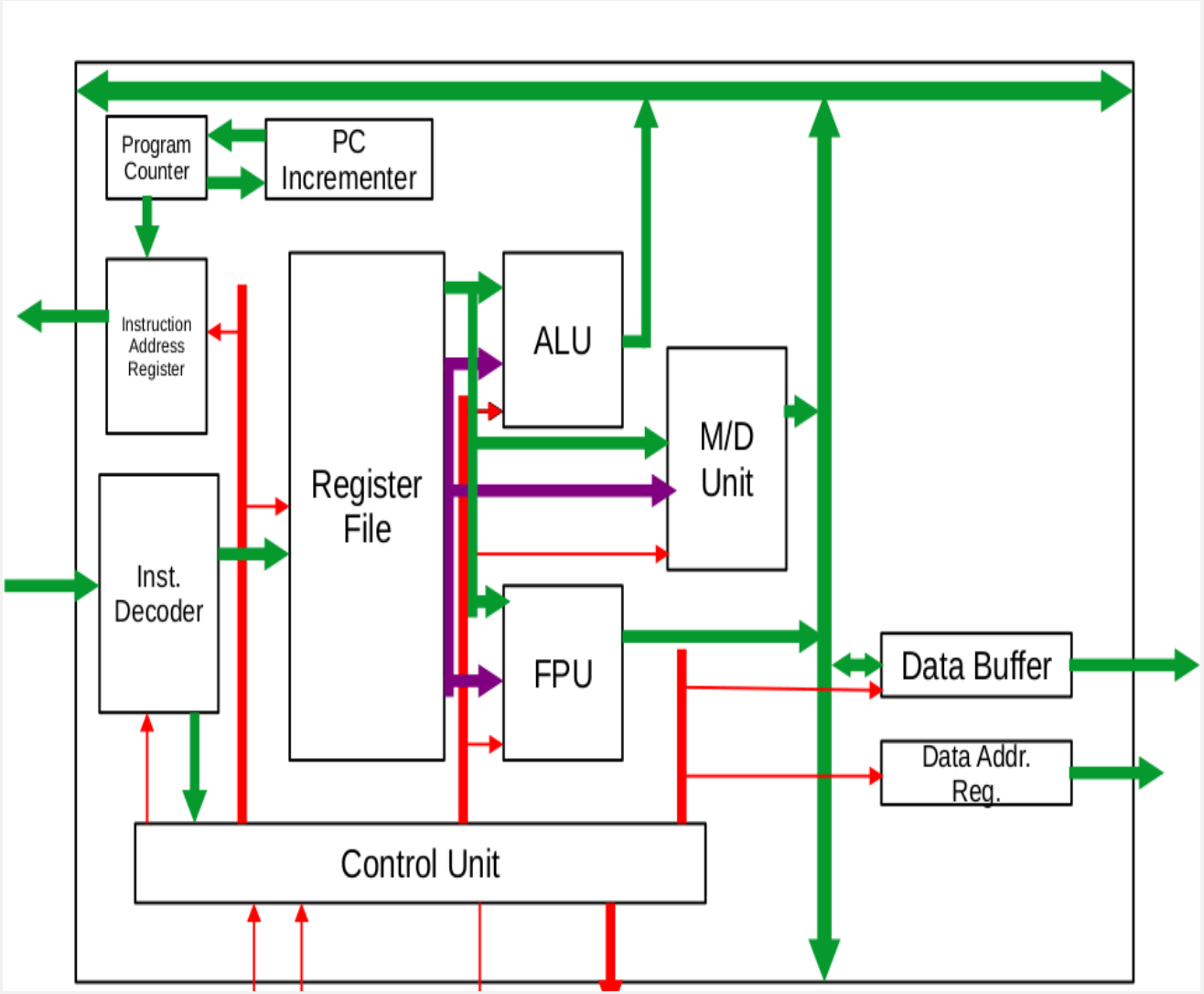
All the peripherals other than ROCC and RV32 , will be exported from AJIT or ARM.



Secure AI SoC Block Diagram

RV-32 TOP LEVEL ARCHITECTURE

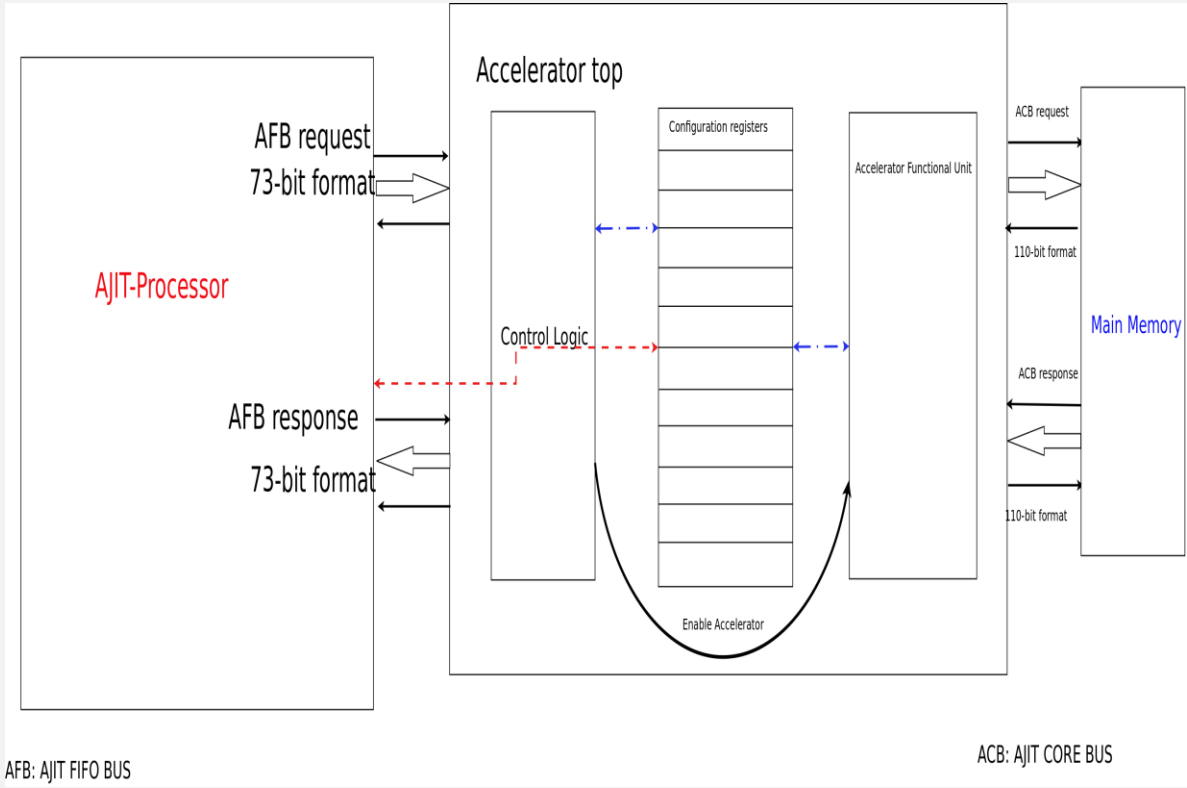
- Verification of only Integer done.
- Verification of M/D unit done.
- Integrated M/D extension.
- Verification of FPU is done.
- Integrated FPU extension.
- ROCC Design and Integration done



Block Diagram of the designed RISC-V

AJIT PROCESSOR INTEGRATION WITH COPROCESSOR MODULE AND COMMUNICATION THROUGH PC

- AJIT IP can be integrated with any accelerator of our choice as a memory mapped IO.
- The control and data inputs are provided from the processor through AFB interface.
- A suitable cortos2 c-program is used to access configuration registers.
- Constraints for setting up the ports of FPGA zynq zc706 are written.
- The bitstream is generated successfully and loaded to the FPGA.
- The ajit_debug_monitor_mt tool is used to execute the cortos2 c-code to write to and read from the interface registers.

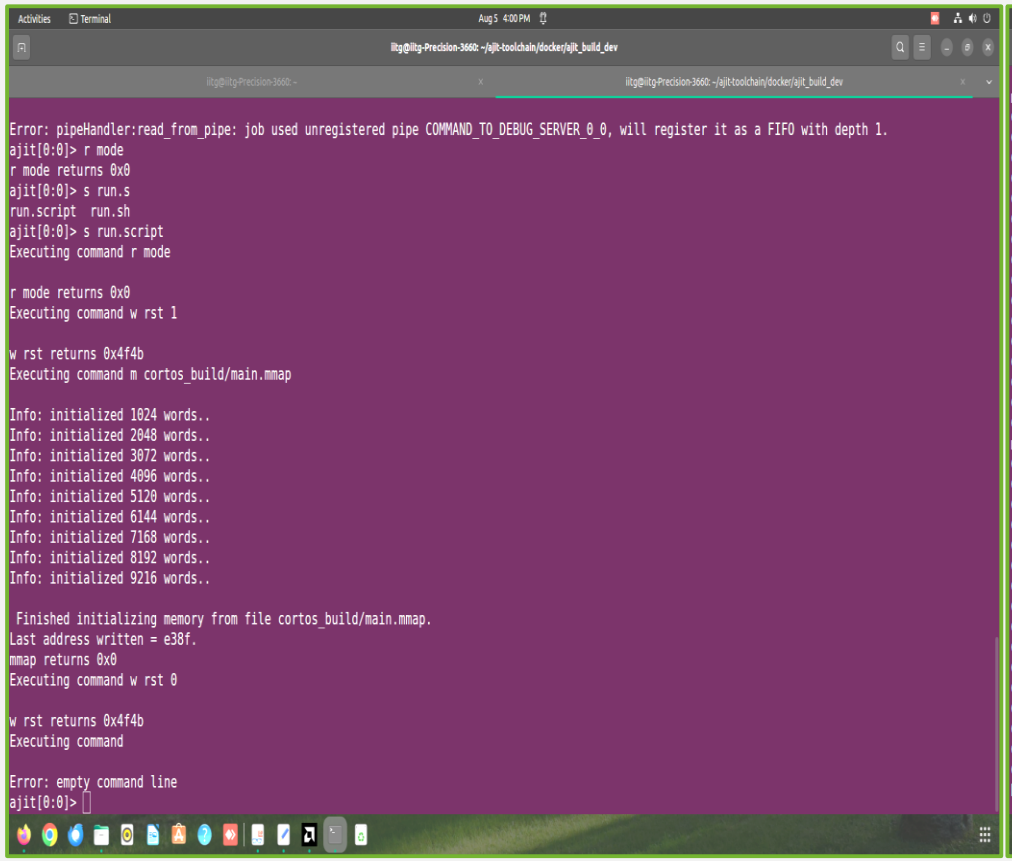


Architecture for accelerator integration with AJIT

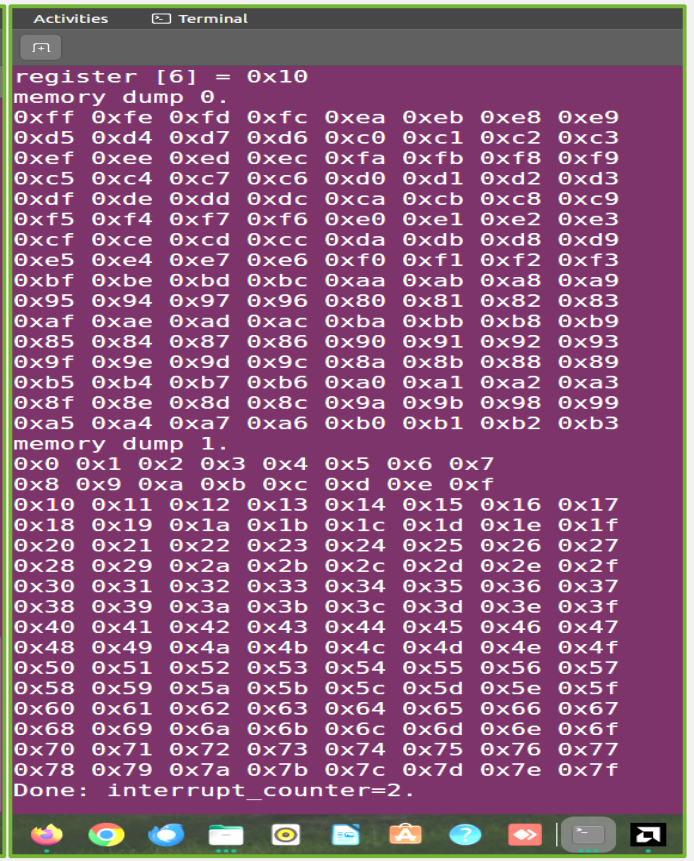
AJIT PROCESSOR FPGA IMPLEMENTATION AND COMMUNICATION THROUGH PC

- Configured constraints for zynq zc706 board
- Minicom setup for output monitoring

Znyq-zc706 FPGA board set up for AJIT IP implementation

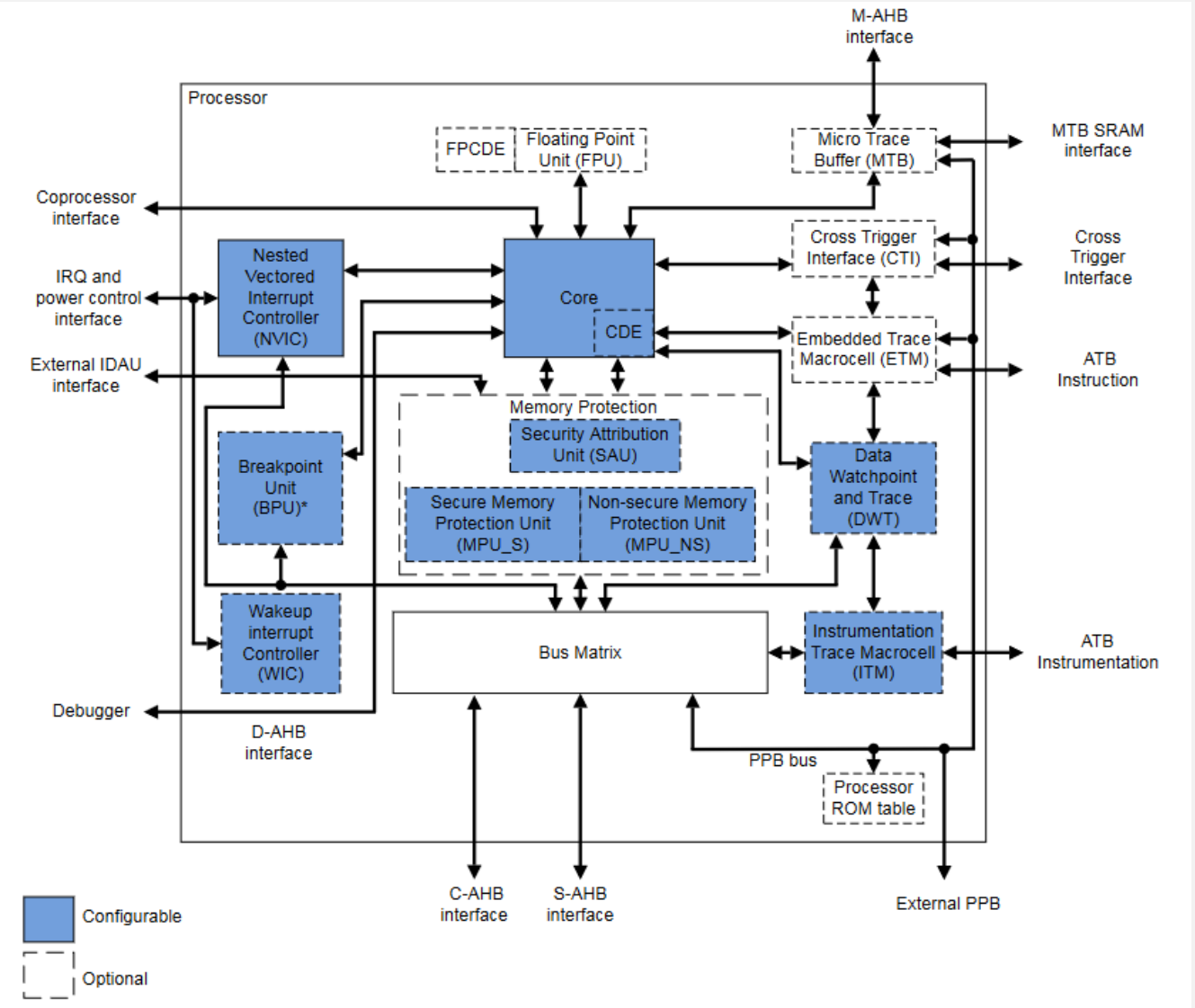


ajit_debug_monitor window - AJIT IP



Minicom output for accelerator program in AJIT IP

ARM CORTEX-M33 APPROACH



Block Diagram of ARM Cortex-M33

Replacing the example core Custom Datapath Extension (CDE) module and floating-point FPCDE module with our own designs and integrating them with the processor.

Need to configure the implementation using support of the Arm Custom Instructions (ACIs).

The architecture extension defines instruction classes that depend on the number of source or destination registers. For each class, an accumulation variant exists.

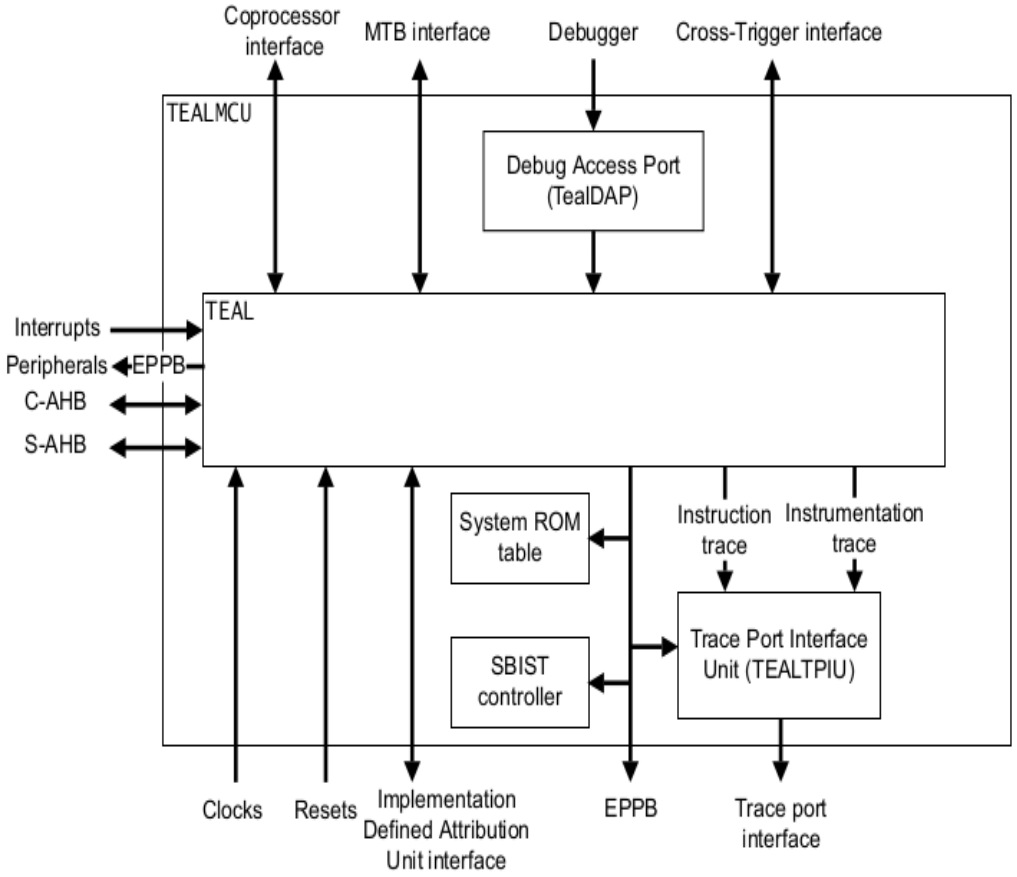
- CX1, CX2, CX3 : These three classes operate on the general-purpose register file, including the condition code flags APSR_nzcv.
- VCX1, VCX2, VCX3 : These three classes operate on the floating-point register file only

IP HIERARCHY & TOOLS REQUIREMENT

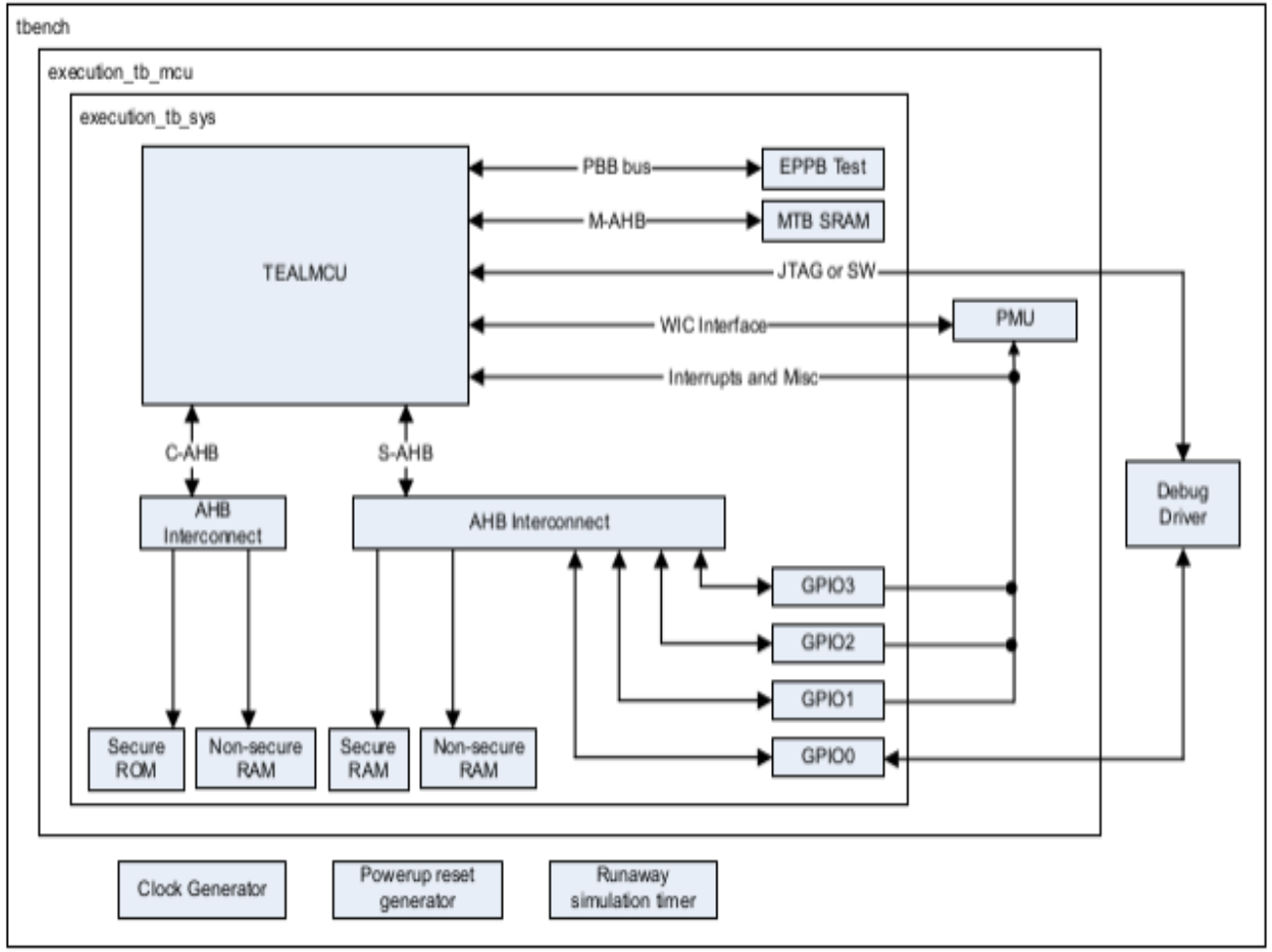
```
iitg@iitg-amolb:~/ARM_IPS/Cortex-M33 Processor_with_FPU_AT624/
.
├── Cortex_M33_AT623_and_Cortex_M33_with_FPU_AT624_Product_Err
├── Cortex_M33_AT623_and_Cortex_M33_with_FPU_AT624_Software_De
├── Cortex-M33_r1p0-00rel0_ReleaseNote.pdf
└── teal
    ├── documentation
    │   ├── arm_cortex_m33_iim_100323_0100_03_en.pdf
    │   ├── arm_cortex_m33_trm_100230_0100_03_en.pdf
    │   ├── arm_cortex_m33_trm_100230_0100_03_en_source.zip
    │   ├── arm_cortex_m33_ugrm_100234_0100_01_en.pdf
    │   ├── arm_cortex_m33_ugrm_100234_0100_01_en_source.zip
    │   ├── Cortex-M33_Cadence_iRM_User_Guide.pdf
    │   └── Cortex-M33_Synopsys_iRM_User_Guide.pdf
    ├── implementation_tsmc_cln40lp
    │   ├── crf_v1.51.s018
    │   │   ├── 15.13-s048_1
    │   │   ├── flow
    │   │   ├── FoundationFlow -> 15.13-s048_1
    │   │   ├── Readme
    │   │   └── scripts
    │   ├── libraries
    │   │   └── README.txt
    │   ├── TEAL_typical_cadence_pg
    │   │   ├── constraints
    │   │   ├── data
    │   │   ├── logs
    │   │   ├── Makefile
    │   │   ├── reports
    │   │   ├── scripts
    │   │   └── work
    │   └── TEAL_typical_synopsys
    │       ├── constraints
    │       ├── data
    │       ├── logs
    │       ├── Makefile
    │       ├── reports
    │       ├── scripts
    │       └── work
    ├── logical
    │   ├── models
    │   │   ├── cells
    │   │   └── modules
    │   ├── shared
    │   │   ├── ipxact
    │   │   ├── tools
    │   │   └── verilog
    │   ├── teal
    │   │   ├── dsm
    │   │   ├── ipxact
    │   │   ├── power_intent
    │   │   └── verilog
    │   ├── tealbpu
    │   │   └── verilog
    │   ├── tealcore
    │   │   └── verilog
    │   ├── tealcti
    │   │   └── verilog
    │   ├── tealdap
    │   │   └── verilog
    │   ├── tealdwt
    │   │   └── verilog
    │   ├── tealfpu
    │   │   └── verilog
    │   ├── tealitm
    │   │   └── verilog
    │   ├── tealmcu
    │   │   └── verilog
    │   ├── tealmpu
    │   │   └── verilog
    │   ├── tealmtx
    │   │   └── verilog
    │   ├── tealnvic
    │   │   └── verilog
    │   ├── tealpcr
    │   │   └── verilog
    │   ├── tealsbist
    │   │   └── verilog
    │   ├── tealsbistc
    │   │   └── verilog
    │   ├── tealtpiu
    │   │   └── verilog
    │   └── testbench
    │       ├── execution_tb
    │       ├── integration_cssoc
    │       └── shared
    └── simulation_models
        ├── TEAL_DSM_noFLEXLM_32bit
        │   └── TEAL_DSM.sh
        └── TEAL_DSM_noFLEXLM_64bit
            └── TEAL_DSM.sh
```

Tool name	Version
Mentor Questasim	10.6
Synopsys VCS	2016.06
Cadence IUS	15.20.008
Perl	5.12.3 (only required for the Execution testbench)
Arm Compiler	6.7.21 (only required for the Execution testbench)
GNU Tools for Arm Embedded Processors	6.3.1 (release 6-2017q1) (only required for the Execution testbench)
Cadence Genus	15.21.000
Cadence Innovus	16.21.000
Cadence Conformal	15.10.140
Cadence QRC extraction	15.23.000
Cadence Tempus STA	15.23.000
Cadence Encounter Test	15.11.000
Synopsys Design compiler	2015.06-SP5-2
Synopsys Formality	2015.06-SP5
Synopsys IC Compiler	2015.06-SP5-2
Synopsys StarRC	2015.12-SP3
Synopsys Primetime	2015.12-SP3
Synopsys Tetramax	2015.06-SP2
GCC	4.8.4 (only required for DSM)
Verilator	3.853 (only required for DSM)
Python	3.2 (only required for DSM)

ARM-CORTEX M33 VERIFICATION PROGRESS



TEALMCU Block Diagram



ARM Testbench architecture

TEST PLAN

TEST NO.	TEST CATEGORIE NAME	TESTCASE STATUS	COMMENT
1	hello_world	Pass	The processor reads the CPUID register and writes to the GPIO registers to print a simple message. This must be the first test run. You can run this test without compiling it, as both the source code and binary executable versions are supplied.
2	config_check	Pass	This test verifies that the processor configuration matches the expected configuration values set in the EXECTB_Config.h file. This must be the second test run.
3	coprocessor	Test Skip	There is not connected any coprocessor, This test demonstrates the operation of the example coprocessor. Note: This test is run only if CPIF is 1 and CDEMAPPEDONCP0 is 0. Otherwise, it is skipped.
4	example_cde	Pass	This test is an example to help understand how the CDE module works. It illustrates the internal functionality of the CDE module example delivered in the execution testbench.
5	example_fpcde	Pass	This test is an example to help understand how the FPCDE module works. It illustrates the internal functionality of the FPCDE module example delivered in the execution testbench. You cannot use this example test as it is for your customized module, however you can create your own test based on this example test.
6	check_cde_if	Pass	This test is an example to help understand how the FPCDE module works. It illustrates the internal functionality of the FPCDE module example delivered in the execution testbench.
7	check_fpcde_if	Pass	This test is an example that puts constraints on the FPCDE module interface to stress it. You cannot use this example test as it is for your customized module, however you can create your own test based on this example Test.
8	debug	Pass	The test checks the pins LOCKUP, EDBGRQ, HALTED, DBGRESTART, and DBGRESTARTED.
9	dhrystone	Pass	This test runs the Dhrystone benchmarking program. The default number of iterations is five. You can change the number of iterations by editing the ITERATIONS value in the Makefile. You can run this test without compiling it.

TEST PLAN (CONTD.)

TEST NO.	TEST CATEGORIE NAME	TESTCASE STATUS	COMMENT
10	eppb	Pass	This test demonstrates access to the small memory on the EPPB bus.
11	sleep	Pass	This test exercises the sleep modes of the processor, and the SLEEPING and SLEEPDEEP signals. The test uses an interrupt to wake the processor, and if the processor includes debug,
12	saxpy_scalar	Pass	This test is used to measure maximum power with the floating-point unit. You can run this test without compiling it, as both the source code and binary executable versions are supplied. To use the pre-compiled binary executable, copy it from the pre_compiled directory to the tests directory before use. The pre-compiled code
13	wfi	Pass	This test measures minimum power when the processor is awaiting an interrupt. You can run this test without compiling it, as both the source code and binary executable versions are supplied.
14	Maxpwr_cpu	Pass	This tests the power consumption of the processor at sustained maximum power running integer operations. You directory before use. The pre-compiled code measures power in the default configuration with the MPU, SAU and DWT enabled. If any other configuration of the MPU, SAU, DWT, ETM and MTB is present in your design,
15	etm_trace	pending	
16	exclusive	pending	
17	idau	pending	
18	interrupt	pending	
19	itm_trace	pending	
20	mtb_trace	pending	
21	non_secure	pending	
22	reset	pending	
23	romtable	pending	

ARM CORTEX-M33 IMPLEMENTATION PROGRESS

Currently we are working on ARM provided flow to test the IP implementation.

Established the required hierarchy by adding TSMC 40nm tech. node data (IMEC Belgium is supporting it)

Used CapTable in absence of foundry specific qrcTech file.

Fixing bugs in flow (e.g. commands/files Paths/dB saves)

Till now following stages completed

- Setup, synthesis, dft_insert, PnR, LEC

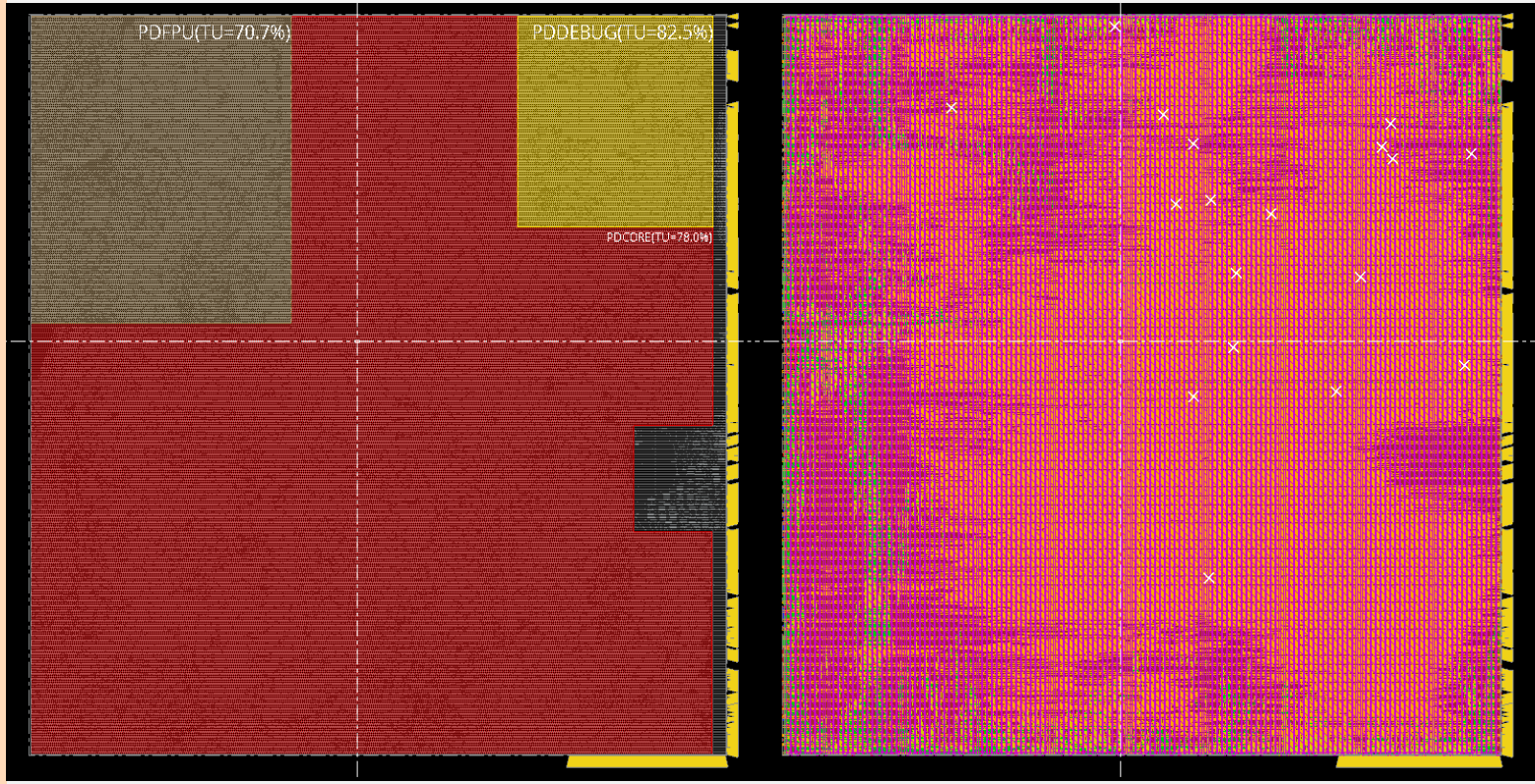
Currently working on Physical verification and will start timing signoff after receiving foundry specific qrcTech file.

Screenshots included in next slide

File Edit Tools Syntax Buffers Window Help

```
================================================================================
                          Verification Report
--------------------------------------------------------------------------------
Category                                                                  Count
--------------------------------------------------------------------------------
1. Non-standard modeling options used:                                        0
     Tri-stated output:                                   checked
     Revised X signals set to E:                          yes
     Floating signals tied to Z:                          yes
     Command "add clock" for clock-gating:                not used
--------------------------------------------------------------------------------
2. Incomplete verification:                                                   1
     All primary outputs are mapped:                      yes
     Not-mapped DFF/DLAT is detected:                     no
     All mapped points are added as compare points:       yes
     All compared points are compared:                    yes
     User added black box:                                no
     Black box mapped with different module name:         no
     Empty module is not black boxed:                     no
     Command "add ignore outputs" used:                   yes *
     Always false constraints detected:                   no
--------------------------------------------------------------------------------
3. User modification to design:                                               0
     Change gate type:                                    no
     Change wire:                                         no
     Primary input added by user:                         no
--------------------------------------------------------------------------------
4. Conformal Constraint Designer clock domain crossing checks recommended:    1
     Multiple clocks in the design:                       yes *
--------------------------------------------------------------------------------
5. Design ambiguity:                                                          0
     Duplicate module definition:                         no
     Black box due to undefined cells:                    no
     Golden design has abnormal ratio of unreachable gates:    no
     Ratio of golden unreachable gates:                   1%
     Revised design has abnormal ratio of unreachable gates:   no
     Ratio of revised unreachable gates:                  1%
--------------------------------------------------------------------------------
6. Compare Results:                                                        PASS
     Number of EQ compare points:                         9081
     Number of NON-EQ compare points:                     0
     Number of Aborted compare points:                    0
     Number of Uncompared compare points :                0
================================================================================
```

LEC mapped2synth report



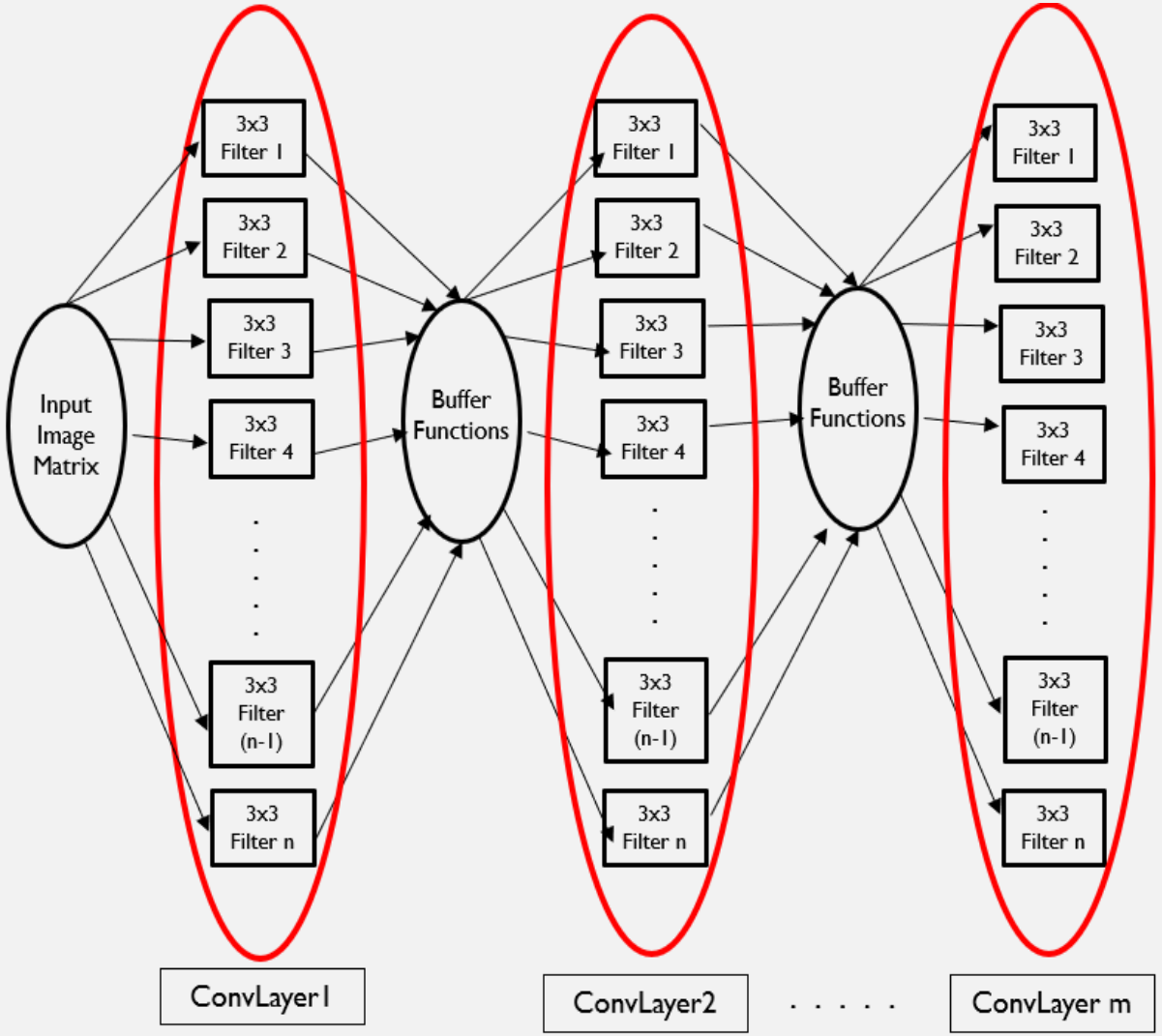
Power domain View

Routing Complete view

- X-dimension= 1124200 um and Y-dimension= 1124200 um
- Total place area is 255249.238 sq.um with 75.95% pre-place utilization/density

AI/ML CO-PROCESSOR IMPLEMENTATION PLAN

- Identify commonly used operations for AI/ML computations i.e. convolution, vector dot product, matrix addition. (All 32-bit FP operations)
- Convolution operation :
  - Designing for 640x480 matrix which contains 32-bit pixel information (RGB) having filter/Kernel Matrix of 1x1, 3x3, 5x5, 7x7.
  - This is done in 8 layers with different filter matrix containing 8 special feature for at least 3 stages.
  - Buffer Function can be any commonly used in CNN
    - ReLU (Exponential Linear Unit) activation function
    - Sigmoid
    - Tanh
    - ELU (Exponential Linear Unit) activation function



Convolution Engine Approach

CONVOLUTION ENGINE DESIGN

The Approach

Designing for 640x480 matrix which contains 32-bit pixel information (RGBA) having filter/Kernel Matrix of 1x1, 3x3, 5x5, 7x7.

- This will be done in 8 different filter matrix containing 8 special feature for at least 3 stages.

Work Done

- The R,G,B channel data store in memory(B-RAM) as a R-channel mem,G-channel mem,B-channel mem. concurrently to the Convolutions get output as result_R,result_G and result_B.
- Final convolution output is summation of result_R,result_G and result_B.
- We verified the code functionality(output values) with python code.

1x1	2X2	3X3	4	5
6X4	7X5	8X6	9	10
11X7	12X8	13X9	14	15
16	17	18	19	20
21	22	23	24	25

5X5 Matrix

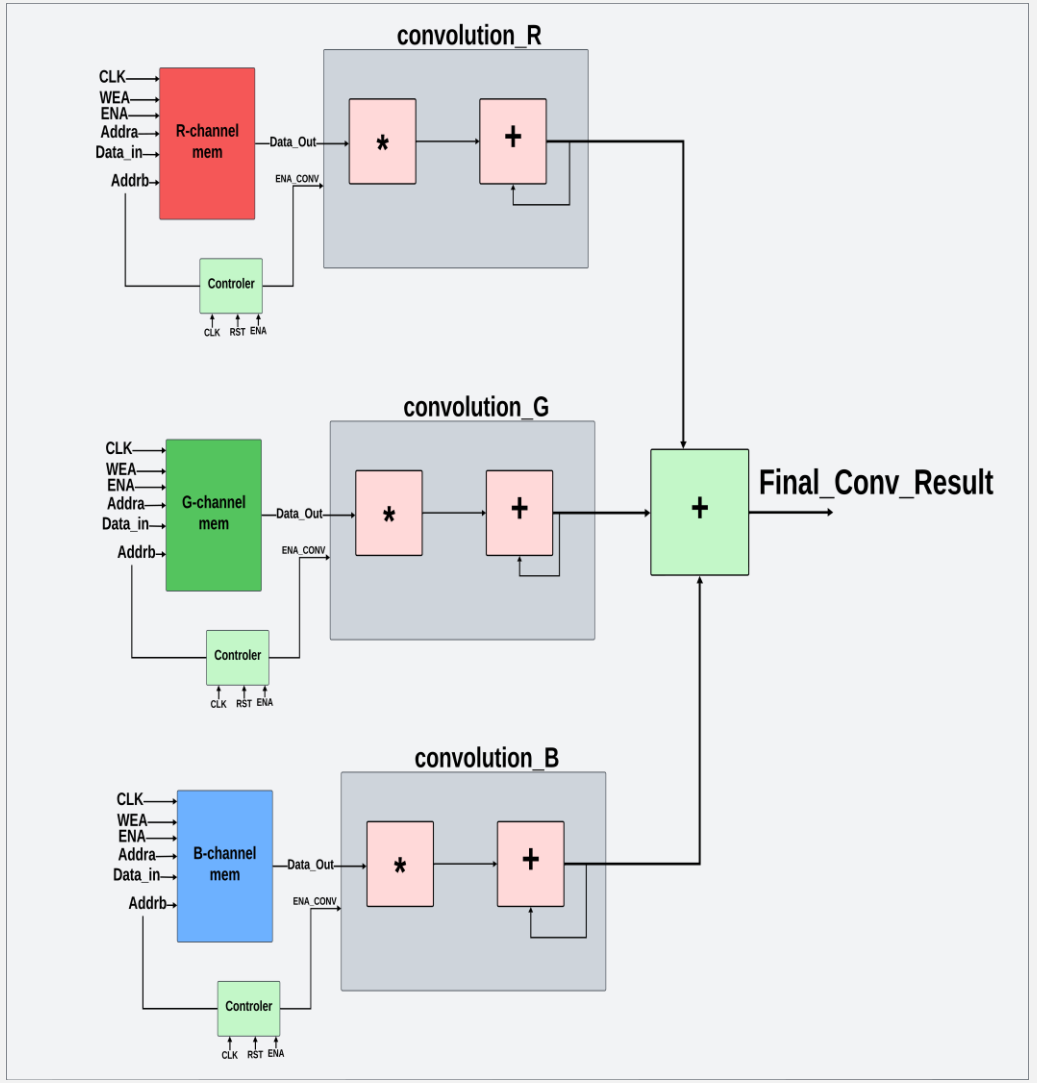
1	2	3
4	5	6
7	8	9

3X3 Filter

411.0	456.0	501.0
636.0	681.0	726.0
861.0	906.0	951.0

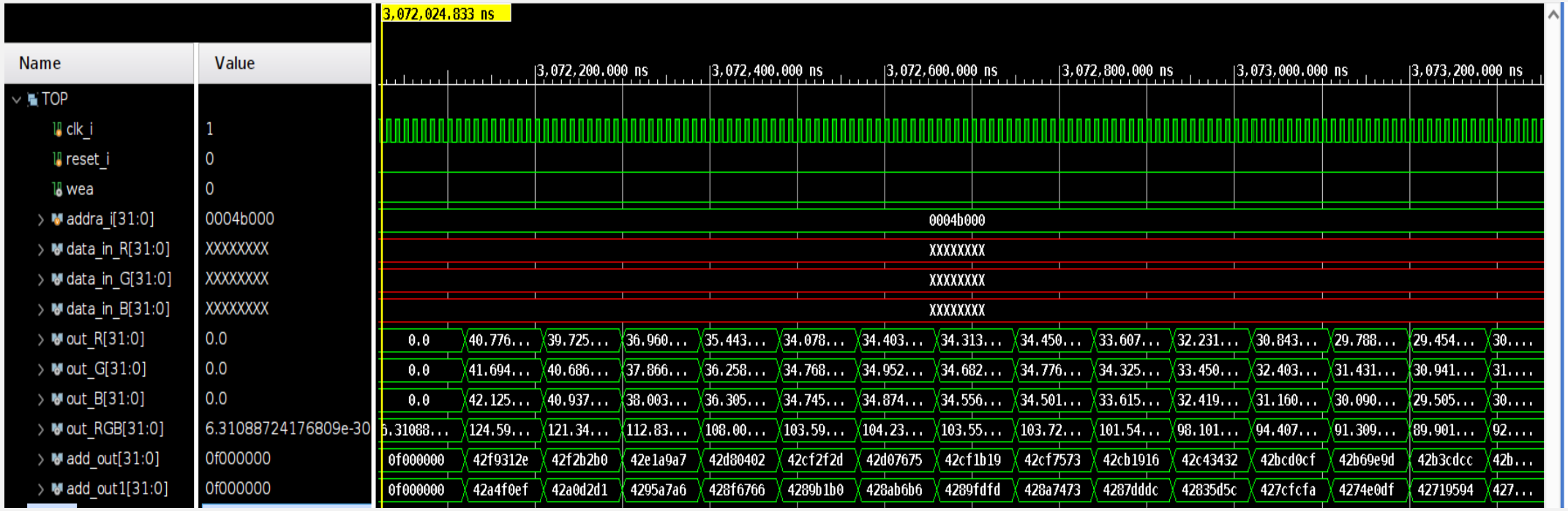
Result

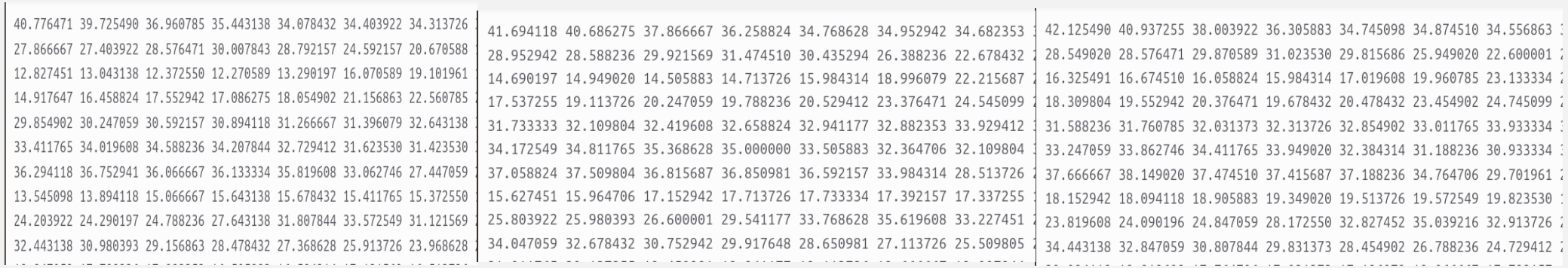
Convolution Operation



Convolution Operation Block Diagram

CONVOLUTION RESULT WITH(R,G,B)





R-channel output G-channel output B-channel output

Convolution Operation Implementation

NEUROMORPHIC COMPUTING

The human brain can correctly identify images seen for as little as 13 milliseconds, Whereas training a CNN with 5-layer network using a data set of 1000 observations takes almost 5 minutes for one iteration.

Properties	Computer	Human Brain
Basic Unit	~10 Billion Transistors	~100 Bilion Neurons ~100 Trillion Synapse
Processing Mode	Serial & Parallel	Massively Parallel
Power Consumption	~100 Watts	~20 Watts
Input Output for each unit	1-3	~1000
Signalling Mode	Digital	Analog

Computer Vs Brain

NEUROMORPHIC COMPUTING

AUTONOMOUS DRONE

CPU/GPU Controller
Power: 50mW

Pre-trained to fly
between known gates

COCKATIEL PARROT

Brain
Power: 50mW

Navigates and learns unknown environments at 35km/h

Can learn to speak English words

Can learn to manipulate cups for drinking

Source: A. Loquercio, E. Kaufmann, R. Ranftl, A. Dosovitskiy, V. Koltun and D. Scaramuzza, "Deep Drone Racing: From Simulation to Reality With Domain Randomization," in *IEEE Transactions on Robotics*, vol. 36, no. 1, pp. 1-14, Feb. 2020, doi: 10.1109/TRO.2019.2942989.

NEUROMORPHIC COMPUTING

CPU
Multicore
Serial Computation

Multiple core's integrated with on-chip memories

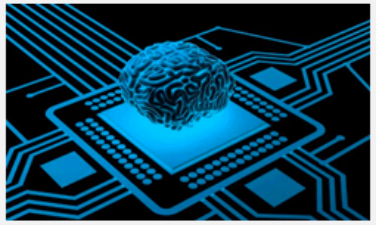
GPU
Parallel
Computation

Multicore parallel functionality

CPU + GPU for hand held devices and other applications

- Energy hungry data transfer
- Limited memory bandwidth

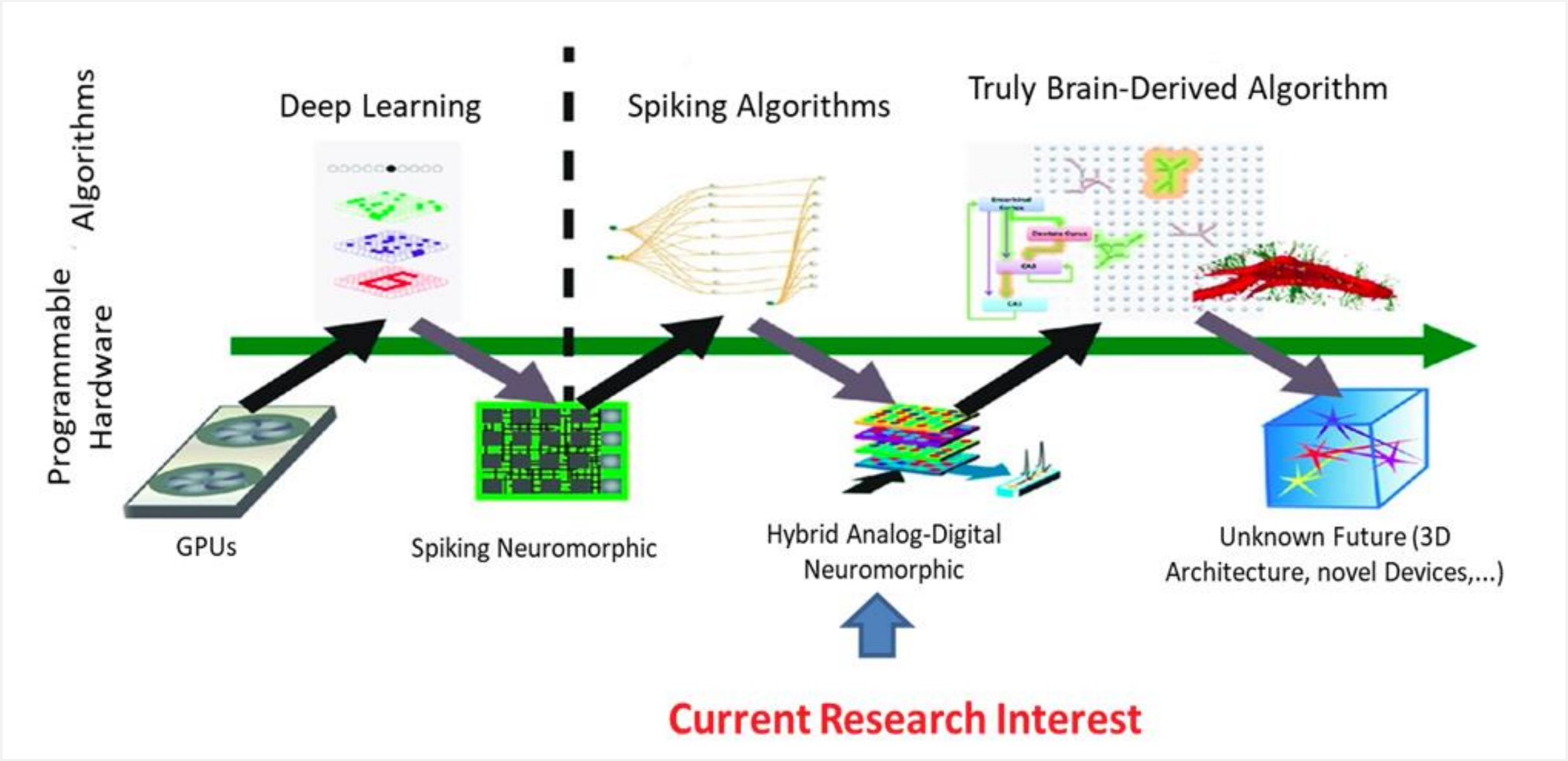
Memory Bottleneck is a problem that is inherent to Von Neumann Architecture.



Neuromorphic Computing

Computing system timeline

NEUROMORPHIC COMPUTING

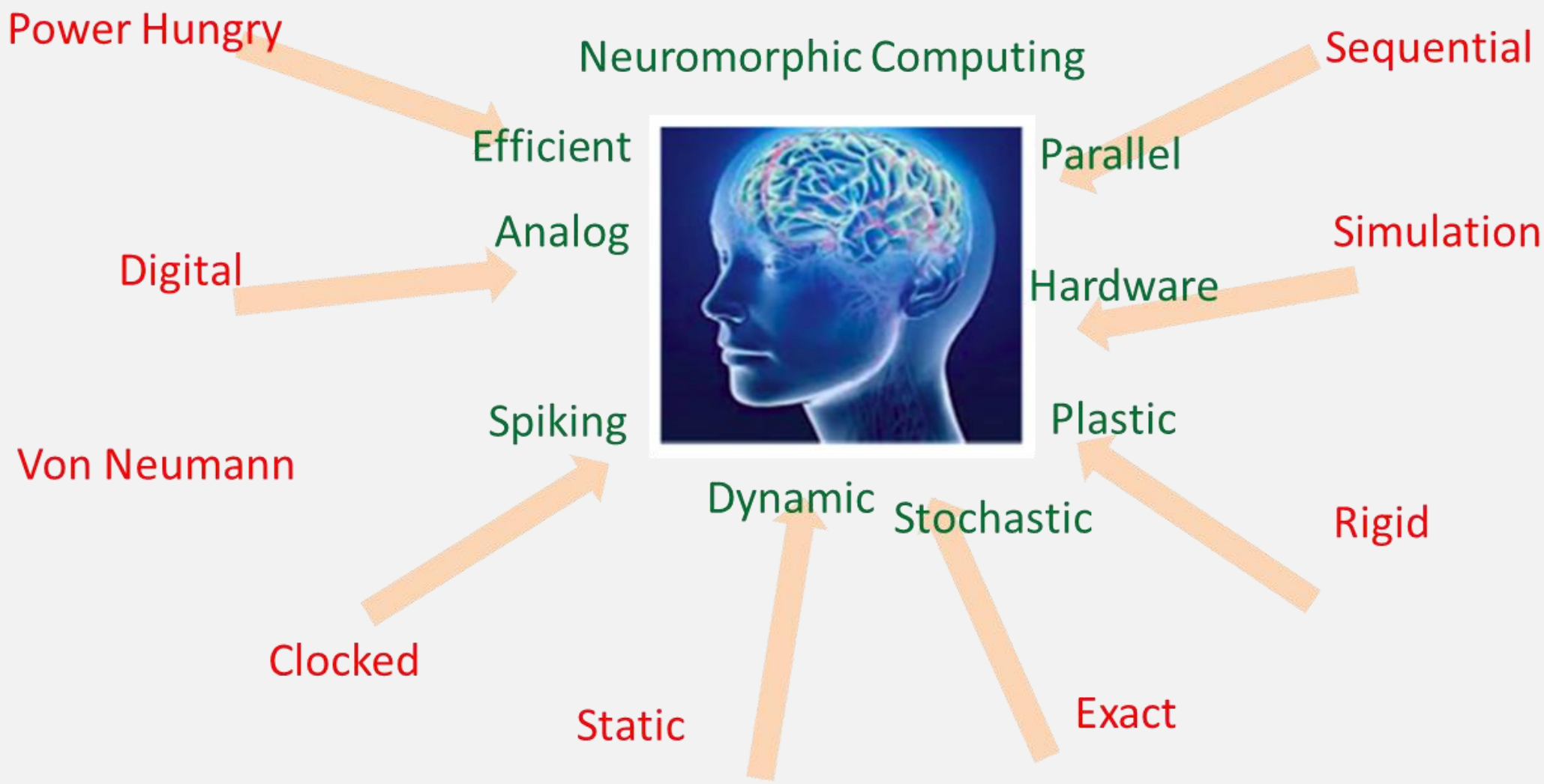


NEUROMORPHIC COMPUTING

Processor	Developer	Configuration	Power Consumption	Advantages	Disadvantages
Loihi 2	Intel 2021	130,000 artificial neurons,130 million synapses, 4,096 cores.	23.6 pJ per synaptic operation	Digital ASIC at 14 nm. FinFET,	Large Area occupied due to Digital Implementation
TrueNorth	IBM 2004	4096 cores with 256 programmable simulated neurons, 268 million synapses each	26 pJ per Synaptic Operation.	Digital ASIC at 28 nm.	SNN emulation without on-chip learning
SpiNNaker	University of Manchester 2018	57,600 ARM9 processors, 1,036,800 cores and over 7 TB of RAM.	100 W and an air-conditioned environment	More flexible. 130 nm process technology	Energy Inefficient as it consumes 100 W of power.
DYNAP-SE	INI Zurich 2018	1024 neurons, 64K synapses (12-bit CAM)	17 pJ per synaptic operation	Mixed signal 180 nm CMOS. Hybrid analog/digital circuits for synapse and neuron.	Area Overhead

Neuromorphic Processors

NEUROMORPHIC COMPUTING



Von Neumann Vs Neuromorphic Computing

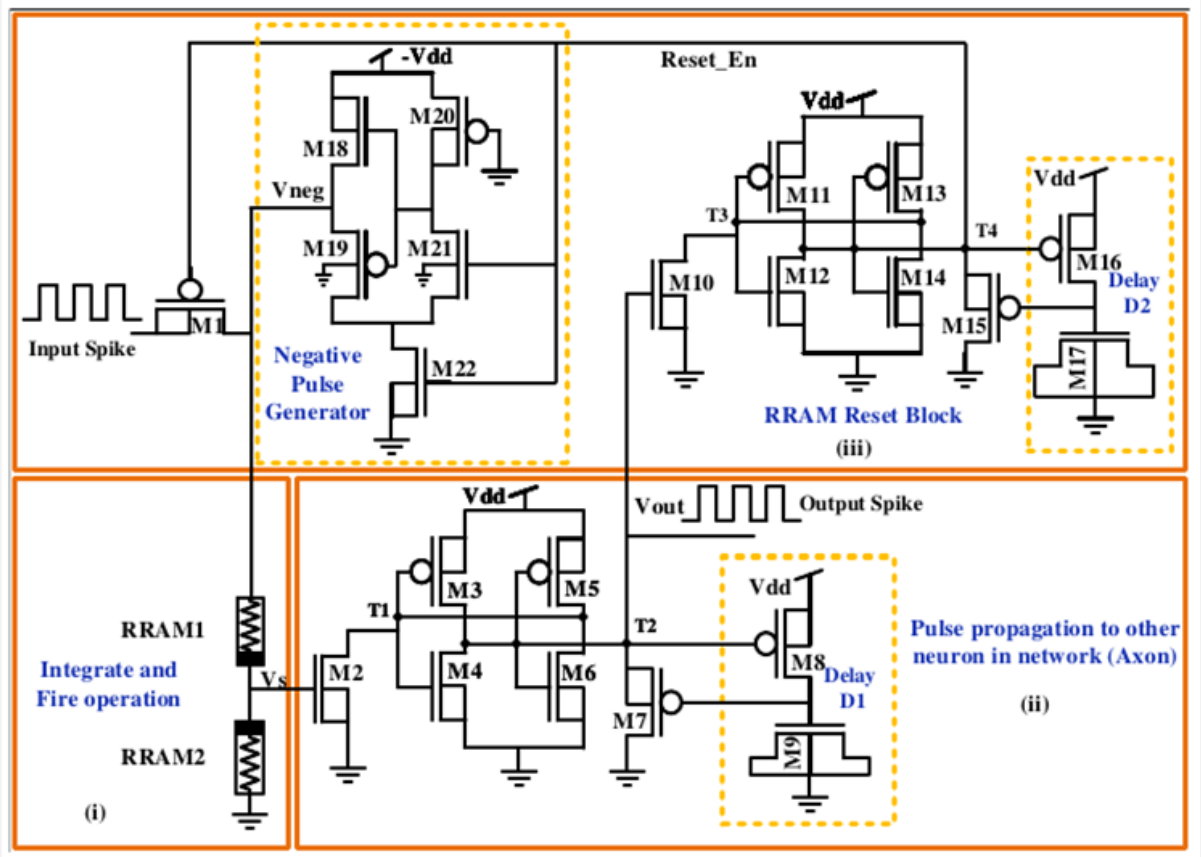
NEUROMORPHIC COMPUTING

x for RRAM1 is set to 5 nm

R_{RRAM1} = 50 MΩ (High Resistance State)

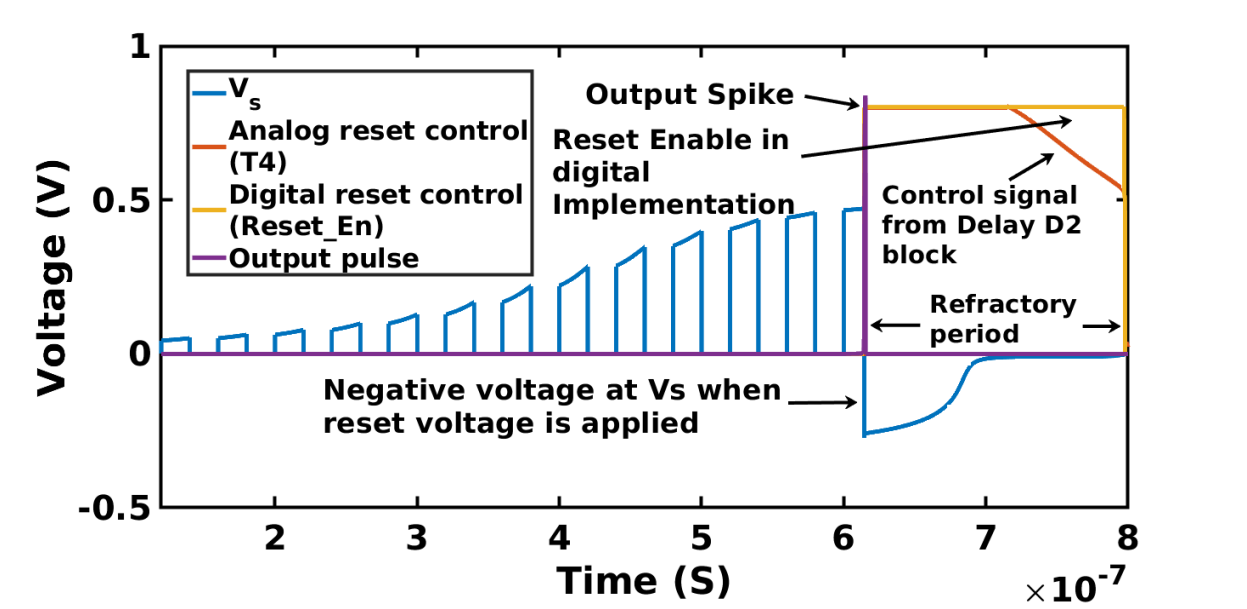
R_{RRAM2} = 1.3 KΩ (Low Resistance State)

Energy/spike = 1.5 x10^{-15} J



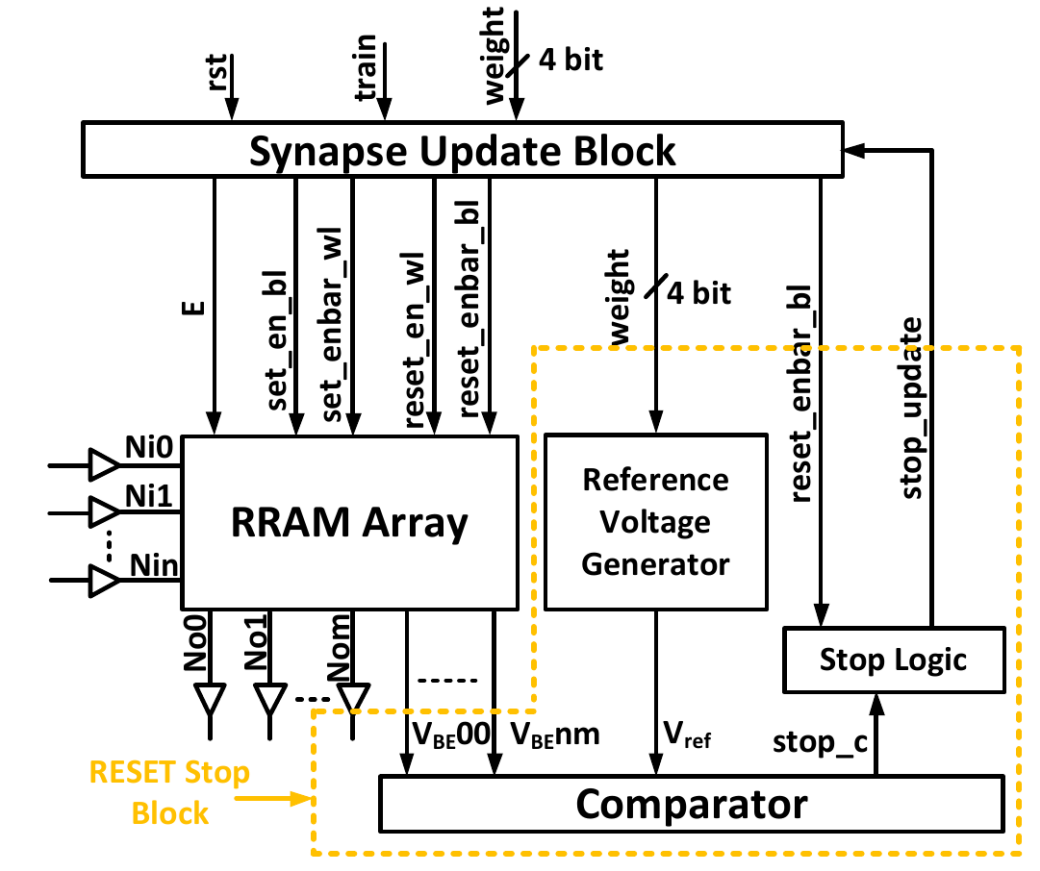
Self resetting I&F neuron

NEUROMORPHIC COMPUTING



Publication	Year	Platform	Neuron Model	Energy per spike(J)	Spiking Frequency	External RESET
[5]	2018	PCMO	IF	4.8×10^{-12}	0.44 MHz – 0.8 MHz	Yes
[6]	2020	SGFBPF	LIF	0.25×10^{-12}	150 kHz	No
[7]	2020	FBFET	IF	2.9×10^{-15}	20 kHz	No
[8]	2020	PDSOI MOSFET	IF	3.2×10^{-15}	150 kHz	Yes
[9]	2021	DG-JLFET	LIF	1.14×10^{-12}	200 MHz	No
[10]	2021	CMOS	IF	0.135×10^{-12}	0.2 kHz	No
Proposed Work	2023	RRAM	IF	1.5×10^{-15}	277 kHz – 3 MHz	No

NEUROMORPHIC COMPUTING



Proposed Synaptic Architecture

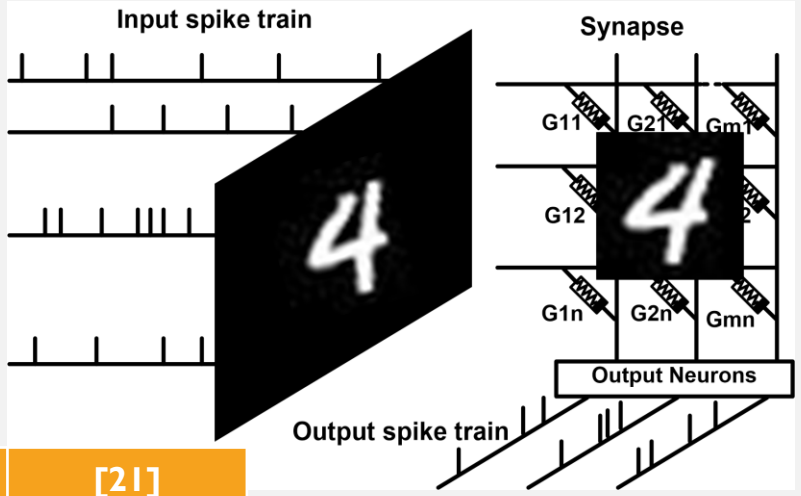
Publication	[11]	[12]	[13]	[14]	[15]	Proposed work
Bit/cell	3-Bit	3-Bit	3-Bit	2-Bit	2-Bit	4-Bit
Programming Mode	IC_{set}	IC_{set}	V_{reset}	IC_{set}	IC_{set}	V_{reset}
Array Size	8 x 8	2k bits	-	16 x 16	Single Cell	10 x 10 (25.6kbits)
Energy/cell	0.85 pJ	30 pJ	240 pJ	-	65 pJ	0.1 pJ
Latency	3.39 µs	5 µs	3.1 µs	15 µs	2.5 ms	1.07 µs
Design Level	Device	Device	Device	Circuit	Device	Circuit

Comparison with contemporary architectures

NEUROMORPHIC COMPUTING

To evaluate the performance of the RRAM-based neuron and the synapse, we trained them in Python, transferred the weights to the synaptic array, and verified the SNN architecture for inference.

We perform training for the MNIST (Modified National Standards and Technology) data-set (with 60,000 training images and 10,000 test images of handwritten digits).



Attributes	This work	[16]	[17]	[18]	[19]	[20]	[21]
Neuron	RRAM Based	Digital	Digital	Analog	Analog	Analog	Analog
Synapse	4T-1R	Analog	Analog	1T-1RRAM	9PCM	1 Memristor	1RRAM
Reprogrammable?	Yes	Yes	Yes	No	No	No	No
Bit/Cell	4-Bit/cell	-	-	2-Bit/cell	2-Bit/cell	2-Bit/cell	2-Bit/cell
Dataset	Full MNIST	Full MNIST	Full MNIST	Full MNIST	Full MNIST	Full MNIST	Full MNIST
Accuracy	89.7 %	94.8 %	93.5 %	75 %	70 %	75.65 %	90.76 %
Input-output neurons	784-10	784-6400	784-300	784-50	784-50	784-30	784-15000
Energy Per Synaptic operation	7.78 pJ	50 pJ	93 pJ	15.5 pJ	27 pJ	23 pJ	-

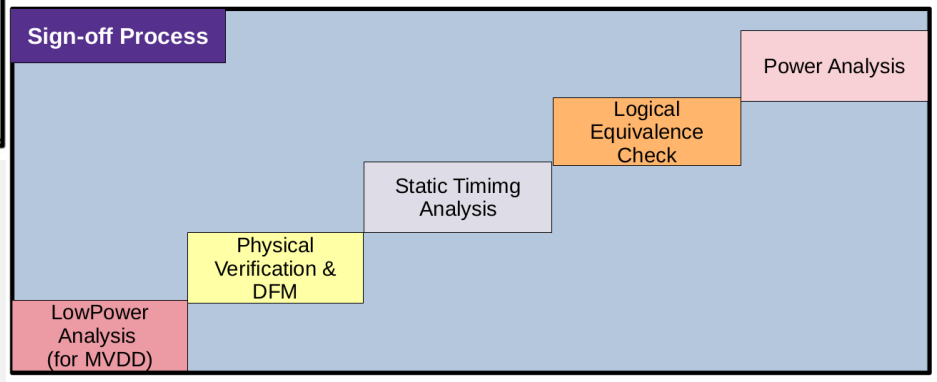
Benchmarking with state-of-the-art works

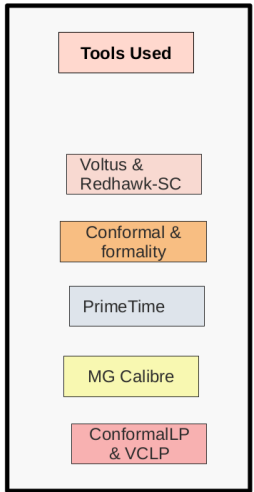
ROADMAP

- **Design (Collaboration Invited)**
  - Post Quantum Cryptography Coprocessor Tapeout and Validation by March 2025
  - Secure AI SoC Tapeout and Validation by March 2025
  - Wearable Healthcare Products by December 2025
  - Applications based on AI SoC and PQC Core by December 2025
  - Neuromorphic Computing Processor with the Complete Ecosystem by December 2026

ELECTRONIC DESIGN AUTOMATION (EDA)

Inputs	STAGES	Tools Process	Check Done	Tools Used
Scan config. UPF .lef .def .tluplus captables .libs .sdc RTL files	RTL Synthesis	Logical optimization and mapping to tech gates.	CheckDesign CheckTiming ReportTiming LEC Check	DesignCompiler & Genus Conformal & Formality
.libs .sdc .v(netlist) .lef .tf(ndm) .tluplus captables	Floorplanning	Macro Placement IO/pins Placement Physical Only Cells insertion	Notches Channel length PO cells insetion	ICC2 & Innovus Conformal & Formality
	Power Planning	PlacingVDD/VSS pins Creating Power ring, mesh and rails. Power Routing.	CheckPgDRC CheckViaMissing CheckConnectivity Power Analysis	ICC2 & Innovus Voltus
Dont use cells list	Placement	Placement of std cells. Leagalization Global routing Congestion and timing checks.	ReportCongestion PinDensity CellDensity ReportTiming LEC Check Power Analysis	ICC2 & Innovus Conformal & Formality Voltus
Target Skew+ID Clk Buff/Inv list Allowed Metal layes NDR	CTS	Insersion of clk Buff/Inv. Skew balancing	Check DRVs, skew, ID, crosstalk, timing. LEC Check Power Analysis	ICC2 & Innovus Conformal & Formality Voltus
	Routing	Detailed signal Routing & optimization RC Extraction	Check DRC, LVS, antenna DRC. CheckTiming. LEC Check Power Analysis	ICC2 & Innovus Conformal & Formality Voltus PT





ELECTRONIC DESIGN AUTOMATION (EDA)

1. **An analog/RF circuit simulator**

1. **VEDA: An indigenous TCAD Engine**

2. **Kapees: Floorplanning, Placement and Routing Tools of 2D and 3D VLSI digital circuits**

3. **ML-based VLSI Power Grid Analyzer**

4. **Analog layout design automation**

ELECTRONIC DESIGN AUTOMATION (EDA)

- **An Analog/RF Circuit Simulator**

- **Specifications:**
  - ✓ **Similar to HSPICE and SPECTRE.**
  - ✓ **Provides all the analyses such as OP, DC, AC, TRAN, NOISE, TF etc.**
  - ✓ **Supports parallelization of circuit analysis at micro as well as macro level**
  - ✓ **Provides single processor multithreaded environment for analysis**
  - ✓ **Supports heterogenous computing environment for circuit analysis**
  - ✓ **Supports all direct and indirect matrix solution methods**
  - ✓ **Simulates circuits of size up to 10 Million nodes**
  - ✓ **Extended up to 100 Million – 01 Billion nodes**

ELECTRONIC DESIGN AUTOMATION (EDA)

- **VEDA (Very Efficient Device Analyzer): A TCAD Simulator (In collaboration with VSD and SCL Chandigarh) : Similar to Sentauras and Silvaco TCAD engine**

- **Specifications:**
  - ✓ **FDM, FEM, FVM and their variants**
  - ✓ **2D and 3D TCAD analysis**
  - ✓ **Parallelization of device analysis at micro as well as macro level**
  - ✓ **Single processor multithreaded environment for analysis**
  - ✓ **Heterogenous computing environment for device analysis**
  - ✓ **All direct and indirect matrix solution methods**
  - ✓ **All necessary numerical techniques for convergence**
  - ✓ **Device design and fabrication using SCL foundry**
  - ✓ **Machine Learning based techniques for faster semiconductor device modelling**
  - ✓ **State-of-the-art techniques for system matrix solution such as random walk, river formation dynamics**
  - ✓ **High power and novel design analysis and modelling**

ELECTRONIC DESIGN AUTOMATION (EDA)

- **Status:**

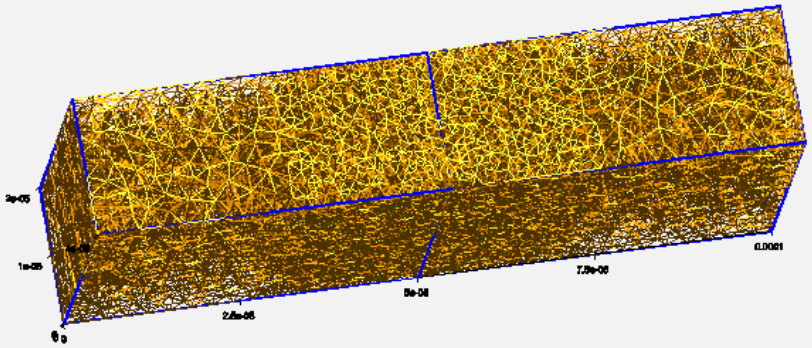
1. Work is in progress. Developed an essential framework for TCAD simulator integrated with Drift-Diffusion and Quantum Ballistic Models

2. Improved FEM (FEM-DG, SUPG etc.) techniques have been incorporated

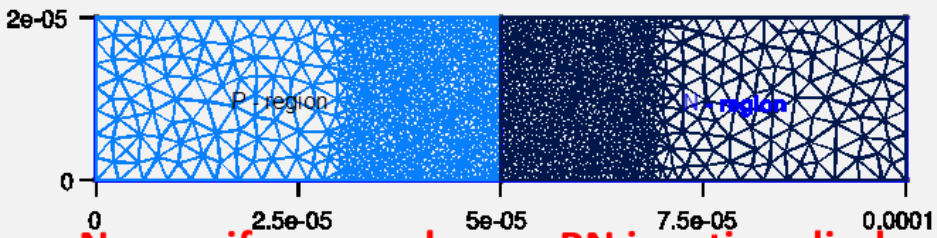
3. The results of VEDA are **10 times** more accurate as compared to Sentaurus, a commercial simulator with a little increase (20% only) in speed. Working on to improve computational speed on a single processor.

4. Integrating a machine learning based interface to VEDA not only to speed up device analysis but also to aid search of new devices irrespective of technology. New schemes for parallel TCAD simulation are being investigated.

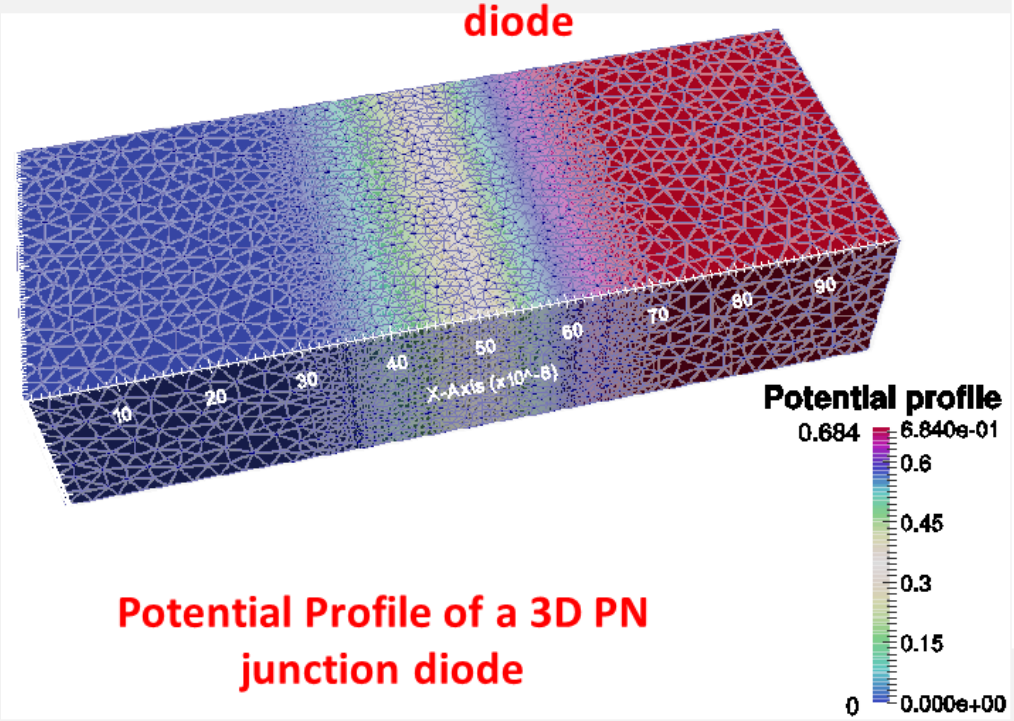
ELECTRONIC DESIGN AUTOMATION (EDA)



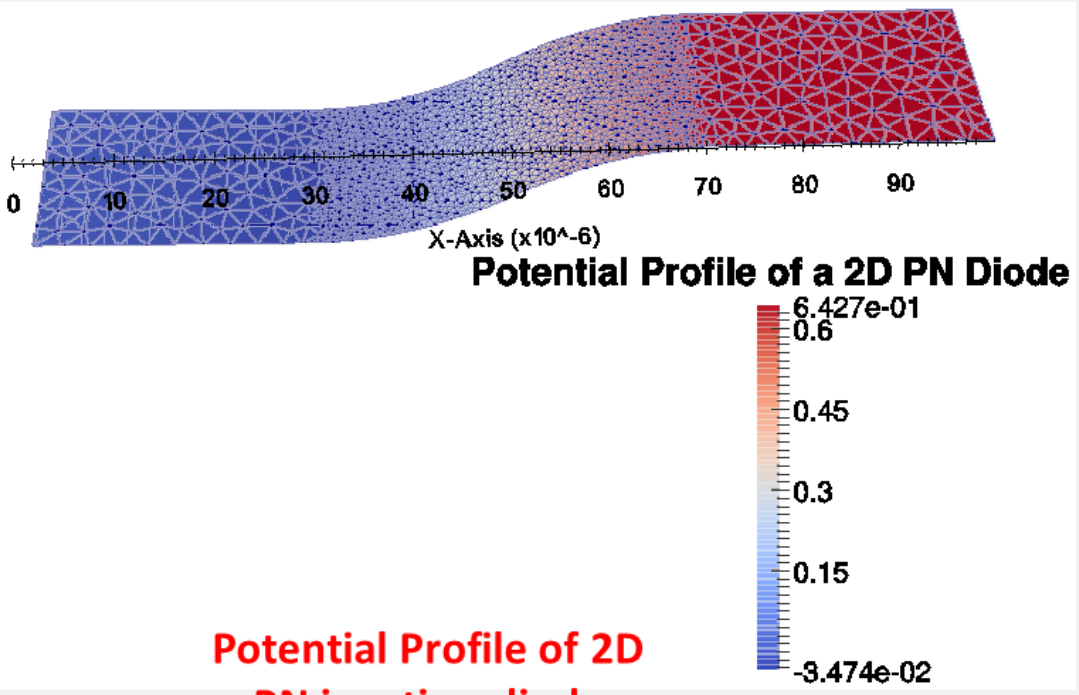
Non-uniform 3D mesh over PN junction diode



Non-uniform mesh over PN junction diode



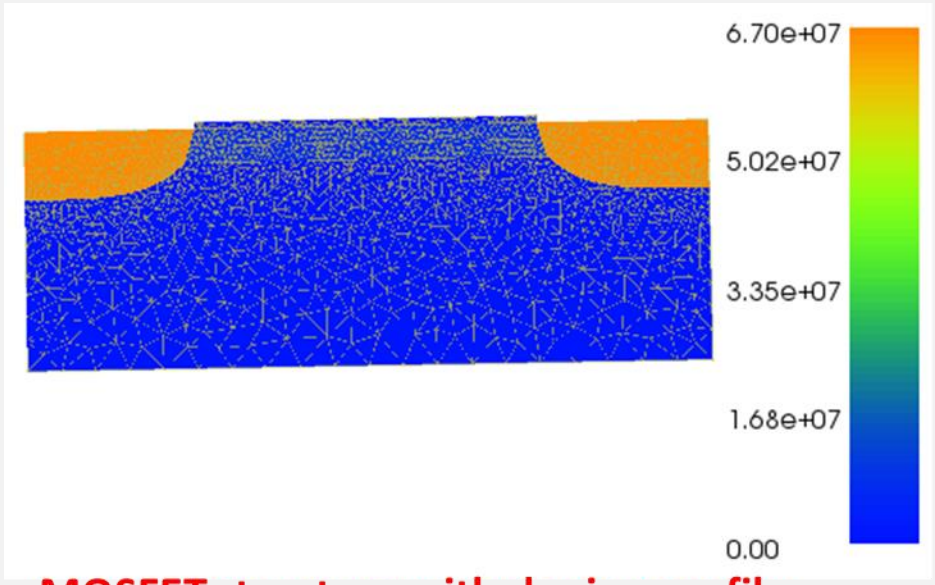
Potential Profile of a 3D PN junction diode



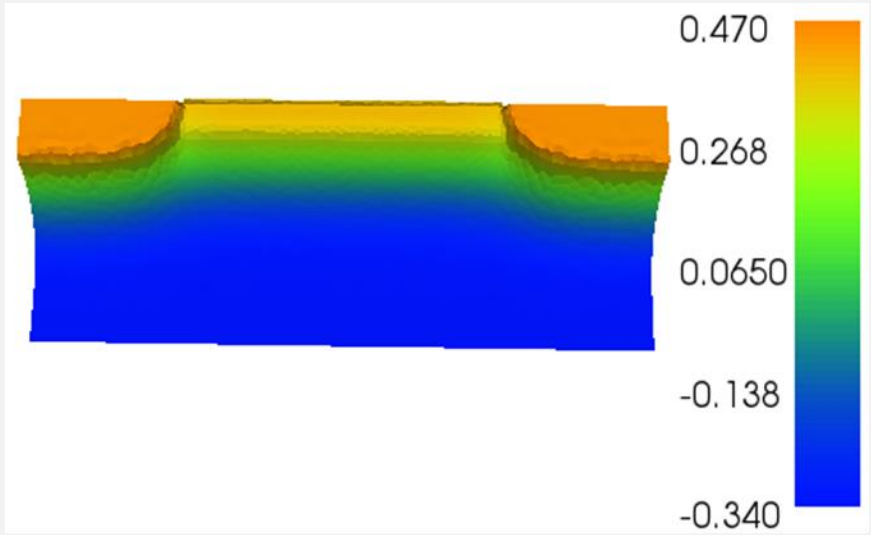
Potential Profile of 2D PN junction diode

Results of our indigenous TCAD Simulator VEDA

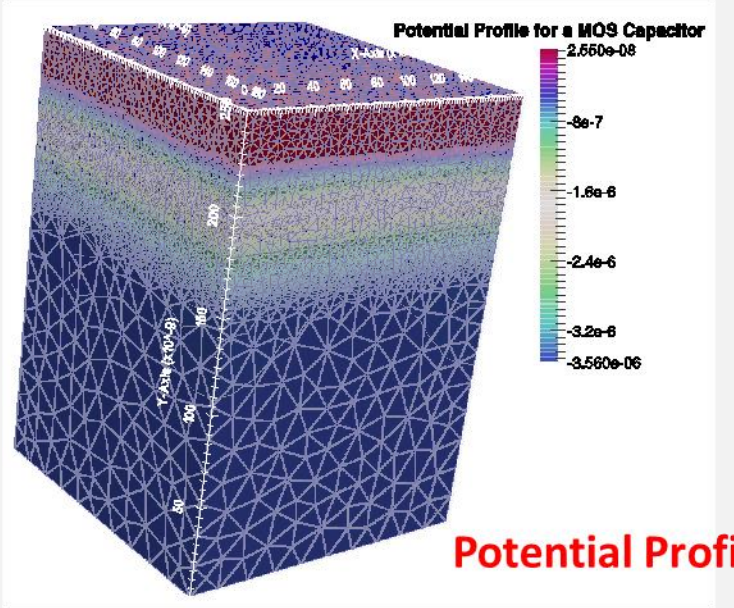
ELECTRONIC DESIGN AUTOMATION (EDA)



MOSFET structure with doping profile



Potential Profile inside the MOSFET at zero drain voltage

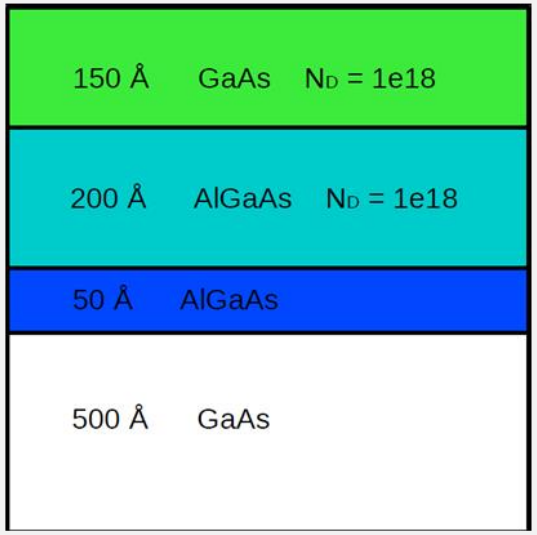


Potential Profile of MOSFET Capacitor

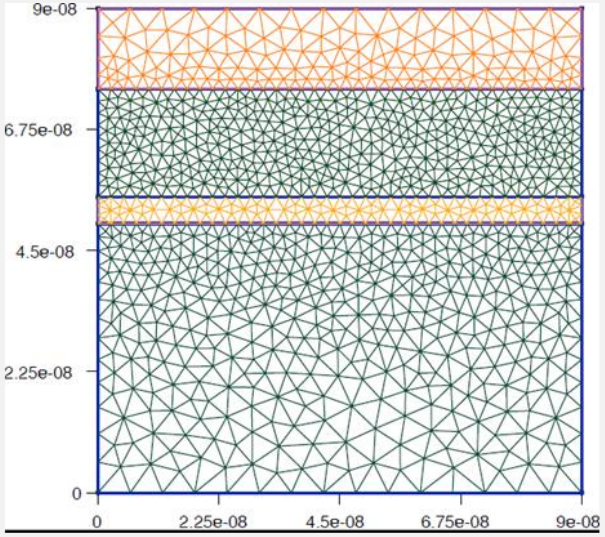
Results of our indigenous device simulator VEDA

It supports drift-diffusion and Quantum-Ballistic models.

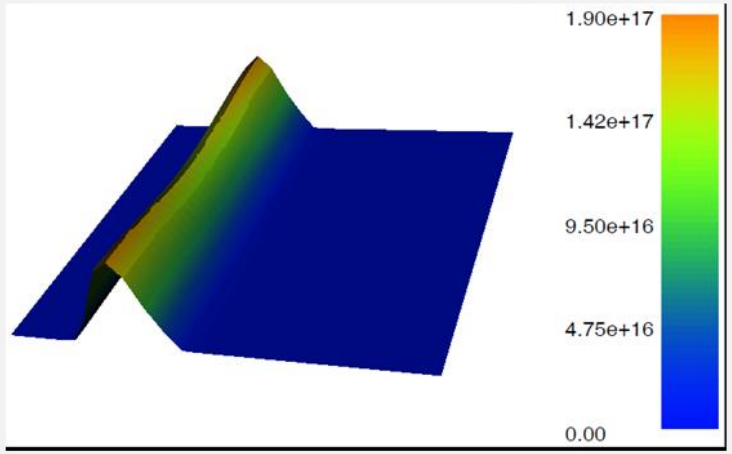
ELECTRONIC DESIGN AUTOMATION (EDA)



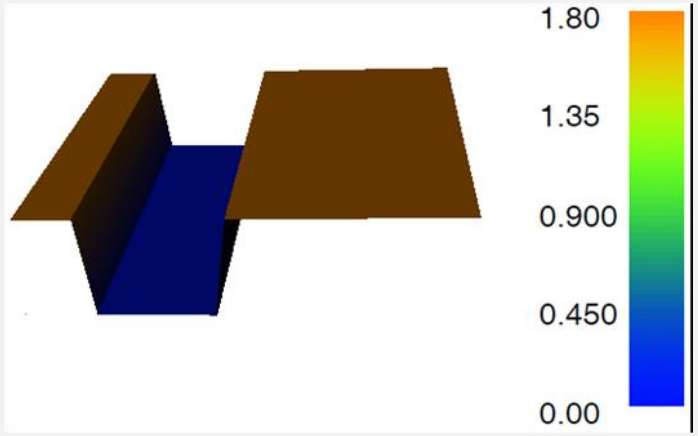
Heterostructure of GaAs/AlGaAs



Meshing



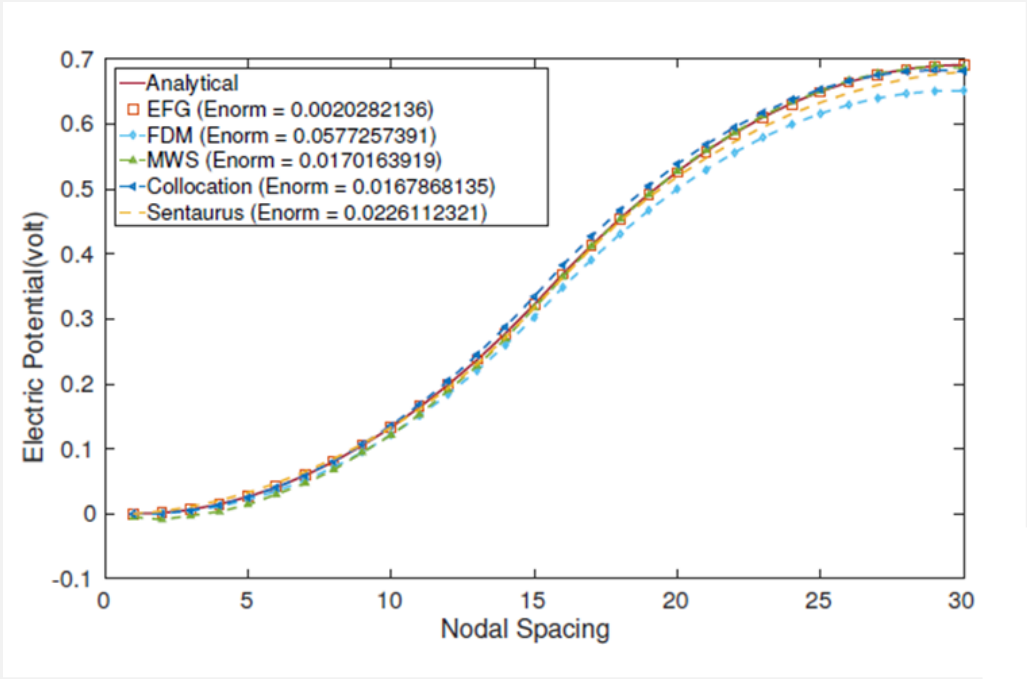
Electron density profile



Potential profile

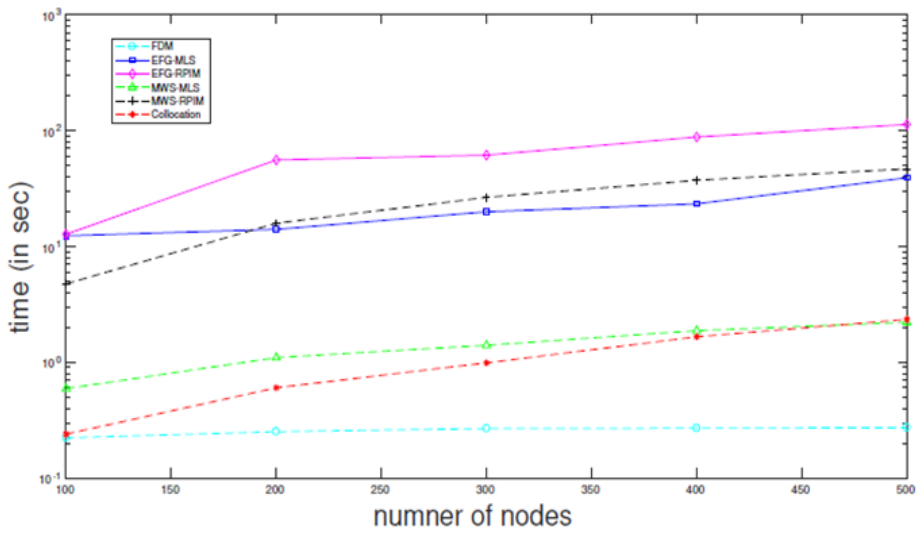
Results of our indigenous device simulator VEDA

ELECTRONIC DESIGN AUTOMATION (EDA)



Comparison with Sentaurus and other methods

Comparison of Computation Time



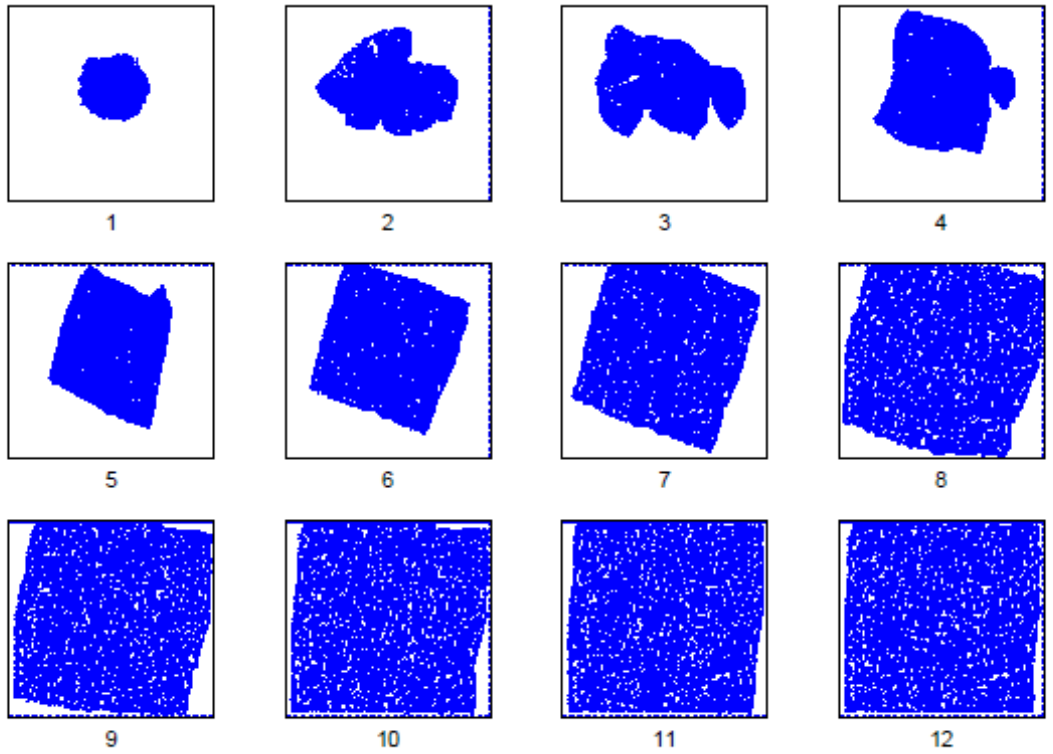
Results of our indigenous device simulator VEDA

ELECTRONIC DESIGN AUTOMATION (EDA)

Algorithm 3 *Kapees3*: Multilevel Algorithm

Require: Hypergraph H_0: standard cell circuit
and n_{max} Number of cells at the coarsest level
Ensure: (x^*, y^*) optimal cell positions

1: First choice clustering till the number of cells is $> n_{max}$
2: Let the levels of FCC be LEV to 0 ▷ LEV is coarsest
3: **if** Pads connected to movable standard cells **then**
4: Initialize cell positions by solving QP
5: **else**
6: Initialize cell positions by randomization
7: **end if**
8: Initialze the value of μ_0 by solving Eq (11)
9: **for** $level = LEV$ to $level = 0$ **do**
10: Estimate grid-cells, $NBx = NBy = \sqrt{n_{level}}$
11: Solve Equation (6.4) and (6.5) for each grid-cell
12: Initialze $\mu_{level} = \mu_{level-1}/2$, $m = 0$, $\mu_m = \mu_l$
13: **while** $overflow\_ratio > 0.01$ **do**
14: Solve min $H(x, y) + \mu_m \sum (B_g - A_g)^2$
15: $m = m + 1$
16: $\mu_m = 2 * \mu_{m-1}$
17: Estimate $overflow\_ratio$
18: **if** $overflow\_ratio < 0.1$ and $level = 0$ **then**
19: Legalize and save best result
20: **end if**
21: **end while**
22: **end for**



Progression of placement solution, starting from initial placement (marked by number 1), till the final global placement (marked by number 12).

ELECTRONIC DESIGN AUTOMATION (EDA)

Circuits	mPL6	NTUPlace3	Dragon	Feng Shui	Capo10.5	Kapees3
	HPWL $\times 10^6$	HPWL $\times 10^6$	HPWL $\times 10^6$	HPWL $\times 10^6$	HPWL $\times 10^6$	HPWL $\times 10^6$
PEKO01	10.1271	15.076	20.248	16.4146	13.5326	12.0781
PEKO02	15.6529	24.0175	31.2822	27.163	21.0727	16.3846
PEKO03	22.4259	28.3669	36.1874	31.7795	33.7368	19.7872
PEKO04	23.6169	32.9212	35.8333	36.2248	41.4622	23.0348
PEKO05	23.8461	35.3598	37.2307	39.8124	45.1628	24.8374
PEKO06	25.7724	38.2358	48.1904	44.5226	38.6956	27.1373
PEKO07	35.7566	53.4979	82.4951	59.9856	67.2508	37.8252
PEKO08	47.1814	57.5143	82.0223	64.5356	80.6975	40.9355
PEKO09	55.8006	62.6516	91.3205	76.6115	92.7892	60.0286
PEKO10	66.178	95.5689	110.9	105.448	132.421	67.4856
PEKO11	74.2934	85.7527	114.442	102.637	120.501	62.2829
PEKO12	82.5655	97.7335	118.453	113.135	123.109	66.0617
PEKO13	86.865	118.926	172.172	134.853	142.334	77.6594
PEKO14	156.285	160.181	NA	213.205	NA	139.908
PEKO15	185.418	202.77	NA	OOM	NA	186.745
PEKO16	207.394	222.271	NA	OOM	NA	209.179
PEKO17	217.015	238.421	NA	OOM	NA	220.95
PEKO18	227.443	234.794	NA	OOM	NA	234.397
Average	1.027	1.302	1.478	1.5757	1.695	1.00

Circuits	Capo10.5	FLOP	FastPlace	ComPLx	POLAR	mPL6	MP3U	Kapees3
AD1	84.77	76.83	82.39	79.05	92.17	77.84	79.05	73.94
AD2	92.61	84.14	88.53	99.11	149.43	88.40	84.26	80.00
AD3	202.37	175.99	187.98	175.78	197.48	180.64	168.11	175.98
AD4	202.38	161.68	187.50	156.75	175.19	162.02	156.33	164.02
AD5	565.88	357.83	338.77	338.67	380.45	376.30	306.12	283.64
BB1	112.58	94.92	104.91	96.18	99.12	99.36	99.78	97.06
BB2	149.54	153.02	145.89	147.19	157.72	144.37	149.96	148.39
BB3	583.37	346.24	400.40	344.63	420.28	319.63	392.72	357.28
BB4	915.37	777.84	775.43	772.53	814.07	804.00	809.41	795.05
NB1	110.54	67.97	73.91	65.26	70.68	66.93	61.75	66.88
NB2	303.25	187.40	197.15	187.87	197.65	179.18	170.80	181.42
NB3	1282.19	345.99	325.72	269.47	601.17	415.86	223.38	294.34
NB4	300.69	256.54	270.70	256.97	277.60	277.69	253.39	200.99
NB5	570.32	510.83	500.09	453.05	450.69	515.49	450.07	377.92
NB6	609.16	493.64	512.19	452.83	475.78	482.44	485.73	441.47
NB7	1481.45	1078.18	1016.10	1010.00	1107.59	1038.66	1125.84	1089.58
Avg WL	1.5662	1.0784	1.1155	1.0458	1.2367	1.0996	1.0296	1.00

HPWL comparison for PEKO and MMS Circuits

ELECTRONIC DESIGN AUTOMATION (EDA)

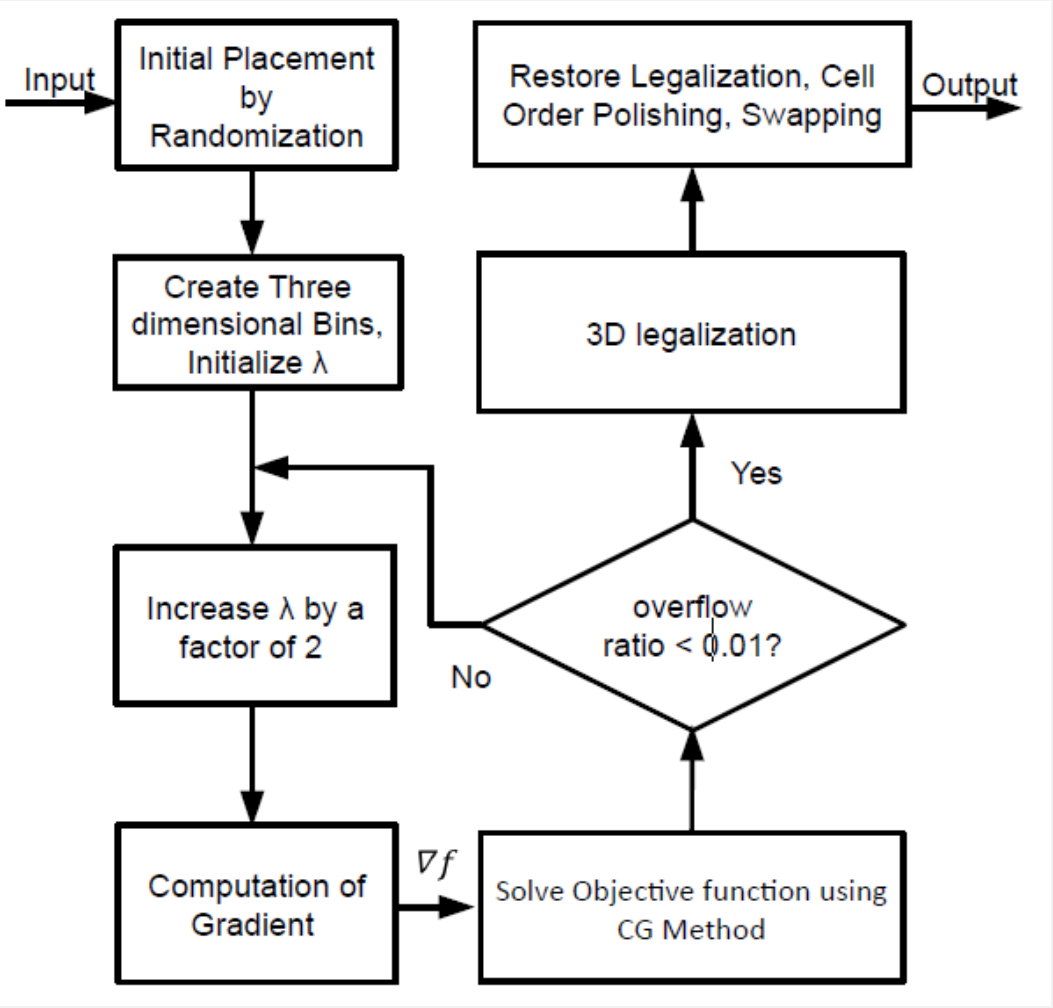
Circuits	mPL6	NTUPlace3	Dragon	Feng Shui	Capo10.5	Kapees3
	Runtime min sec	Runtime min sec	Runtime min sec	Runtime min sec	Runtime min sec	Runtime min sec
PEKO01	11m46s	8m33s	51m54s	11m2s	13m30s	2m33s
PEKO02	17m9s	10m19s	79m7s	19m34s	25m53s	4m30s
PEKO03	21m31s	17m48s	79m9s	21m46s	73m58s	4m55s
PEKO04	24m7s	18m52s	82m45s	25m50s	89m43s	6m25s
PEKO05	25m29s	18m32s	122m17s	28m27s	91m11s	6m57s
PEKO06	28m46s	18m16s	104m30s	32m32s	110m2s	8m6s
PEKO07	46m5s	32m27s	209m15s	45m59s	219m3s	12m11s
PEKO08	56m58s	36m38s	299m1s	54m4s	236m8s	15m20s
PEKO09	57m53s	24m29s	252m56s	57m57s	254m16s	20m12s
PEKO10	74m25s	47m32s	199m36s	78m34s	362m17s	22m58s
PEKO11	69m28s	38m44s	161m15s	77m25s	362m10s	21m2s
PEKO12	82m11s	56m59s	219m46s	83m33s	398m43s	22m24s
PEKO13	89m31s	72m1s	346m47s	97m36s	530m44s	26m30s
PEKO14	179m0s	83m45s	>12hrs	178m30s	>12hrs	69m16s
PEKO15	213m16s	110m30s	>12hrs	NA	>12hrs	74m12s
PEKO16	230m3s	92m46s	>12hrs	NA	>12hrs	91m46s
PEKO17	240m52s	95m11s	>12hrs	NA	>12hrs	88m28s
PEKO18	256m3s	106m50s	>12hrs	NA	>12hrs	97m29s
Average	3.38	2.134	14.26	3.746	14.10	1.00

Circuits	mPL6	NTUPlace3	Dragon	Feng Shui	Capo10.5	Kapees3
	Runtime min sec	Runtime min sec	Runtime min sec	Runtime min sec	Runtime min sec	Runtime min sec
PEKO01	11m46s	8m33s	51m54s	11m2s	13m30s	2m33s
PEKO02	17m9s	10m19s	79m7s	19m34s	25m53s	4m30s
PEKO03	21m31s	17m48s	79m9s	21m46s	73m58s	4m55s
PEKO04	24m7s	18m52s	82m45s	25m50s	89m43s	6m25s
PEKO05	25m29s	18m32s	122m17s	28m27s	91m11s	6m57s
PEKO06	28m46s	18m16s	104m30s	32m32s	110m2s	8m6s
PEKO07	46m5s	32m27s	209m15s	45m59s	219m3s	12m11s
PEKO08	56m58s	36m38s	299m1s	54m4s	236m8s	15m20s
PEKO09	57m53s	24m29s	252m56s	57m57s	254m16s	20m12s
PEKO10	74m25s	47m32s	199m36s	78m34s	362m17s	22m58s
PEKO11	69m28s	38m44s	161m15s	77m25s	362m10s	21m2s
PEKO12	82m11s	56m59s	219m46s	83m33s	398m43s	22m24s
PEKO13	89m31s	72m1s	346m47s	97m36s	530m44s	26m30s
PEKO14	179m0s	83m45s	>12hrs	178m30s	>12hrs	69m16s
PEKO15	213m16s	110m30s	>12hrs	NA	>12hrs	74m12s
PEKO16	230m3s	92m46s	>12hrs	NA	>12hrs	91m46s
PEKO17	240m52s	95m11s	>12hrs	NA	>12hrs	88m28s
PEKO18	256m3s	106m50s	>12hrs	NA	>12hrs	97m29s
Average	3.38	2.134	14.26	3.746	14.10	1.00

Runtime comparison for PEKO Suite1 and PEKO Suite2 benchmarks

ELECTRONIC DESIGN AUTOMATION (EDA)

- **3D-Kapees:**



Flow diagram of our 3D placement tool

Circuits	Comparison 1					
	F3D [36]			Proposed Placement Tool (TSV Oblivious)		
	HPWL $\times 10^7$	#TSVs $\times 10^3$	runtime min	HPWL $\times 10^7$	#TSVs $\times 10^3$	runtime min
IBM01	0.37	0.87	7.19	0.28	9.8	18.7
IBM03	0.84	2.92	12.31	0.70	18.1	55.5
IBM04	1.11	3.36	24.21	0.98	22.1	39.45
IBM06	1.45	3.40	27.07	1.25	28.4	60.2
IBM07	2.27	4.46	36.00	1.92	38.0	68.1
IBM08	2.36	4.43	30.81	2.09	40.9	120.2
IBM09	2.08	3.37	30.14	2.03	42.9	116
Avg	1.164	0.1135	0.38	1.0	1.0	1.0

3D Placement results comparison with Cong and Luo [36] on IBM version 1 benchmarks

Circuits	Comparison 2					
	F3D [36]			Proposed Placement Tool(TSV aware)		
	HPWL $\times 10^7$	#TSVs $\times 10^3$	runtime min	HPWL $\times 10^7$	#TSVs $\times 10^3$	runtime min
IBM01	0.37	0.87	7.19	0.45	0.463	3.5
IBM03	0.84	2.92	12.31	1.09	2.108	7.5
IBM04	1.11	3.36	24.21	1.53	2.263	7.7
IBM06	1.45	3.40	27.07	2.28	2.653	11.54
IBM07	2.27	4.46	36.00	4.18	3.385	18.8
IBM08	2.36	4.43	30.81	4.47	2.850	23.95
IBM09	2.08	3.37	30.14	4.36	1.912	21.52
Avg	0.64	1.52	1.96	1.0	1.0	1.0

ELECTRONIC DESIGN AUTOMATION (EDA)

Power Distribution Network (PDN)

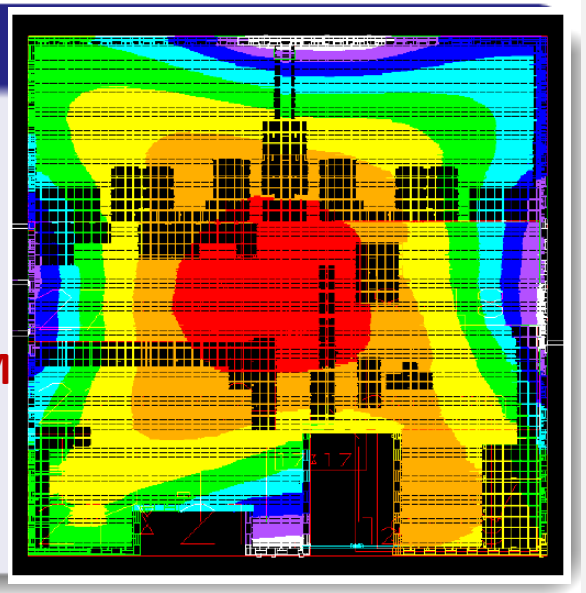
- Power grids are metallic grids → Distribute power to different functional blocks of a chip.
- Major concerns
  - Reliable on-chip power delivery
  - Maintenance of signal integrity

Issues in PDN design

- IR drop
- $L\frac{di}{dt}$ noise
- Electromigration

→with consideration of minimum **Area**.

A real industrial chip with cell instances = 0.5M and P/G resistors = 0.6M, Courtesy IBM



ELECTRONIC DESIGN AUTOMATION (EDA)

Benchmarks	SLP [1]				RFD [2]				MRFD			
	$\vartheta'(\%)$[1]	$A(\%)$[1]	Constr.[2]	Time (sec)	$\vartheta'(\%)$[1]	$A(\%)$[1]	Constr.[2]	Time (sec)	$\vartheta'(\%)$[1]	$A(\%)$[1]	Constr.[2]	Time (sec)
ibmpg2	0.91	03.90	72	98 (+ 0.23)	6.60	02.02	86	92 (+ 0.02)	1.06	04.00	89	39 (+ 0.02)
ibmpg4	1.84	06.00	162	913 (+ 0.50)	4.38	01.30	151	1146 (+ 0.11)	1.08	06.70	176	553 (+ 0.11)
ibmpg5	1.80	08.90	139	1221 (+ 0.62)	4.05	01.56	179	1427 (+ 0.30)	0.89	12.40	149	626 (+ 0.30)
ibmpg6	2.05	07.12	136	1734 (+ 0.67)	5.21	02.12	121	2201 (+ 0.31)	1.91	08.20	132	989 (+ 0.32)
industry1	1.24	03.95	200	258 (+ 0.45)	3.03	00.50	230	397 (+ 0.03)	0.06	06.56	312	189 (+ 0.03)
industry2	1.80	07.00	1123	1233 (+ 0.60)	4.03	02.02	1521	1310 (+ 0.32)	0.23	13.96	1035	571 (+ 0.32)
industry3	2.61	07.89	1406	3058 (+ 4.30)	6.13	03.34	2010	3732 (+ 1.23)	1.52	10.11	2256	1181 (+ 1.23)
industry4	-	-	-	-	9.25	04.56	2313	7310 (+ 5.23)	1.59	18.23	2751	1634 (+ 5.23)
industry5	-	-	-	-	12.40	06.23	3942	8897 (+ 12.34)	1.78	22.21	5127	2418 (+ 12.34)
industry6	-	-	-	-	-	-	-	-	1.98	28.63	5748	4394 (+ 23.41)

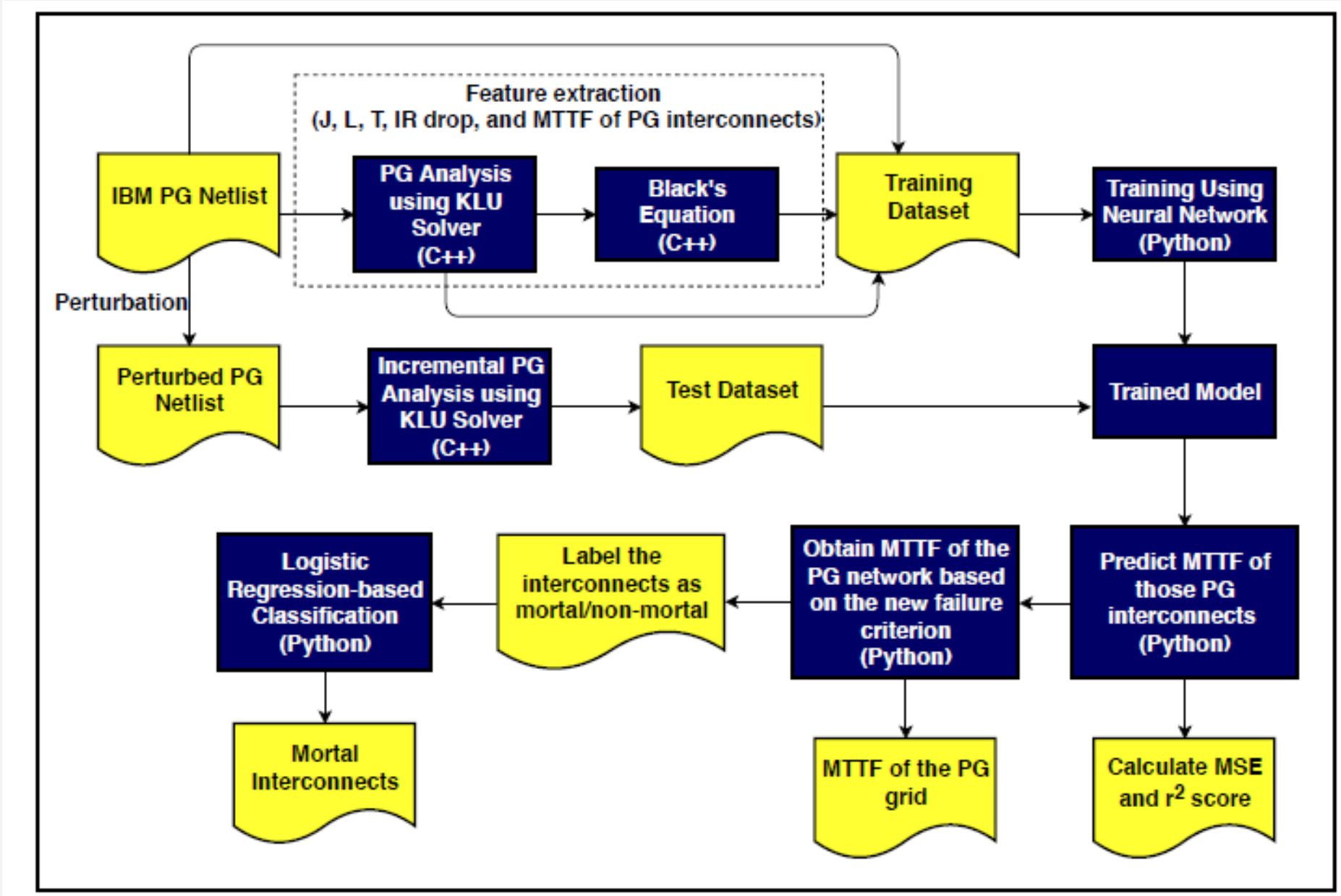
1 ϑ' denotes percentage of affected nodes (above threshold) after optimization.
'A' denotes percentage of reduction in wire area after optimization.

2 'Constr.' denotes number of constraint violations during optimization.
'Time' denotes computational time (algorithm time + process time) required for entire optimization process.

[1] S. D. Tan, C. Shi, and J. Lee, "Reliability-constrained area optimization of VLSI power/ground networks via sequence of linear programmings," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 22, no. 12, pp. 1678-1684, 2005.

[2] S. Dash, D. Joshi, and G. Trivedi, "CMOS Analog Circuit Optimization via River Formation Dynamics," in *IEEE* 26^{th} *International Conference Radioelektronika*, Kosice, Slovak Republic, Apr 2016.

ELECTRONIC DESIGN AUTOMATION (EDA)



ML-based Electromigration-aware aging prediction flow

ELECTRONIC DESIGN AUTOMATION (EDA)

	Time (sec)		Speedup
PG circuits	Conventional	PowerPlanningDL	$\frac{\text{Time}_{\text{Conventional}}}{\text{Time}_{\text{PowerPlanningDL}}}$
ibmpg1	6.85	3.56	1.92×
ibmpg2	23.46	11.88	1.97×
ibmpg3	29.50	8.07	3.59×
ibmpg4	52.4	11.83	4.42×
ibmpg5	74.80	12.74	5.87×
ibmpg6	97.5	17.41	5.60×
ibmpgnew1	102.58	21.50	4.77×
ibmpgnew2	48.60	10.86	4.47×

COMPARATIVE STUDY OF CONVERGENCE TIME FOR CONVENTIONAL POWER PLANNING APPROACH AND PROPOSED ML FRAMEWORK

	Worst-case IR drop (mV)	
PG circuits	Conventional	PowerPlanningDL
ibmpg1	69.8	68.2
ibmpg2	36.3	36.1
ibmpg3	18.1	18.0
ibmpg4	4.0	4.1
ibmpg5	4.3	4.2
ibmpg6	13.1	13.0

COMPARATIVE STUDY OF WORST-CASE IR DROP USING CONVENTIONAL POWER PLANNING APPROACH AND PROPOSED ML FRAMEWORK

ELECTRONIC DESIGN AUTOMATION (EDA)

Methods	CPU Runtime (t) (Hours)					Speedup			
	TCAD2016 [14] (t_H)	**ICCAD2017** [16] (t_{Ch})	**TCAD2018** [17] (t_C)	**IRPS2019** [18] (t_N)	**Proposed** (t_{ML})	$\frac{t_H}{t_{ML}}$	$\frac{t_{Ch}}{t_{ML}}$	$\frac{t_C}{t_{ML}}$	$\frac{t_N}{t_{ML}}$
PG Circuits									
$PG1$	0.02	0.02	0.001	0.000166	0.0001	200×	200×	10×	1.66×
$ibmpg1$	0.05	0.03	0.003	0.01000	0.0003	166.66×	100×	10×	33.33×
$ibmpg2$	0.11	0.31	0.04	0.02000	0.002	55×	155×	20×	10×
$ibmpg3$	5.83	4.27	0.41	0.07000	0.009	647.77×	610×	45.55×	7.77×
$ibmpg4$	14.71	6.81	2.31	0.11000	0.007	2101.42×	972.85×	330×	15.71×
$ibmpg5$	0.69	0.25	0.06	0.03000	0.006	115×	41.66×	10×	5×
$ibmpg6$	1.75	2.07	0.79	0.23330	0.009	194.44×	230×	87.77×	25.92×
$ibmpgnew1$	16.78	0.42	1.24	0.08000	0.013	1290.76×	32.06×	95.38×	6.15×
$ibmpgnew2$	15.32	2.60	0.43	0.06000	0.008	1915×	325×	53.75×	7.50×
$PG2$	10.94	1.12	1.06	0.10166	0.010	1094×	112×	106×	10.06×
$PG3$	-	-	-	0.13666	0.04200	-	-	-	3.25×
$PG4$	-	-	-	0.25666	0.10100	-	-	-	2.54×
Avg. Speedup						778×	277.85×	76.84×	10.74×

COMPARATIVE STUDY OF CPU RUNTIME FOR OUR PROPOSED ML-BASED APPROACH WITH WORKS OF [14], [16]–[18] FOR IBM POWER GRID BENCHMARKS.

ROADMAP

- **Electronic Design Automation (EDA)** **(Collaboration Invited)**

  1. **Analog/RF Circuit Simulator:**

     - Planned release of the analog/RF circuit simulator for beta version with standard libraries by December 2025 with SCL PDK integration and testing
     - Release to the academia free of cost
     - Integration with the VLSI Design Flow

- **TCAD Simulator**
  - Advanced models such as Quantum Ballistic, Hydrodynamic transport models **December 2025**
  - Supports NEGF and GW Approximation by **March 2026**

- **Floorplanning, Placement and Routing Engine** to be released by **December 2025**

- **ML-based Power Grid Analyzer** to be released by **December 2025**

ADVANCED ESDM WORKFORCE DEVELOPMENT

A GLIMPSE OF INDIAN ACADEMIA

- 800+ Universities
- 35000+ Colleges affiliated with the universities
- 2100+ Diploma colleges in India
- 38 Million Students in science stream
- 1.1 Million students in Engineering domain every year
- Top 100 universities including 23 IITs produce < 10,000 students (probably!) every year in the VLSI domain

ADVANCED ESDM WORKFORCE DEVELOPMENT

- **Daksh Gurukul** is a joint initiative of **National Skill Development Corporation (NSDC)** under **Ministry of Skill Development and Entrepreneurship (MSDE)** and **IIT Guwahati.**

- **Objectives:**
  - Outcome-driven credit-linked advanced certification programs ensuring the Indian students/industry professionals industry-ready by enhancing their knowledge skill set providing sessions
  - Designing workforce-ready curriculum for students to maintain a sustainable career.
  - This initiative envisages to support Government of India's Start-up India, Make-in-India and Atmanirbhar Bharat initiatives and also work towards India's collective visions for Industry 4.0, Healthcare 4.0, Smart City and Look East Policy for Vikshit Bharat.
  - **500,000** Advanced ESDM Workforce in coming **05-10 years through Product-based Advanced Certification Programs**

ADVANCED ESDM WORKFORCE DEVELOPMENT

Sl. No.	Course Name	Duration (hours)	Credits
1	Advanced Certification on FPGA based Digital IC Design	600	20
2	Advanced Certification on Digital Design Verification	750	25
3	Advanced Certification on Design for Testing (DFT)	750	25
4	Advanced Certification on VLSI Design Synthesis and Static Timing Analysis	570	19
5	Advanced Certification on VLSI Physical Design and Signoff	840	28
6	Advanced Certification on Complete ASIC Design Flow	1500	50
7	Advanced Certification on IC Packaging and Manufacturing (Kaynes Technology)	540	18
8	Advanced Certification on Multilayer PCB Design	540	18
9	Advanced Certification on Analog IC Design	600	20
10	Executive Certification on Analog IC Design	600	20
11	Advanced Certification on Radio Frequency Integrated Circuit (RFIC) Design	600	20
12	Executive Certification on Radio Frequency Integrated Circuit (RFIC) Design	600	20
12	Advanced Certification on Industrial IoT and Edge computing	720	24
12	Advanced Certification on Artificial Intelligence and Machine Learning	720	24

ADVANCED ESDM WORKFORCE DEVELOPMENT

Course Name	**RTL Design and FPGA Implementaion (Short-term)**
Min Qualification	**BTech/BE/BSc 3rd Year Completed**
Code	**VLSI01**
NSQF Level	**5.5**
Credits Earned	**20**

Code	NOS Module Name	No. of Hrs	Credits Earned
VLSI05N01	VLSI Digital Integrated Circuits	60	2
VLSI05N02	VLSI System Design	60	2
VLSI05N03	VLSI DSP	60	2
VLSI05N04	Hardware Description Language	120	4
VLSI06N02	High Level Synthesis	60	2
VLSI06N03	FPGA Implementation	90	3
	On the Job	150	5
	Total	600	20

Course Name	**RTL Design & Data Verification (Short-term)**
Min Qualification	**BTech/BE/BSc Completed**
Code	**VLSI02**
NSQF Level	**6**
Credits Earned	**25**

Code	NOS Module Name	No. of Hrs	Credits Earned
VLSI05N01	VLSI Digital Integrated Circuits	60	2
VLSI05N02	VLSI System Design	60	2
VLSI05N03	VLSI DSP	60	2
VLSI06N01	Introduction to Scripting	120	4
VLSI05N04	Hardware Description Language	120	4
VLSI06N04	Data Verification	180	6
	On the Job	150	5
	Total	750	25

ADVANCED ESDM WORKFORCE DEVELOPMENT

Course Name	**Design for Testing (DFT) (Short-term)**
Min Qualification	**BTech/BE/BSc Completed**
Code	**VLSI03**
NSQF Level	**6**
Credits Earned	**25**

Code	NOS Module Name	No. of Hrs	Credits Earned
VLSI05N01	VLSI Digital Integrated Circuits	60	2
VLSI05N02	VLSI System Design	60	2
VLSI05N03	VLSI DSP	60	2
VLSI06N01	Introduction to Scripting	120	4
VLSI05N04	Hardware Description Language	120	4
VLSI06N05	Design for Testing (DFT)	180	6
	On the Job	150	5
Total		750	25

Course Name	**RTL Synthesis & Static Timing Analysis (Short-term)**
Min Qualification	**BTech/BE/BSc Completed**
Code	**VLSI04**
NSQF Level	**6**
Credits Earned	**19**

Code	NOS Module Name	No. of Hrs	Credits Earned
VLSI05N01	VLSI Digital Integrated Circuits	60	2
VLSI05N02	VLSI System Design	60	2
VLSI05N03	VLSI DSP	60	2
VLSI06N01	Introduction to Scripting	120	4
VLSI06N06	RTL Synthesis	60	2
VLSI06N07	Static Timing Analysis	60	2
	On the Job	150	5
Total		570	19

ADVANCED ESDM WORKFORCE DEVELOPMENT

Course Name	**VLSI Physical Design (Short-term)**
Min Qualification	**M.Tech Completed / Ph.D. 2nd year**
Code	**VLSI04**
NSQF Level	**7**
Credits Earned	**19**

Code	NOS Module Name	No. of Hrs	Credits Earned
VLSI05N01	VLSI Digital Integrated Circuits	60	2
VLSI05N02	VLSI System Design	60	2
VLSI05N03	VLSI DSP	60	2
VLSI06N01	Introduction to Scripting	120	4
VLSI06N07	Static Timing Analysis	60	2
VLSI06N08	PnR flow in PD	120	4
	On the Job	180	6
	Total	660	22

Course Name	**ASIC Design (Long-Term)**
Min Qualification	**BTech/BE/BSc Completed**
Code	**VLSI04**
NSQF Level	**6**
Credits Earned	**50**

Code	NOS Module Name	No. of Hrs	Credits Earned
VLSI05N01	VLSI Digital Integrated Circuits	60	2
VLSI05N02	VLSI System Design	60	2
VLSI05N03	VLSI DSP	60	2
VLSI06N01	Introduction to Scripting	120	4
VLSI05N04	Hardware Description Language	120	4
VLSI06N04	Data Verification	180	6
VLSI06N05	Design for Testing (DFT)	180	6
VLSI06N06	RTL Synthesis	60	2
VLSI06N07	Static Timing Analysis	60	2
VLSI06N08	PnR flow in PD	120	4
VLSI06N09	Sign-Off Methods and Tapout Process	120	4
	On the Job	360	12
	Total	1500	50

THANK YOU