Digital system design at IIT Bombay

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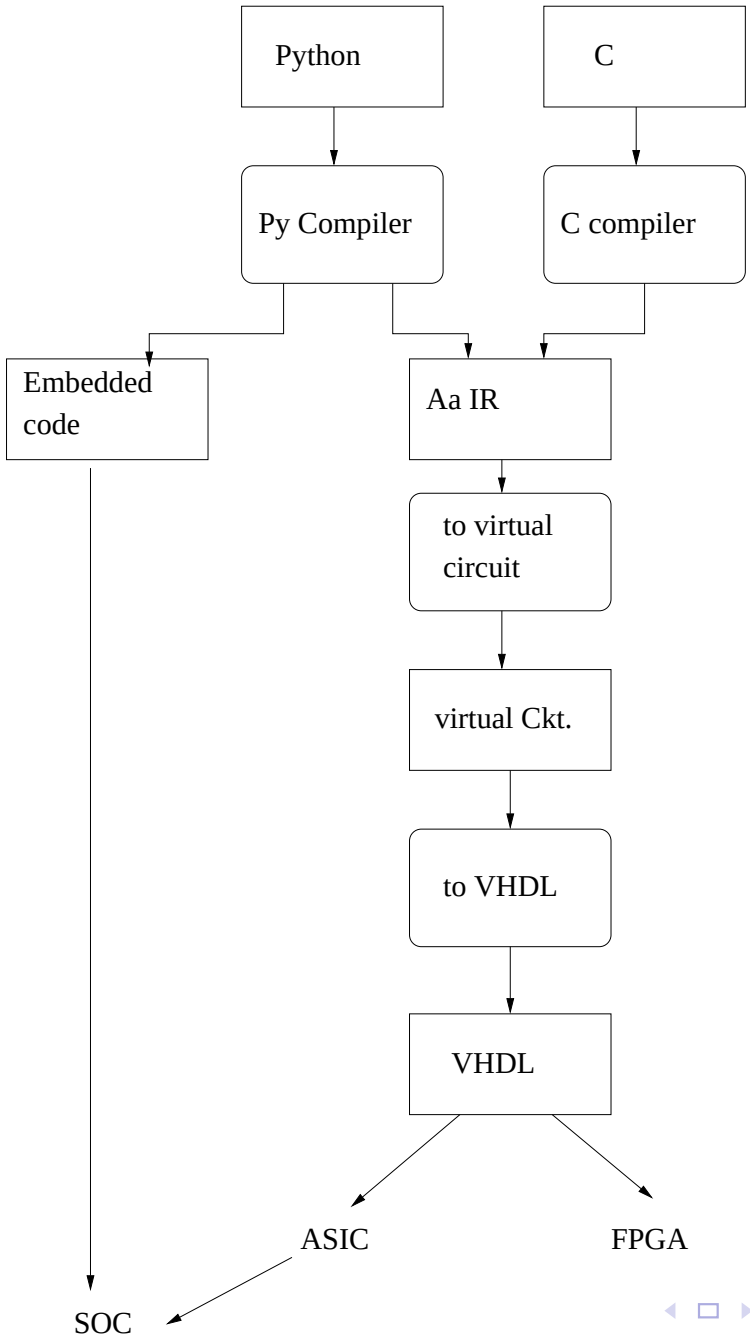
Overview

- Tools:
  - High level algorithm to hardware synthesis.
  - C to VHDL, Python to VHDL.
  - Have been used to design several successful and complex systems.
- System realizations:
  - 32-bit, 64-bit, multi-core processor systems.
  - Used in NAVIC system on chip realization (65nm).
  - Currently being used to develop secure processors and embedded systems, high performance accelerators.

High level algorithm to to hardware



Systems: AJIT processor

- Sparc V8 RISC ISA.
- General purpose, with FPU, MMU, L1, L2 caches.
- Single core, dual core, quad core.
- Single/Dual threaded cores.
- Silicon proven: 180nm SCL, 65 nm (UMC, via Europractice).

Systems: NAVIC SOC

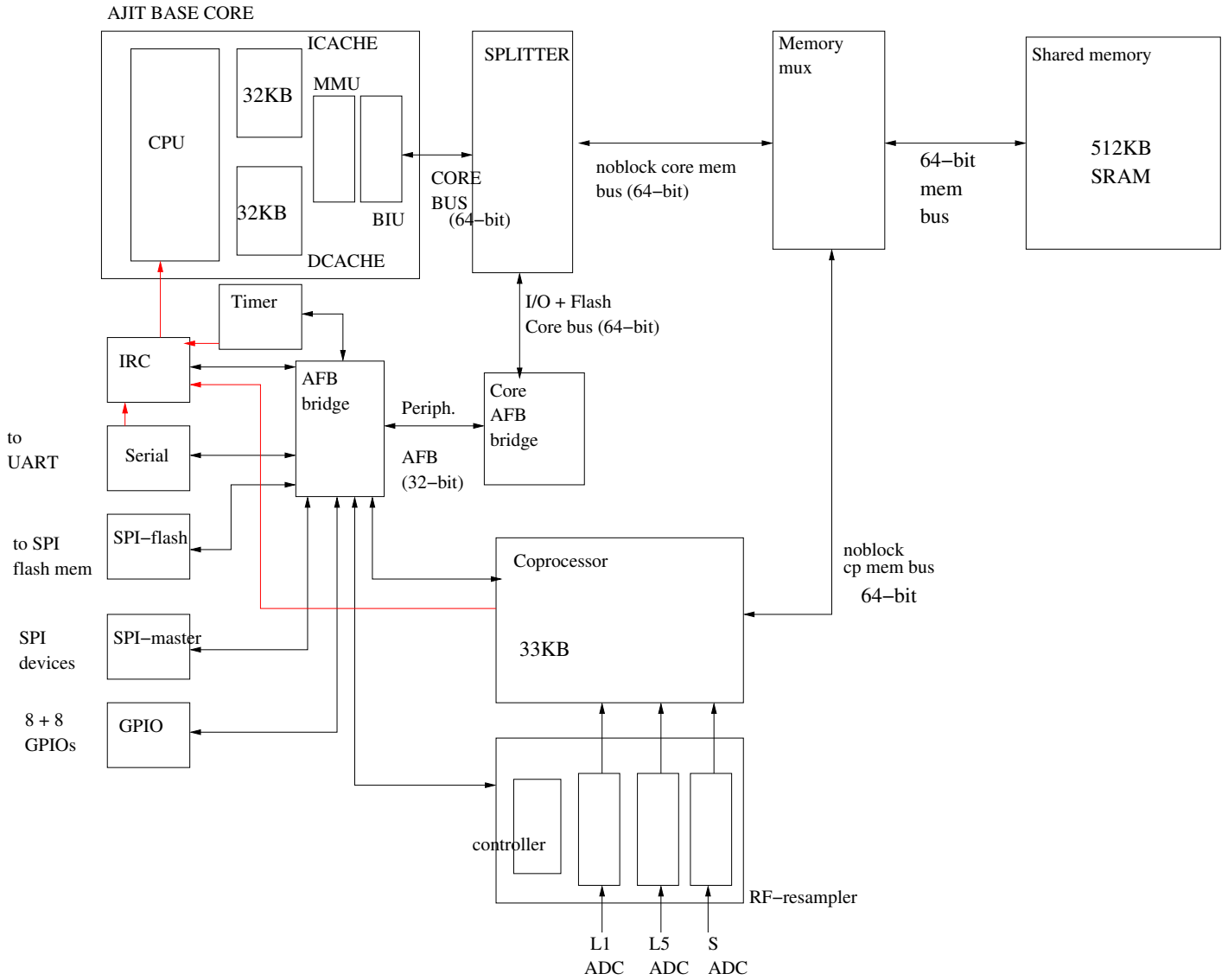


Figure: NAVIC SOC block diagram

Systems: NAVIC SOC

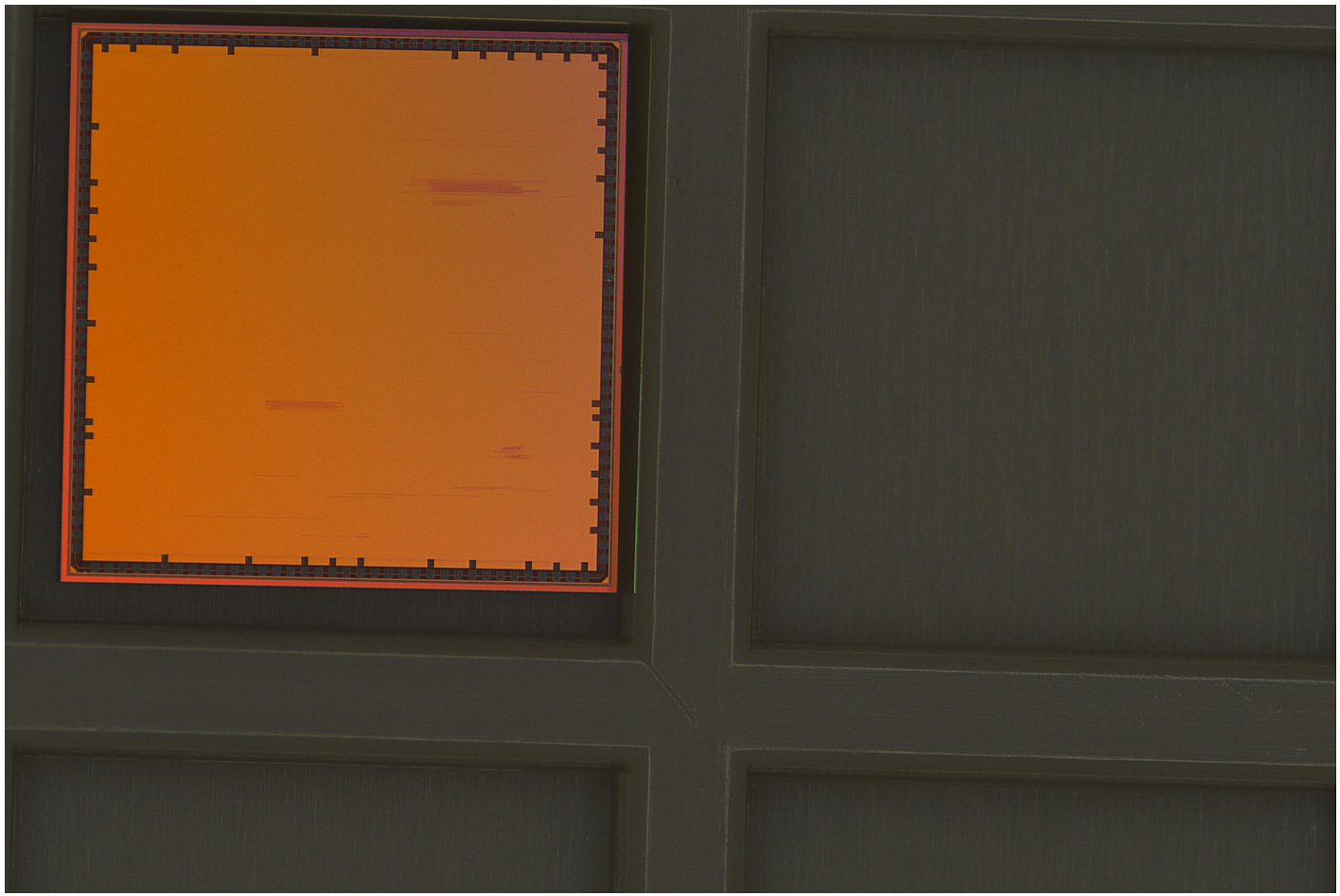


Figure: NAVIC SOC die: fabricated at UMC 65 nm, via Europractice.

Ongoing work

- Algorithm to SOC tool-chain.
- Secure processors.
- High performance embedded systems.
  - many-core.
  - integrated accelerators.