

# Towards Sustainable electronic

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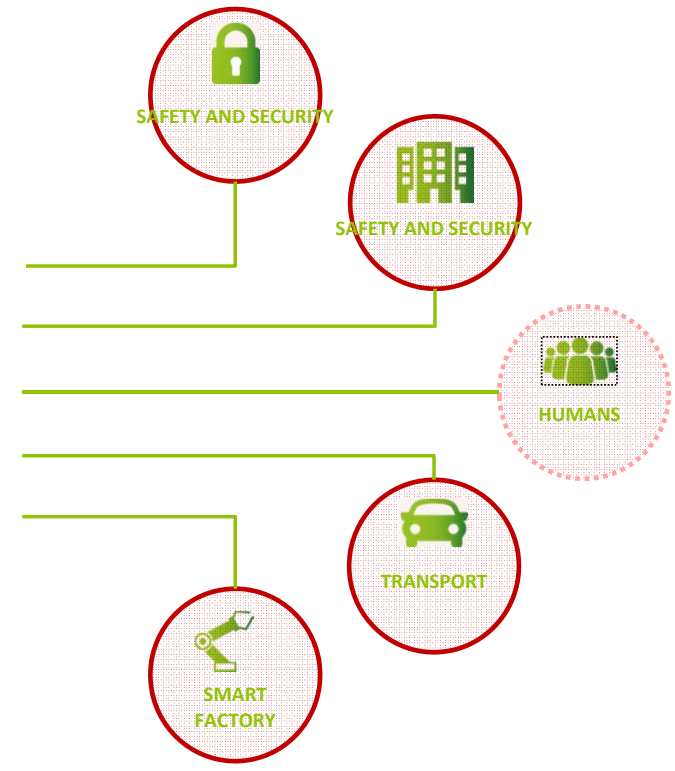
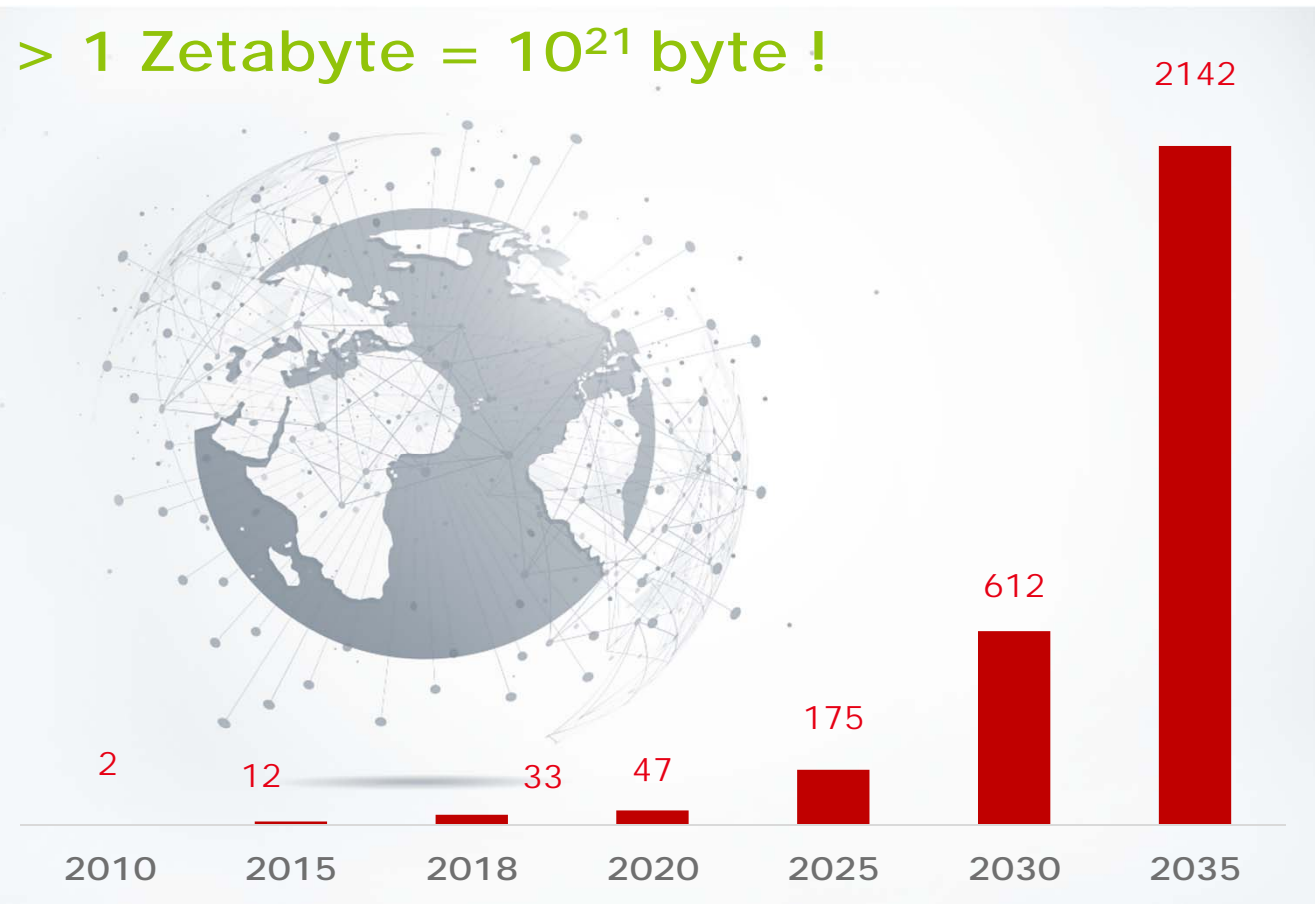


# Outline

- **Context**
- What means Sustainable Electronic?
- How to address Sustainability during manufacturing?
- How to achieve “greener” IC’s (during design, choice of technology?...)

# Global data generation (actual & forecast)

> 1 Zetabyte =  $10^{21}$  byte !



> A true data deluge, not only generated by humans!

# Planetary boundaries not be exceeded



## Climate

- Tipping points, future climate stability, warming of the planet
- Paris agreement (1.5°C), 2030 – 70%, 2050 – 100%



## Non-toxic environment

- Chemical pollution, particles, plastics
- Human health-based targets for pollution levels (food, environmental exposure)



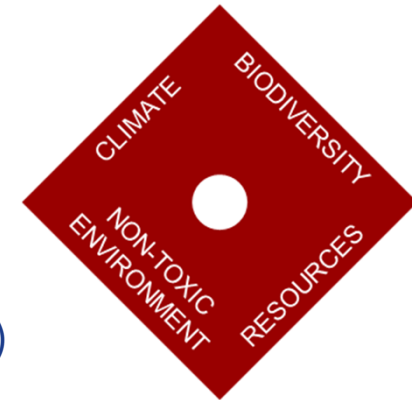
## Resources

- Availability of resources for current and future generations
- Renewable and non-renewable resources, occupation and dissipation



## Biodiversity

- Sixth mass extinction, loss of genetic and functional diversity and ecosystem functioning
- Land use, water use, nutrients, ecotoxicity, ... – targets based on ecosystem thresholds



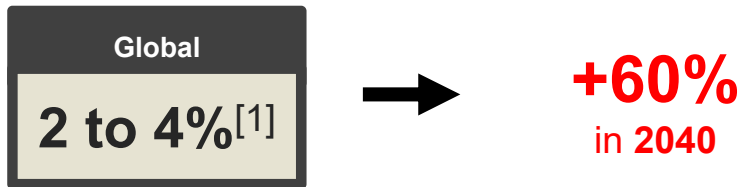
Today **seven out of the nine** boundaries **have been transgressed.**

<https://www.stockholmresilience.org/research/planetary-boundaries.html>

# Growing environmental impacts of ICT

2019, 34 billions of devices ~ 8 devices/user

- Share of ICT in Greenhouse gases emissions :



Main environmental impacts from :

- manufacturing phase (especially for impact on minerals and metals resource use)
- Use phase (electricity consumption)

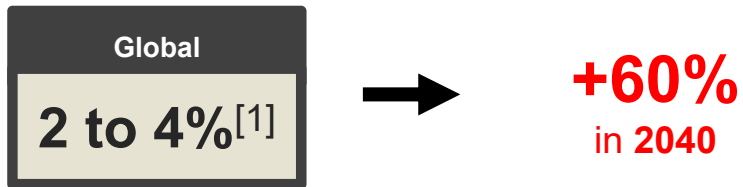
[1] Bordage, F. (2019). The environmental footprint of the digital world. *GreenIT: France*.



# Growing environmental impacts of ICT

2019, 34 billions of devices ~ 8 devices/user

- Share of ICT in Greenhouse gases emissions :



- E-waste is the fastest growing waste category
- Growing number of ‘critical raw materials’ (CRM) for the EU economy [2]

Ex: Gallium

- High Supply Risk
  - High ultimate reserves but low annual production
  - Europe imports 71% of Ga from China
- Economic Importance

[1] Bordage, F. (2019). The environmental footprint of the digital world. *GreenIT: France*.



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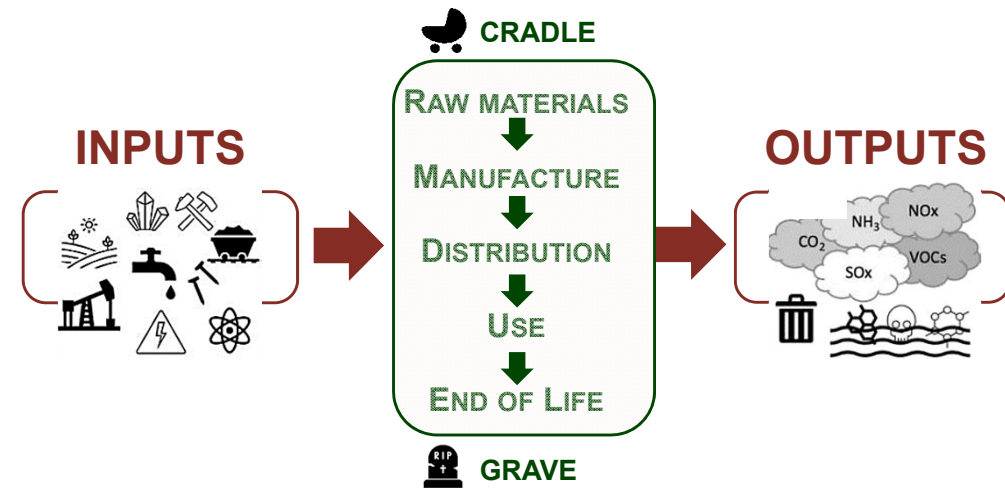
- **Reducing each device/technology footprint (towards « greener » devices):**

- Ecodesign to lower the impacts during manufacturing, use phase, end of life
- One of the tools: **Life Cycle Assessment (LCA)** to identify the hotspots

- EF 3.1 impact method



**Product Environmental Footprint (PEF)**





# Absolute sustainability



- Energy or resources savings initially planned thanks to a new greener technology can be partially or totally compensated by behavioral or other systemic response (rebound effect).
- To be sustainable, the environmental impacts of electronics should stay below the planetary boundaries.
- Reduction of the number of devices, with increased lifetime (towards a more circular economy) is necessary
- Sharing economy
- Repair & reduction of material and software obsolescence
- Refurbishing / Reuse

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## ❖ Life Cycle Inventory (LCI):

- High electricity consumption

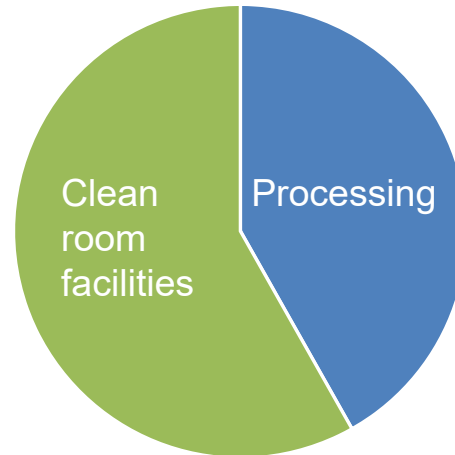
Manufacturing of a 200mm GaN on Si wafer with MOSc-HEMT transistors in CEA-Leti clean room [1]:

### Processing

286 kWh of electricity,  
0.6 m<sup>3</sup> of deionized water  
and 61 kg of chemicals

### Clean room facilities

342 kWh of electricity,  
9.8 m<sup>3</sup> of process cooling water  
and 2.8 kg of natural gas



## ❖ Life Cycle Assessment (LCA):

### Large impacts on

- Ressource use, fossils (MJ)
- Ionizing radiation (kBq U-235 eq)

*In case of French electricity mix, high share of nuclear*

- Climate change (kg CO<sub>2</sub> eq)

- Ressource use, minerals and metals (kg Sb eq)

*Electricity distribution and transmission network (copper)*



[1] Vauche, L.; Guillemaud, G.; Lopes Barbosa, J.-C.; Di Cioccio, L. Cradle-to-Gate Life Cycle Assessment (LCA) of GaN Power Semiconductor Device. *Sustainability* **2024**, *16*, 901.

# Process and Material hotspots

## ❖ Life Cycle Inventory (LCI):

- Direct emissions into air of fluorinated (PFC) gases with high Global Warming Potential (GWP)

Dry etch steps for FDSOI 28nm technology, 300mm [1]:

- CF4 weak abatement rate + GWP x6,600
- NF3 using in chamber conditioning at each step

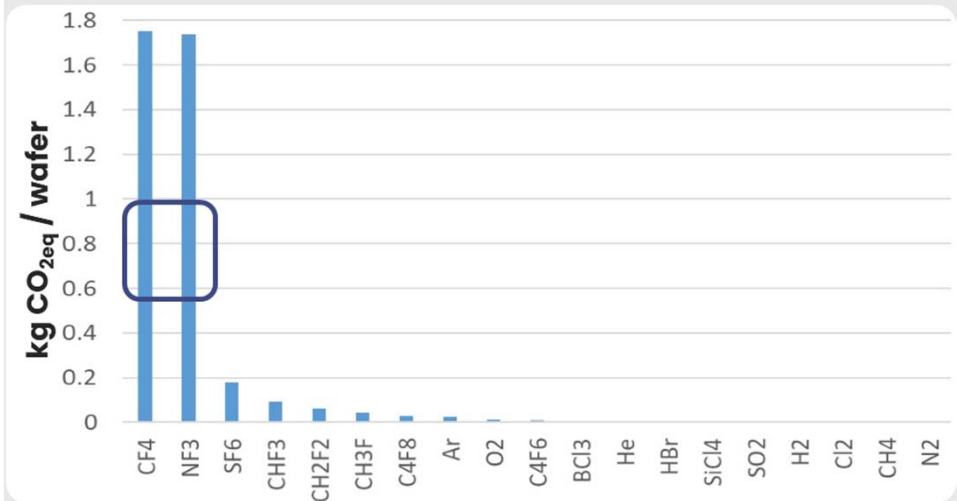
## ❖ Life Cycle Assessment (LCA):



### Large impacts on

- Climate change (kg CO<sub>2</sub> eq)

7 dry etch processes (FEOL & MEOL **FDSOI 28nm**)



[1] Renaud M, Sarrazin A, Lopes-Barbosa J, Rivoira Y, Servin I, Boulard F. Life cycle assessment of etching processes for FDSOI transistors technologies. In Advanced Etch Technology and Process Integration for Nanopatterning XIII 2024 Apr 9 (Vol. 12958, pp. 141-151). SPIE.

## ❖ Life Cycle Inventory (LCI):

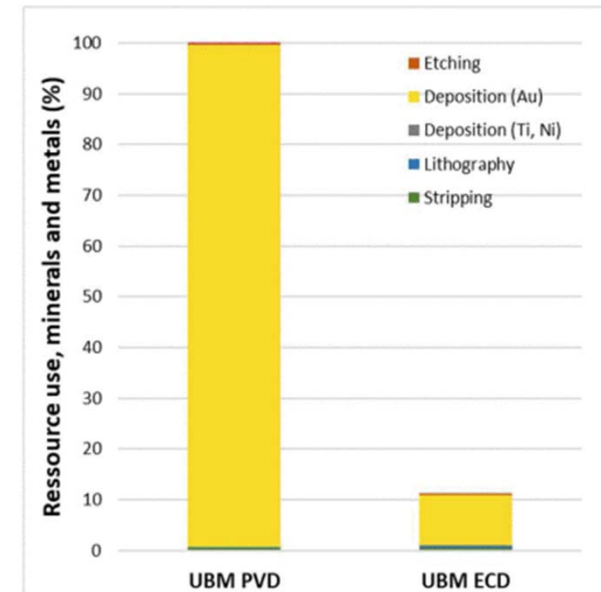
- Consumption of Gold Metal

Gold metal  
by Physical Vapor Deposition or  
by Electrochemical Deposition for  
metallizations [1]

## ❖ Life Cycle Assessment (LCA):

### Large impacts on

- Resource use, minerals and metals (kg Sb eq)



<sup>[1]</sup>S. Guillou *et al.*, "Comparative Life Cycle Analysis of Redistribution Layer for 3D Integrations," *2024 Electronics Goes Green 2024+ (EGG)*, Berlin, Germany, 2024, pp. 1-11, doi: 10.23919/EGG62010.2024.10631207.er

# Manufacturing | 4 major work areas

1

## INFRASTRUCTURE

### Energy efficiency

- ✓ Certification ISO 50001
- ✓ Energy management system

### Water efficiency

- ✓ Reclaim & re-use

### Effluent treatment

- ✓ controls / regulations
- ✓ Segregation / Recycling

- Gas re-use

2

## EQUIPEMENTS

### Optimizing parameters

- ✓ flow rate
- ✓ mode idle

### Powerful abatement systems

- GHG emissions reduction with high destruction removal efficiency
- With limited additional consumption of water, gas, electricity

3

## PROCESS

### GWP gas alternatives

- ✓ Cleaning of deposition or plasma etching chambers
- ✓ PFCs replacement (CF<sub>4</sub>, NF<sub>3</sub>, SF<sub>6</sub>,...)

### Tailor to your needs

- ✓ For each process/technology
- ✓ Volume, time

### Effluents waste

- ✓ CMP (flow rate, novel slurry)
- ✓ GRINDING : filters

4

## MATERIALS

### 5Rs scenarii

- ✓ Replace classified chemicals (CMR, REACH...) Ex: TMAH, PFAS...
- ✓ Recycle PVD targets (Au), chemicals, etc.
- ✓ Reduce PFCs gases
- ✓ Replace by alternatives
- ✓ Rationalise Si wafers



Developing initiatives to reduce our **environmental impacts**  
**Eco-score** calculation within complete digitalization of our cleanrooms

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## Post-etch polymer removal

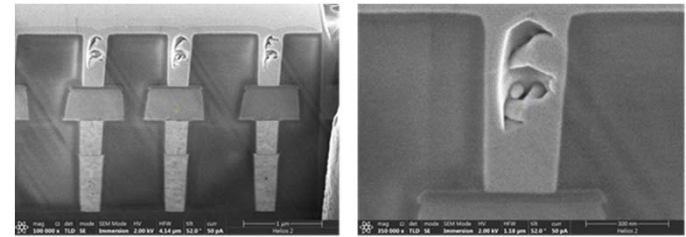
- With toxic-free compounds

- Reduced toxicity vs POR chemistry
  - REACH compliant (no CMR, without cathecol and hydroxylamine)
- Reduced carbon footprint
  - Lower temperature process (<50°C)
  - Reclaim mode and recyclability potential
  - Without IPA rinsing (if possible)
- Secure and sustainable sourcing
- Similar process performances
- Life cycle assessment (POR versus new chemistry)

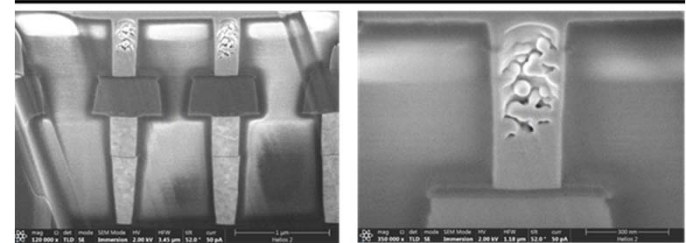
*In progress : evaluation of the selected chemistry at the pilot line of CEA Leti*

**Application: metal post-etch  
Both 200 mm / 300 mm**

**POR**



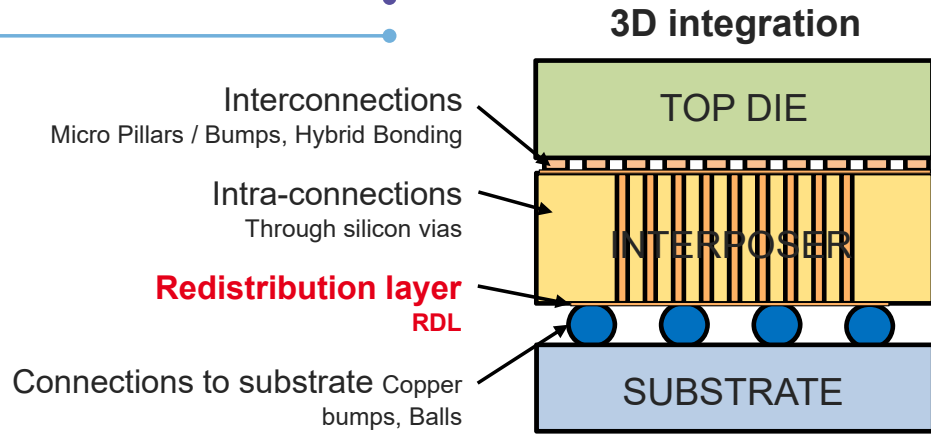
**Without CMR**



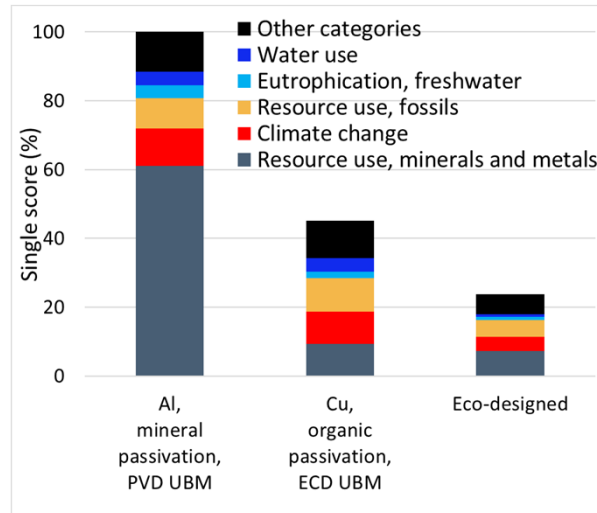
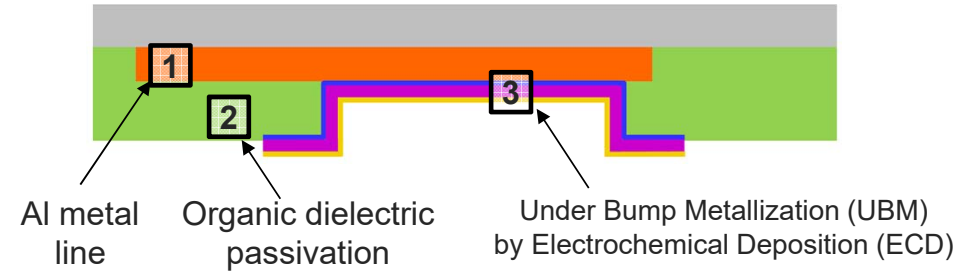
*M. Stigliani et al. PESH, June 2024  
Development of a sustainable post plasma-etch residues cleaning solution*

**Similar process performances**





### Schematic cross-section of a eco-designed redistribution layer

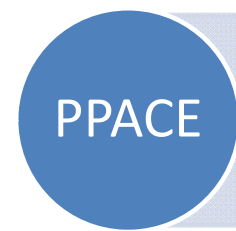
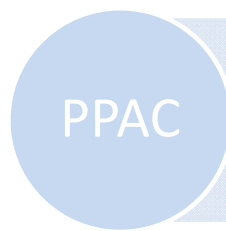


- ✓ **LCA single score clearly shows environmental benefits** in comparison with 2 state-of-the-art reference integrations : **reduction of 50-75% of the impacts**
- ✓ **Electrically valid** (leakage current, sheet resistance) initially & after JEDEC humidity storage and temperature cycling

S. Guillou *et al.*, "Comparative Life Cycle Analysis of Redistribution Layer for 3D Integrations," 2024 *Electronics Goes Green 2024+* (EGG), Berlin, Germany, 2024,

# IC design improvement

## Multi-criteria optimization



Environmental impact assessment and interpretation of results



Library of components

**LCA dynamic e-score platform**



**MES (Manufacturing Executive System)**

Process integration data

Equipment used

Process flow

Local Inventory



EU – INDIA – Joint Researchers Workshop on Semiconductors  
Olivier FAYNOT | CEA-Leti

Real measurements

Bottom-up estimation

Top-Down Allocation

Process, Equipment, Clean Room and Treatments data



# Reduce IC manufacturing footprint: *GENESIS* project

- **Consortium**
  - 63 partners from 12 pays – CEA-Leti coordinator
  - Duration 3 years
  - Expected start : Q2/25 (pending EU final approval)

**Full proposal submitted  
Pending to EU final approval**

**Gas & water monitoring & abatement:** EDWARDS, ThermoFisher Scientific, PFEIFFER VACUUM, centrotherm, VOCsens, GASERA, FATHGROUP, VARIOLYTICS, TOFWERK, HQ-Dielectrics

**Materials & chemicals:** ARKEMA, MERCK, PIBond, Heraeus, LayerOne, MOLYMEM, soitec, MERSEN, TECHNIC

**Semiconductor manufacturing:** GlobalFoundries, ST, BOSCH, infineon, intel, NXO, LEONARDO AUTOMOTIVE

**Equipment:** APPLIED MATERIALS, Besi, trymax, TEL Tokyo Electron & Europe, SCHMIDT HAENSCH, SCREEN, RIXTRON

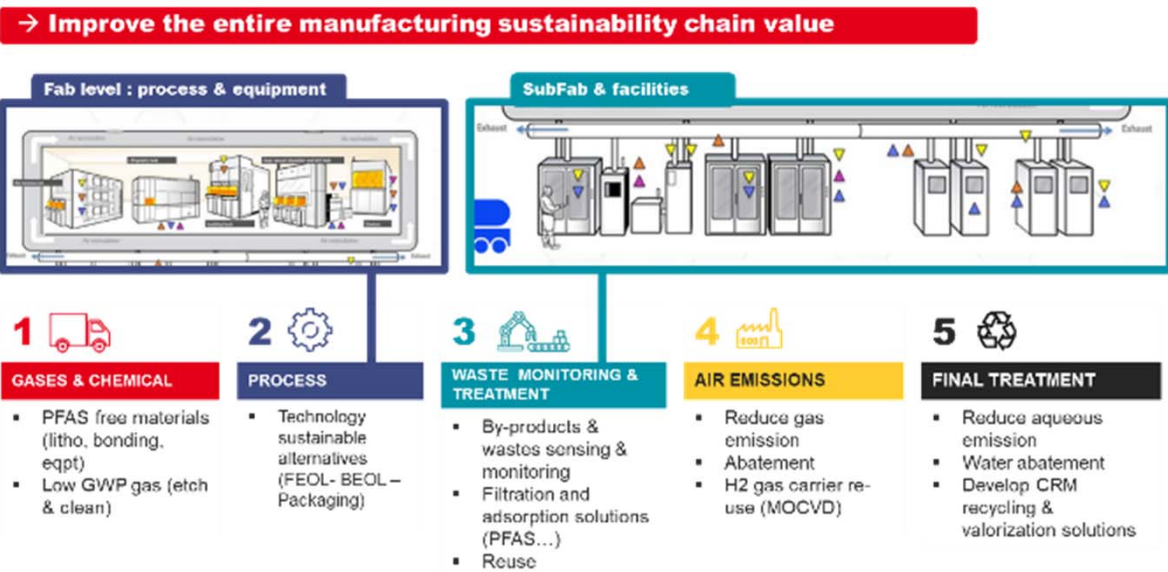
**Communication:** ArgYou.com, semi

**Recycling:** CS CLEAN SOLUTIONS, WEEECycling

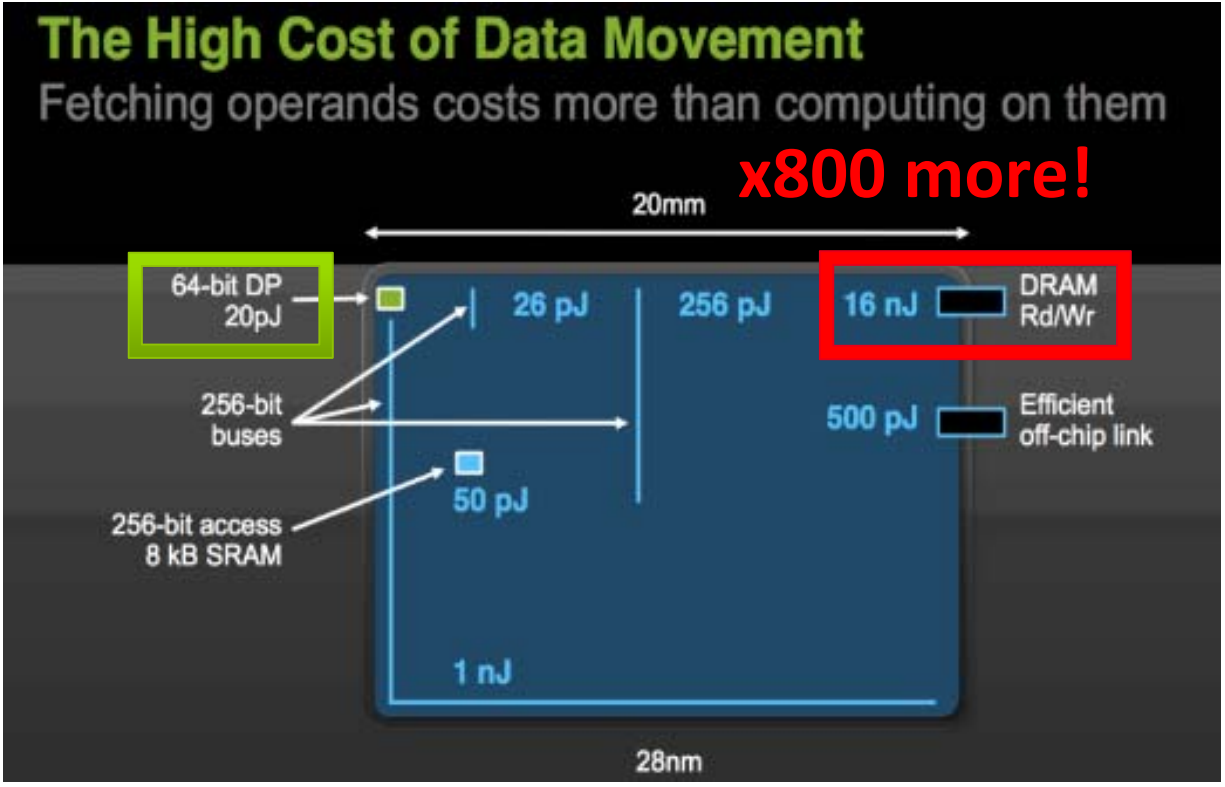
**Research:** TOR VERGATA, A?, UCLouvain, ICRA, UNIVERSITY OF LEICESTER

**RTOs:** csem, Tyndall, SINTEF, imec, TNO, Fraunhofer

**Flags:** Belgium, Finland, France, Germany, Italy, Netherlands, Norway, Spain, Switzerland, United Kingdom

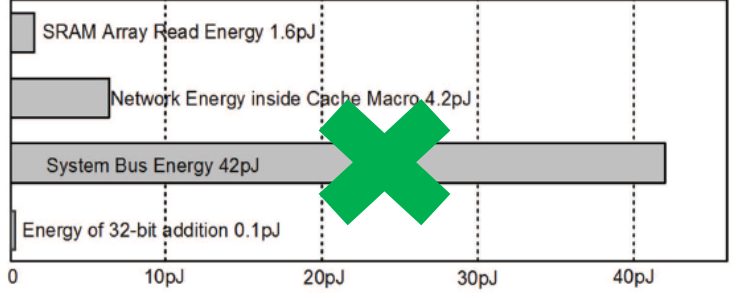


# The cost of moving data



Bill Dally, "To ExaScale and Beyond", 2010

[J. Wang – ISSCC'19]



~90% of energy is in **data transfer**  
 → IMC could lead **8x reduction**

Operation energy is negligible

Memory access and control energies dominate

A close-up, high-angle photograph of a microchip die, showing its intricate circuitry and various colored regions (blue, purple, orange, green) under a dramatic, low-key lighting scheme.

THANK YOU



EU – INDIA – Joint Researchers Workshop on Semiconductors

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**[www.icos-semiconductors.eu](http://www.icos-semiconductors.eu)**