How 3D integration can help the emergence of Power efficient innovative architectures?

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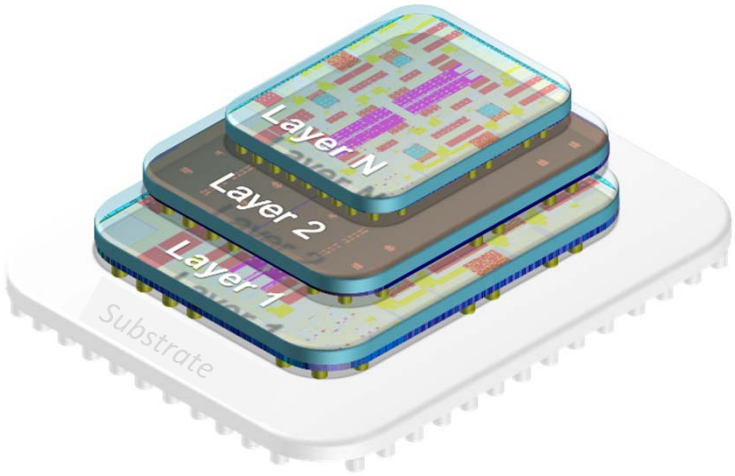
CEA-Leti

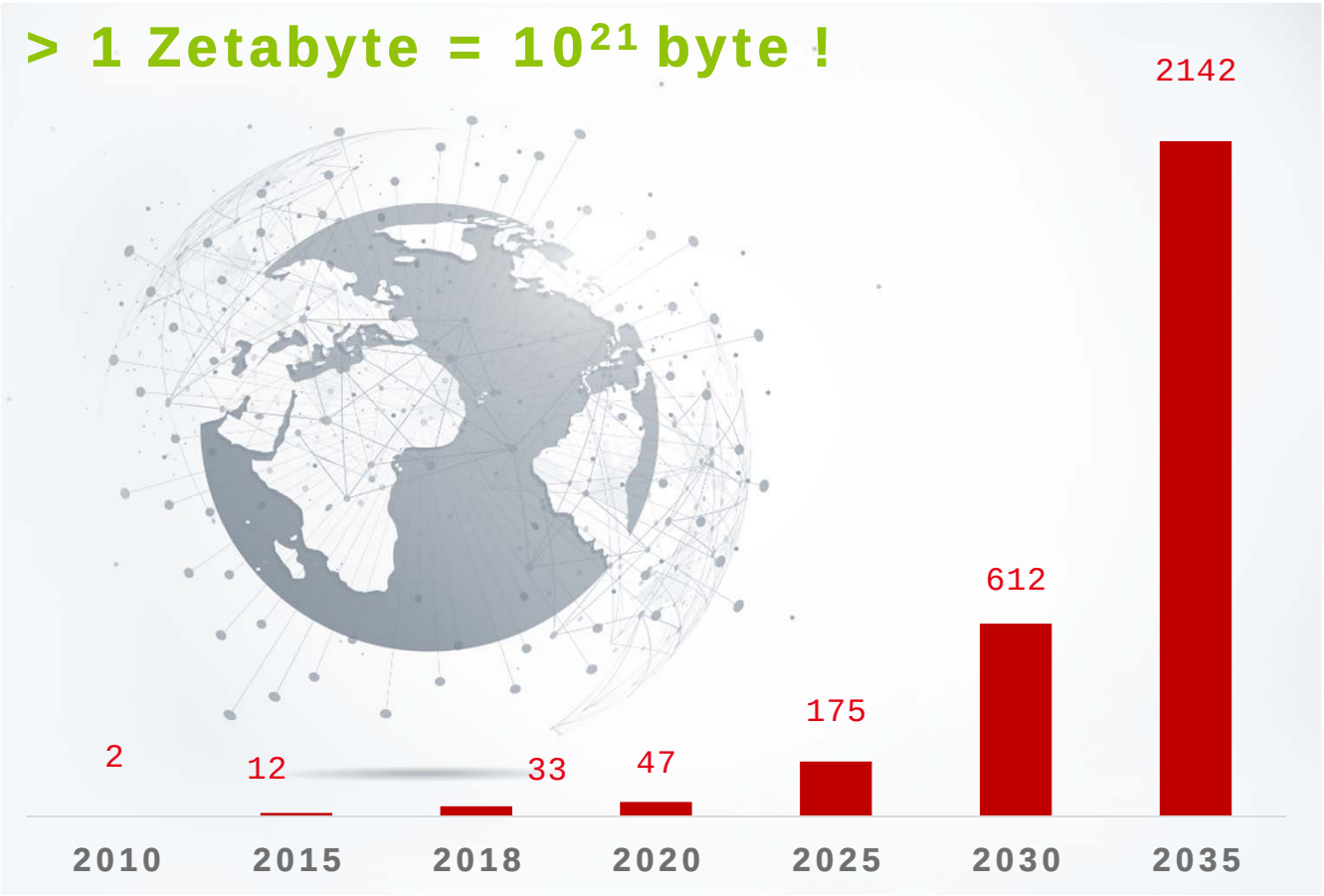
Outline

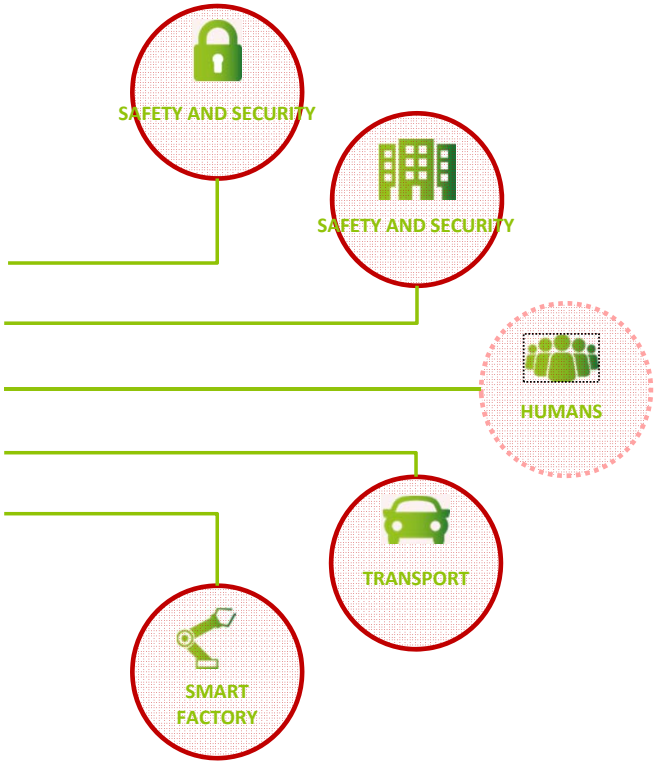


- Why going Vertical?
- 3D Integration Building Blocks
- 3D integration for innovative architectures

Global data generation (actual & forecast)

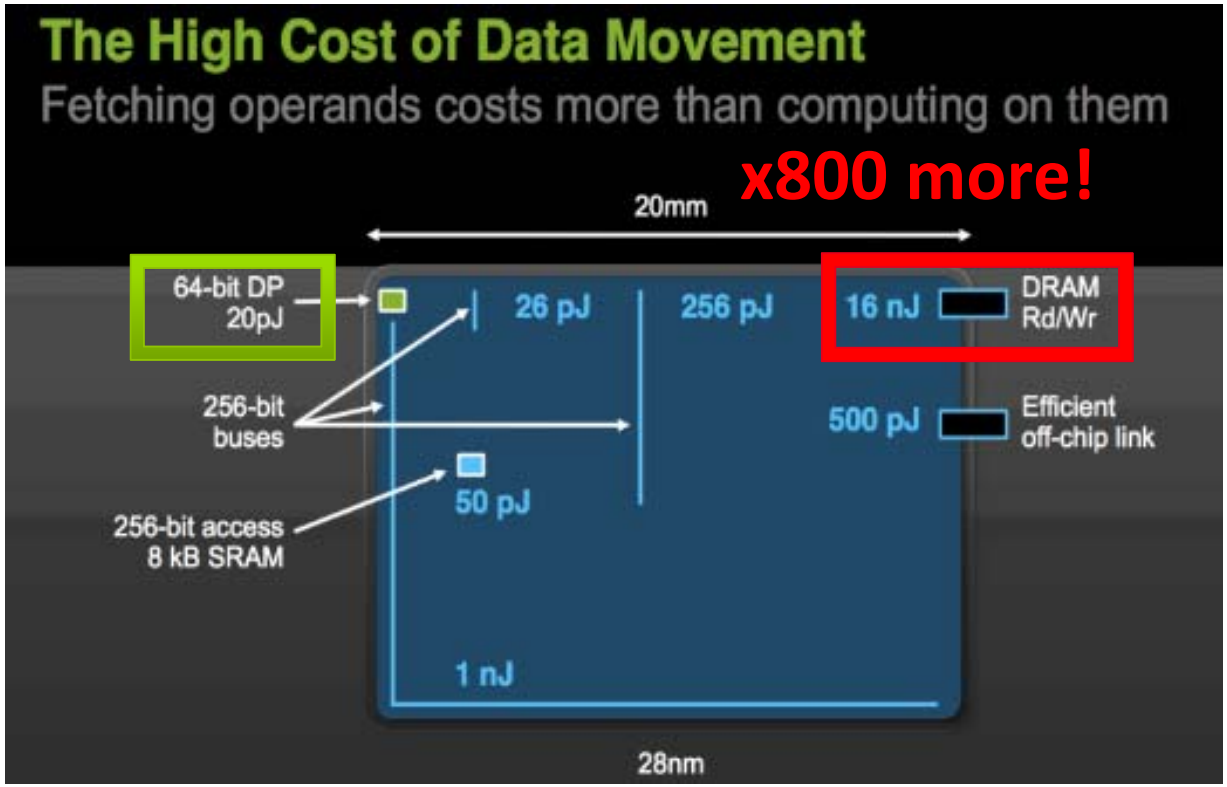
> 1 Zetabyte = 10^{21} byte !





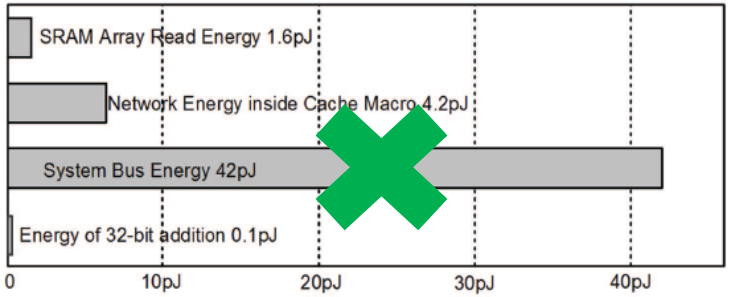
> A true data deluge, not only generated by humans!

The cost of moving data



Bill Dally, "To ExaScale and Beyond", 2010

[J. Wang – ISSCC'19]



~90% of energy is in **data transfer**
→ IMC could lead **8x reduction**

Operation energy is negligible

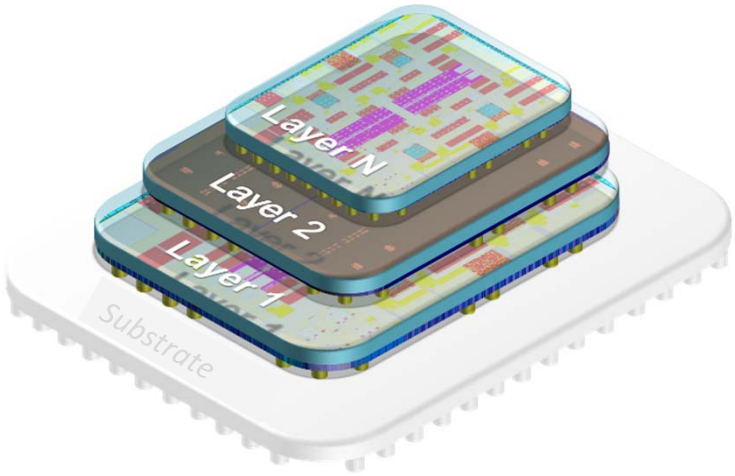
Memory access and control energies dominate

The required gain in energy efficiency

>1000x by 2030

- FEOL CMOS scaling
- Memory technologies
- Disruptive Computing
- Chiplet & 3D System

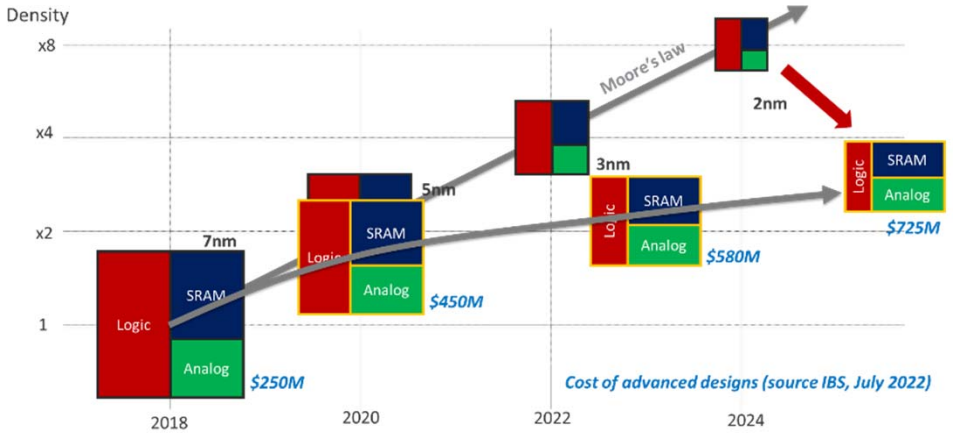
Outline



- Why going Vertical?
- 3D Integration Building Blocks
- 3D integration for innovative architectures

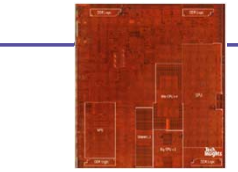
New paradigms are needed

- Interconnects Bottleneck
  - Dramatic R.C increase → strong impact on latencies
  - Gate delay << interconnects delay
- Scaling becomes costly
  - High development cost (mask, IP porting, verif…)
  - High manufacturing cost (low yield with large die)
- Heterogeneous architectures needed
  - More processing (AI, perception accelerators…)
  - More data to handle (memory capacity, fusion…)
  - Reuse of legacy (ISA, I/O interface…)
  - More modularity, scalability & sustainability

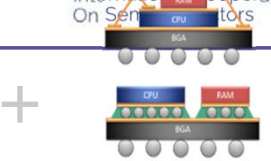


3D benefits for advanced systems

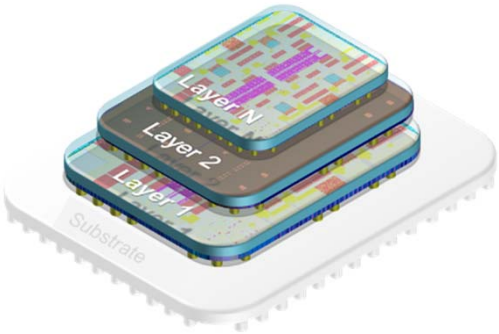
- High-performance interconnections
  - Low R, L, C → latencies, bandwidth, energy efficiency
  - Massively parallel processing with vertical links
- Answers to modern design needs
  - Reduced form factors, I/O number non limited by pad size
  - Partitioning, IP reuse, scalability & density
- Heterogeneous integration
  - Mixed CMOS nodes & materials (Si, III-V, II-VI, passives, MEMS)

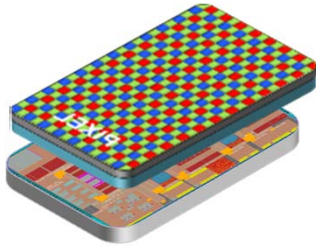


SoC performance

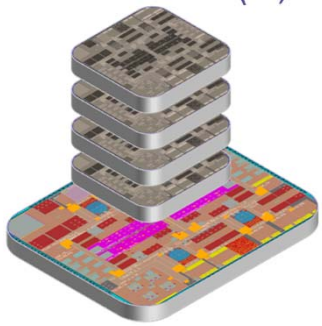


SiP benefits

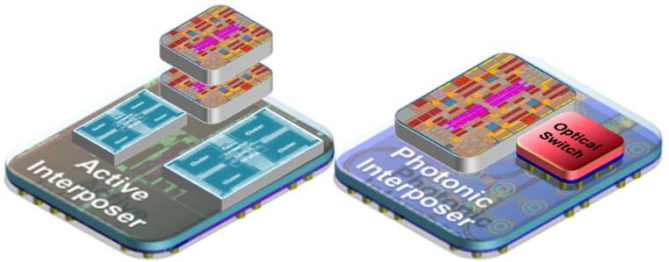




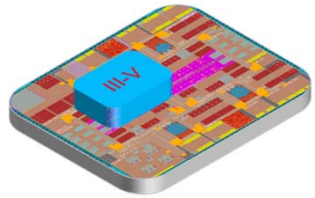
Sensor on logic



Memory on Logic

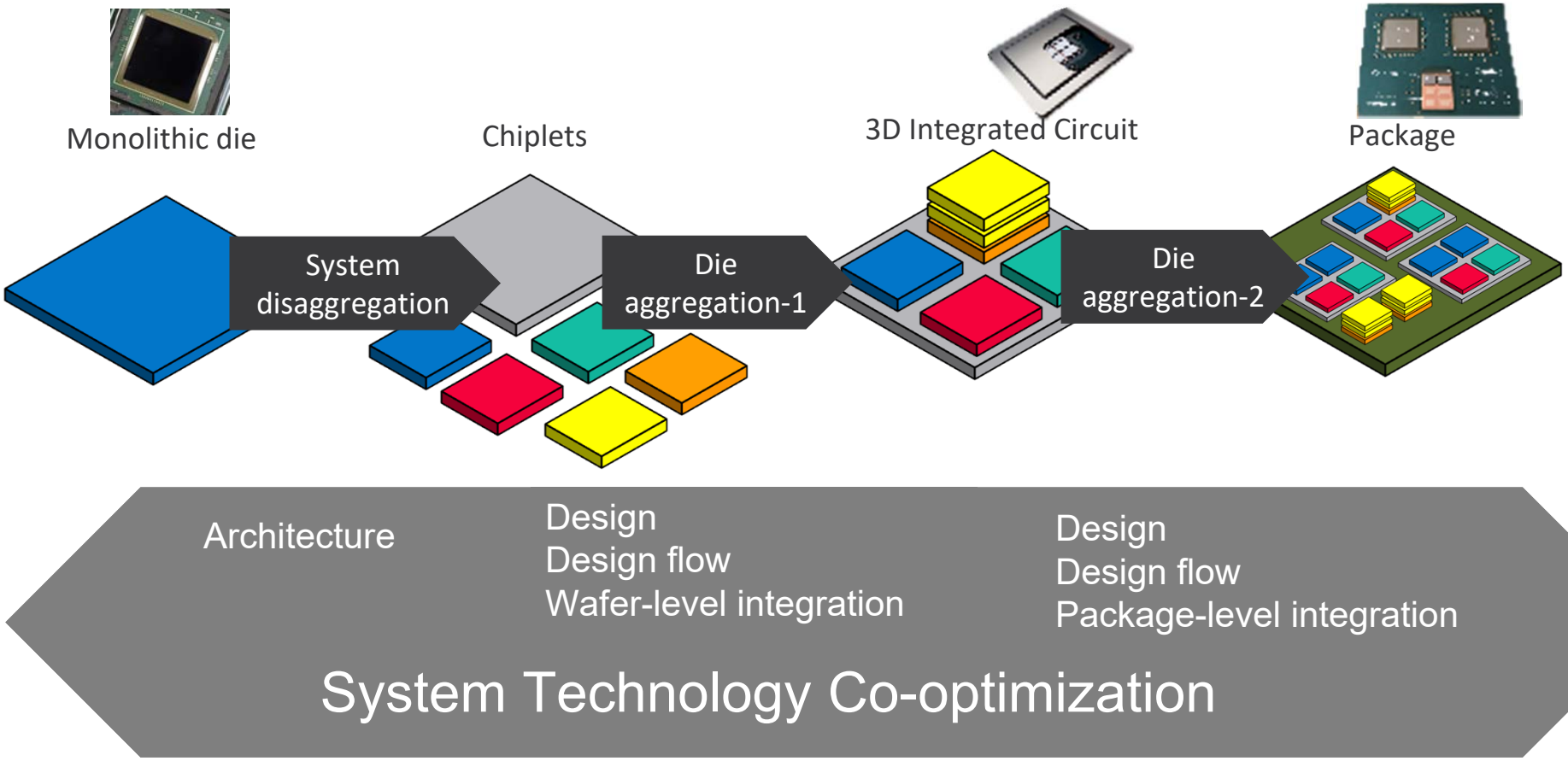


Chiplet-based integrations



III-V on Logic

Chiplets: the new IC design paradigm



Up to 100x gain on Power Efficiency with 3D

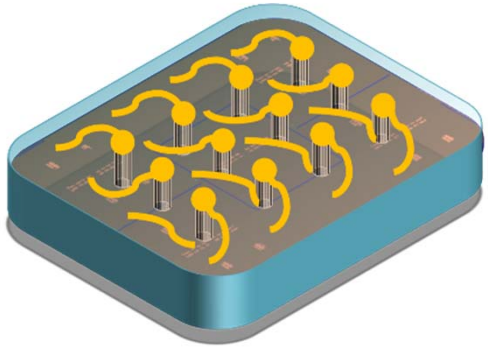
Morphology of a 3D circuit

- **Layer-to-layer vertical interconnects**

  Miniaturization trend: pillars, hybrid bonding …

- **Intra-layer vertical interconnects**

  Communication between frontside and backside of each layers
  Through silicon Vias (TSV)

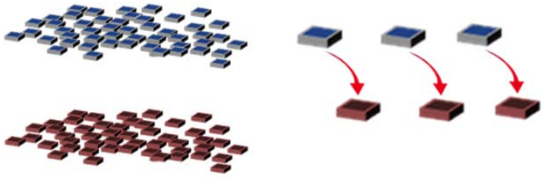


- **Intra-layer in-plane interconnects (2D)**

  ReDistribution Layers (RDL)

Assembly configurations

Die to die

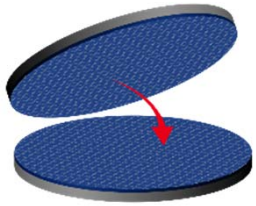


- Known Good Dies → yield
- Heterogeneous integration
- Flexible design

- Low assembly throughput
- Low alignment accuracy
- Very high cost

Pure packaging operation

Wafer to wafer

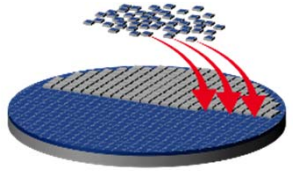


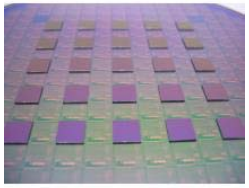
- Collective process
- High assembly throughput
- High alignment accuracy

- Yield loss
- Strong design limitation

Mass production for imagers and memories

Die to wafer





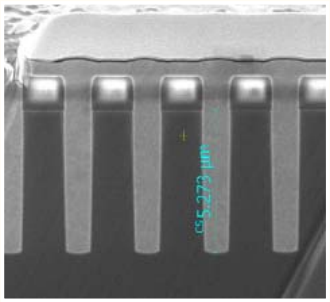
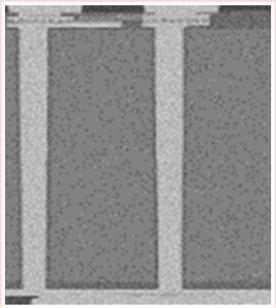
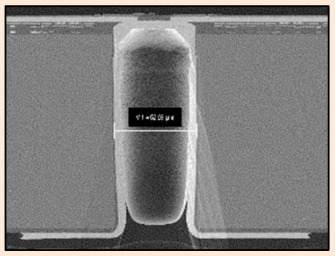
- Known Good Dies → yield
- Heterogeneous integration
- Flexible design

- Low assembly throughput
- Low alignment accuracy

Breakthrough processes needed

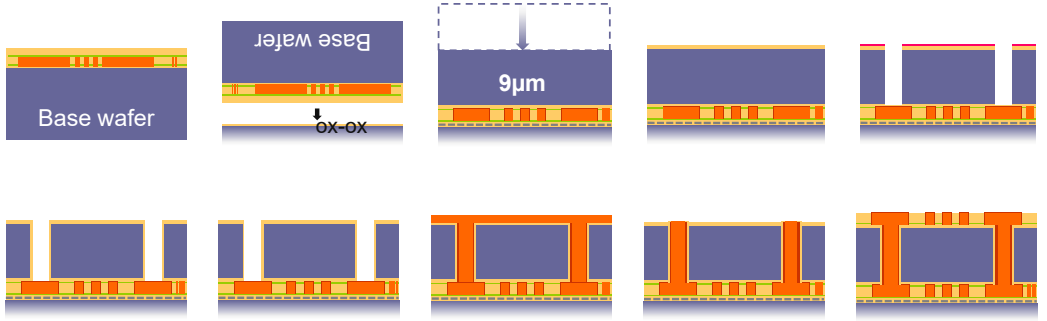
Through silicon via (TSV) technologies

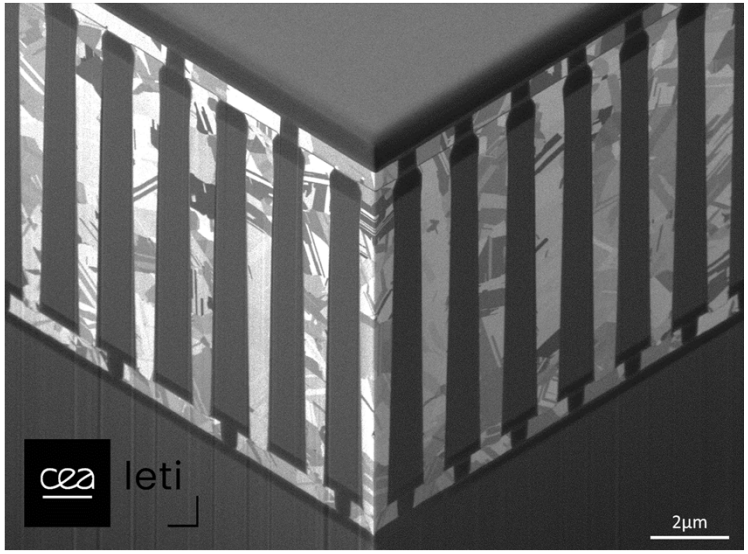
TSV pitch

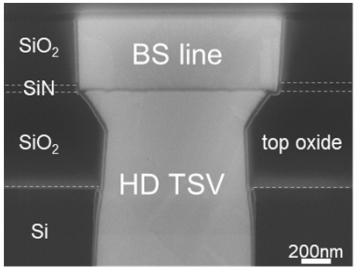
1-10 µm Ø <2 µm R_{TSV} = 0,5-1 Ω	High density TSV		100 000 TSV/mm² ➔ Logic blocs	**3D Imagers** **Displays** **Power Delivery Network**
20-50 µm Ø 2-15 µm R_{TSV} = 20 mΩ C_{TSV} = 0.1 pF	TSV middle		1 000 TSV/mm² ➔ Core/Chips	**System in Package** **Interposers / Chiplets**
100-500µm Ø 40-100µm R_{TSV} = 2-10 mΩ C_{TSV} = 2 pF	TSV last low density		100 TSV/mm² ➔ low I/O	**CMOS Image Sensors** **X-Ray focal plane arrays** **IR sensors**

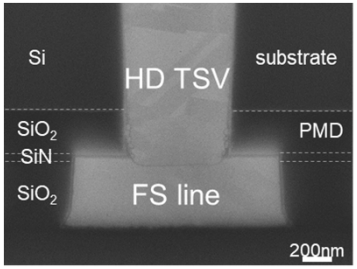
“High density TSV” (HD-TSV) process flow

- TSV done after circuit processing*
  - Diameter typically < 2µm & height <15 µm
  - Uniform silicon thinning needed (TTV < 1µm)
  - TSV fully filled with Cu

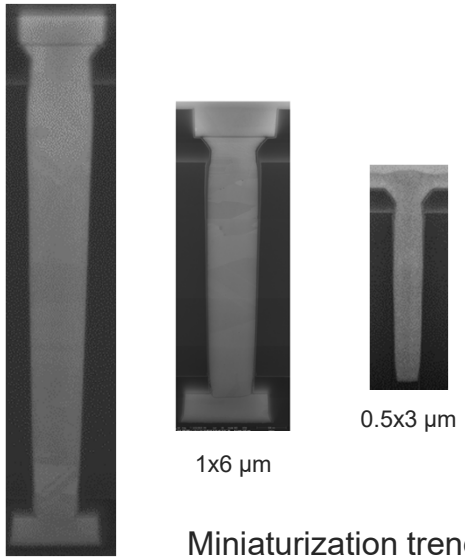




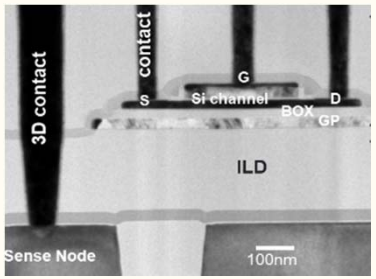
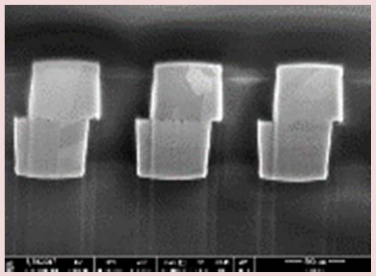
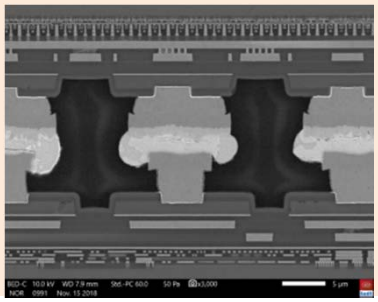




S. Borel et al., Electronic Components and Technology Conference, 2023

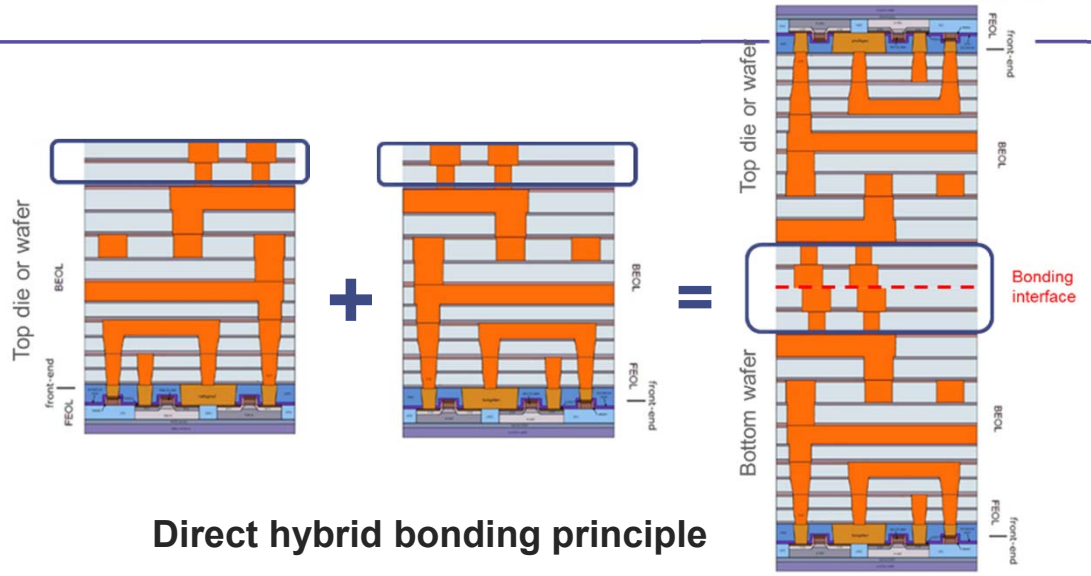


Technologies for 3D interconnects

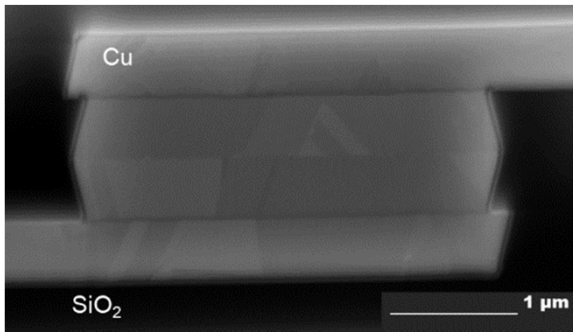
Interconnect pitch				
<100nm	Sequential 3D		10^8/mm^2 Transistor level	Wafer to Wafer
100nm-10µm	Hybrid bonding		10^6/mm^2 Logic-block level	Die to Wafer Wafer to Wafer
> 10µm	Soldering & adhesive bonding		10^3/mm^2 Circuit level	Die to Die Die to Wafer Wafer to Wafer

Direct hybrid bonding process: a hot topic !

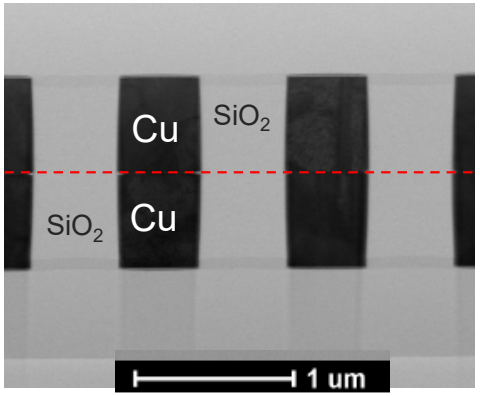
- Mix SiO_2/SiO_2 & Cu/Cu bonding
- Precautious CMP process
- Proper design rule manual
- Unprecedented benefits
- Ultra dense interconnections
- Improved mechanical strength, no organics



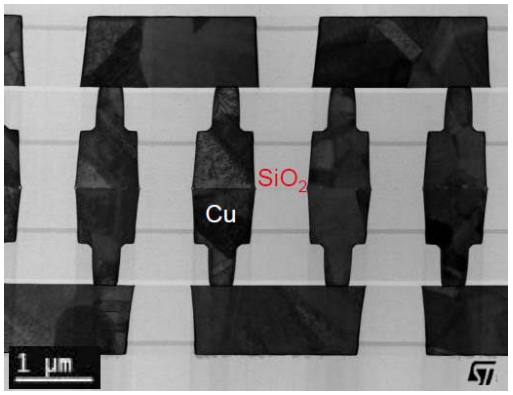
Direct hybrid bonding principle

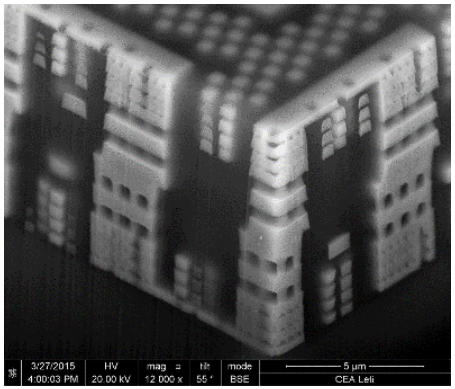


Y. Beilliard et al., IJSS, Vol. 117, June 2017, pp. 208-220



J. Jourdon et al., IEDM 2018

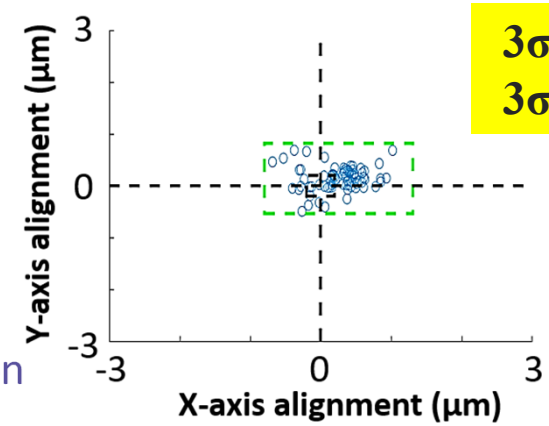


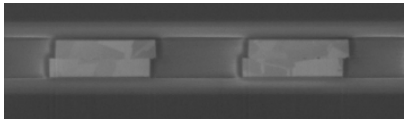


L. Millet et al., VLSI 2018

Die-to-wafer hybrid bonding

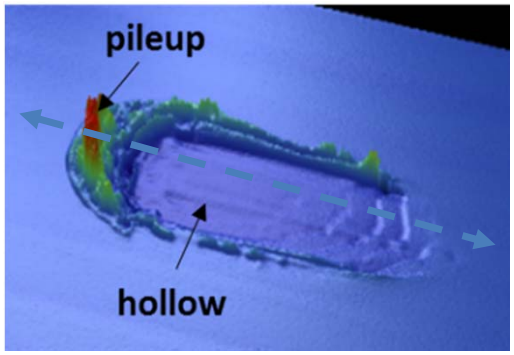
- Challenges
  - Known Good Die → test before bonding
  - Pitch reduction & multi-pitch process
  - Alignment precision & interdie space reduction





5µm interconnection pitch

A. Jouve *et al.*, 3DIC, 2019

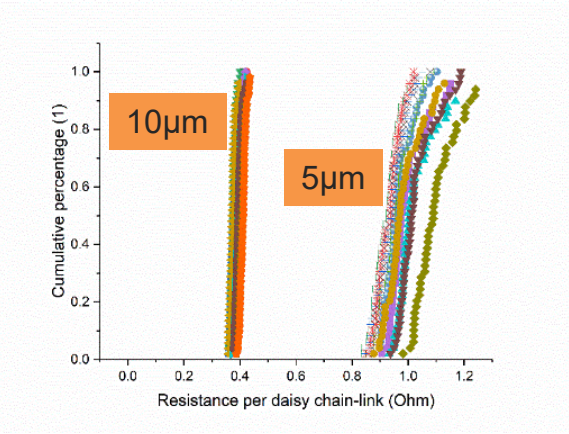


E. Bourjot *et al.*, ECTC 2021

40µm inter-die spacing

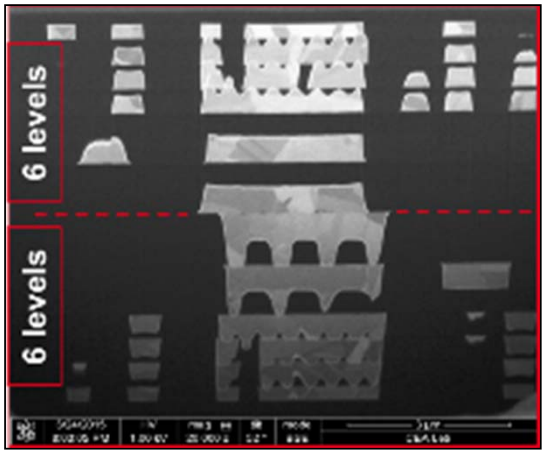
4 x 5 mm² | 3 x 3 mm² | 3 x 3 mm² (post thinning)

P. Metzger et al., Minapad forum 2022

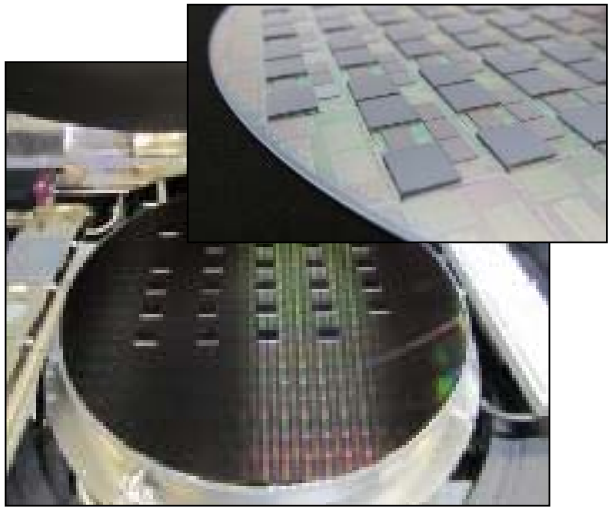


E. Bourjot et al., « Towards a Complete Direct Hybrid Bonding D2W Integration Flow: Known-Good-Dies and Die Planarization Modules Development », 3DIC
E. Bourjot et al., "Known Good Dies (KGD) strategies compatible with D2W Direct Hybrid bonding", MAM 2020
E. Bourjot et al., « 10µm and 5µm die-to-wafer direct hybrid bonding », in 2022 ESTC, sept. 2022.

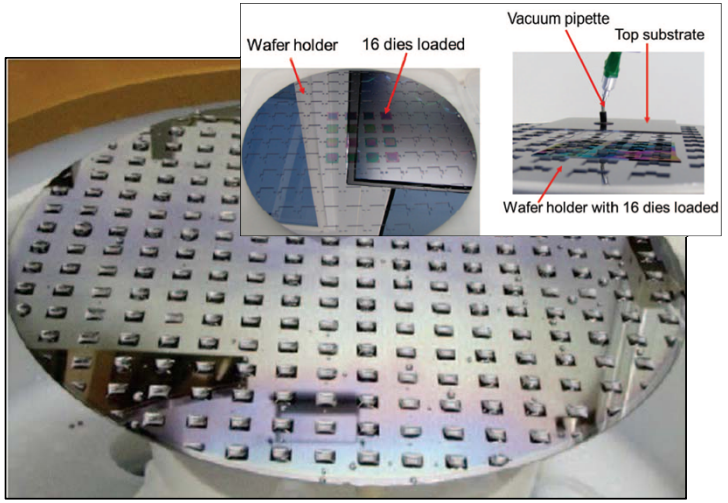
Hybrid Bonding Solutions



- Direct bonding of metal and dielectric
- Down to 1 micron pitch interconnects



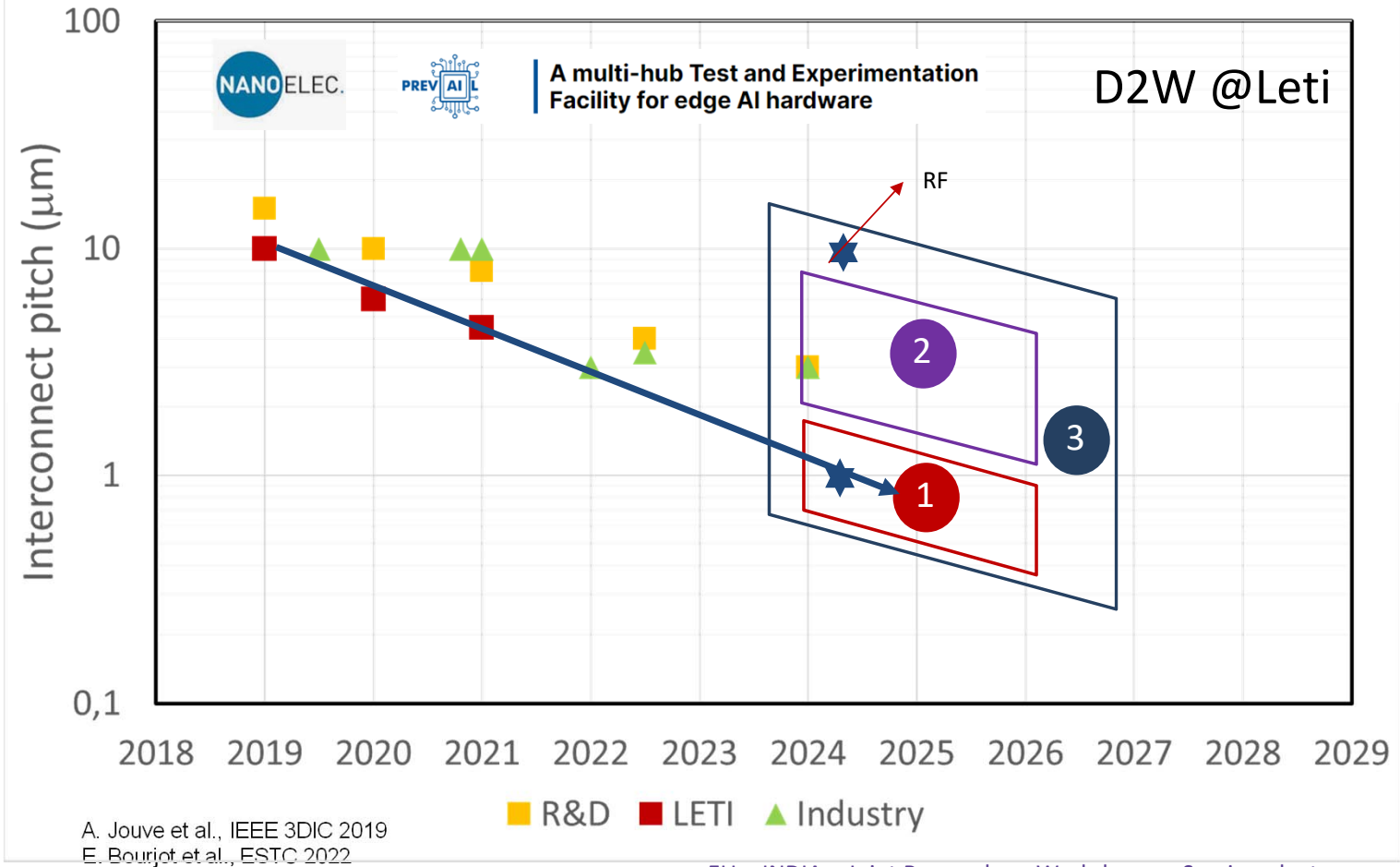
- Wafer-to-wafer (W2W) or Die-to-wafer (D2W) technologies
- High heterogeneity allowed by D2W



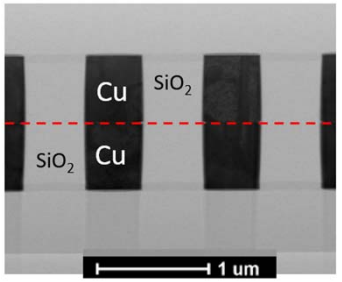
- Collective D2W approaches
- Self-assembly for high precision & high throughput

Hybrid bonding pitch roadmap

Pitch down to 1µm



A. Jouve et al., IEEE 3DIC 2019
E. Bourjot et al., ESTC 2022



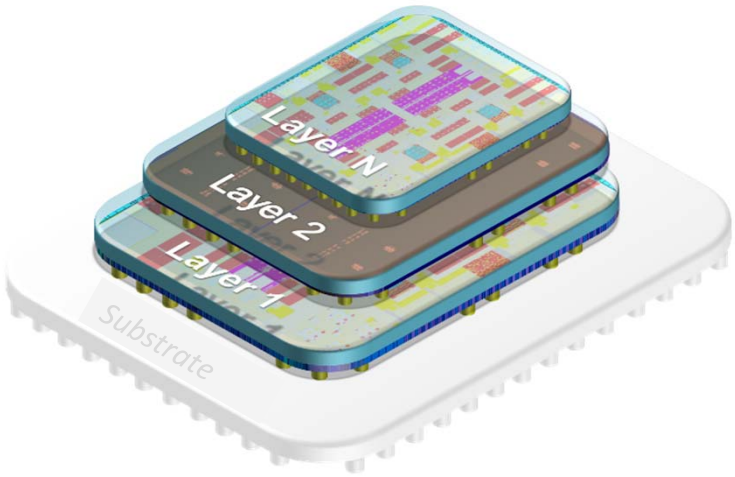
TEM on W2W bonding at LETI

1 **Pitch reduction** (towards < 1µm)
Interconnect / bandwidth density
Towards 3DIC

2 **New capabilities** for heterogeneity
- Temp. reduction (150-300°C)
- Self-assembly (precision, throughput)
- New materials (III-V, supraconductors)

3 **Architectures & Demonstrators**
- Multistacking with TSV
- Smart Imagers & displays
- Edge AI, based on chiplets
- RF mmW, incl. III-V

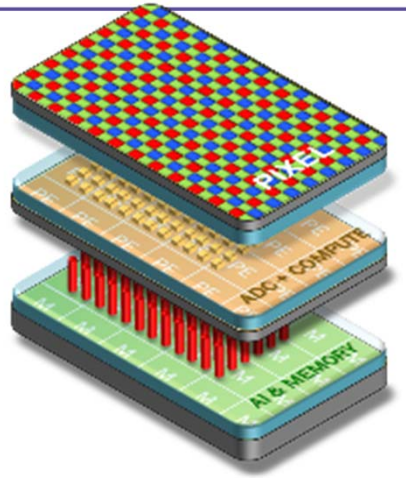
Outline

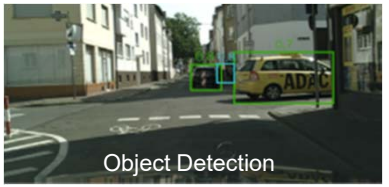


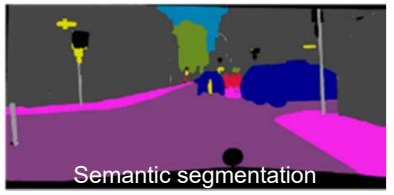
- Why going Vertical?
- 3D Integration Building Blocks
- 3D integration for innovative architectures

Smart imager developments

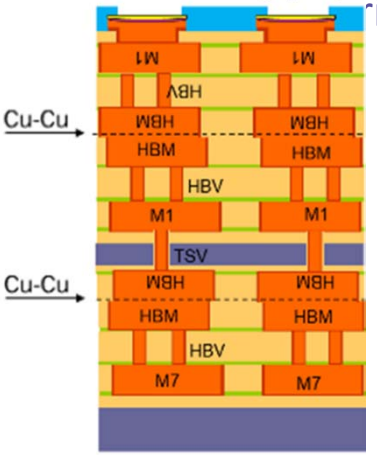
- From imagers to vision sensors
  - Edge-AI targeted applications (autonomous vehicle)
- 3-layer scheme:
  - Pixel array / Readout IC / AI & memory layer
  - Hybrid bonding with 1x10µm HD-TSV

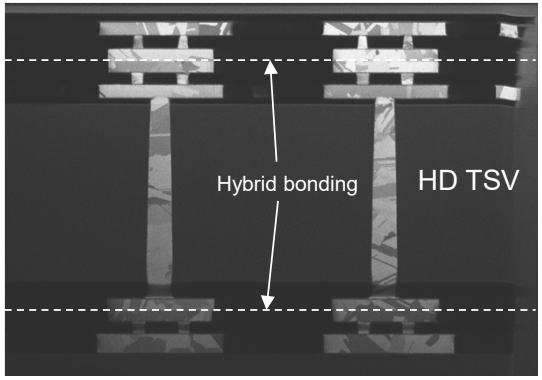


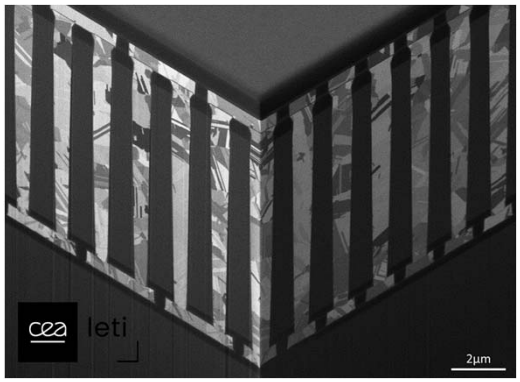




Autonomous vehicle functions





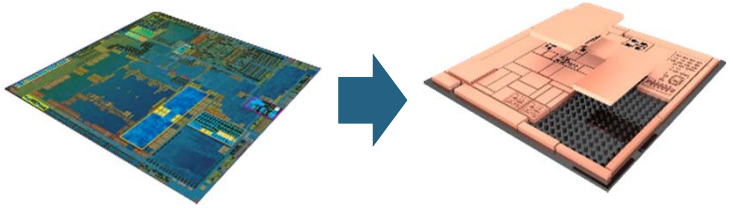


1x10µm HD TSV (2µm pitch)
100% yield on 10 000 TSV daisy chains
R_{TSV} = 500mΩ
Misalignment HB2: max. 1 µm (avg 200 nm)
Misalignment HB1: max. 350 nm (avg 100 nm)
1x5µm HD TSV under development

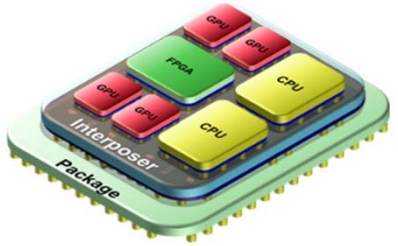
J. J. Suarez Berru , 2023 IEEE 73rd Electronic Components and Technology Conference (ECTC), Orlando, FL, USA, 2023, pp. 97-102,

Chiplet approach: Heterogenous IC design

- Interposer & chiplets
  - Interconnects performance → R.C delay
  - Exceeding latency & bandwidth limits
  - Cost/form factor advantages

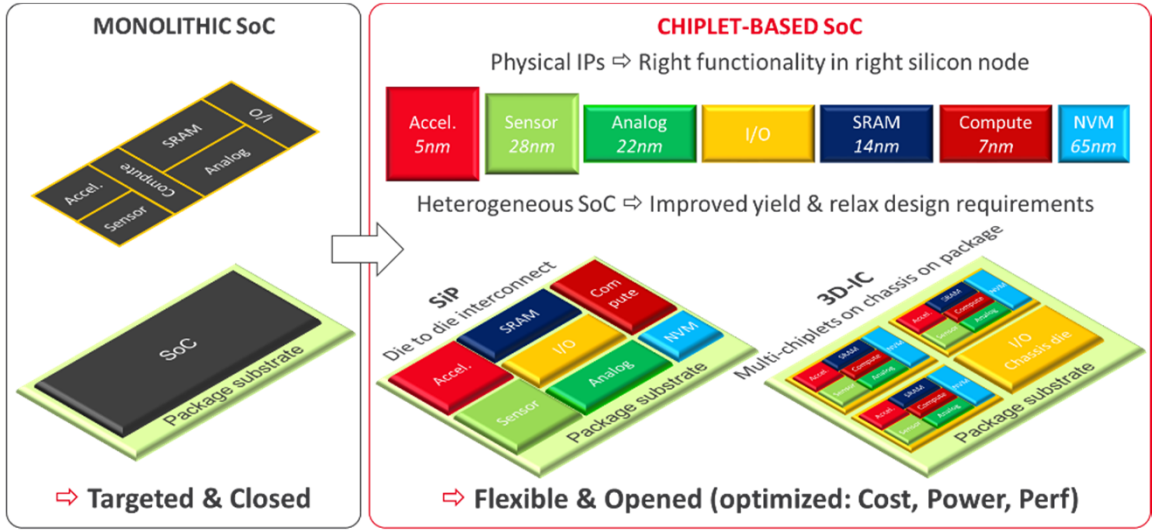


The end of "all for the SoC" paradigm (image from DARPA)

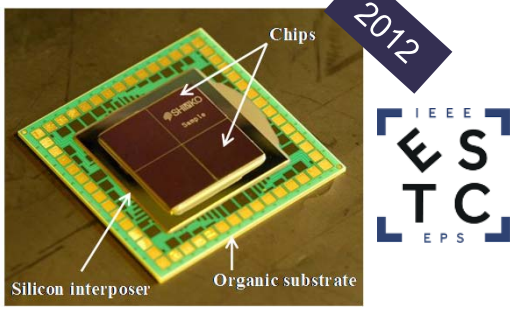


Chiplet topology on interposer

- Appropriate partitioning
- Heterogeneous IC design
  - Optimized technology for each function
  - specialization by app.: CPU, GPU, AI (...)
  - Standardization (coming soon, hopefully)



HPC and AI converging roadmaps

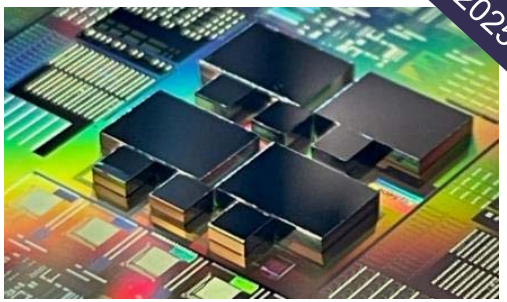


Metallic Passive interposer

- ✓ Chip-to-chip side-by-side communication

Active interposer (ENoC) Intact

- ✓ Extended communication capability (increased distance, routing, power management, …)



Photonic interposer (ONoC) Starac

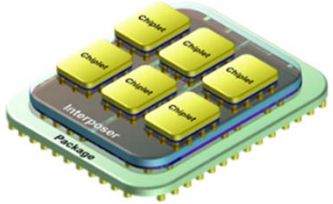
Optical communication:
- ✓ Reduction of on-chip latencies
- ✓ Higher throughput
- ✓ Lower energy consumption
- ✓ Scalability

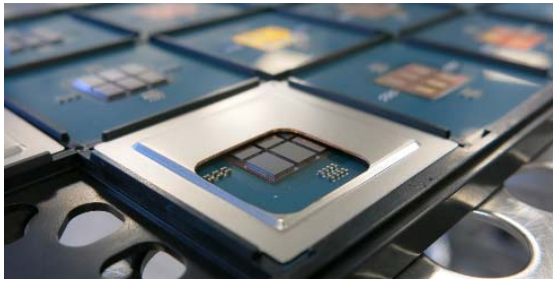
More than 12 years expertise on Silicon Interposers

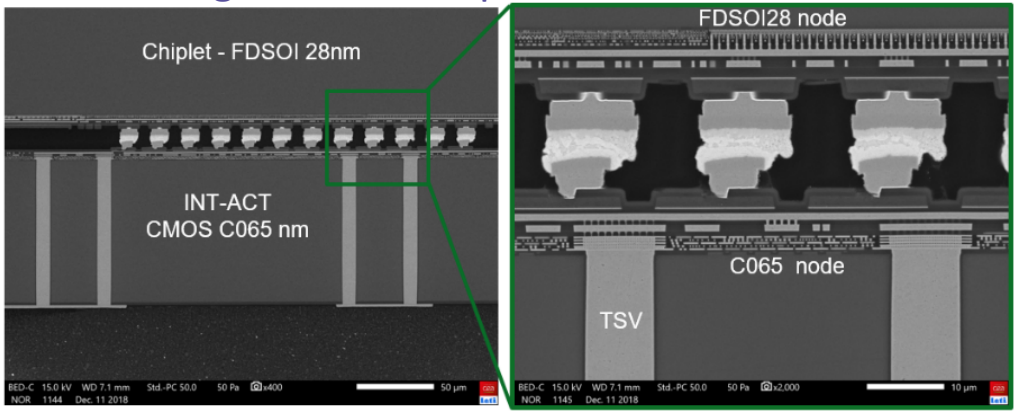
Y. Thonnart et al., "POPSTAR: a Robust Modular Optical NoC Architecture for Chiplet-based 3D Integrated Systems," Proc. DATE, 2020, p. 6.
D. Saint Patrice et al, "Process Integration of Photonic Interposer for Chiplet-Based 3D Systems" Proc. IEEE ECTC, 2023

Active interposers (INTACT)

- 1st functional architecture with active interposer
  - Si interposer: 65nm including TSV middle 10x100µm
  - Chiplets FDSOI 28nm
  - State of the art 20µm pitch Cu pillars (diam. 10µm)
  - High performance 3D connecting between chiplets and DC/DC convertors



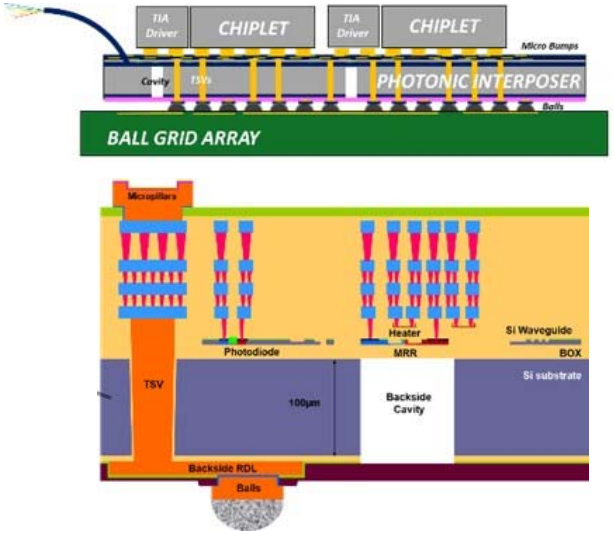




D. Lattard et al., 3DIC 2016 *E. Guthmuller et al., ESSIRC 2018* *D. Dutoit, D43D 2018* *P. Coudrain et al., ECTC, 2019*

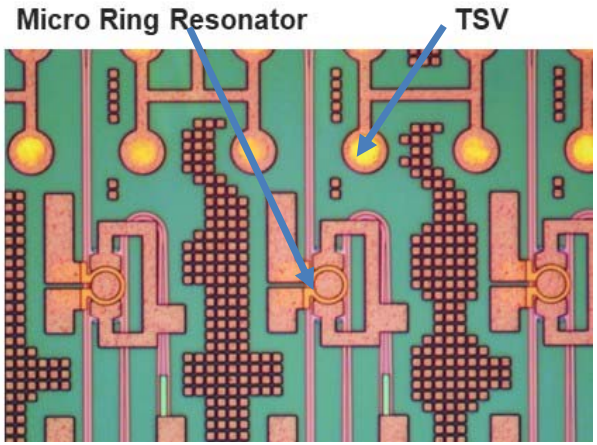
Interposer level optical links for HPC

Architecture



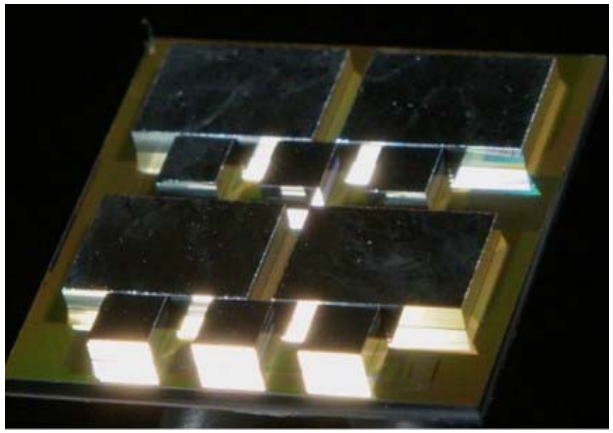
ONoC Popstar Interposer

Co-Integration & test



Co-integration TSV mid (12x100µm) and photonic FEOL after Metal 1

3D Assembly

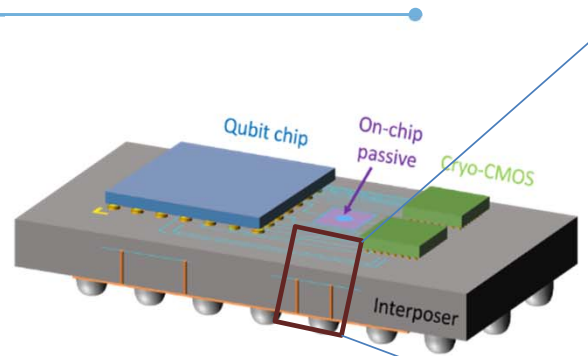


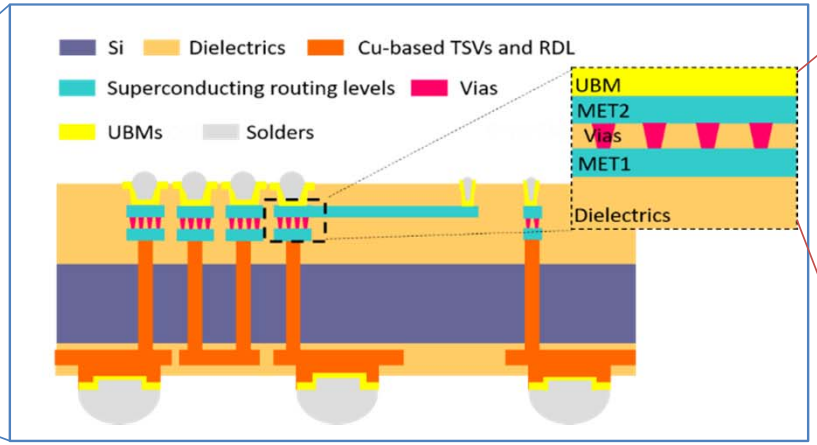
Silicon Photonic Interposer front side: 4 chiplets and 6 electro-optical drivers in 28nm FD-SOI

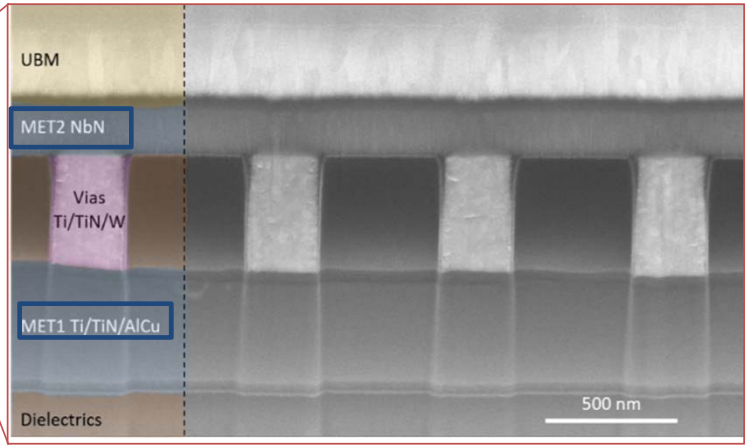
- 4 x 16 cores FDSOI 28nm Chiplet
- 6 electro-optical drivers (Rx/Tx) in 28nm FDSOI
- Silicon photonic interposer: Full integration @CEA-Leti

Full demonstration expected in 2025

Leti Quantum interposers

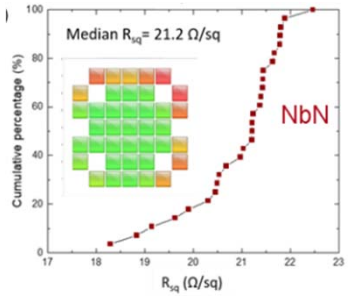




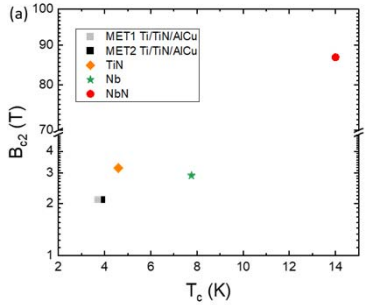


✓ Integration qualified with Ti/TiN/AlCu, TiN, Nb and NbN

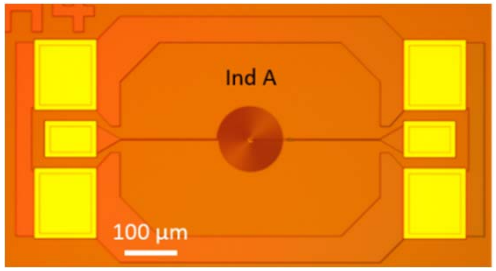
✓ Superconducting routing with embedded passive compounds



Example of parametric tests @ 300K



Extraction of superconducting properties with low temperature measurements



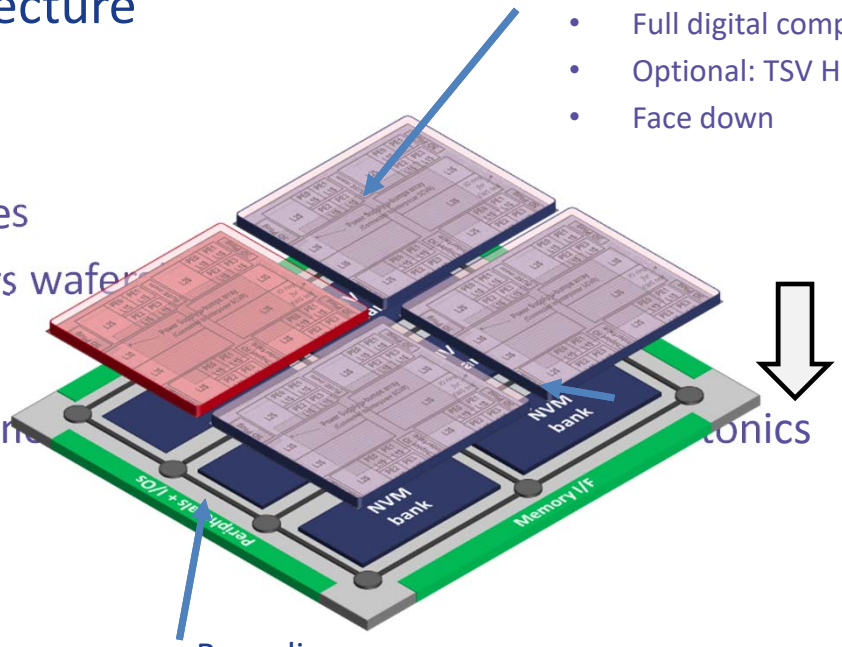
C. Thomas et al., Materials for Quantum Technology, 2, 3, 035001, (2022)

What's next

- More Moore : Wafer level chip architecture
  - Interconnection density increase (x, y z)
  - Power delivery network
  - Minimized TSV footprint on active devices
  - **TSV HD + W2W** allows many active layers wafer
- More than Moore : system level
  - Heterogeneous Integration of advanced n… …tonics
  - Combination of DTW + TSV (Mid or HD)
  - Applications HPC &IA

Heterogeneous compute chiplets:

- Advanced node (7nm, 5nm)
- Heterogeneous (size, pitch, node)
- Full digital compute chiplet
- Optional: TSV HD for memory cube
- Face down



3D assembly:

- Die-to-Wafer
- Hybrid Bonding
- Face-to-Face

Base die:

- Mature node (FD28, GF22FDX,…)
- Face up
- TSV for power delivery and Ios (preferred mid process)

ICOS International Cooperation On Semiconductors

European Commission

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EU – INDIA – Joint Researchers Workshop on Semiconductors

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