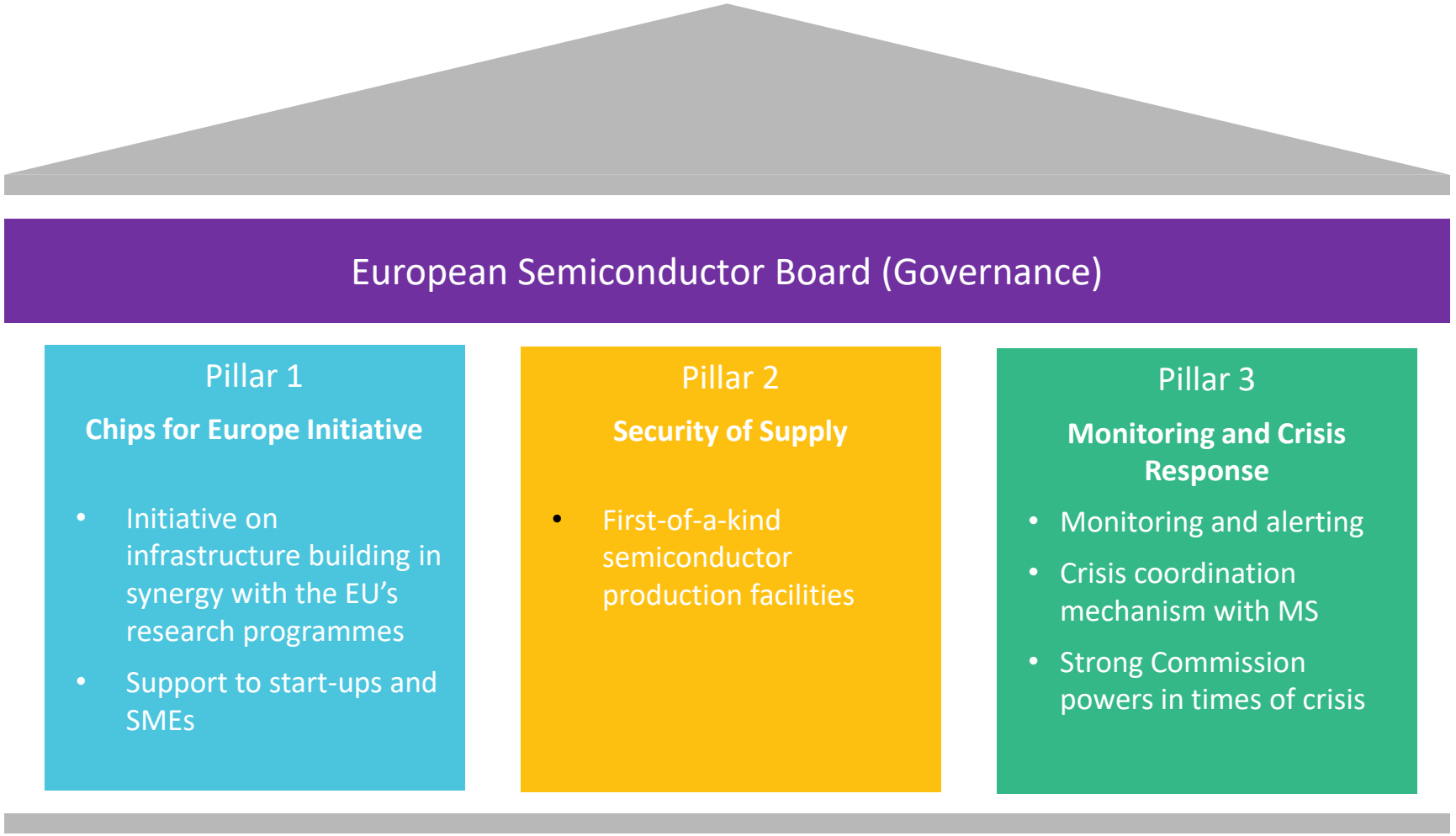
EU Chips Act State of Play

EU – India R&D Workshop

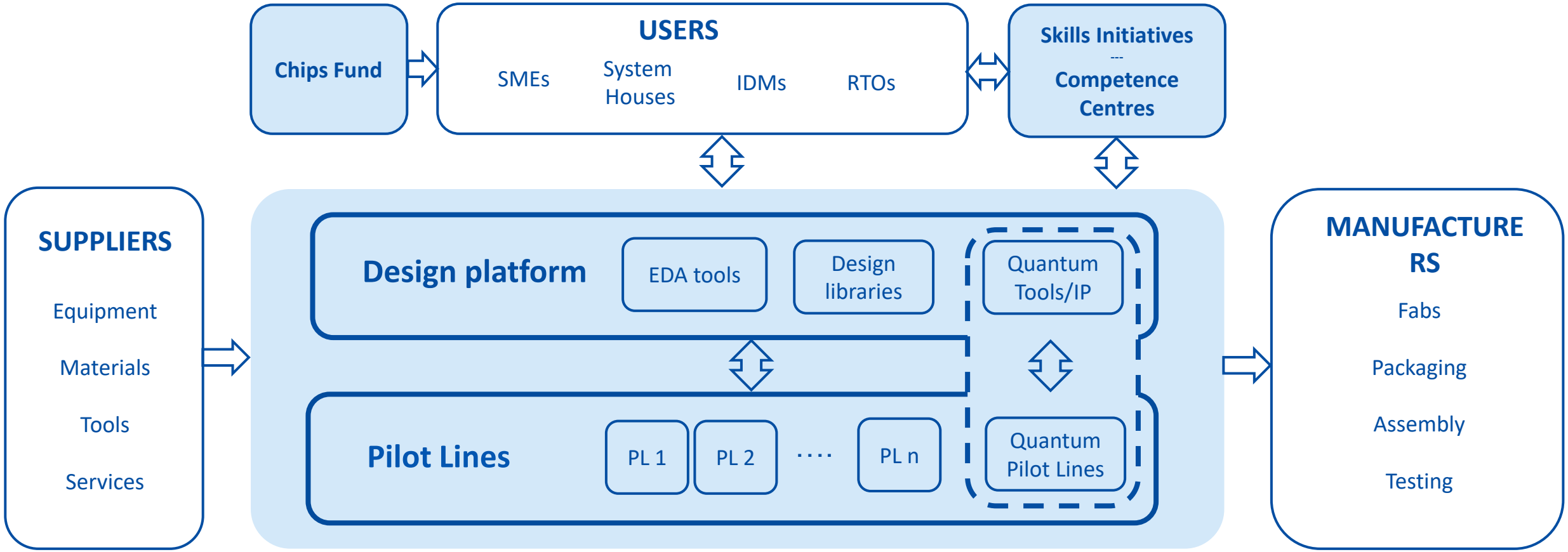
European Commission – Pierre Chastanet
Head of Unit – Microelectronics and Photonics
9 October 2024

Three pillars of the EU Chips Act



Signed by the European Parliament and the Council September 2023

Chips for Europe Initiative
Bridging the gap from lab to fab

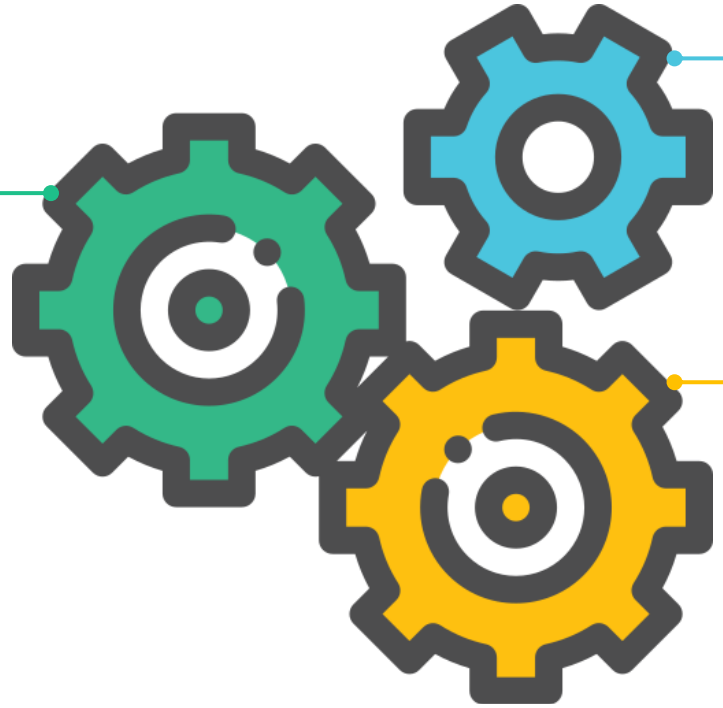


European Commission

State of Play

Chips JU

Implementing vehicle of the Chips for Europe Initiative



First calls on **pilot lines** launched on 1 Dec 2023 for ~ EUR 3.3 billion

EUR 5.75 billion [EU + MSs] investment in infrastructures expected by 2027

European Commission

Chips for Europe Initiative – current status (I)

Pilot lines

Leading-edge nodes
below 2nm

FD-SOI scaling
towards 7nm

Heterogeneous
systems integration
and assembly

Wide-bandgap
semiconductors

Photonics

Call opened in July 2024

European Commission

Chips for Europe Initiative – current status (II)
Design platform

Main objectives

- **Reduce entry barriers** and admin burden for EU companies in design
- **Facilitate access** to pilot lines and foundries
- Foster **collaboration** among EU stakeholders on new developments

Instrument

ning and support to boost design skills

Develop a **virtual design platform,** offering **cloud-based** access to tools, libraries and support services to accelerate development and reduce time-to-market

European Commission

Chips for Europe Initiative
Design Platform Services

Level 1

- Tool-oriented and practical training
- Academic/PoC access to EDA tool licenses and IP
- Faster access to design tool licenses with reduced contract negotiation time
- Academic access to IP repository (open-source + commercial)
- EDA / IP sandbox (community-based testing + validation)
- Access to pilot line and foundry PDKs/ADKs

Access open to qualified designers from entities (commercial and non-) based in EU or 'Chips JU' PS

Level 2

- Commercial access to IP repository (open-source + commercial)
- Application engineering support (design enablement)
- Support for EDA licensing
- Customised cloud instance with scalable compute + storage resources
- Foundry access and tape-out support
- Mentoring

Market rates or access to selected entities with support granted by EU + PS of 'Chips JU'

European Commission

Chips for Europe Initiative – current status (III)
Competence centres

EU support for at least one centre per Member State

Co-investment with Member States and Regions

Supporting industry and public services

Access to design platform and pilot lines

Focus on Semiconductors Skills

A strong European network of Competence Centres

Chips Act – Pillar II
Facilitate investments in manufacturing facilities

State aid *distorts competition and is prohibited in the Union (TFEU) - unless justified by economic development needs*

First-of-a-kind (FOAK) facility: to qualify, facility needs to offer innovation in terms of products or process that is not yet present in the Union (not to distort competition)

Conditions: positive impact, security of supply and commitment to next generation

Integrated Production Facility (IPF)

First-of-a-kind facility which produces the chips (mostly) for the same undertaking

Open EU Foundry (OEF)

First-of-a-kind facility that produces chips (mostly) for unrelated undertakings

European Commission

Update on Applications for State aid

✓ The Commission **already approved State aid for the following four projects.**

- On 5 October 2022, the Commission approved EUR 293 million of State aid under the NextGenEU Recovery and Resilience Facility (RRF) to **STMicroelectronics** for the construction and operation of a Silicon Carbide wafer plant in Catania using 150mm technology.
- On 27 April 2023, the Commission approved a €2.9 billion French aid measure to support **ST and GlobalFoundries** in the construction and operation of a new microchips manufacturing facility in Crolles, France.
- On 31 May 2024, the Commission approved EUR 2 billion of aid for an additional project for **STMicroelectronics** in Catania, Italy for a fully integrated production facility based on 300mm Silicon Carbide wafer technology.
- On 20 August 2024, the Commission approved EUR 5 billion German aid measure to support European Semiconductor Manufacturing Company (‘**ESMC**') in the construction and operation of a microchip manufacturing plant in Dresden.

Chips Act Pillar III

Update on general activities of the European Semiconductors Board

- **Monitoring supply chain vulnerabilities**: the objective is to create a mechanism to monitor the semiconductor value chain and to spot semiconductor crises (in coordination with the JRC).
- **Monitoring mature-node chips investments in third countries:** Launch a questionnaire for users of chips and for suppliers of chips.
- **Multilateral engagement:** G7, OECD, GAMS.
- **International cooperation :** TTC with US & India and Digital Partnerships with Japan, Korea, Singapore, and Canada.
- **Skills for Chips Initiative**: Launch of the Thematic Working Group on Skills managed by ALLPROS.eu.

International partnerships and frameworks

- Semiconductor value chain is global and spread over different world regions
- We need to **cooperate**, proactively managing **interdependencies** to ensure a reliable global **marketplace** for EU products and **security of supply** including in crisis situations

Bilateral

Digital Partnerships:

- Japan
- South Korea
- Singapore
- Canada

Trade and Technology Council (TTC):

- US
- India

Multilateral

OECD Informal network on semiconductors:

Coordinated approach to gain a better understanding of global semiconductor ecosystems through information sharing on identified parts of the value chains and policy efforts across countries

- 38 OECD members + accession candidates

European Commission

Thank you

https://ec.europa.eu/info/strategy/priorities-2019-2024/europe-fit-digital-age/european-chips-act_en

@EU_Microelectronics

European Commission