Driving Net-Zero with GaN:

Advancing Power and RF GaN Technology through Industry-oriented Models for Foundry & Circuit Designers

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Department of Electronics and Communication
National Institute of Technology Srinagar (NITSRI)

Outline

- Net Zero and Background
  - Global landscape
  - Indian initiatives
- GaN forecast
- State-of-the-art
- Models
  - ASM-GaN
  - NITSRI-GaN
- Call to Action
- Summary

Where we are located - NITSRI

Background:

Global and Indian Perspective

Net Zero – Call for action

"Cutting greenhouse gas emissions to as close to **zero** as possible, with any remaining emissions re-absorbed from the atmosphere, by oceans and forests"

Limit the global warming to 1.5°C w.r.t pre-industrial levels – **Paris Agreement [2] (2015)**

Top 5 emitters[1]:

China, US, India, EU, Russia

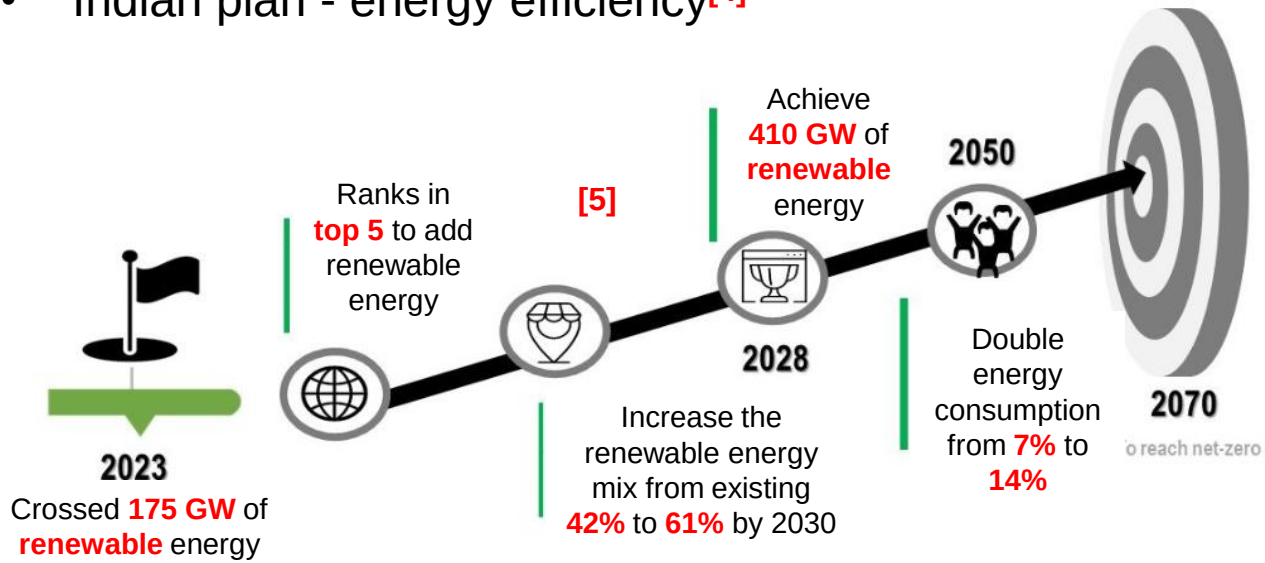
Global energy sector [3]

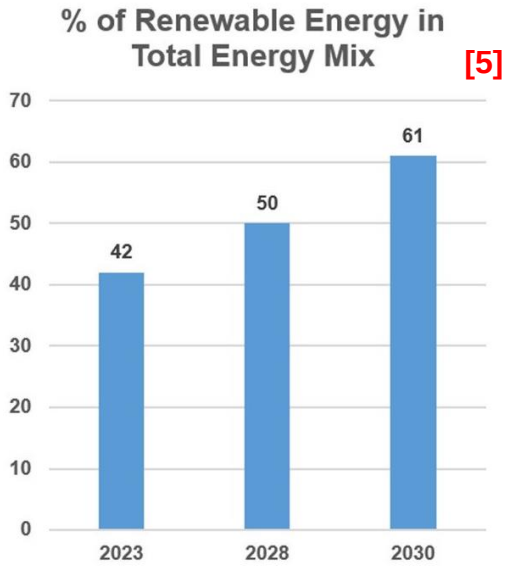
- ✓ Renewables
- ✓ Energy efficiency
- ✓ Electrification
- ✓ Hydrogen based fuels

[1] www.un.org/en/climatechange/net-zero-coalition
[2] www.un.org/en/climatechange/paris-agreement
[3] Net Zero by 2050: A Roadmap for the Global Energy Sector, **International Energy Agency**, Paris, [Online] iea.org/reports/net-zero-by-2050, May 2021.

Our Commitment

- Indian Commitment to Net-zero by 2070[1]
- Global Carbon neutral plan[2]
- US taking the lead[3]
- Indian plan - energy efficiency[4]





[1] Press Information Bureau, **Min. Environment, Forest and Climate Change**, 1847813, Aug 2022.

[2] "Net Zero by 2050: A Roadmap for the Global Energy Sector", **International Energy Agency**, Paris, May 2021.

[3] "The Long-Term Strategy of the US: Pathways to Net-Zero Greenhouse Gas Emissions by 2050", **US Department of State and the US Executive Office of the President**, Nov 2021.

[4] "India's Long-Term Low-Carbon Development Strategy", **Min. Environment, Forest and Climate Change, Gov. of India**, Aug 2022

[5] "India's Race to Net-Zero", **Sgurr Energy**, 2023

India SemiCon Landscape - 2024

- Semiconductor Market – **$34B** (2023) → **$100B** (2032)

Three semiconductor manufacturing units **($15B Investment)**:

1. Semiconductor Fab with 50,000 wfsm capacity – at Dholera, Gujarat
Tata Electronics Private Limited (TEPL) will collaborate with Powerchip Semiconductor Manufacturing Corp (PSMC), Taiwan

2. Semiconductor ATMP (Assembly, Test, Marking and Packaging) unit – at Morigaon, Assam
48 million per day, catering to segments such as automotive, electric vehicles, consumer electronics

3. Semiconductor ATMP unit for specialized chips – at Sanand, Gujarat
CG Power, in partnership with Renesas Electronics, is responsible for consumer, industrial, automotive, and power applications, with a capacity of 15 million per day.

- **300 thousand** jobs created by 2026

Indian Compound Semi Initiative

MINISTRY OF ELECTRONICS AND INFORMATION TECHNOLOGY

(IPHW Division)

NOTIFICATION

New Delhi, the 4th October, 2022

Subject: **Modified scheme for setting up of Compound Semiconductors / Silicon Photonics / Sensors Fab/ Discrete Semiconductors Fab and Semiconductor Assembly, Testing, Marking and Packaging (ATMP)/ Outsourced Semiconductor Assembly and Test (OSAT) facilities in India**

- Indian Semiconductor Mission - Compound Semiconductor and associated fabs[1]
  - **SiC**, **GaN** and other WBG materials
- GaN[2] and other Wide-bandgap tech - GaN to a market of $ 2 billion by 2027[2]
- Electric mobility, consumer and industrial sector – GaN power electronics[2] and 5G
- GEECI [3] – Gallium Nitride Ecosystem Enabling Centre and Incubator

[1] Modified scheme for setting up of Compound Semiconductors, **Gazette of India**, CG-DL-E-06102022-239341, Oct 2022

[2] Power GaN: the next wave, **Yole Group**, Jun 2022

[3] www.geeci.in

GaN Technology:

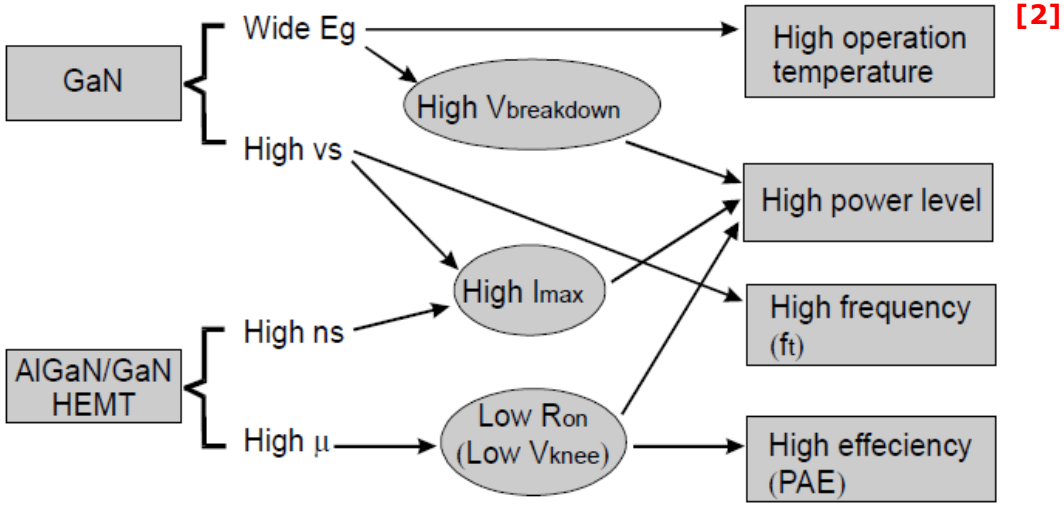
Forecast and State of the art

GaN Material Properties +

	Si	GaAs	4H-SiC	GaN
E_g (eV)	1.1	1.42	3.26	3.39
n_i (cm^{-3})	1.5×10^{10}	1.5×10^{6}	8.2×10^{-9}	1.9×10^{-10}
ε_r	11.8	13.1	10	9.0
μ_n (cm^2/Vs)	1350	8500	700	1200(Bulk) 2000(2DEG)
v_{sat} (10^7cm/s)	1.0	1.0	2.0	2.5
E_{br} (MV/cm)	0.3	0.4	3.0	3.3
Θ (W/cm K)	1.5	0.43	3.3-4.5	1.3
$JM = \frac{E_{br}v_{sat}}{2\pi}$	1	2.7	20	27.5

Johnson's figure of merit (rel. to Si)

[1]

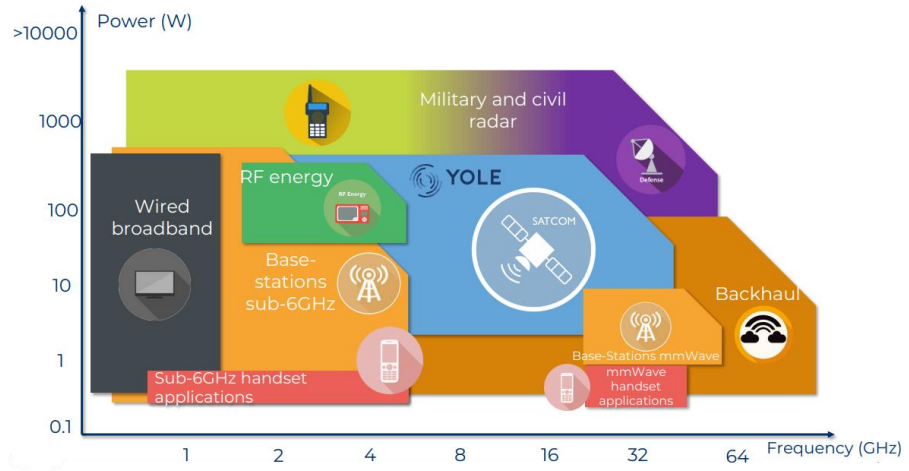


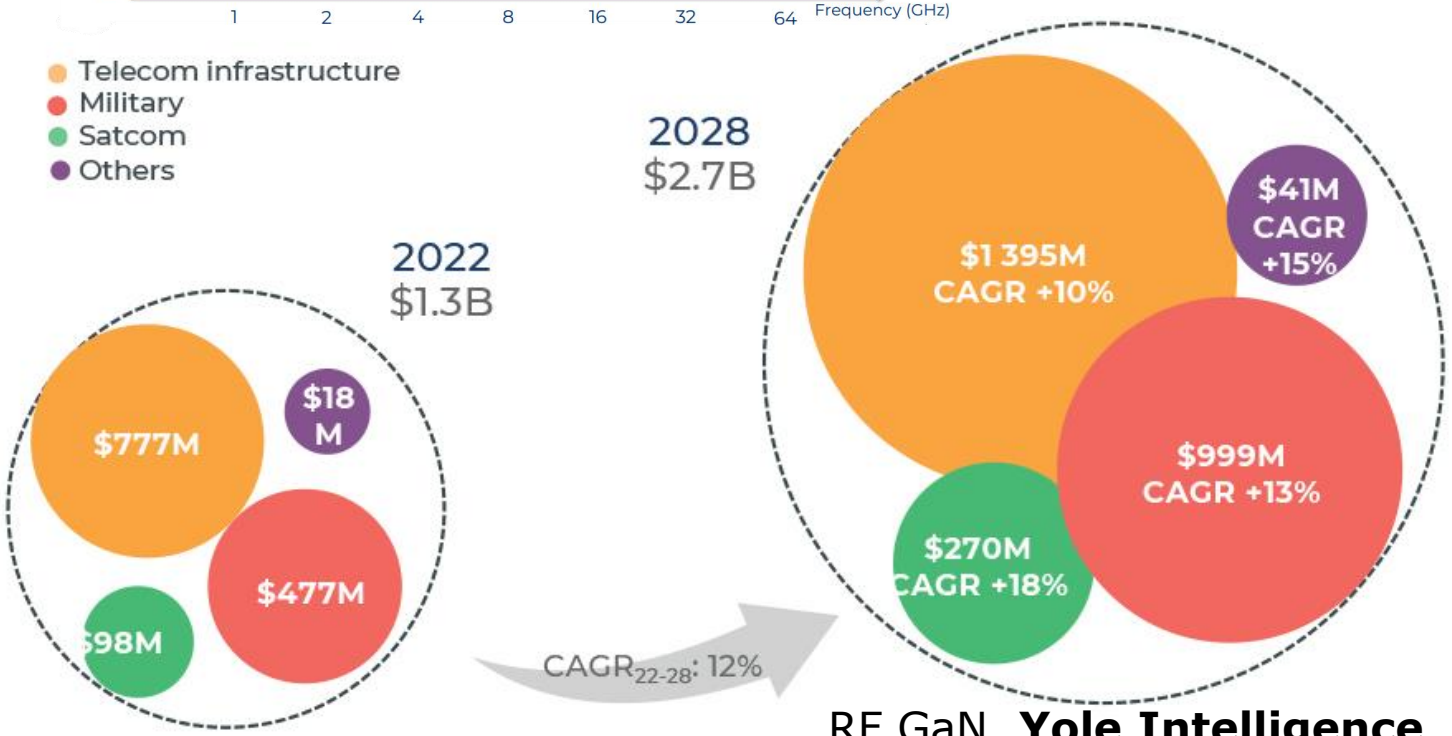
[2]

[1] U. K. Mishra *et al.*, **Proc. IEEE**, **96 (2),** 2008

[2] M. A. Briere, Tech. Rep., **International Rectifier**, Dec. 2008

GaN RF Projections





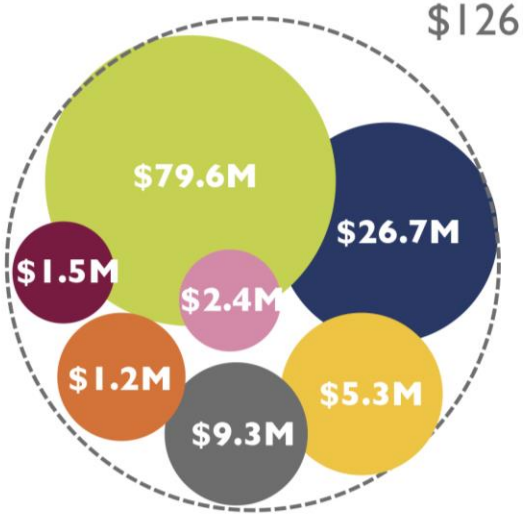
RF GaN, **Yole Intelligence**, Jun 2023

GaN Power Projections



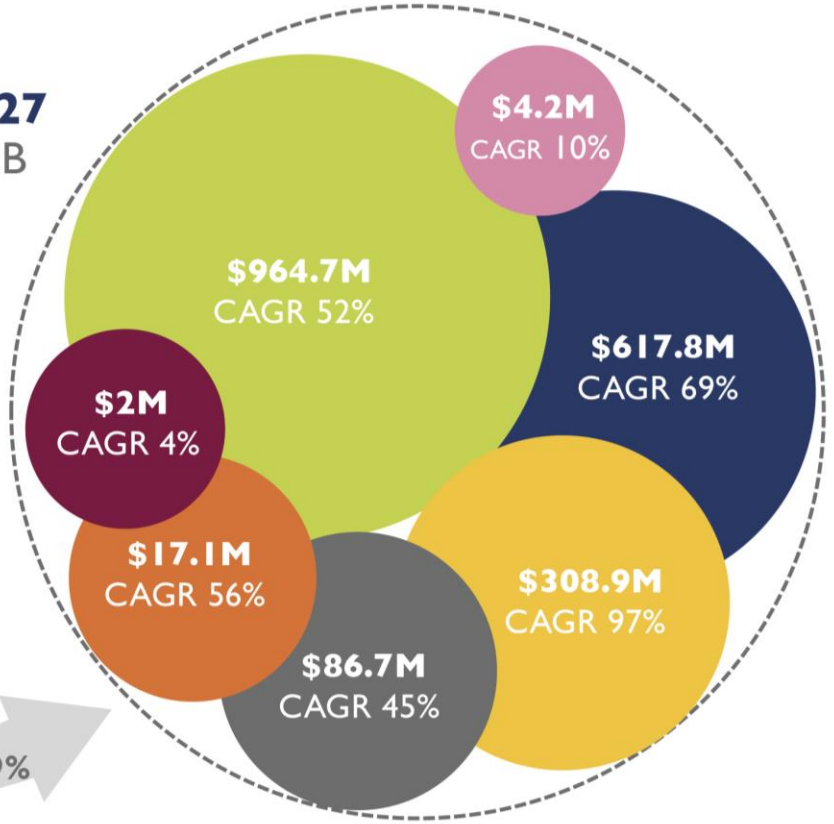

- Consumer
- Telecom, datacom
- Automotive, mobility
- Industrial
- Energy
- Defense, aerospace
- Others

2021
$126M



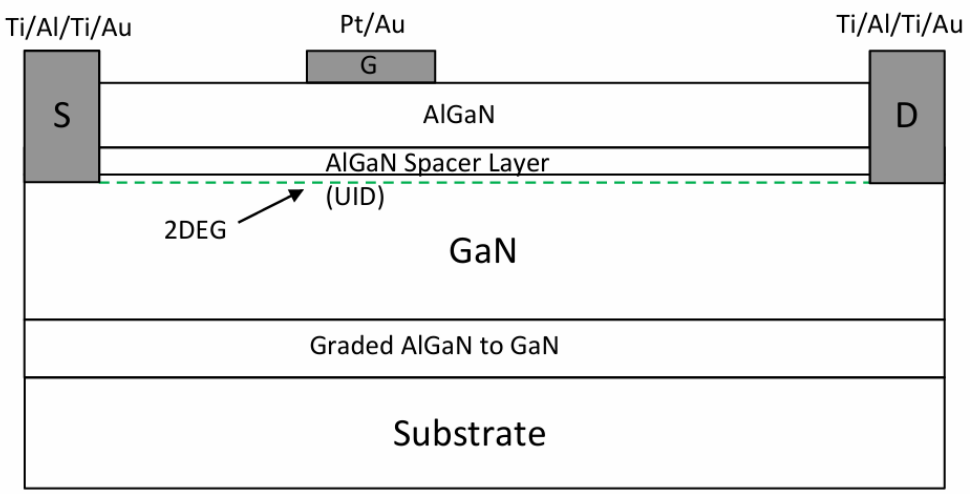
CAGR$_{21\text{-}27}$: 59%

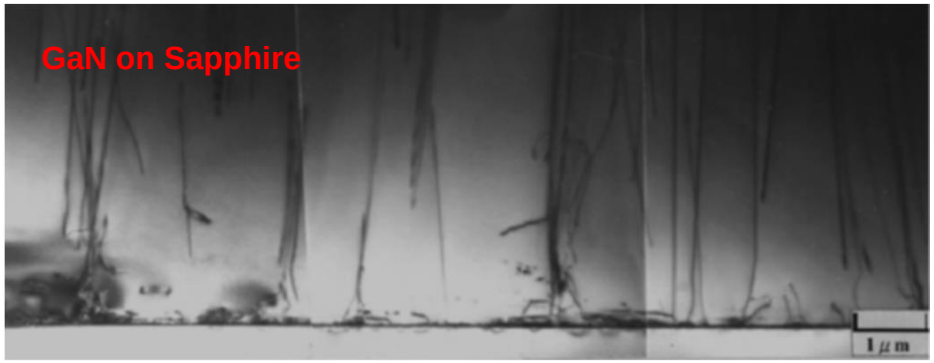
2027
$2B



Power GaN, **Yole Development**, Dec 2022

Conventional Structure and Substrate

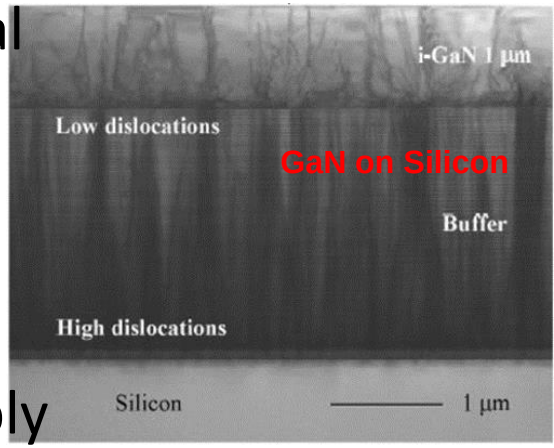




Sapphire: good from strain perspective, bad thermal resistance

Si: cheap, large wafer size, abundant

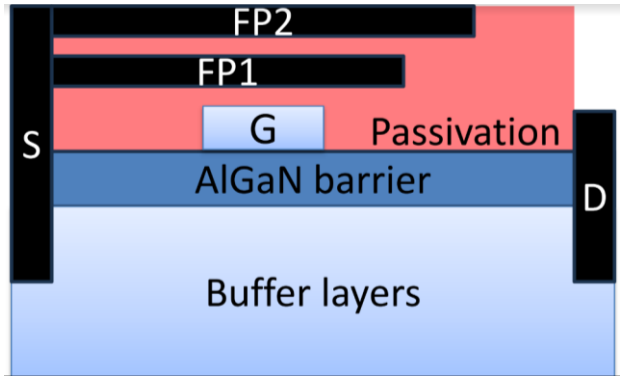
SiC: expensive, less defects, limited wafer size, supply

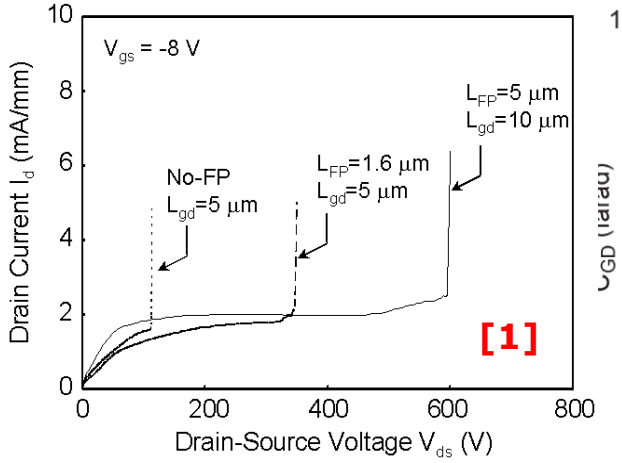


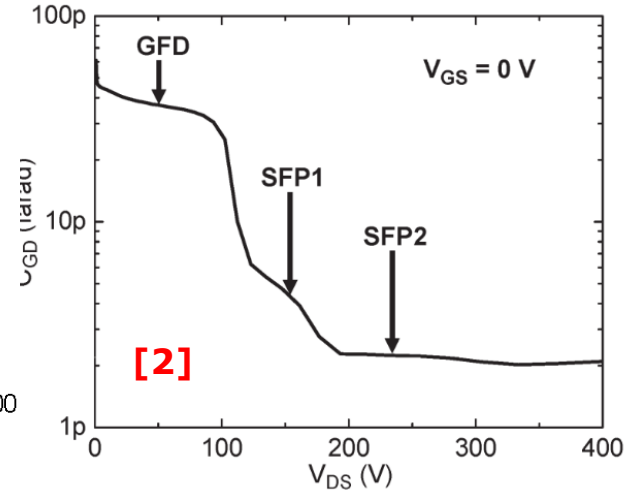
S. Huang, **Jap. J. Appl. Phys.**, 47 (10), 7998, 2008

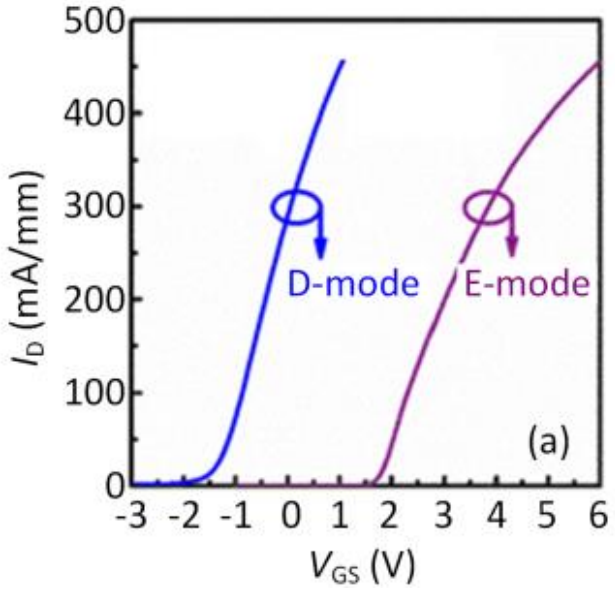
S. L. Selvaraj et al., **Proc. DRC**, 53, 2012

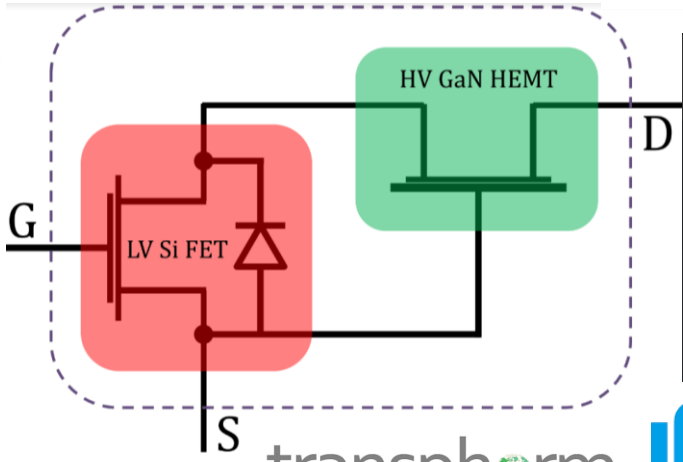
Power GaN design considerations

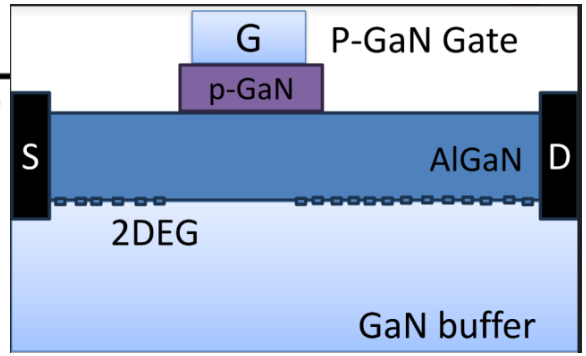












transphorm

Innoscience

nexperia

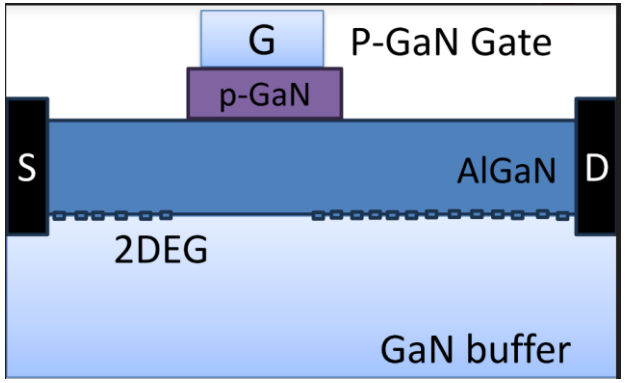
Infineon

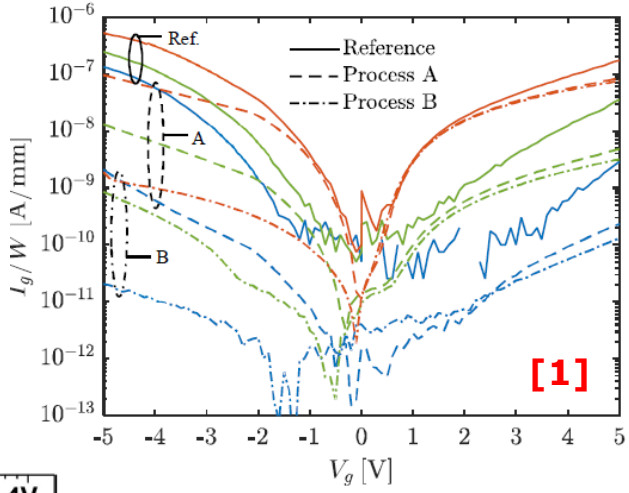
life.augmented

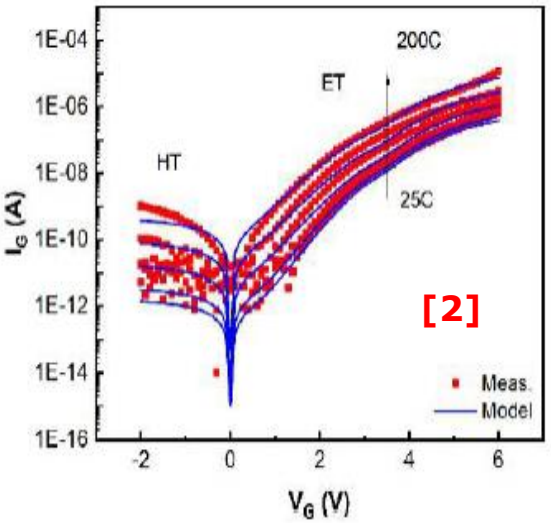
[1] W. Saito *et al.*, **IEEE Trans. Electron Devices**, 50 (12), 2003

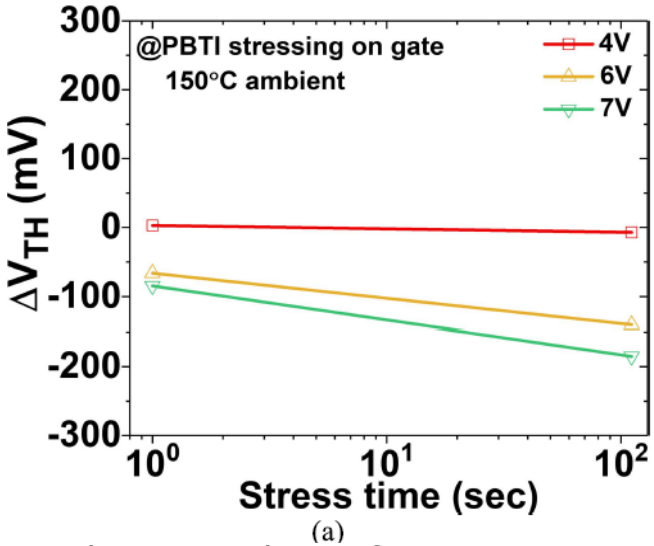
[2] R. Chu *et al.*, **IEEE Electron Device Lett.**, 32 (5), 2011

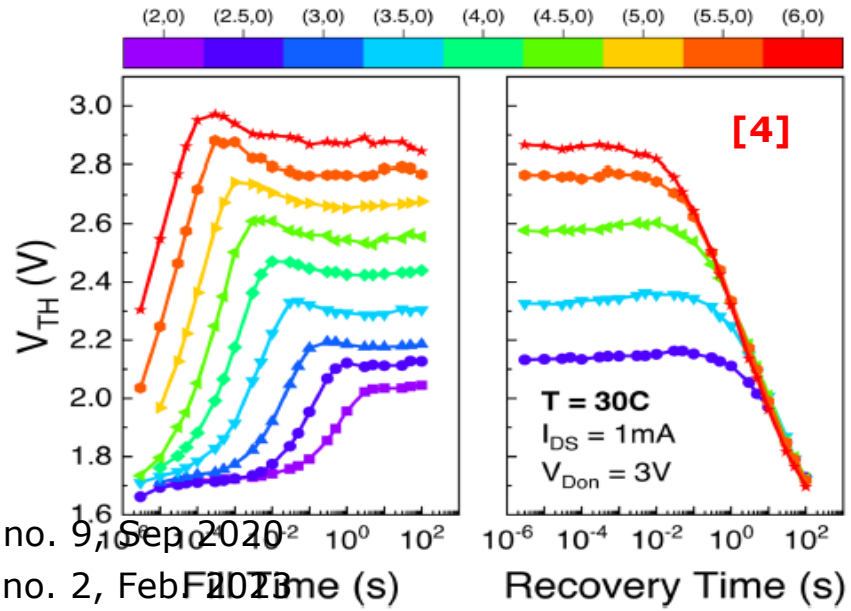
Gate Leakage and Vth Instability











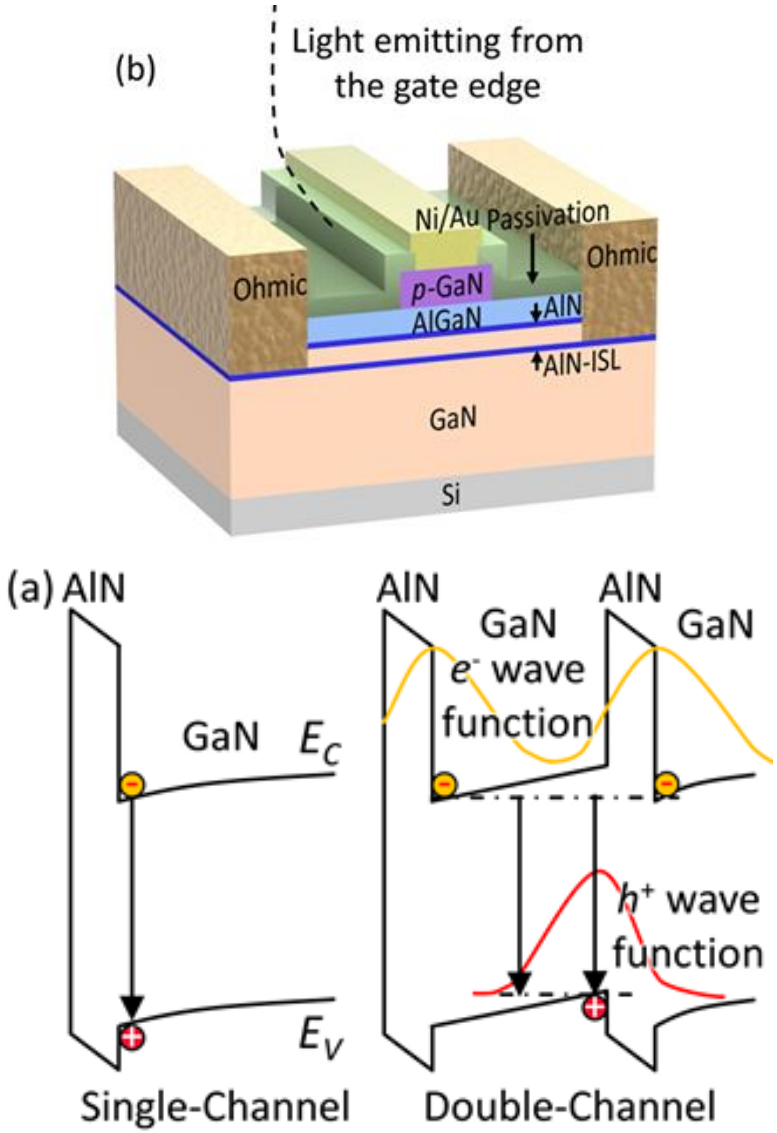
[1] Stockman et al., Prof. **IEEE IRPS**, 2018

[2] Wang et al, **IEEE Trans Electron Devices**, vol. 67, no. 9, Sep 2020

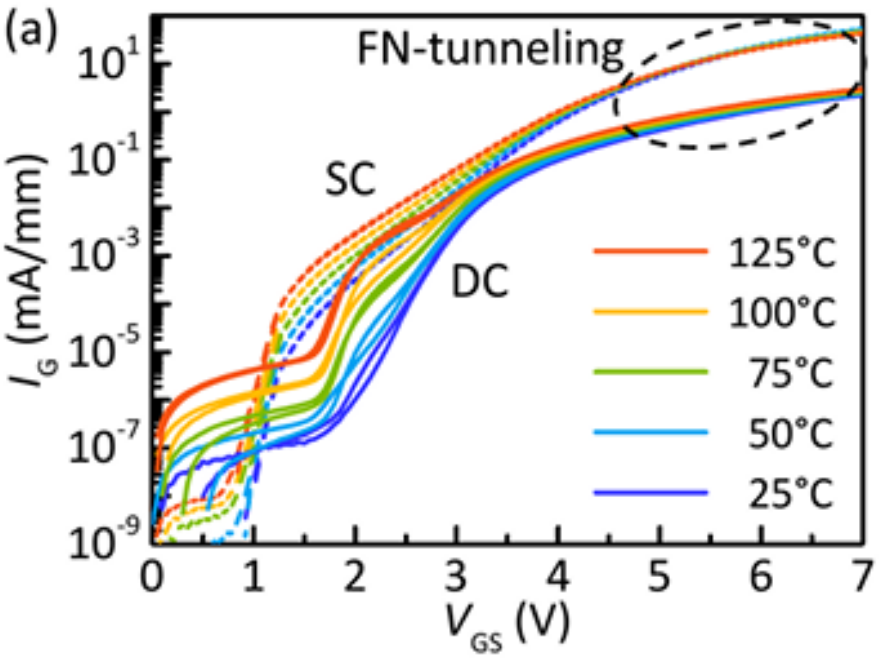
[3] Tang et al., **IEEE Trans Electron Devices**, vol. 70, no. 2, Feb 2023

[4] Modolo et al., **IEEE Trans. Power Electron**, vol. 39, no. 6, Jun 2024

Double Channel – Minimize Leakage

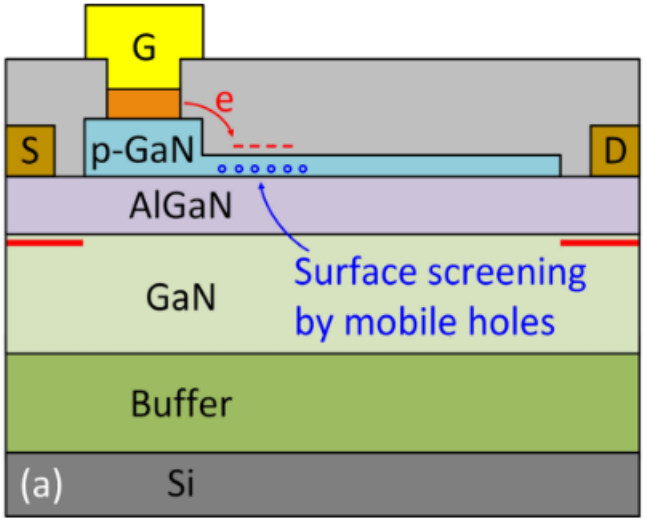


HKUST

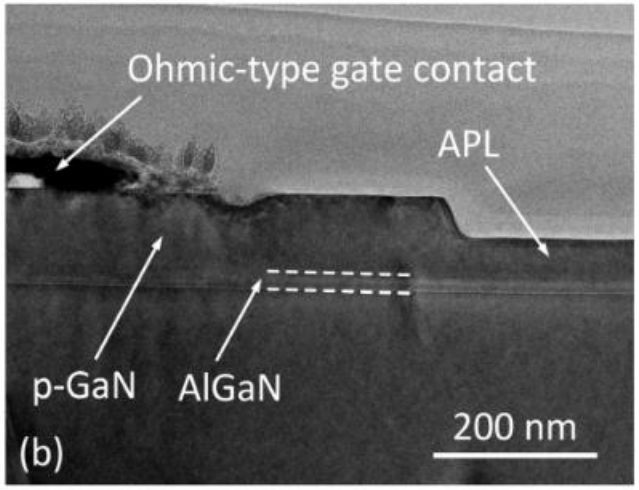


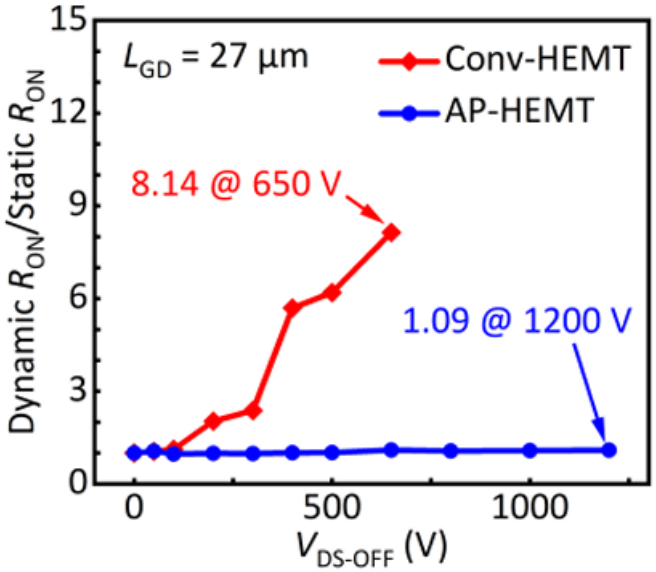
[1] Feng *et al.*, **IEEE Electron Device Lett.**, 44 (10), Oct. 2023

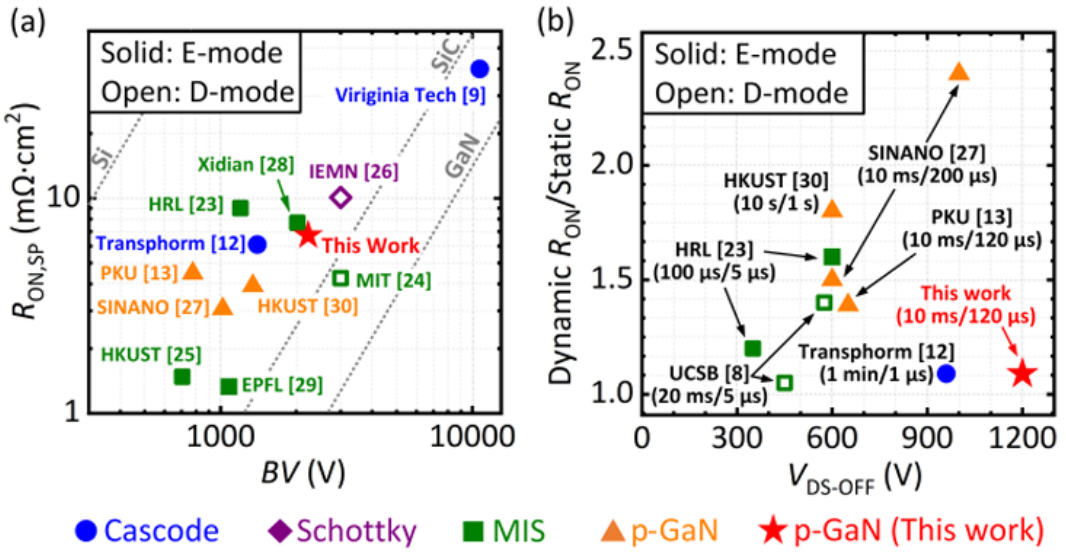
Active Passivation pGaN – Dynamic Ron



Peking University

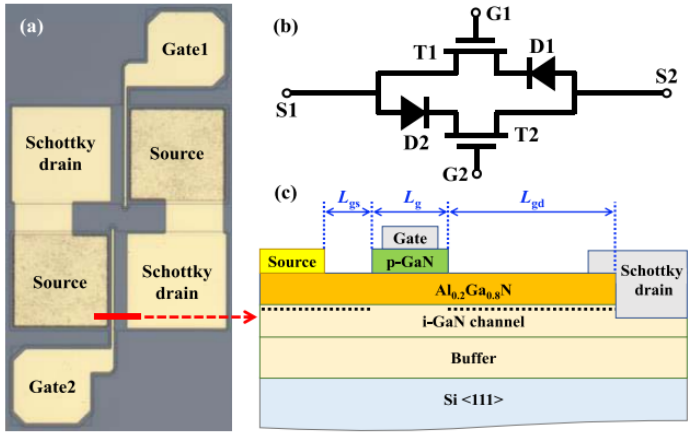


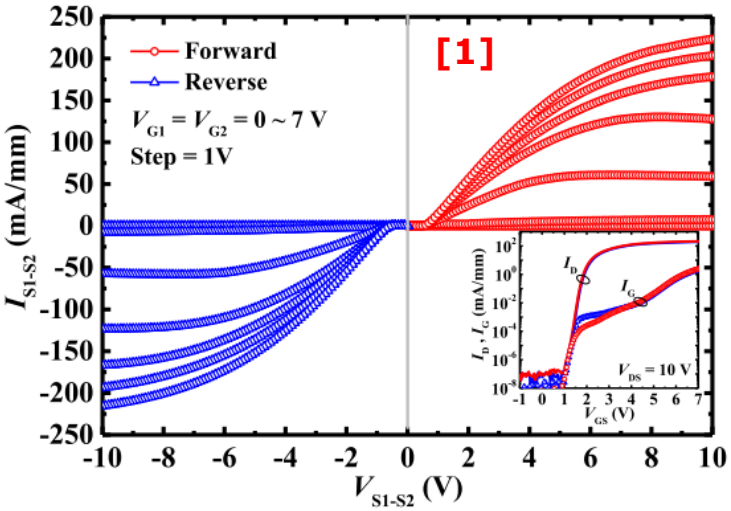


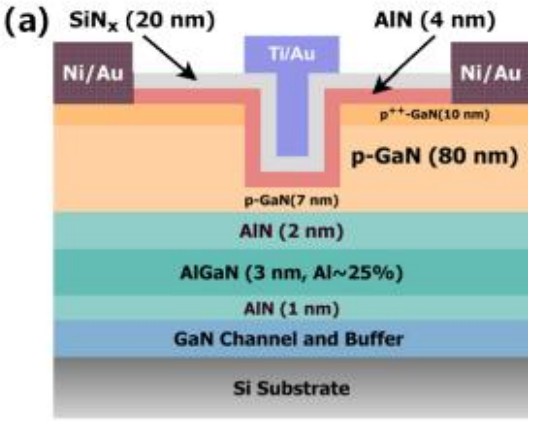


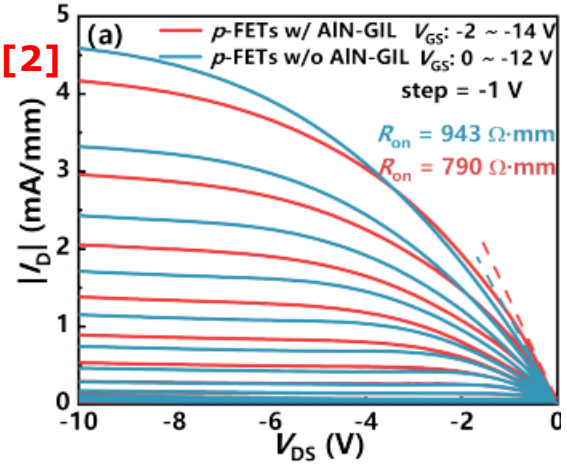
[1] Cui *et al.*, **IEEE Electron Device Lett.**, 45 (2), Feb. 2024

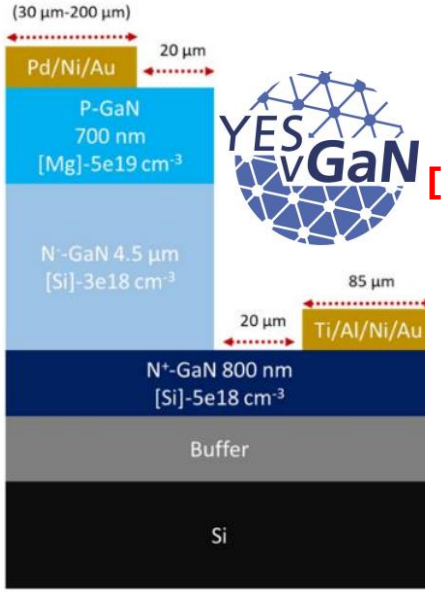
Power GaN integration: BiGaN, pFET, Vertical GaN

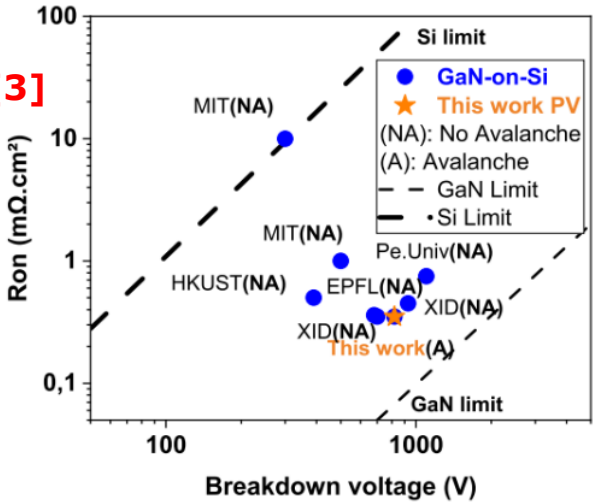










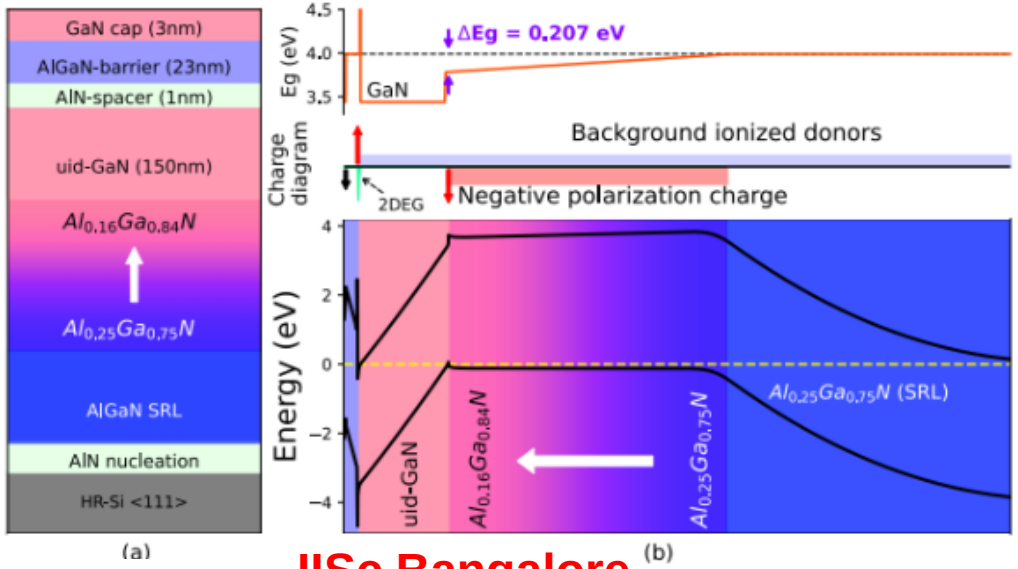


[1] Wang *et al.*, **IEEE Electron Device Lett.**, 42 (9), Sep. 2021

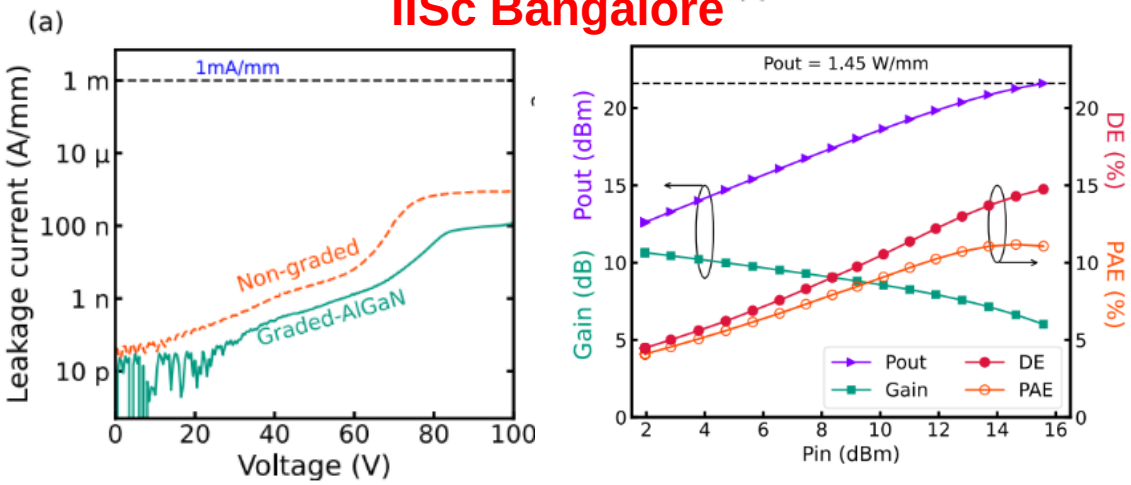
[2] Wang *et al.*, **IEEE Electron Device Lett.**, 45 (3), Mar. 2024

[3] Hamdaoui et al, **Appl. Phys. Express**, 17, 016503, 2023

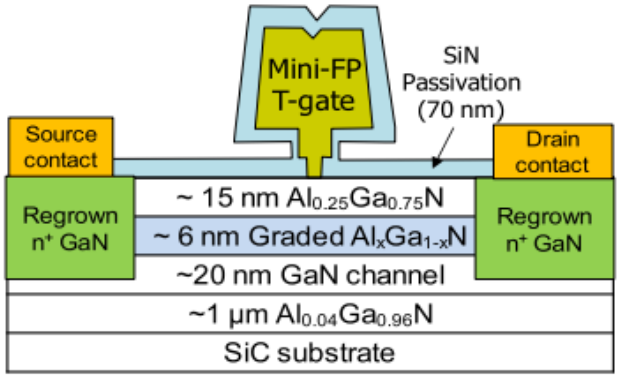
RF GaN – Graded structures



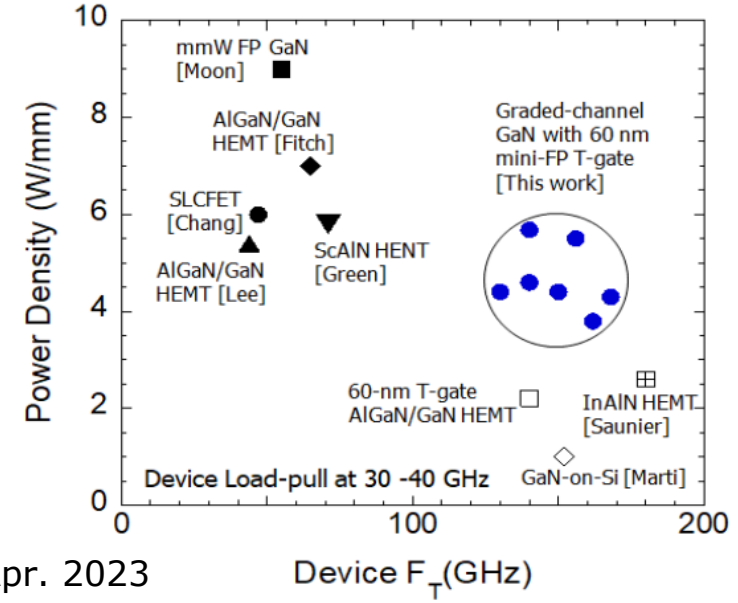
IISc Bangalore



(a) Graded-channel GaN HEMT



Uni. Notre Dame



[1] Gowrisankar *et al.*, **IEEE Trans Electron Devices**, 70 (4), Apr. 2023

[2] Moon *et al.*, **IEEE Electron Device Lett.**, 42 (6), Jun. 2021

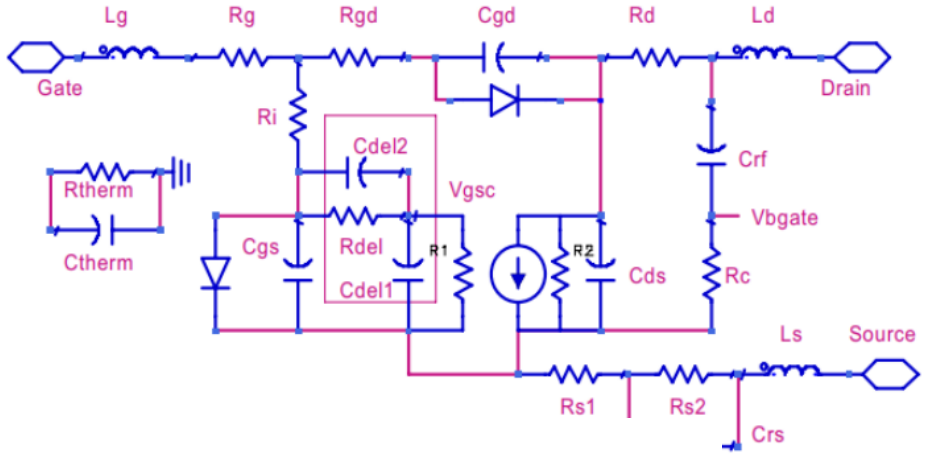
Modeling GaN

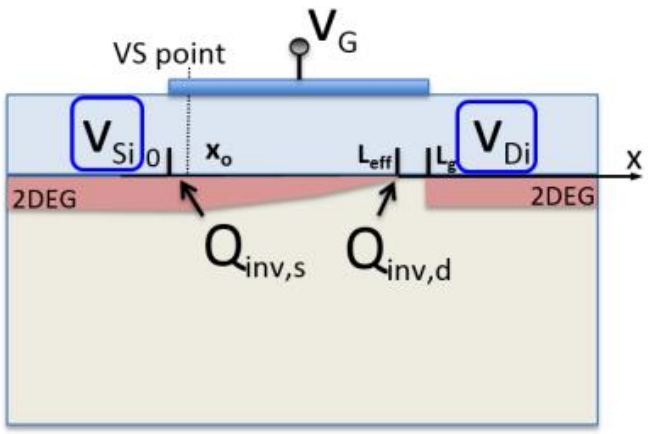
Industry Standards – CMC models

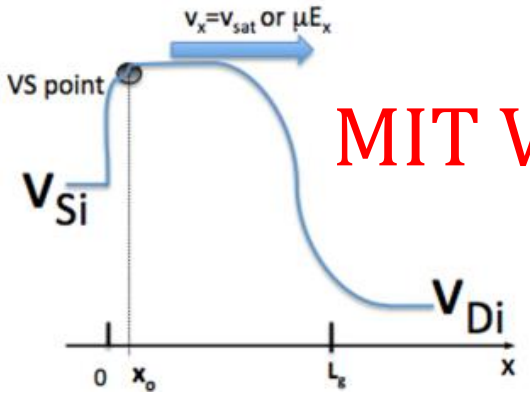
Application development (Circuit simulation)

Aid device technology evolution (Underlying Physics)

Angelov GaN







MIT VS GaN

FET Models
Curtice3 [12]
Motorola Electrothermal (MET) [25]
CMC (Curtice/ Modelithics/Cree) [26]
BSIMSOI3 [24]
CFET [5]
EEHEMT [13]
Angelov [14]
Angelov GaN [11]
Auriga [4]

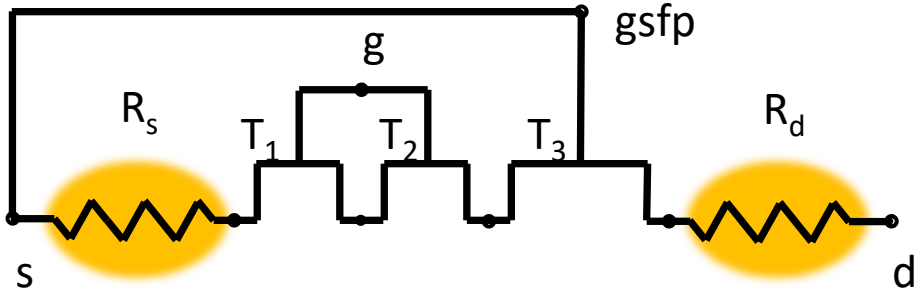
L. Dunleavy, **IEEE Microw. Mag.**, 2010

U. Radhakrishna et al, **IEEE IEDM**, 2014

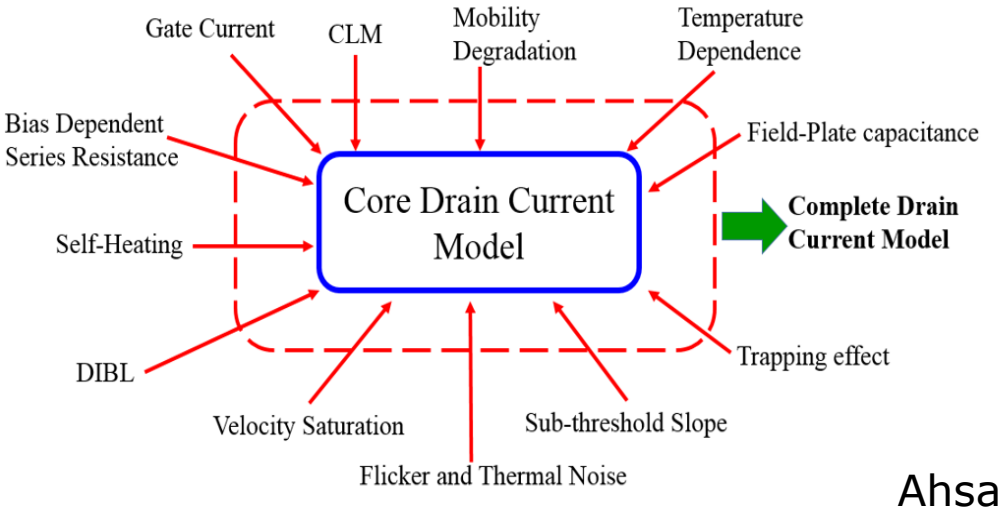
Advanced SPICE Model – Standard

IIT Kanpur and UCB

- Drain current expression
  - Using drift-diffusion framework
  - Nonlinear access region resistances



$$I_{ds} = \frac{\mu_{eff}}{\sqrt{1+\theta_{sat}^2\psi_{ds}^2}} \frac{W}{L} C_g N_f \left[V_{go} - \left(\frac{\psi_s + \psi_d}{2} \right) + V_{th} \right] \times \psi_{ds}(1 + \lambda V_{ds})$$

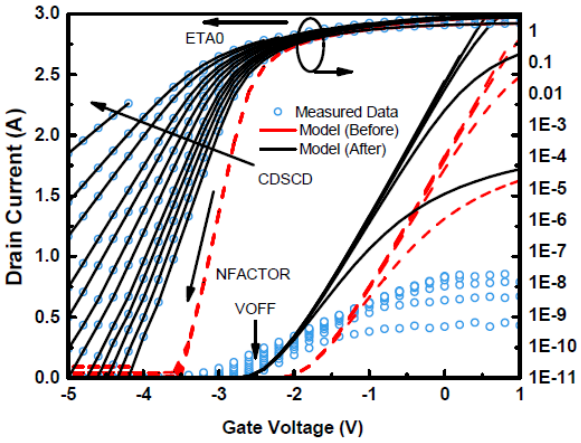


Chosen Industry Standard along with MIT

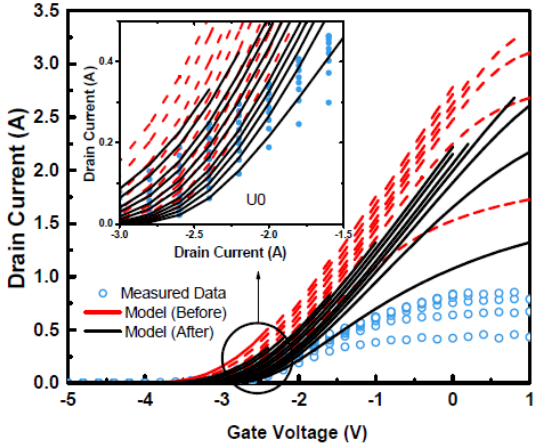
Ahsan, **PhD Thesis**, IIT Kanpur, 2017

Khandelwal et al, *IEEE Trans. Electron Devices*, 2013 Ghosh et al., **IEEE EDSSC**, 2016

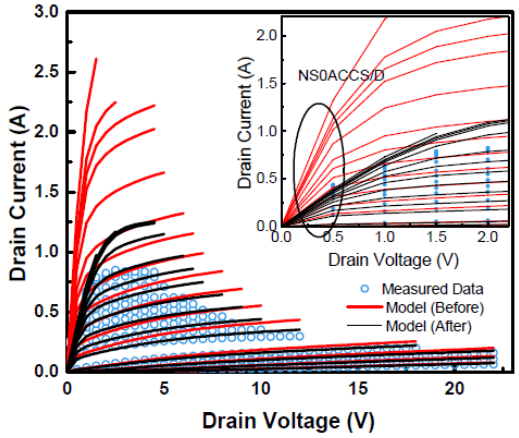
Well defined extraction procedure



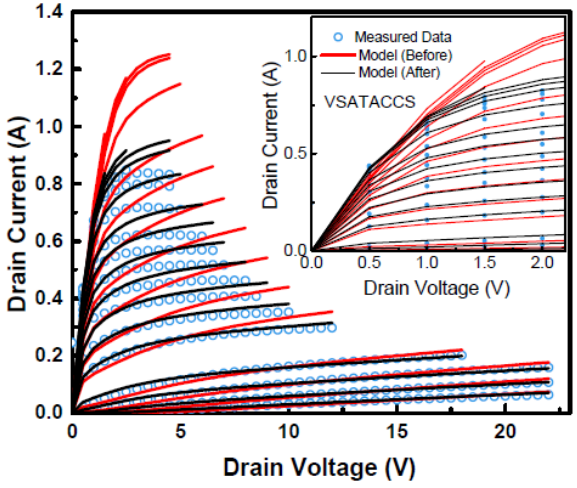
$I_d - V_g$ (Extract V_{OFF}, N_{FACTOR}, C_{DSCD})



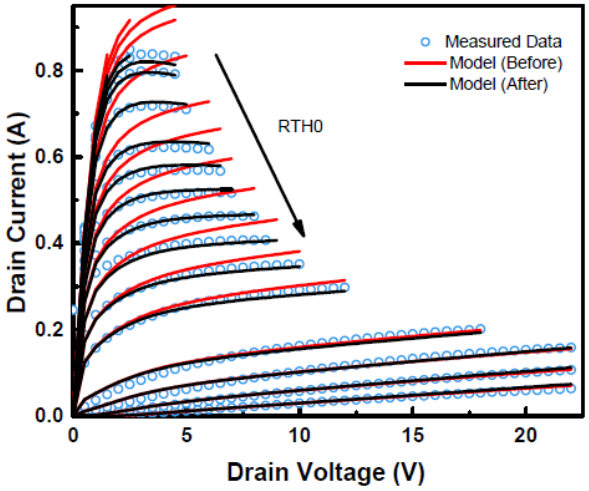
$I_d - V_g$ (Extract U_0)



$I_d - V_d$ (Extract N_{S0ACCS})



$I_d - V_d$ (Extract $V_{SATACCS}$)

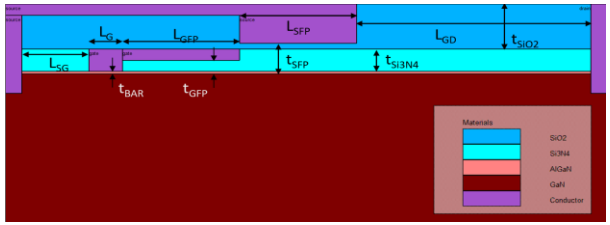


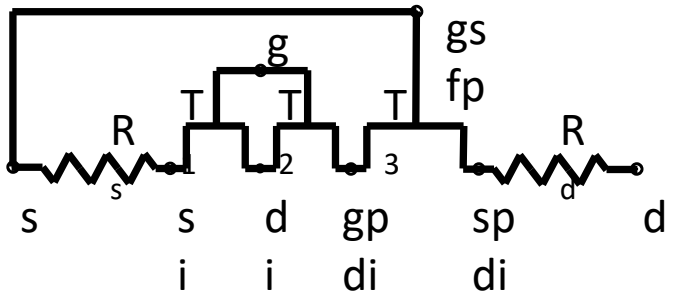
$I_d - V_d$ (Extract R_{TH0})

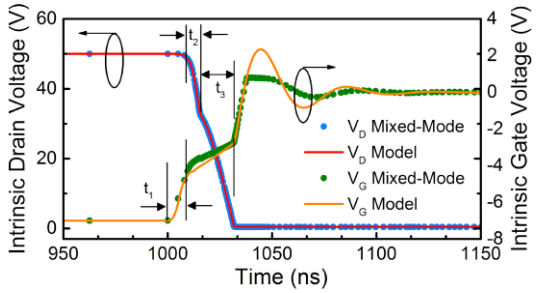
Incorporated in **Keysight's** latest **Pathwave** Design Tool

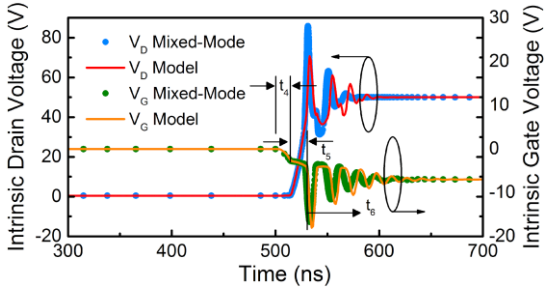
Ahsan et al, **MOS-AK Workshop**, Shanghai, 2016

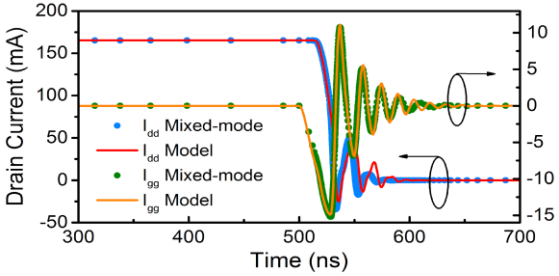
Power GaN Tech & App Development

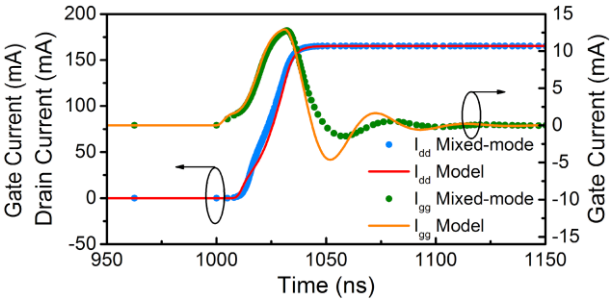


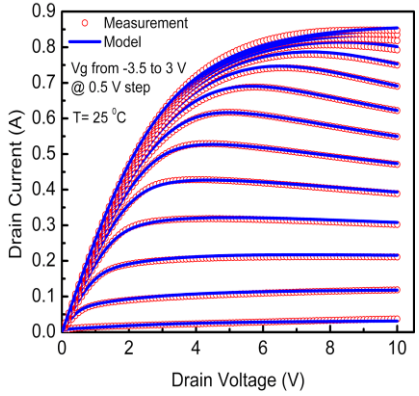


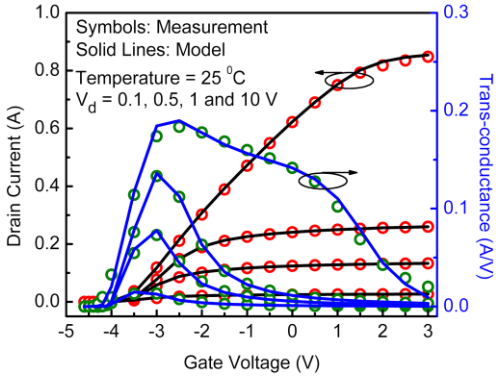


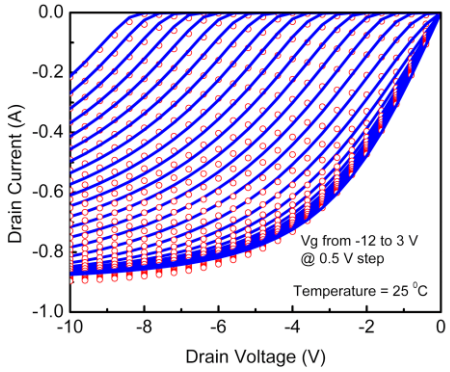


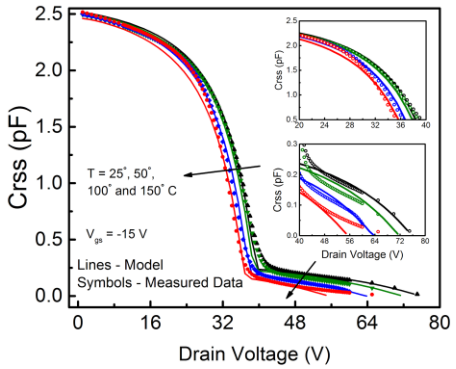






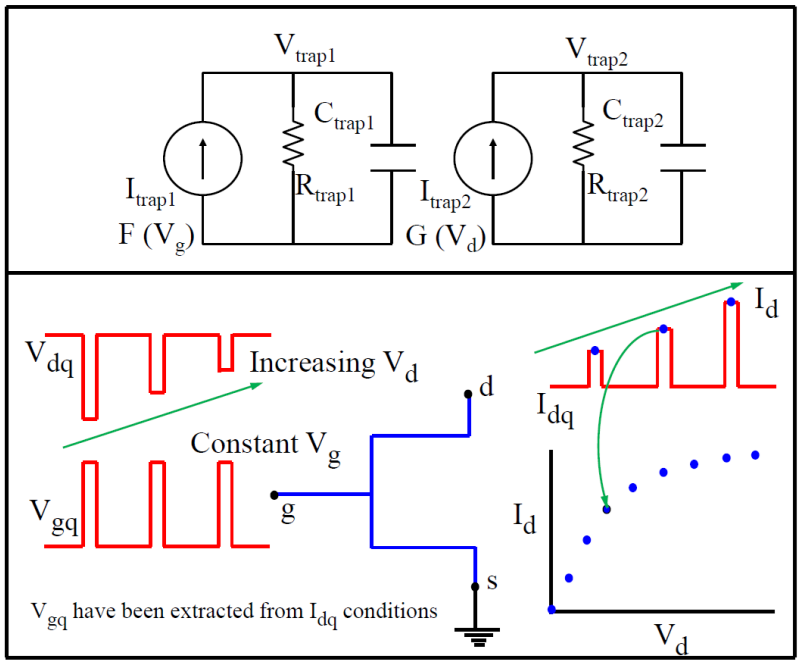




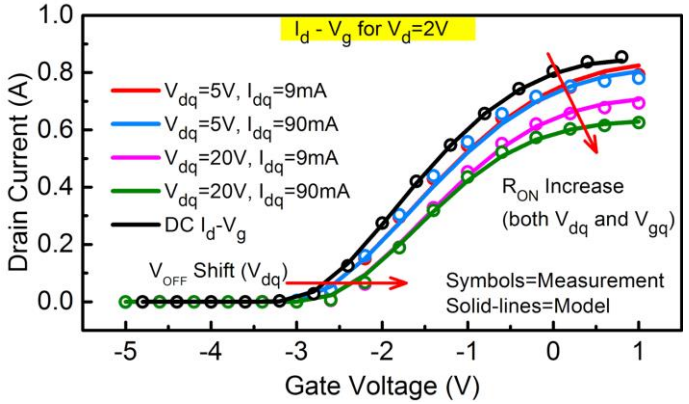


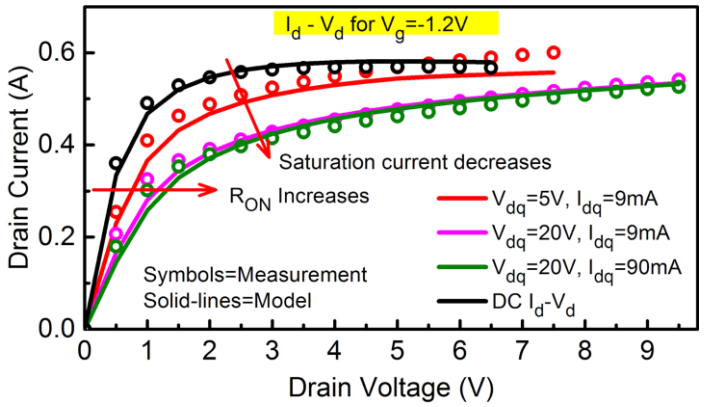
[1] Ahsan *et al.*, **IEEE Trans. Electron Devices**, 62 (2), 2016
[2] Ahsan *et al.*, **IEEE Trans. Electron Devices**, 63 (3), 2017

Modeling Traps



Pulsed-IV Scheme used to simulate the P-IV Characteristics in IC-CAP





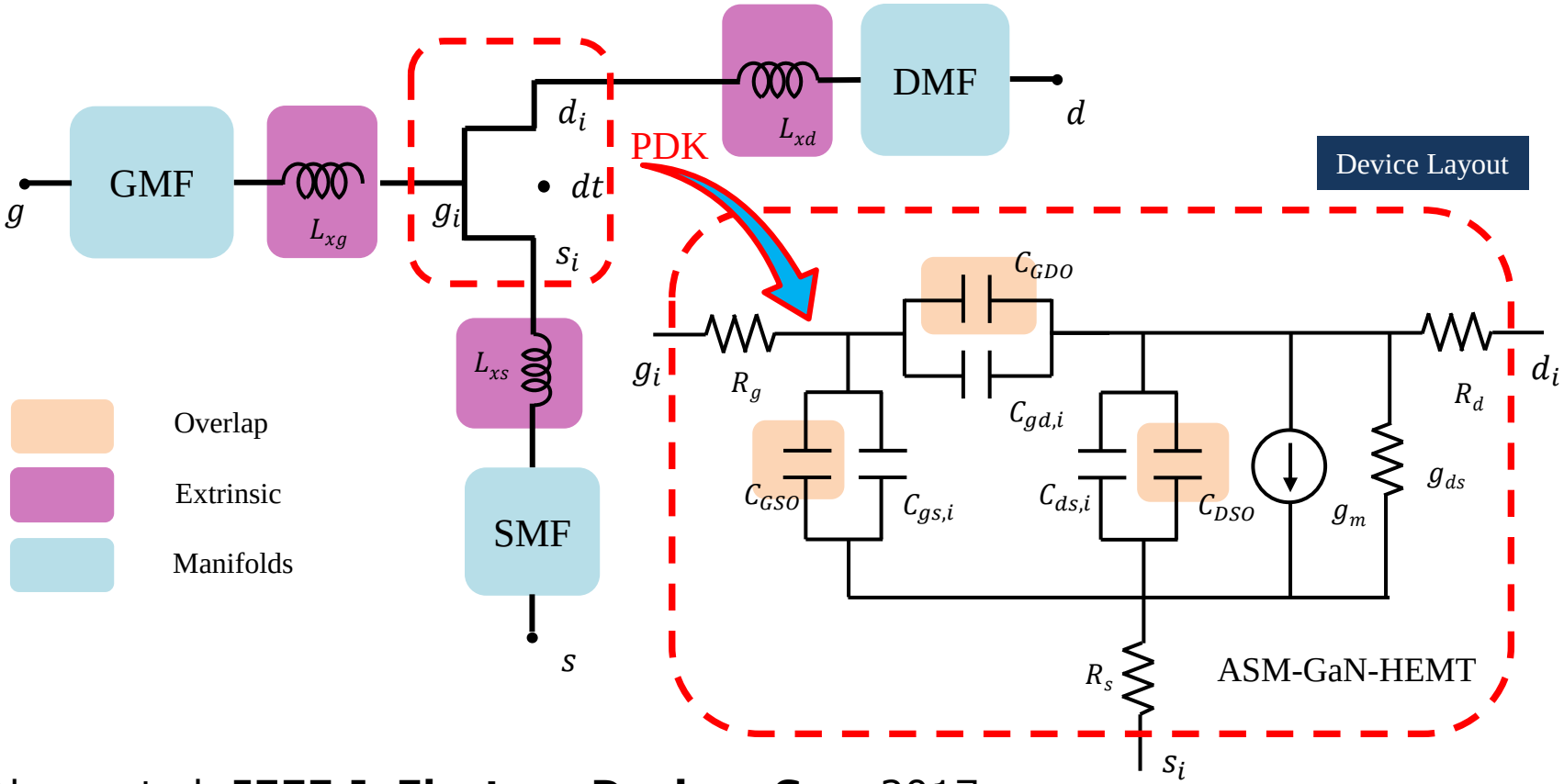
Pulsed – IV chacteristics for multiple quiescent conditions

Pulse Width – 200 ns,
Duty-cycle – 0.02 %

Ahsan et al, **IEEE J. Electron Devices Soc.** 2017

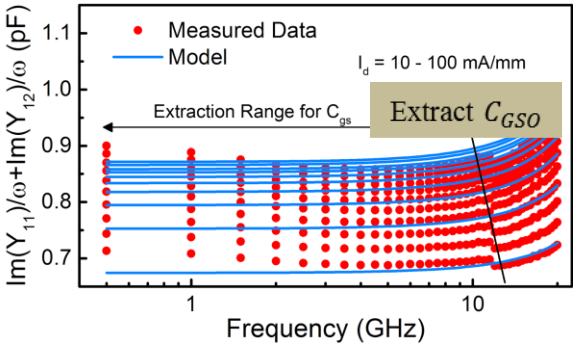
ASM for GaN RF

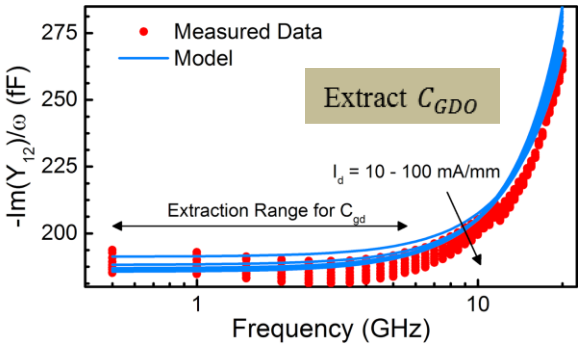
- Model
  - Core surface potential based kit
  - Access region resistances included in core
  - Bus-inductances in extrinsics

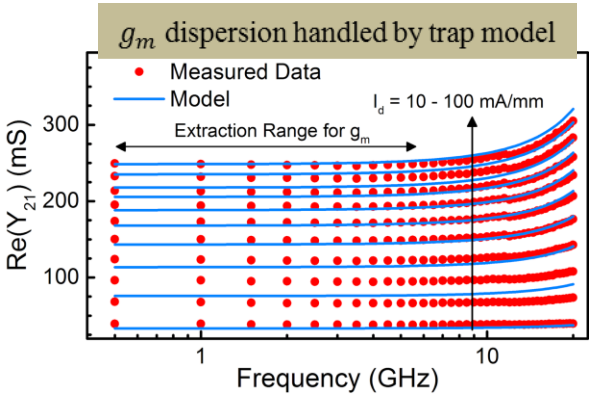


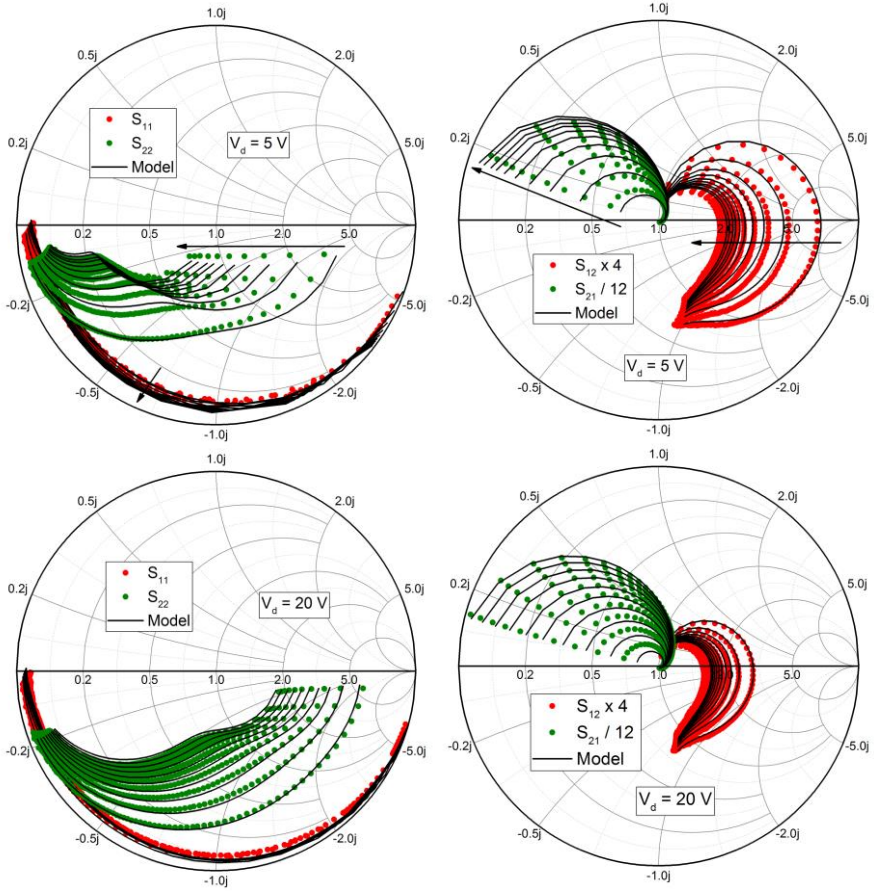
Ahsan et al, **IEEE J. Electron Devices Soc.** 2017

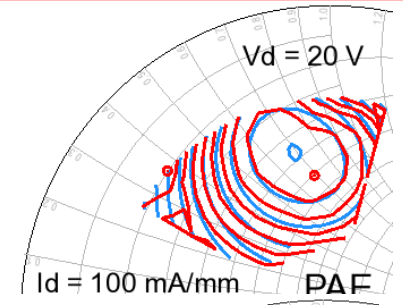
RF Extraction & large-signal model

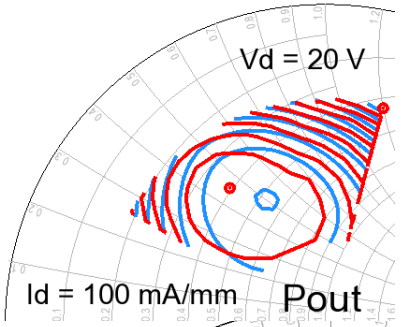


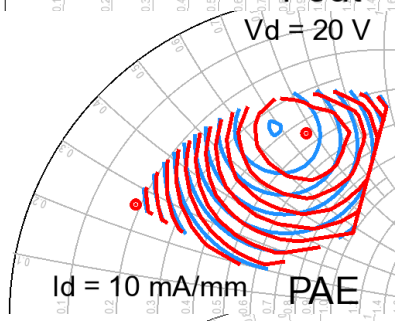


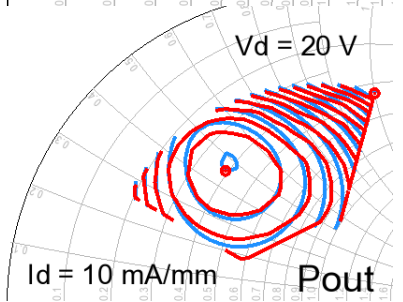












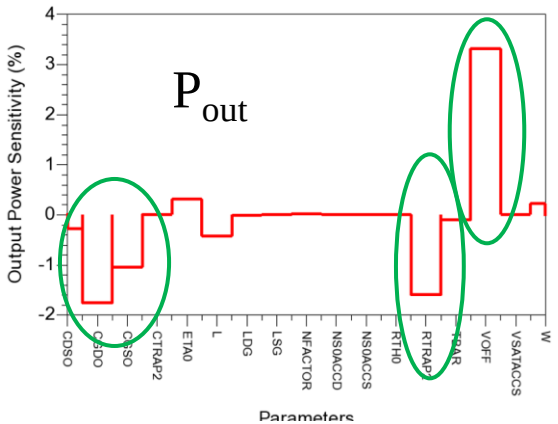
Ahsan et al, **IEEE J. Electron Devices Soc**. 2017

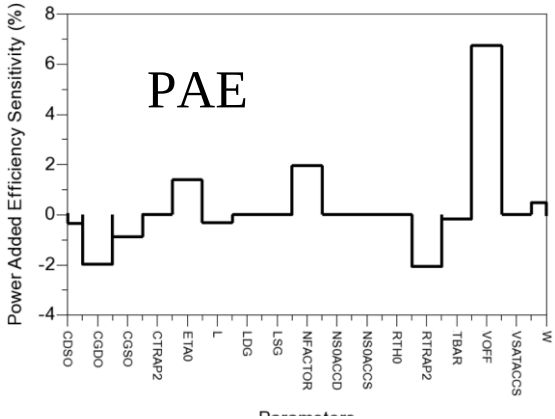
Statistical Simulation - Variability

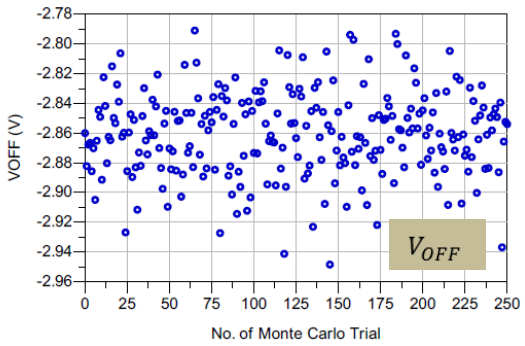
The need for a statistical simulations

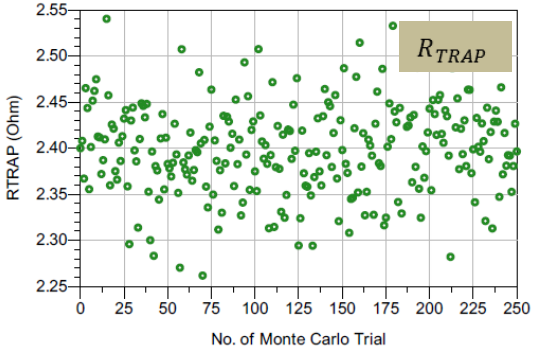
- Variation in device performance
- Obtain a production-level **yield-oriented** optimized circuit design

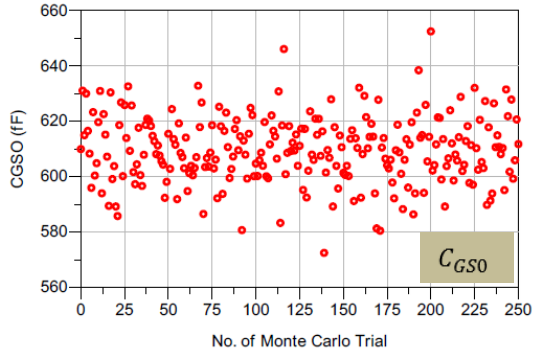
Model Parameter
Width
Length
Access region length
AlGaN Barrier Thickness
Cutoff Voltage
Low Field Mobility
Subthreshold Slope Factor
DIBL Parameter
AR 2DEG Density
AR saturation velocity
Thermal Resistance
Trap Resistance
Gate-Source Overlap Cap.
Gate-Drain Overlap Cap.
Drain-Source Overlap Cap.

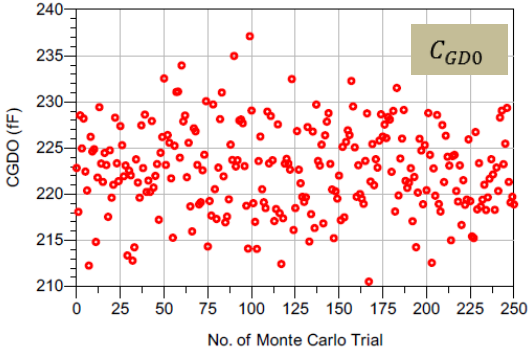






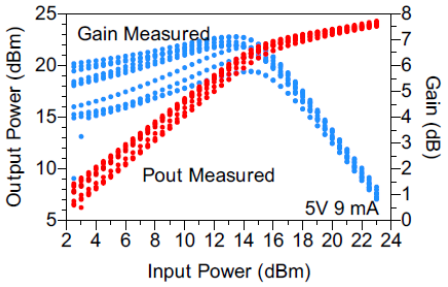


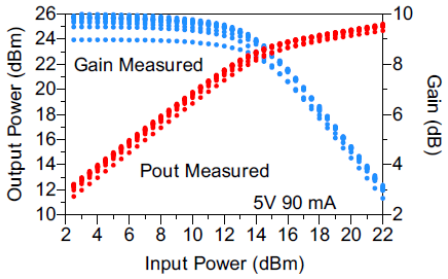


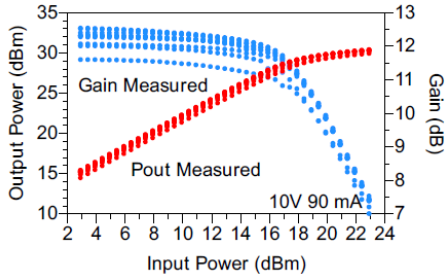


RF Variability results

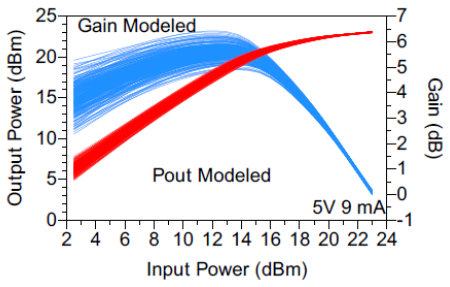
Measured

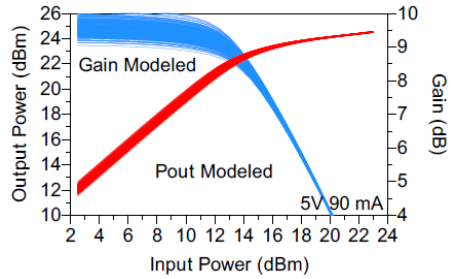


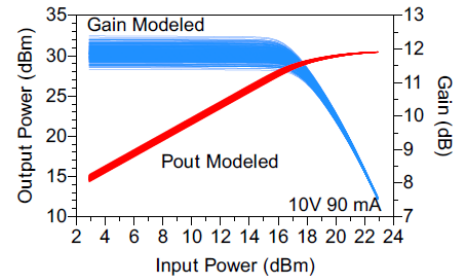




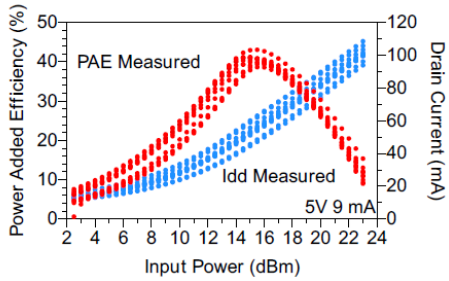
Model

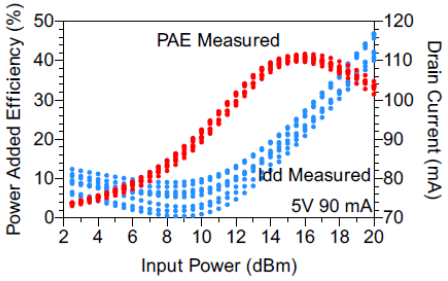


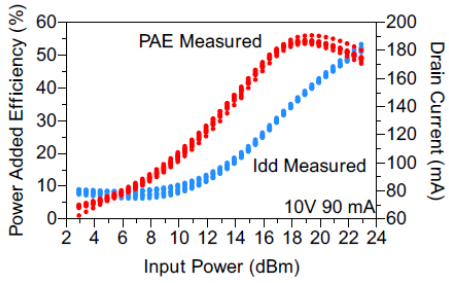




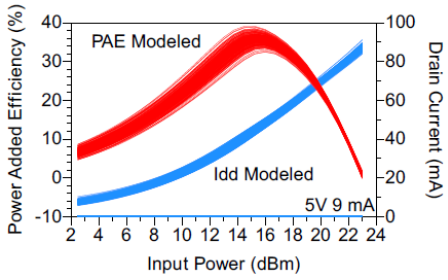
Measured

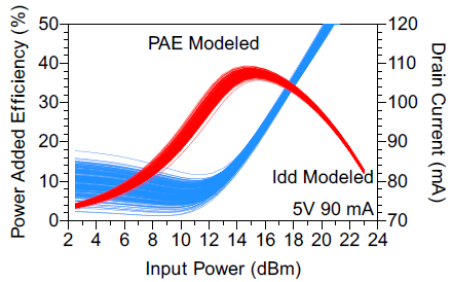


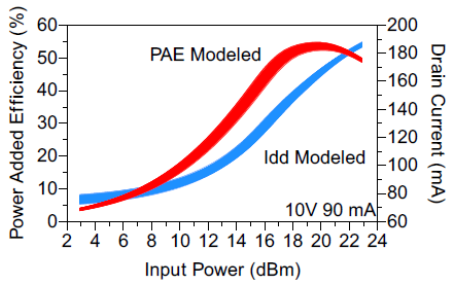




Model



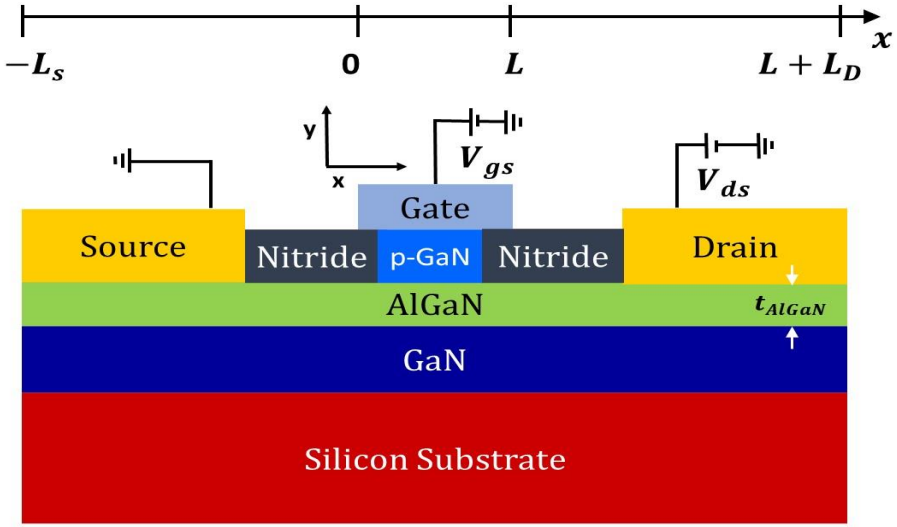


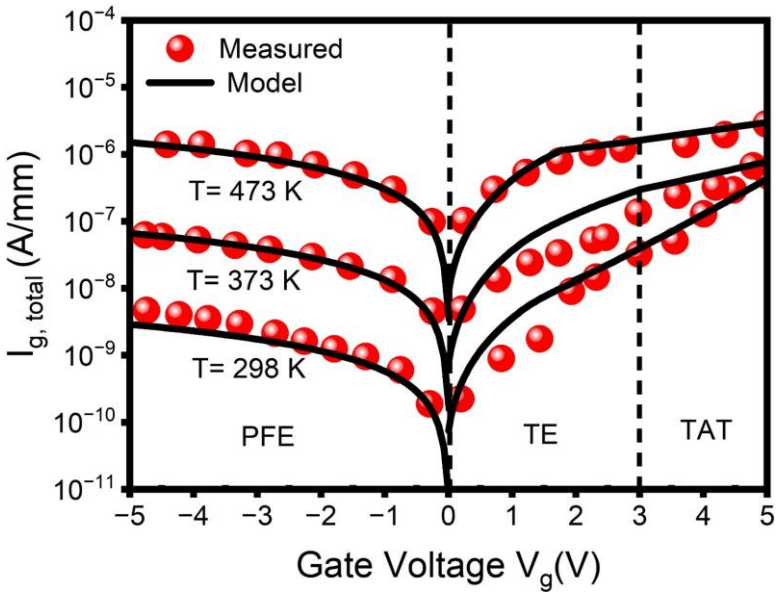


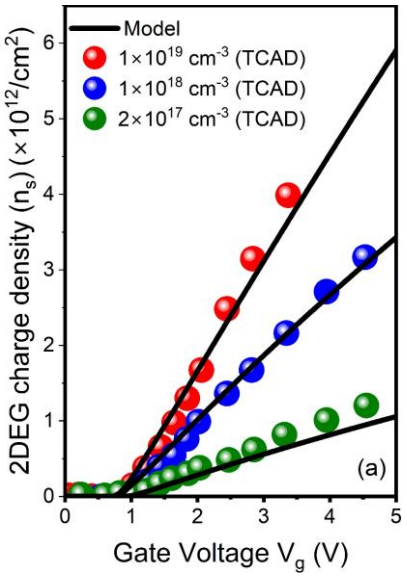
Pout, Gain & PAE & Idd for 250 trials of MC & measured data for a batch of 10 devices

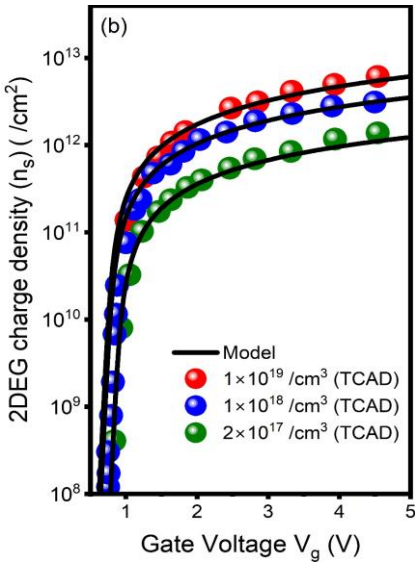
NITSRI-GaN Class of Models

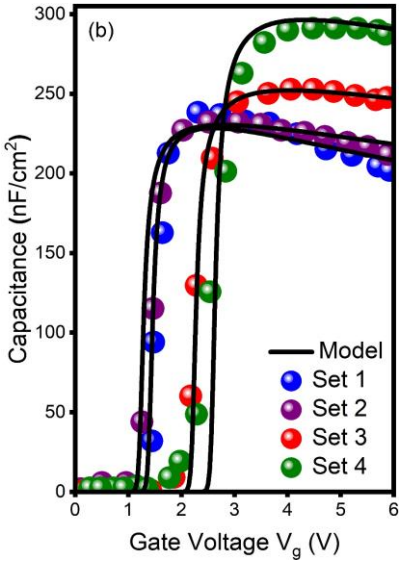
p-GaN HEMTs

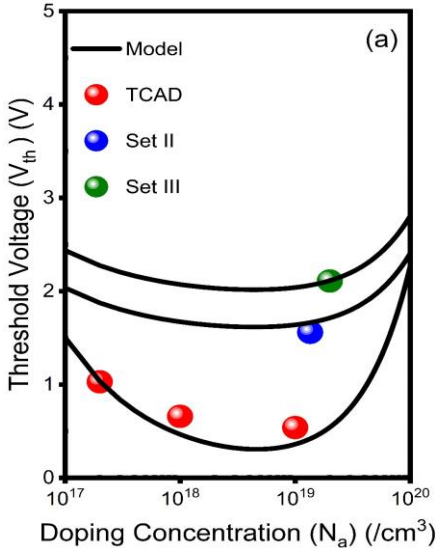






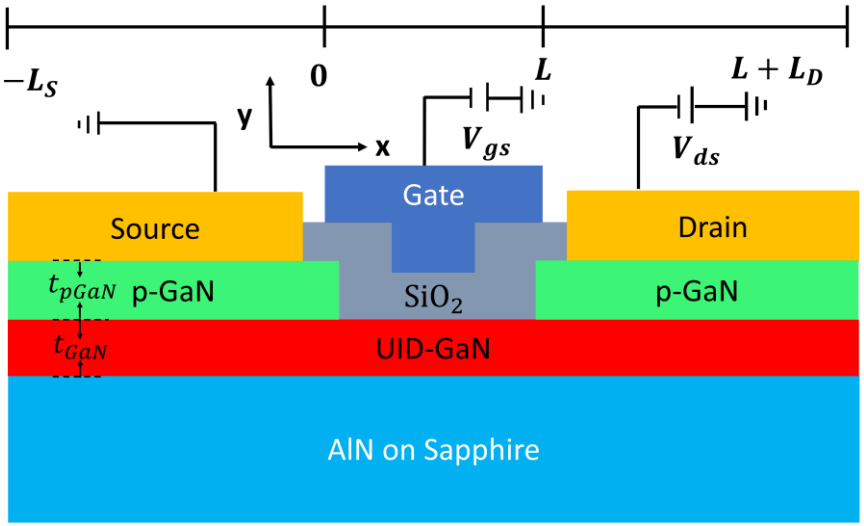


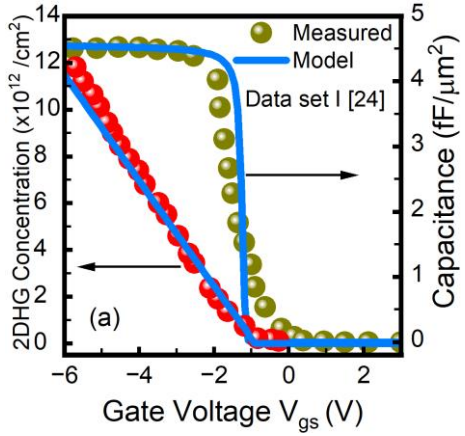


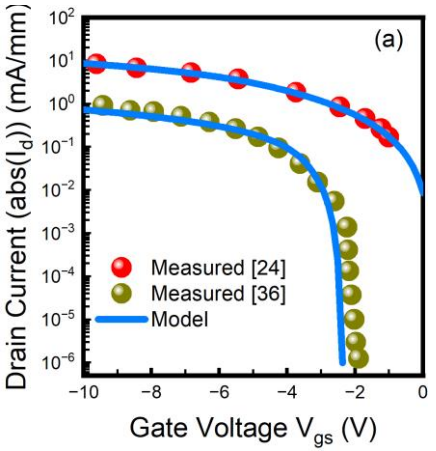


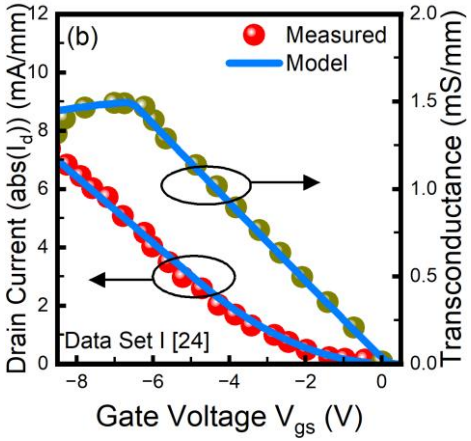
Z. Bhat et al, **IEEE Trans Electron Devices**, vol. 71, no. 3, Mar. 2024

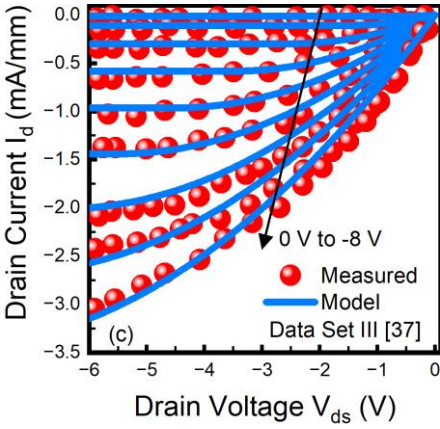
GaN p-Channel FETs











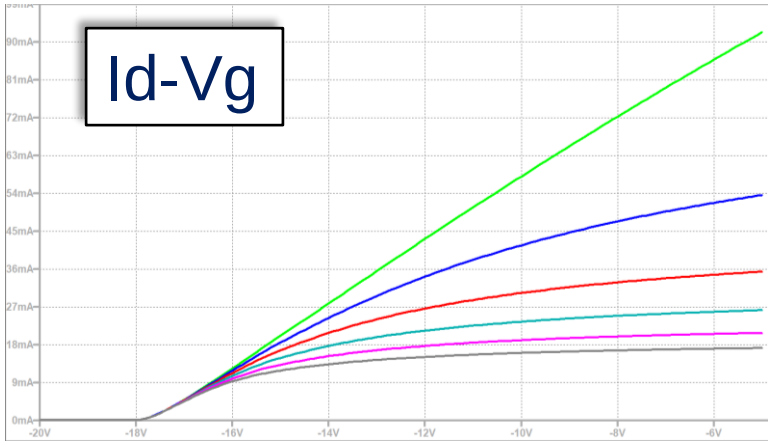
GaN complimentary FETs

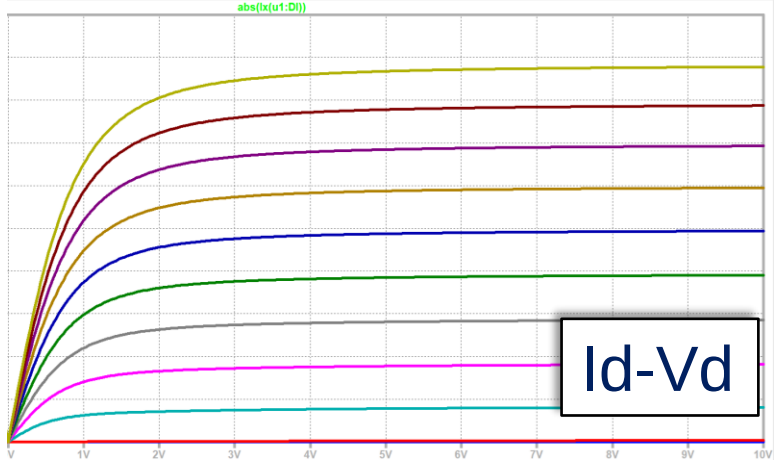
p–channel counterpart

Z. Bhat et al, **IEEE Trans Electron Devices**, vol. 71, no. 3, Mar. 2024

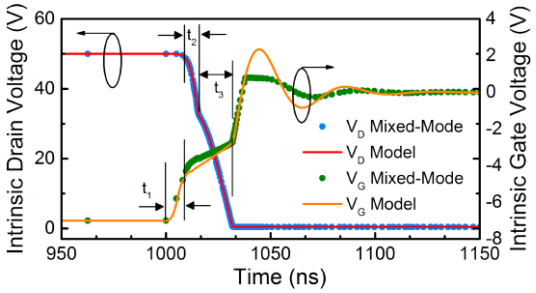
Efforts towards open-source / free models

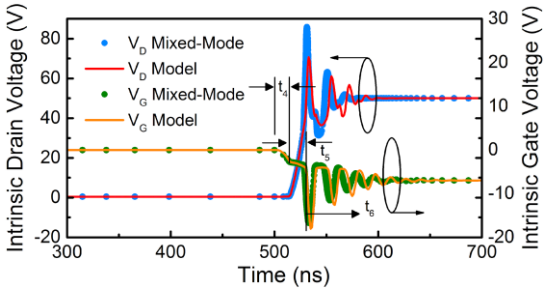
- Implementation of the Verilog-A model in free softwares – LTSPICE, Microcap, PSPICE libraries
- This feature is not available in the standard CMC ASM

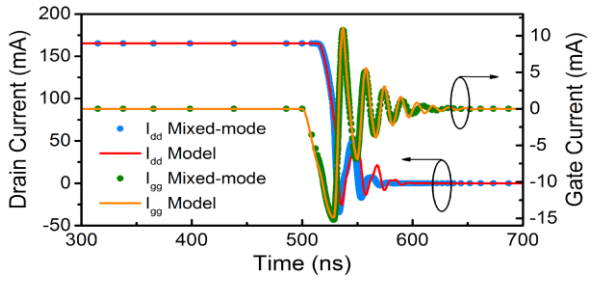




Transients Behavior







Call to action – the value huddle

Governments: Joint undertakings and policy

Academic Researchers & R&D Orgs:

New Technology Development and Transfer

GaN Industry:

Foundries and Appl. developers

Sub-systems and Tech Industry:

Automotive, Consumer, Comm

Open-Source:

Design frameworks & Models

Summary

India and EU common goal towards **Net-Zero**
GaN – promise in the **RF** and **power electronics** market
Device topologies
    pGaN, Cascode, Double Channel, Active Passivation etc
    Graded buffer - linearity
Models – **Industry Standards**:
    MIT VS, Angelov
    ASM: Surface-potential (Physics-based)
NITSRI GaN Class of Models
Essential to have **open-source** models
Joint initiative between different stakeholders

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Thank You!