The Dawn of the New Electronics Industry

(Surfing on Chips Acts Waves)

Paolo Gargini

Chairman IRDS

Chairman ICOS IAB*

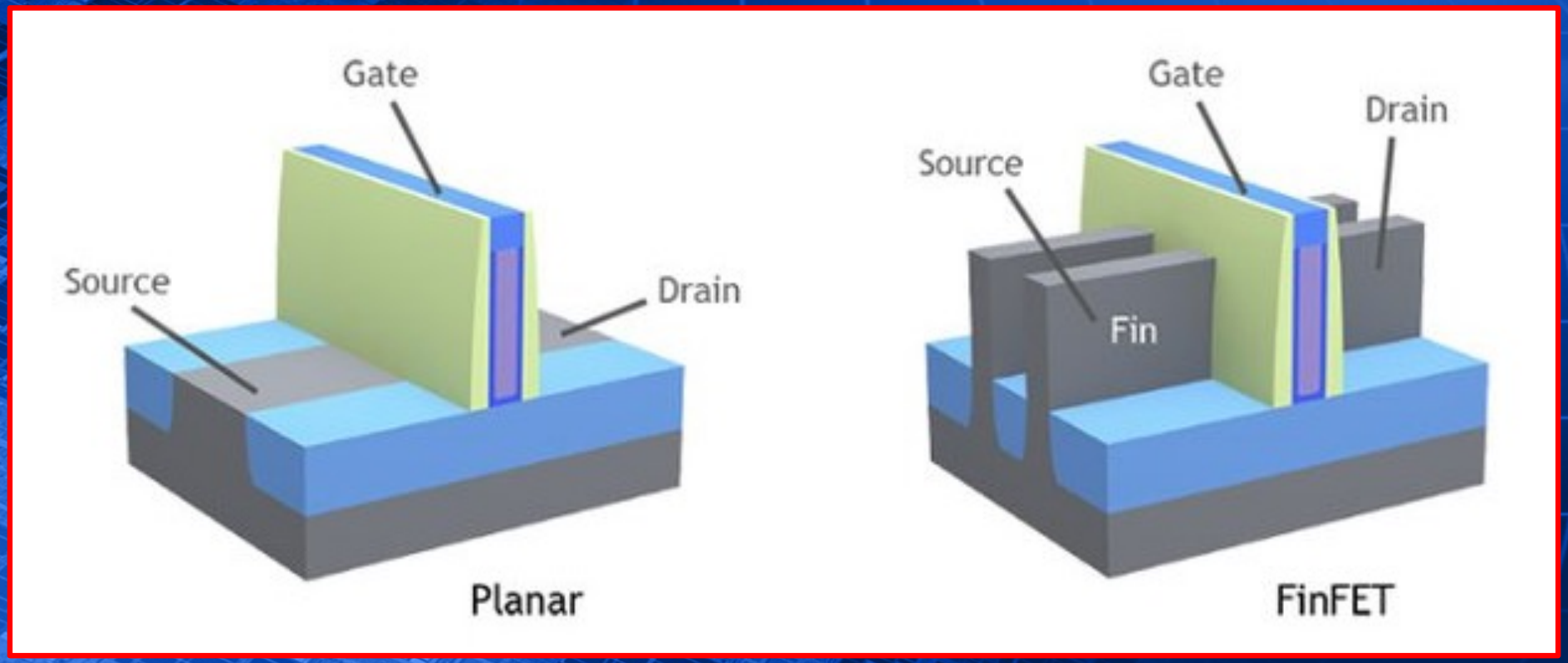
Life-Fellow IEEE, Fellow I-JSAP

* International Advisory Board

Shockers involving Governments occur every 20 years

1. 1957: Sputnik
2. 1987: US DRAM Collapse
3. 1997: Gate oxide vanishing by 2005
4. 2020: Pandemic

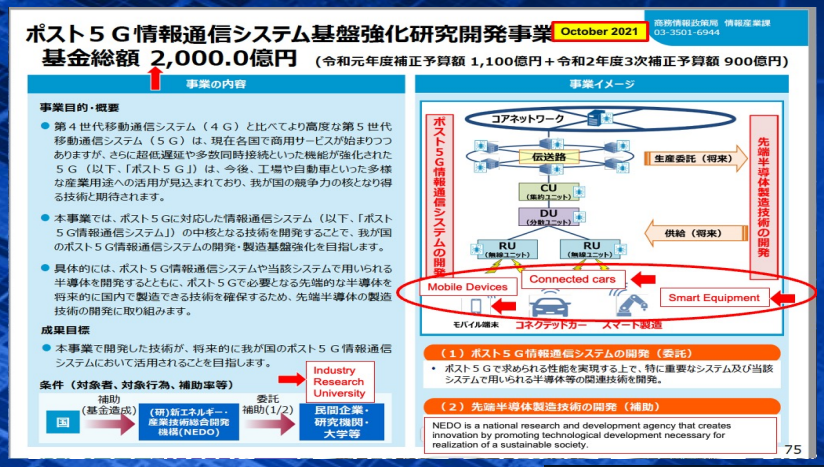
1965-2011: From Planar Transistor to FinFET



Fourth Shocker


COVID - 19
CHANGES AND CHALLENGES
A Picture Collage
January 2020
COVID - 19

Governments Investing Hundreds of $Billions



May 2022

Investments to support the Chips Act Europe

The Chips Act itself should result in additional public and private investments of more than €15 billion.

These investments will complement:

- existing programmes and actions in research and innovation in semiconductors such as Horizon Europe and the Digital Europe programme
- announced support by Member States

In total, more than €43 billion of policy-driven investment will support the Chips Act until 2030, which will be broadly matched by long-term private investment.

The Chips Act proposes:

- Investments in next-generation technologies
- Providing access across Europe to design tools and pilot lines for the prototyping, testing and experimentation of cutting-edge chips
- Certification procedures for energy-efficient and trusted chips to guarantee quality and security for critical applications
- A more investor-friendly framework for establishing manufacturing facilities in Europe
- Support for innovative start-ups, scale-ups and SMEs in accessing equity finance
- Fostering skills, talent and innovation in microelectronics
- Tools for anticipating and responding to semiconductors shortages and crises to ensure security of supply
- Building semiconductor international partnerships with like-minded countries

CHIPS Act At A Glance

Creating **H**elpful **I**ncentives to **P**roduce **S**emiconductors for America (CHIPS Act)

$52 billion total budget over 5 years

Financial Incentives Programs	Research and Development
$39 billion	$11 billion Technology Center Packaging Program MFG USA Institute(s) Metrology program

Workforce Development

US Code: 15 USC 4652: Semiconductor incentives

IEEE ICOS IRDS International Roadmap for Devices and Systems

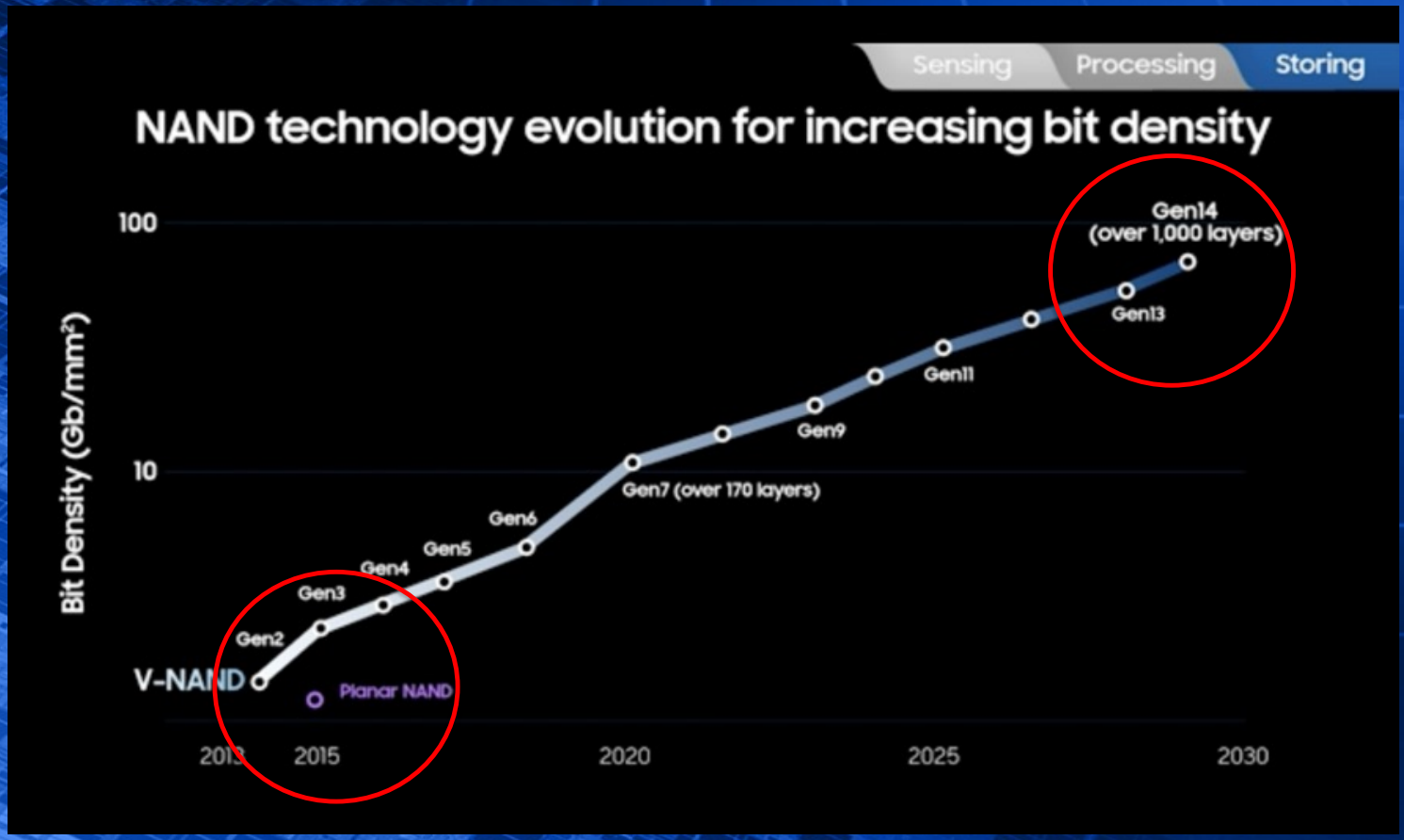
2016

The New Electronics Industry

- 3D Transistors
- Beyond Silicon
- 3D Everything
- System In Package
- New Products
- New Architecture
- SOC: Endless Die Size
- SOC and SIP

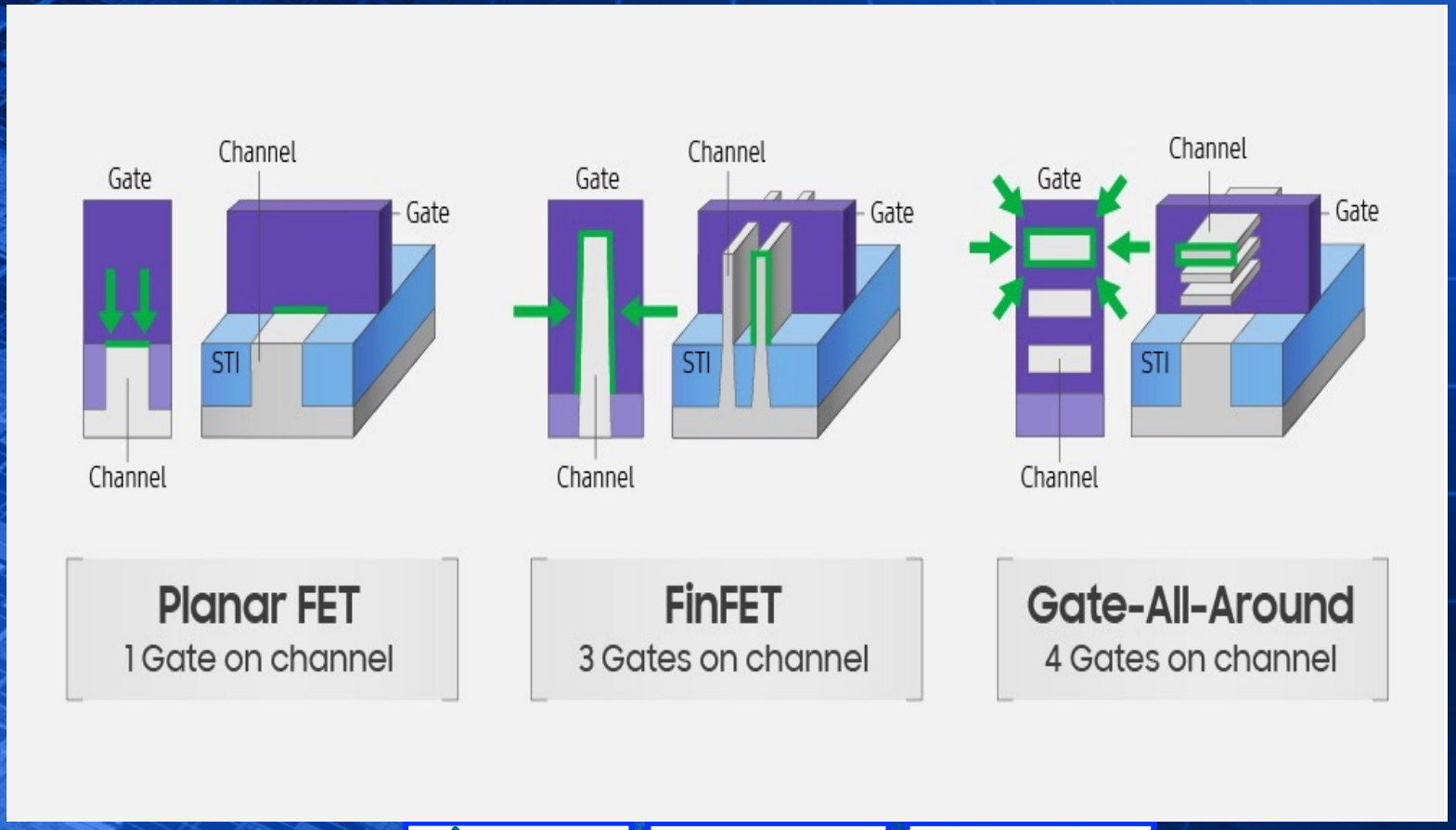
ITRS, ITRS 2.0, and IRDS FORECAST

Samsung, IEDM 2021



ITRS, ITRS 2.0, and IRDS FORECAST

3 Steps to Surrounding the Channel

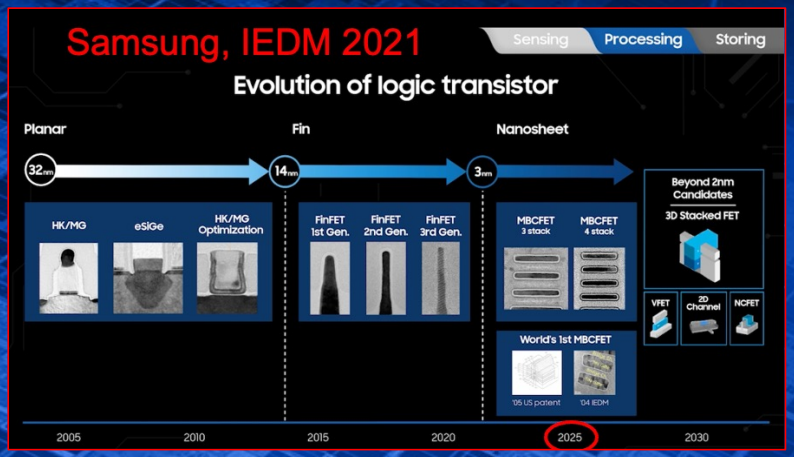


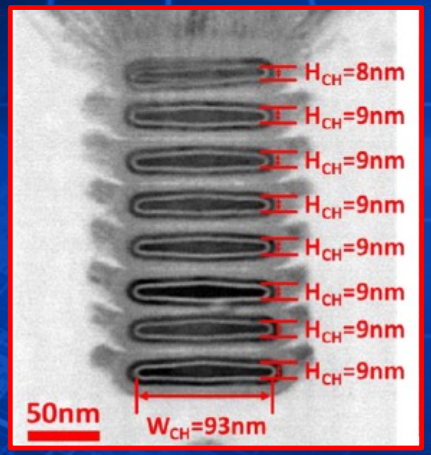
2018 IRDS

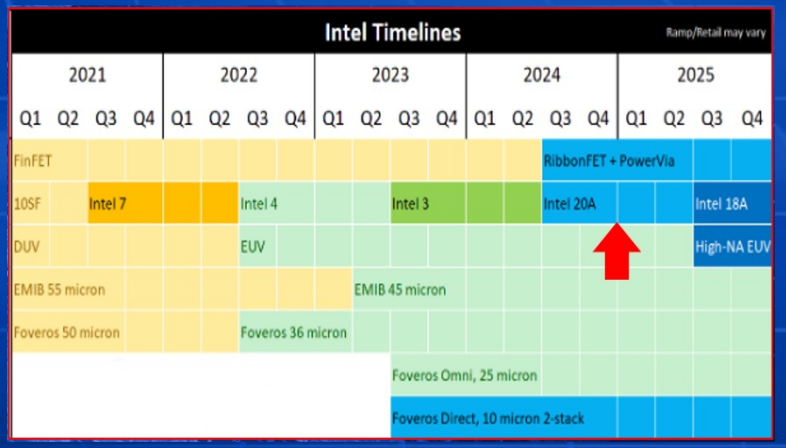
YEAR OF PRODUCTION	2018	2020	2022	2025	2028	2031	2034
	G54M36	G48M30	G45M24	G42M21	G40M16	G40M16T2	G40M16T4
Logic industry "Node Range" Labeling (nm)	"7"	"5"	"3"	"2.1"	"1.5"	"1.0 eq"	"0.7 eq"
IDM-Foundry node labeling	i10-i7	i7-i5	i5-i3	i3-i2.1	i2.1-i1.5	i1.5e-i1.0e	i1.0e-i0.7e
Logic device structure options	FinFET	finFET	finFET LGAA	LGAA	LGAA VGAA	LGAA-3D VGAA	LGAA-3D VGAA
Mainstream device for logic	finFET	finFET	finFET	LGAA	LGAA	LGAA-3D	LGAA-3D
							
LOGIC DEVICE GROUND RULES							
Mx pitch (nm)	40	36	32	24	20	16	16
M1 pitch (nm)	36	32	30	21	20	20	20
M0 pitch (nm)	36	30	24	21	16	16	16
Gate pitch (nm)	54	48	45	42	40	40	40
L_g: Gate Length - HP (nm)	20	18	16	14	12	12	12
Lg: Gate Length - HD (nm)	22	20	18	14	12	12	12
Channel overlap ratio - two-sided	0.20	0.20	0.20	0.20	0.20	0.20	0.20
Spacer width (nm)	8	7	6	6	6	6	6
Contact CD (nm) - finFET, LGAA	18	16	17	16	16	16	16
Contact CD (nm) - VGAA							
Device architecture key ground rules							
FinFET pitch (nm)	32.0	28.0	24.0				
FinFET Fin width (nm)	8.0	7.0	6.0				
FinFET Fin height (nm)	40	50	60				
Footprint drive efficiency - finFET	2.75	3.82	5.25				
Lateral GAA lateral pitch (nm)				22.0	20.0	20.0	20.0
Lateral GAA vertical pitch (nm)				18.0	16.0	14.0	14.0
Lateral GAA (nanosheet) thickness (nm)				7.0	6.0	5.0	5.0
Number of vertically stacked nanosheets				3	3	4	4
LGAA width (nm) - HP				25	20	15	10
LGAA width (nm) - HD				15	11	6	6
LGAA width (nm) - SRAM				7	6	6	6
LGAA total height (nm)				53	48	57	57
Footprint drive efficiency - lateral GAA - HP				4.80	4.59	5.52	5.00
Device effective width (nm) - HP	88.0	107.0	126.0	192.0	156.0	160.0	120.0
Device effective width (nm) - HD	88.0	107.0	126.0	132.0	102.0	88.0	88.0
Device lateral pitch (nm)	32	28	24	22	20	20	20
Device height (nm)	40.0	50.0	60.0	53.0	48.0	57.0	57.0
Device width (nm) - HP	8	7	6	25	20	15	10
Device width (nm) - HD	8	7	6	15	11	6	6
Device width (nm) - SRAM	8	7	6	7	6	6	6

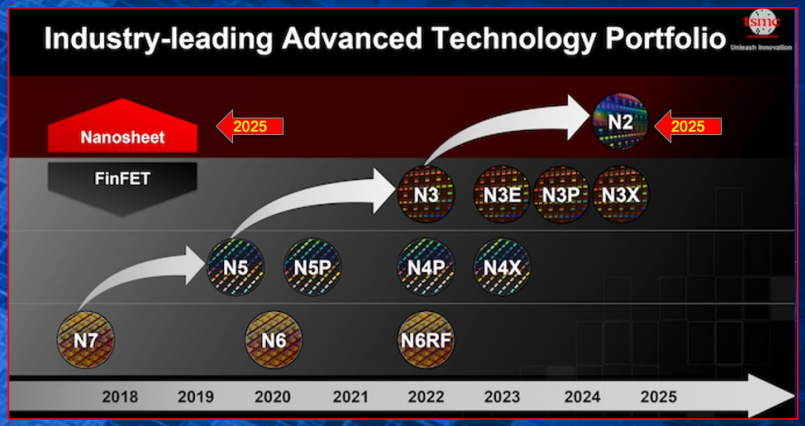
Acronyms used in the table (in order of appearance): FDSOI—fully-depleted silicon-on-insulator, LGAA—lateral gate-all-around-device (GAA), VGAA—vertical GAA, 3DVLSI—fine-pitch 3D logic sequential integration.

Gate All Around (GAA) by nanosheets technology in 2024-5

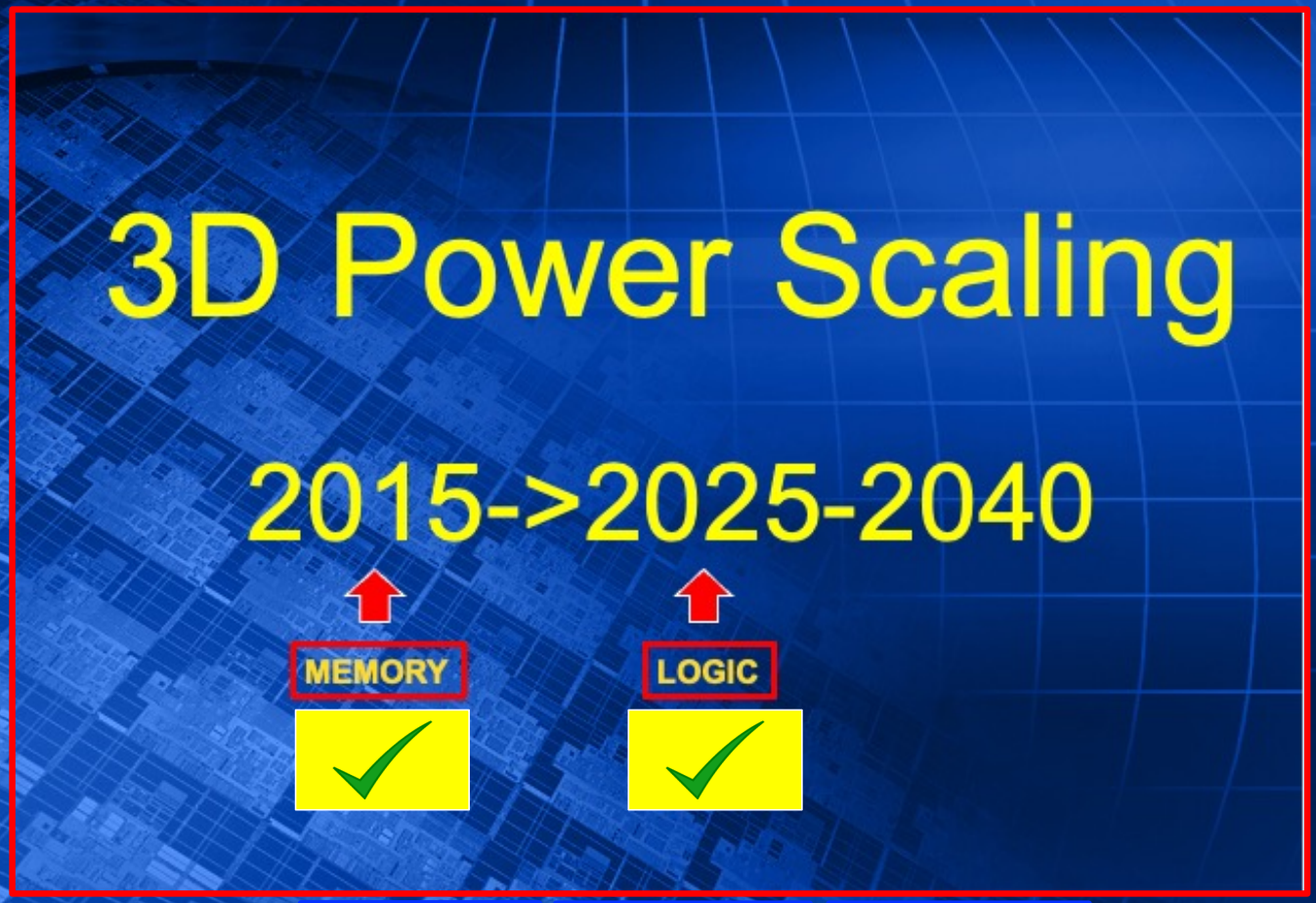






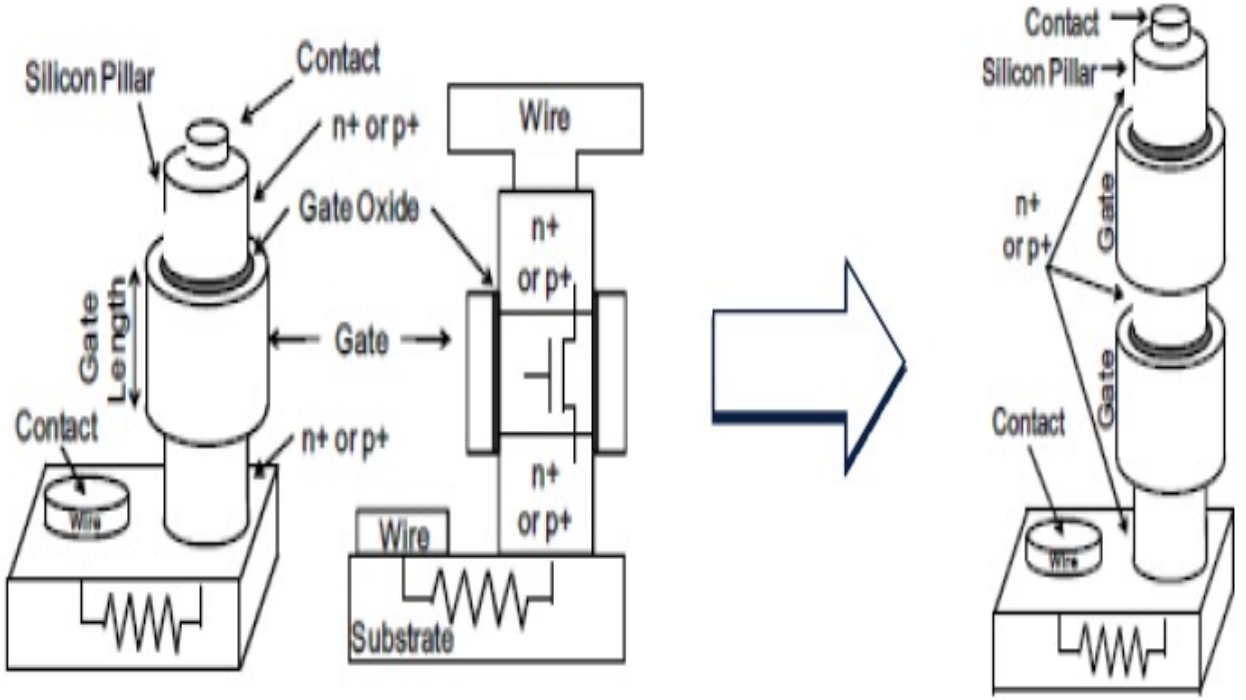


ITRS, ITRS 2.0, and IRDS FORECAST

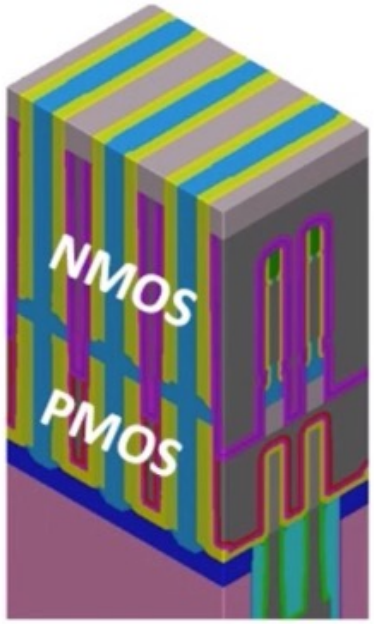


What Comes Next?

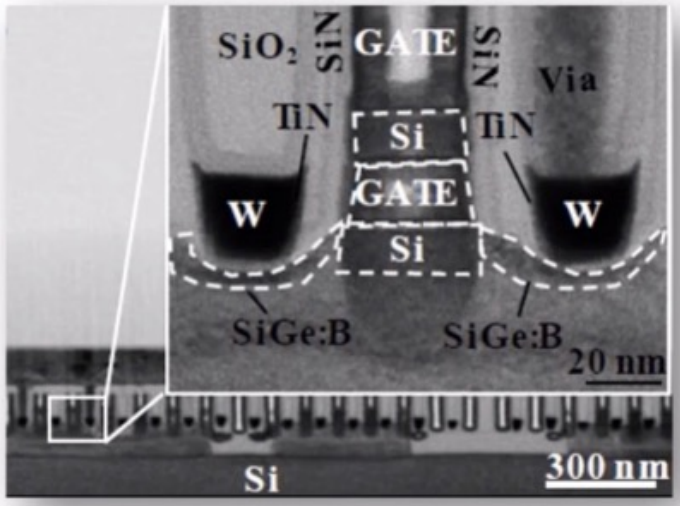
Vertical Logic Architecture 2015



Complementary FET (CFET)



CFET



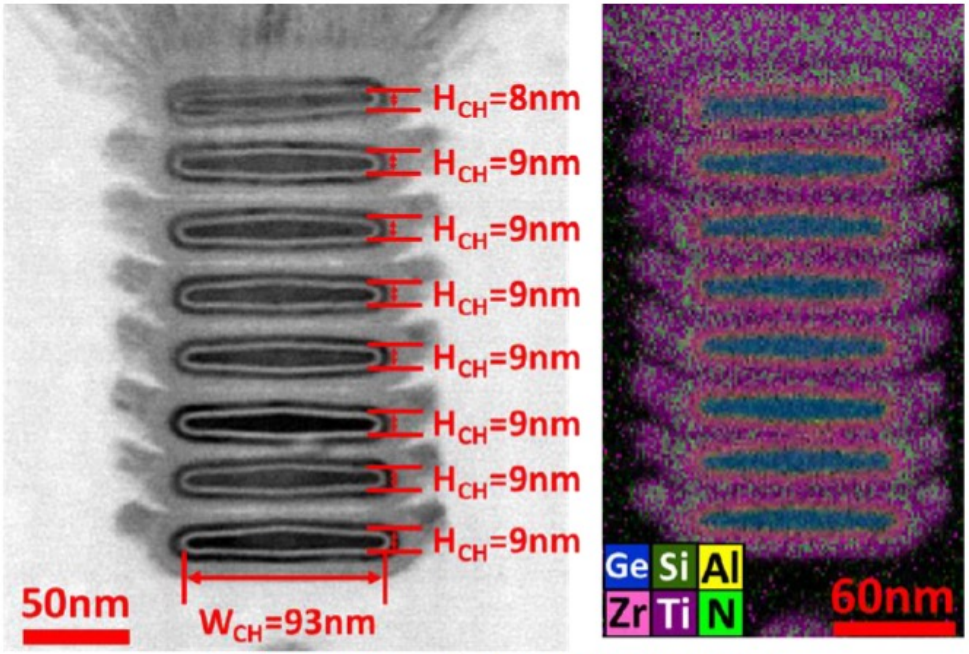
Monolithic Approach

S. Subramanian, VLSI 2020

Highly Stacked Channels

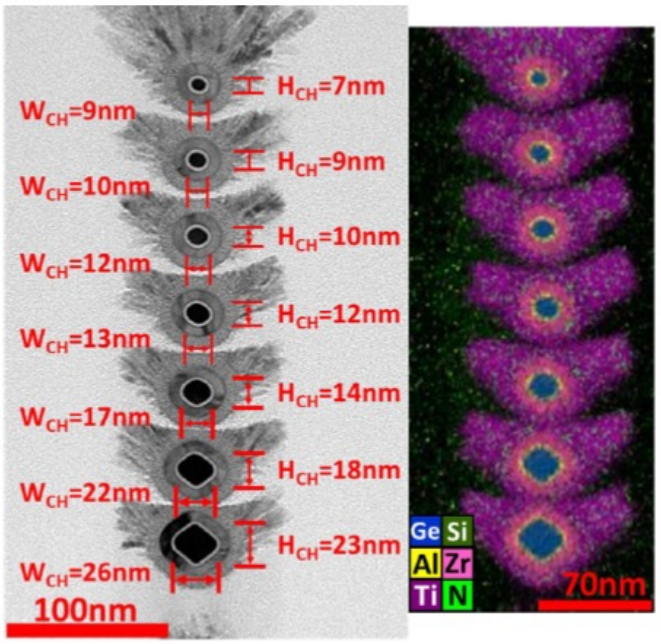
$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{OV}^{\ 2}$$: Highly stacked channels

8 $Ge_{0.75}Si_{0.25}$ Nanosheets



Yi-Chun Liu *et al.*, *VLSI*, 2021, T15-2.

7 $Ge_{0.95}Si_{0.05}$ Nanowires



Yi-Chun Liu *et al.*, *VLSI*, 2021, T15-2.

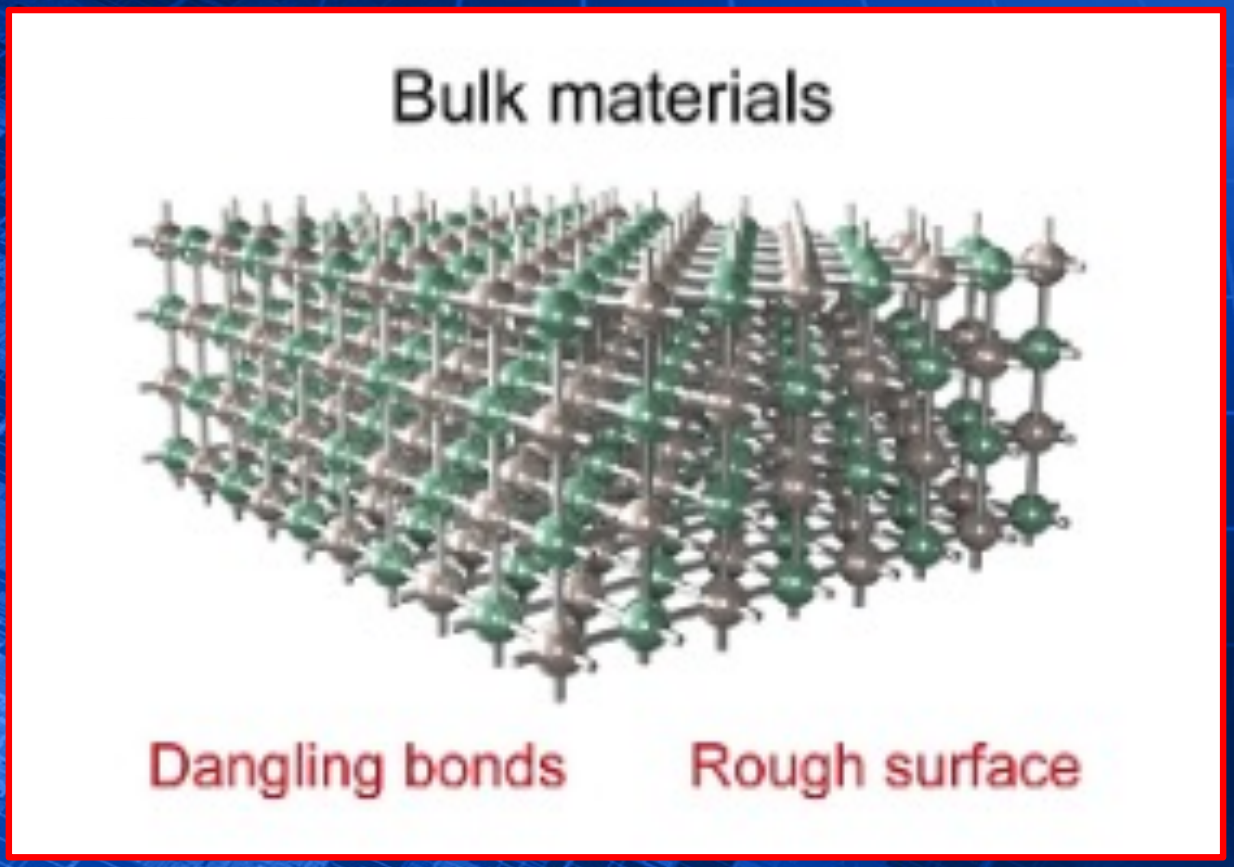
- The higher number of stacked channels can further improve the I_{ON} for the fixed footprint.

The New Electronics Industry

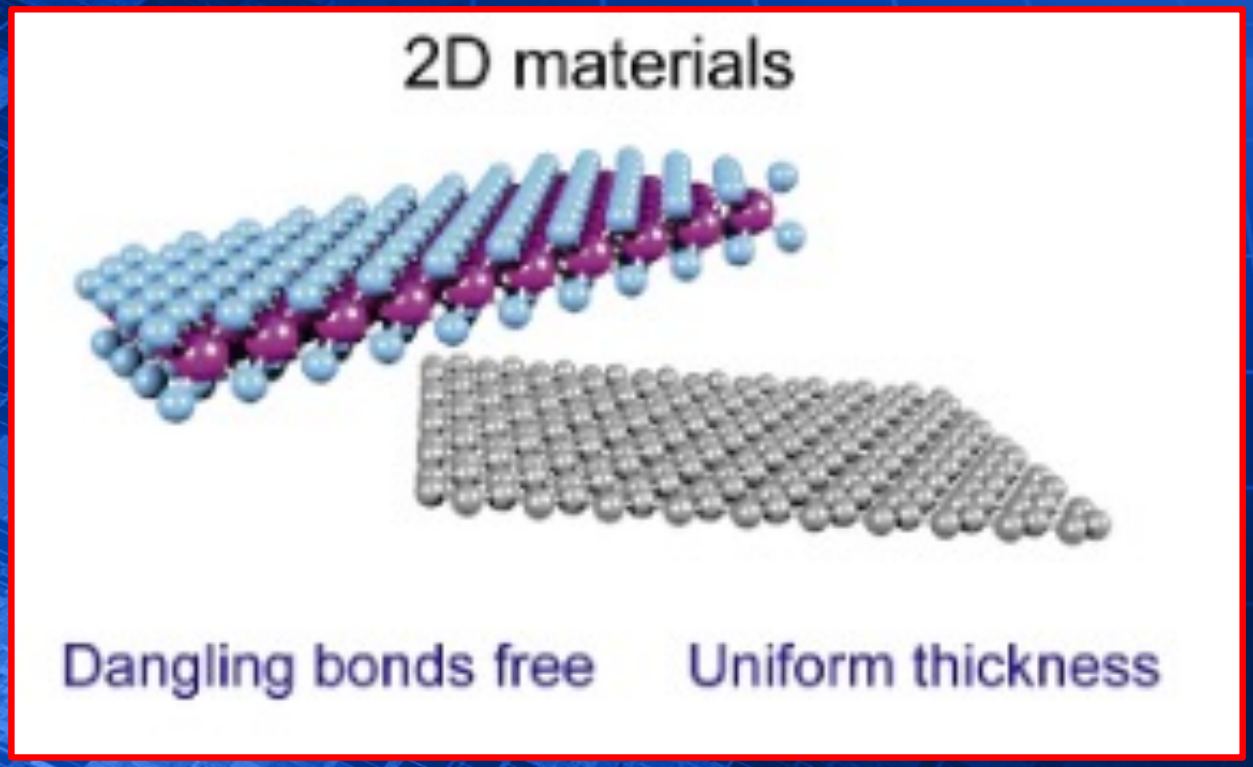
- 3D Transistors
- Beyond Silicon
- 3D Everything
- System In Package
- New Products
- New Architecture
- SOC: Endless Die Size
- SOC and SIP

GAA
Beyond Silicon

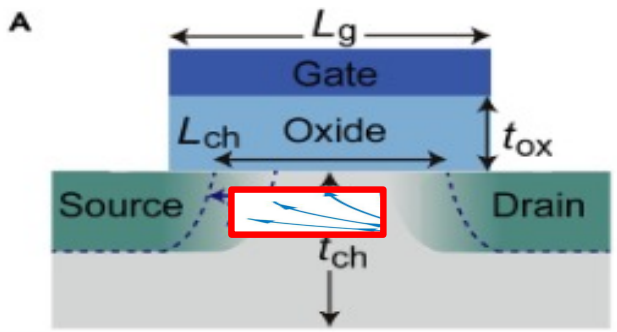
Intrinsic Challenges of Bulk Material

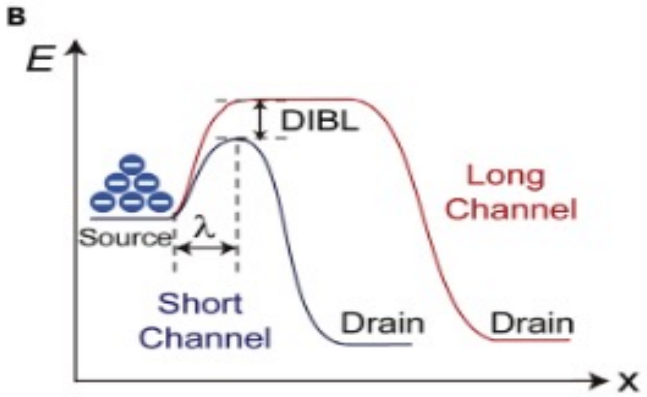


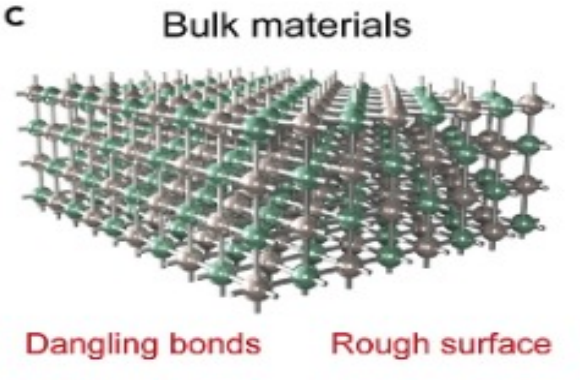
2D Materials

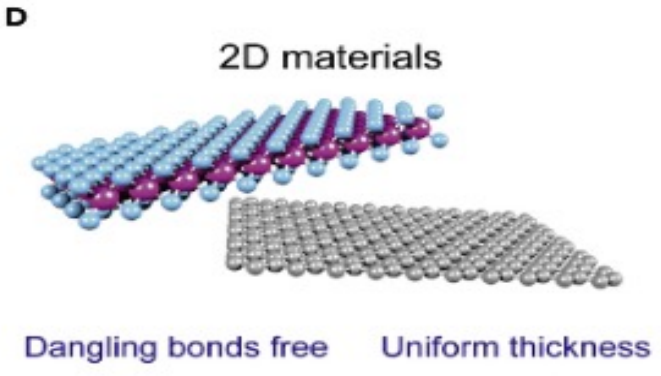


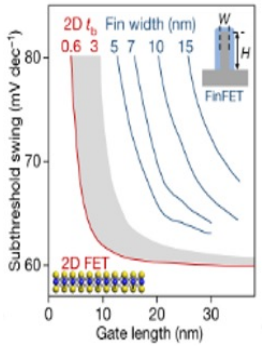
Towards Elimination of Dangling Bonds

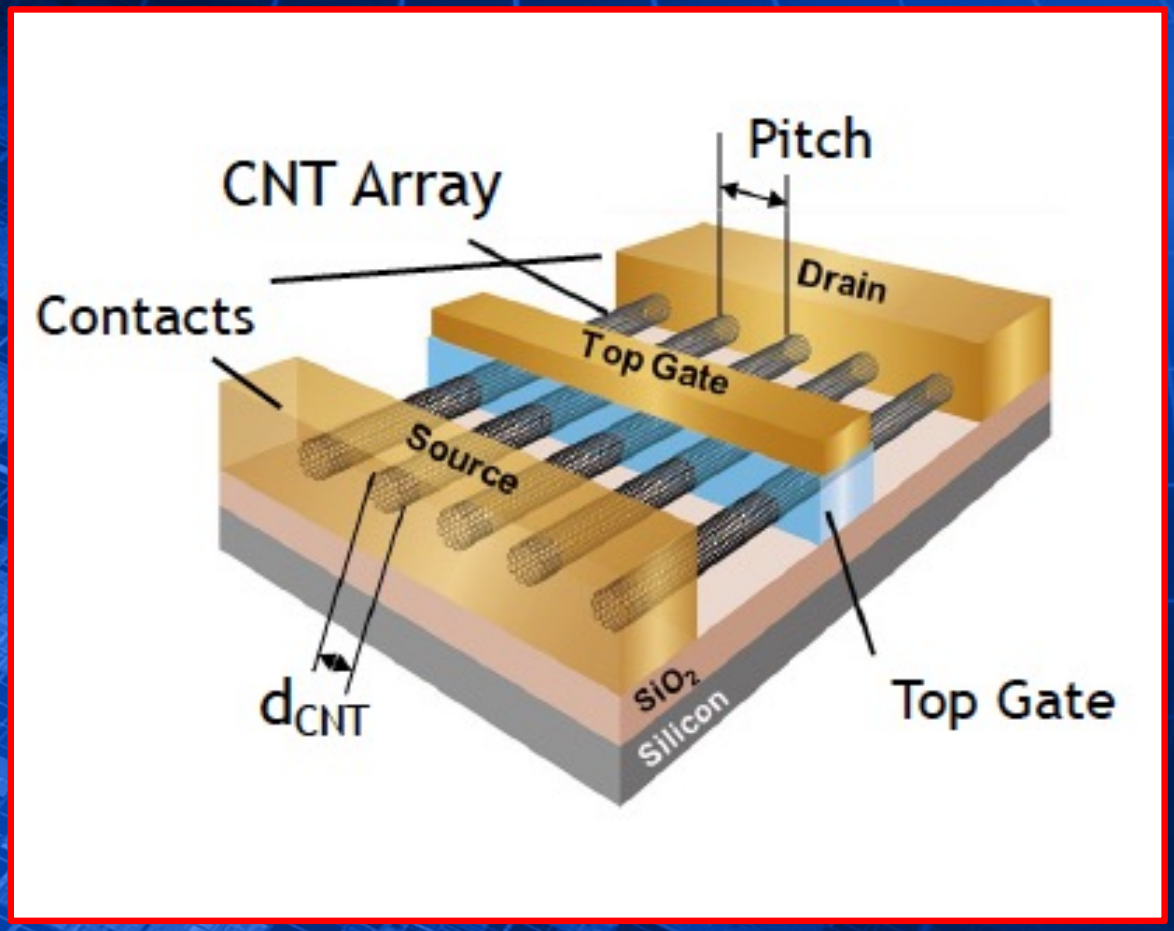




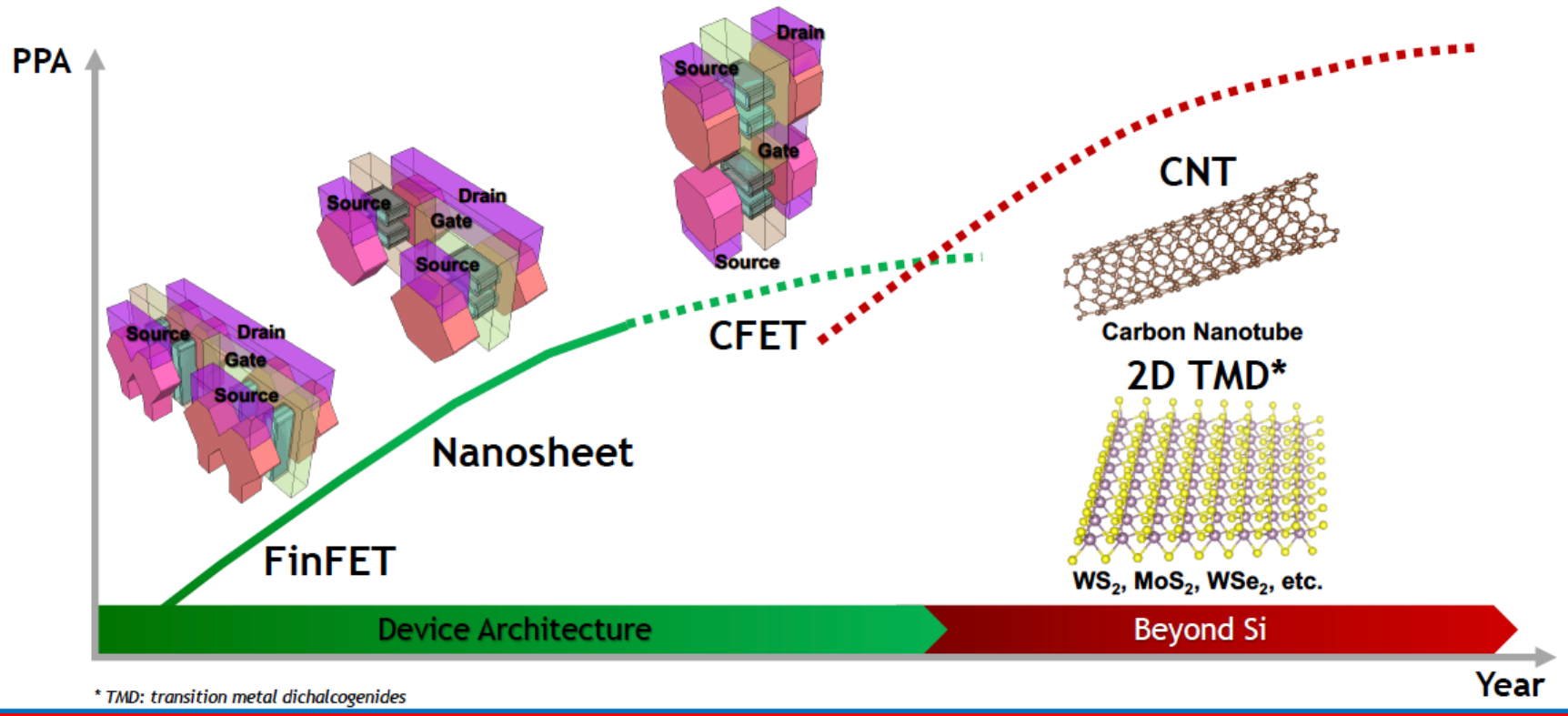







Pitch
CNT Array
Drain
Contacts
Top Gate
Source
d_{CNT}
SiO_2
Silicon
Top Gate

Device Architecture Outlook



* TMD: transition metal dichalcogenides

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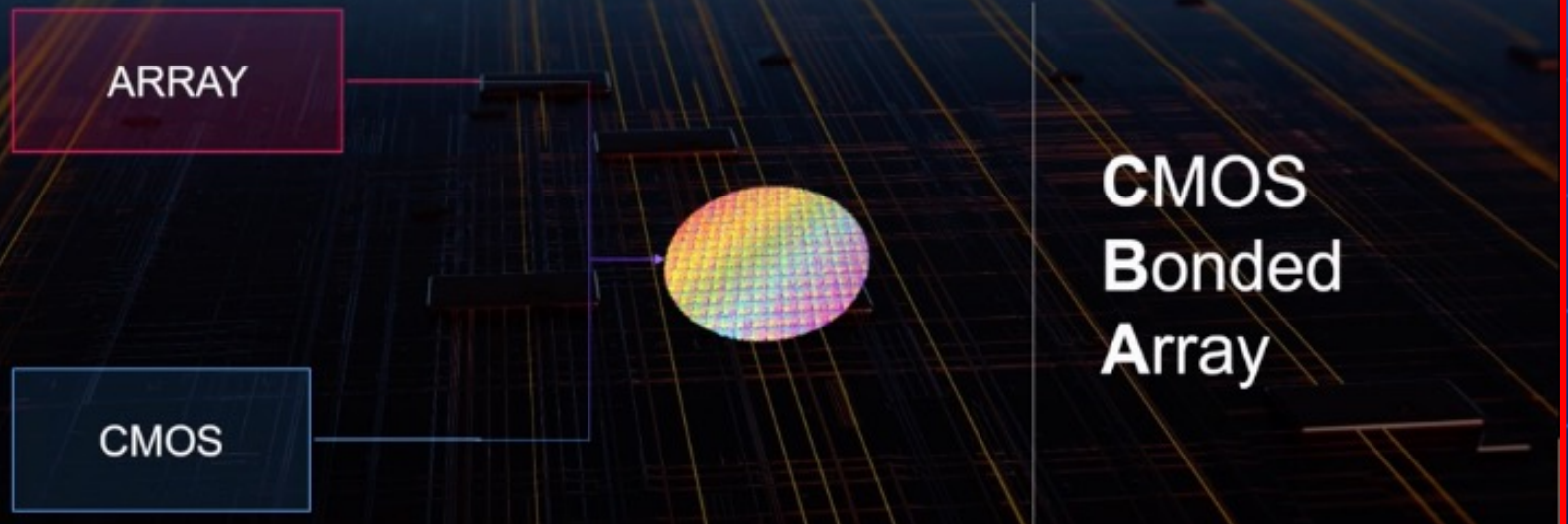
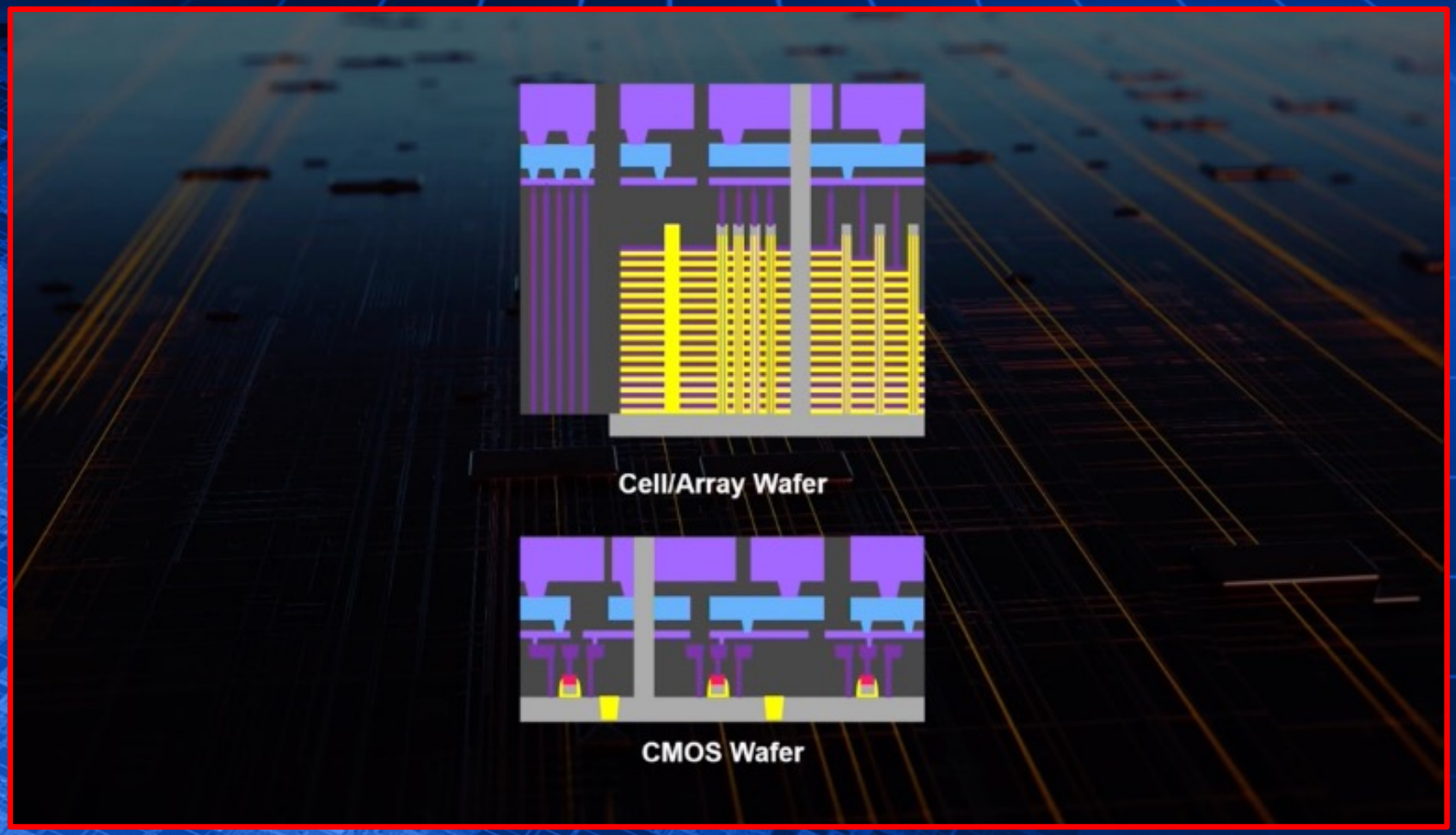
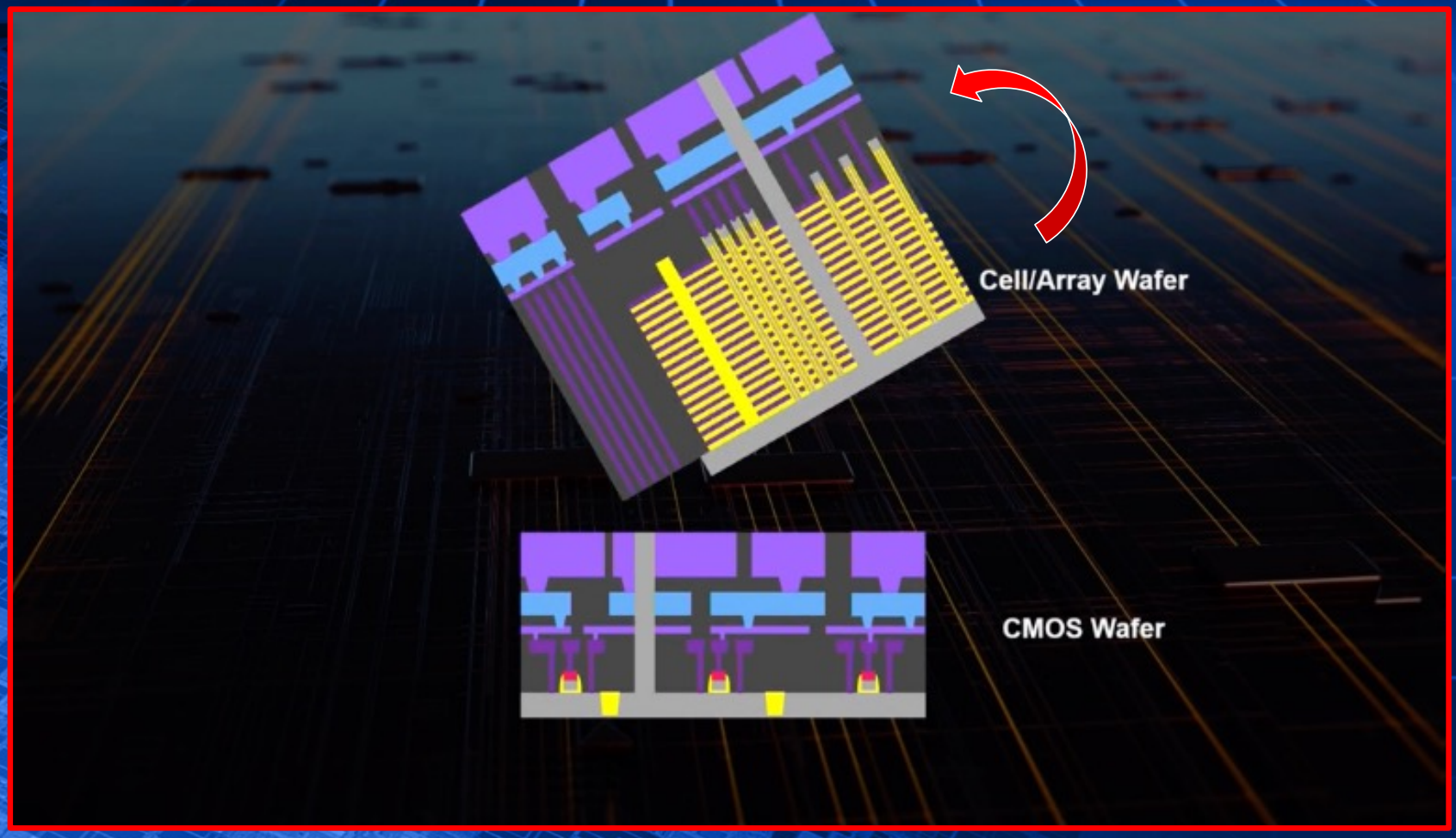
3D Everything

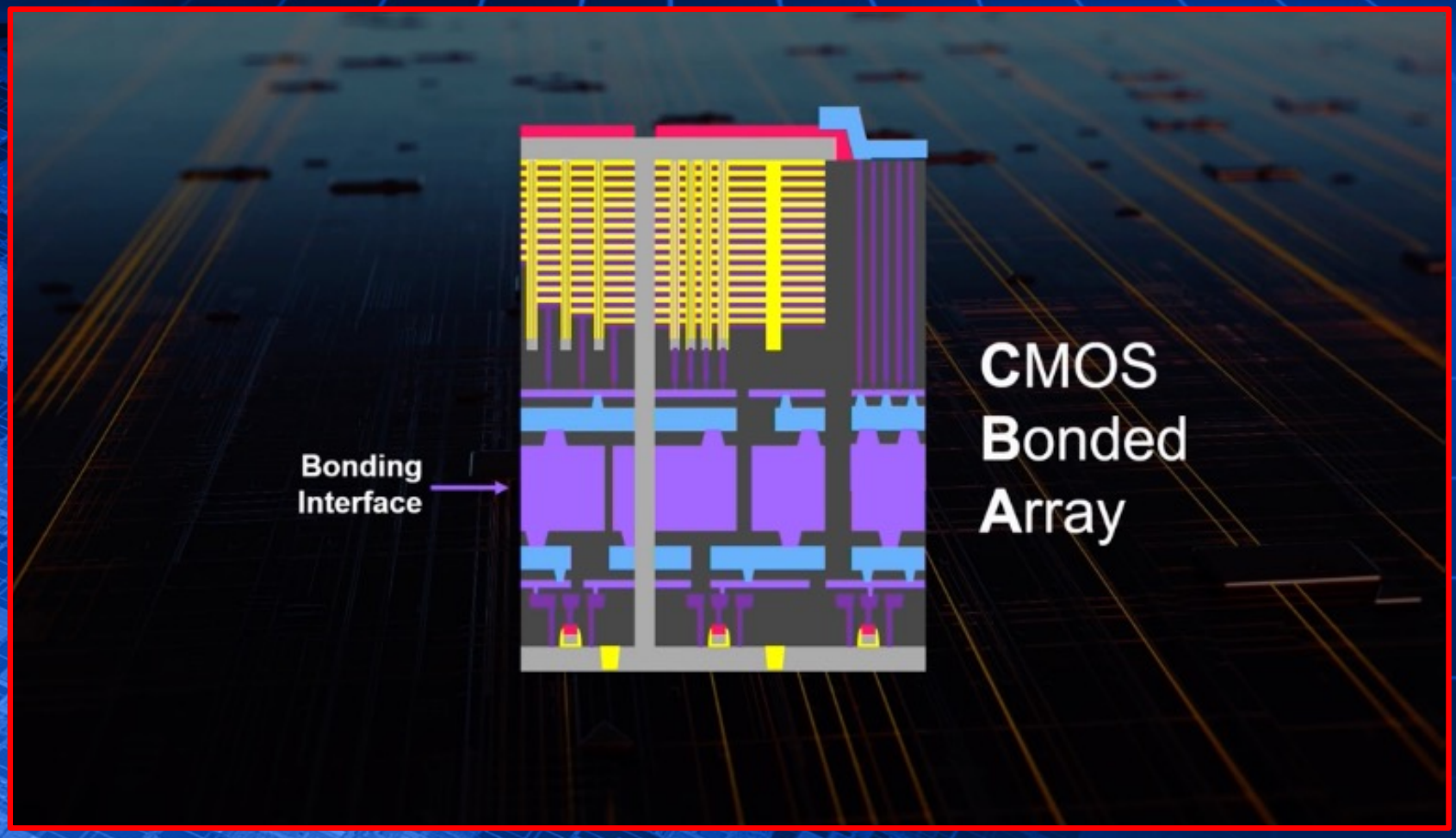
Vertically Stacked NAND Challenge

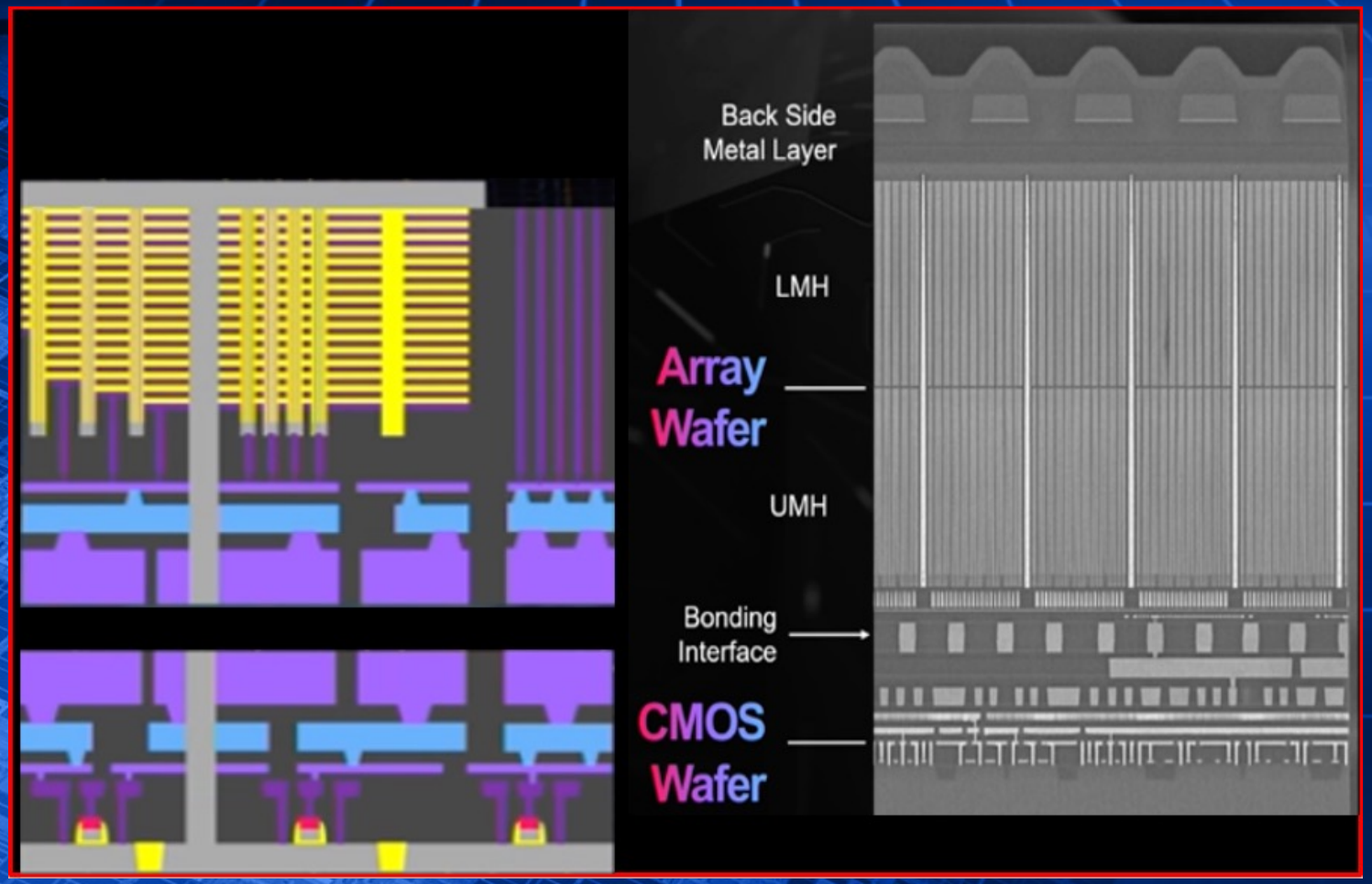


CMOS circuits are not affected by high temperature Array processes

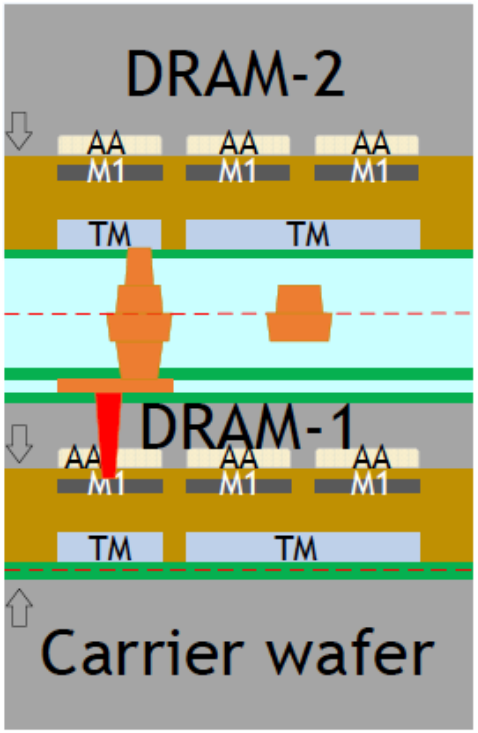

Cell/Array Wafer
CMOS Wafer

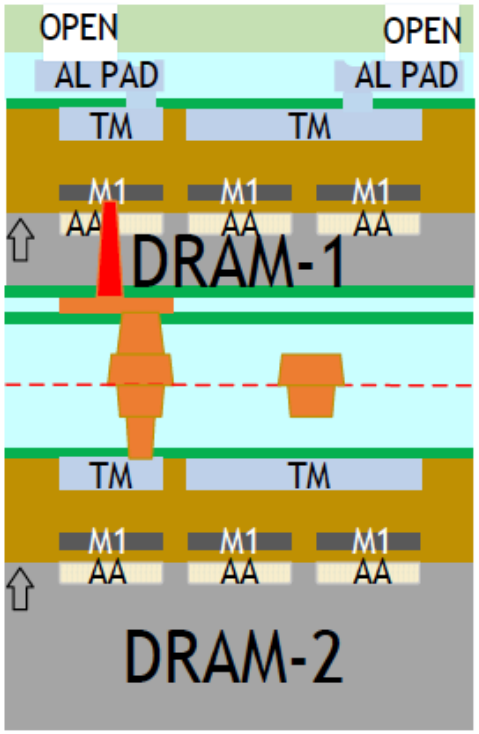

Cell/Array Wafer
CMOS Wafer


Bonding
Interface
CMOS
Bonded
Array


Back Side
Metal Layer
LMH
Array
Wafer
UMH
Bonding
Interface
CMOS
Wafer

Process of Proposed SeDRAM

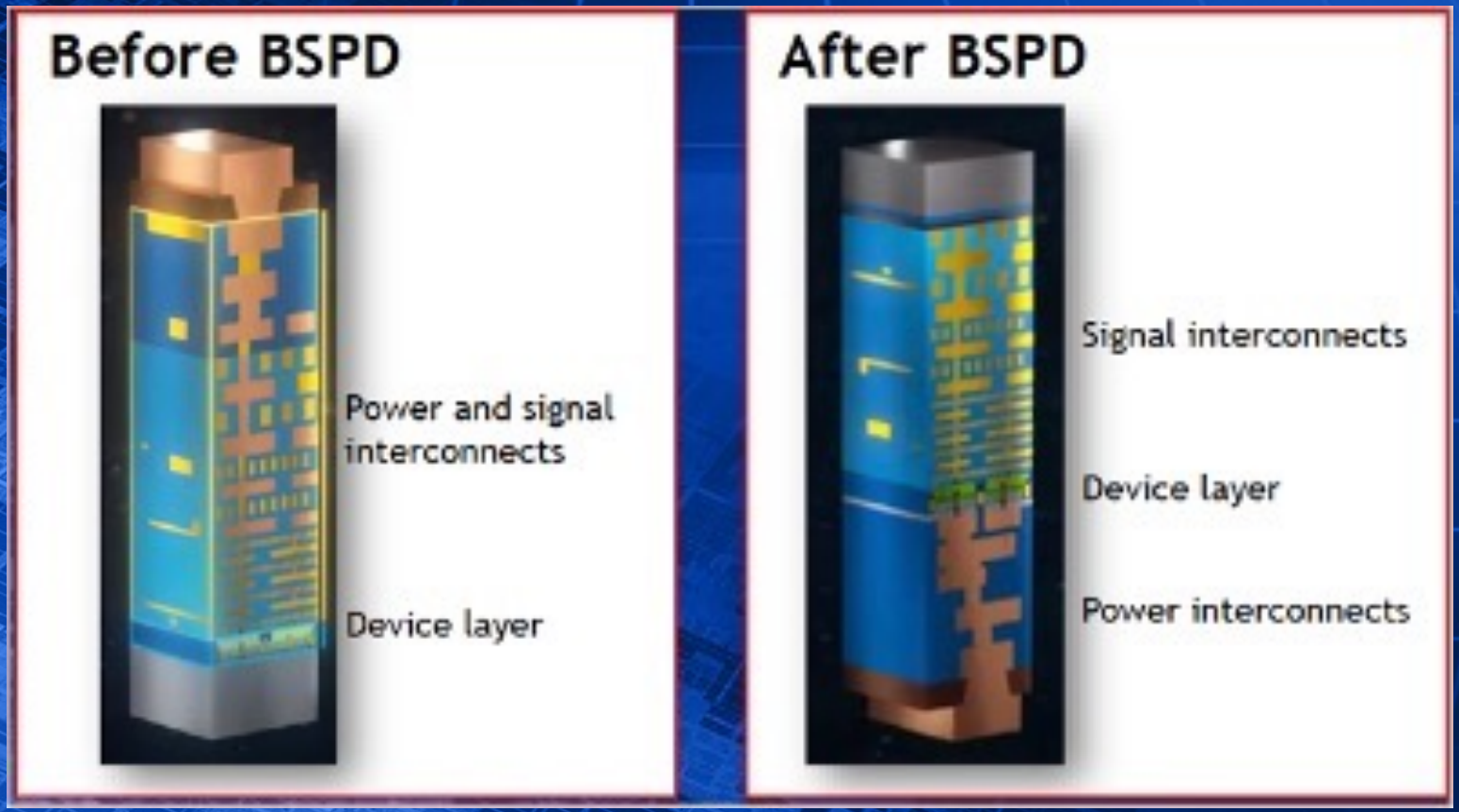




4. DRAM-1 and DRAM-2 bonding

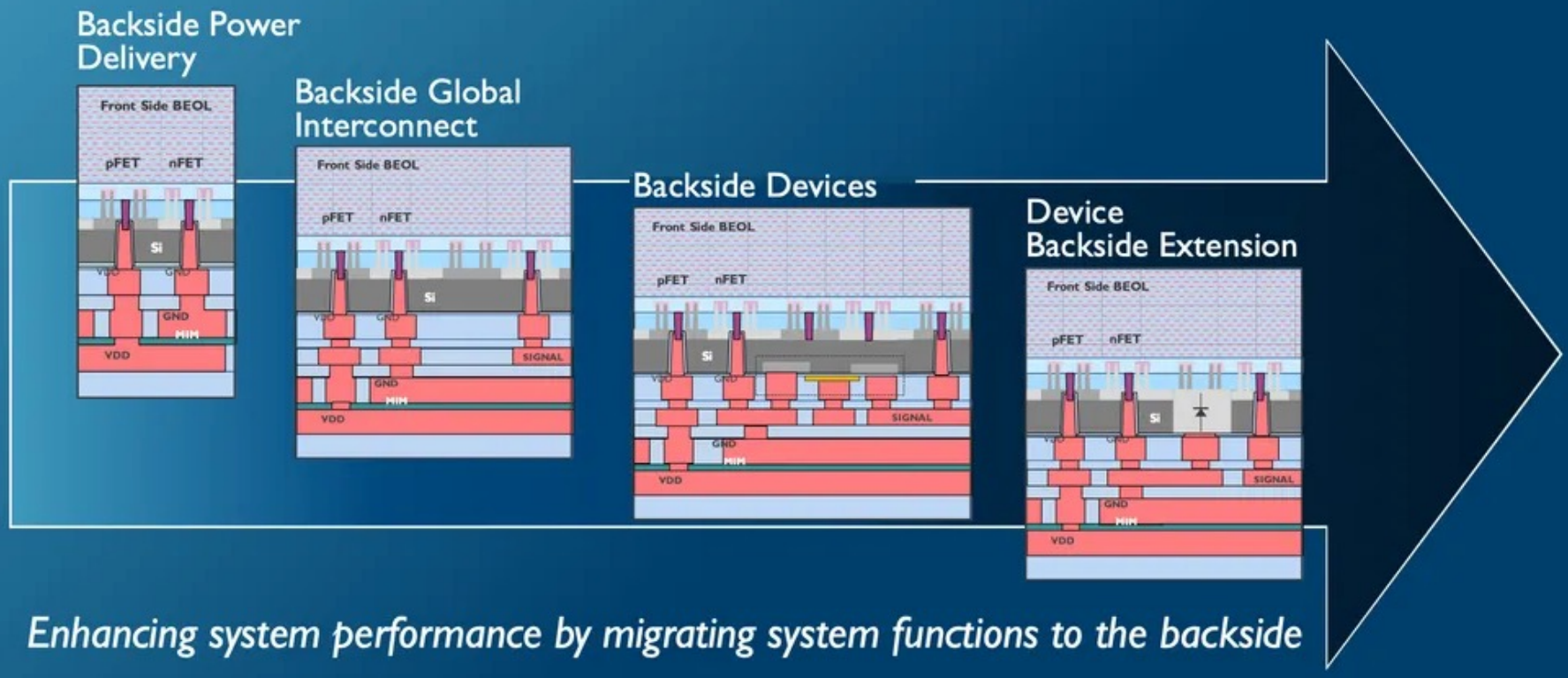
5. Remove carrier,and then pad out on DRAM-1

Back Side Power Distribution



Source: 2023 VLSI Symposium, Intel

Backside PDN paving the way to a truly functional backside



Enhancing system performance by migrating system functions to the backside

imec

ITF WORLD

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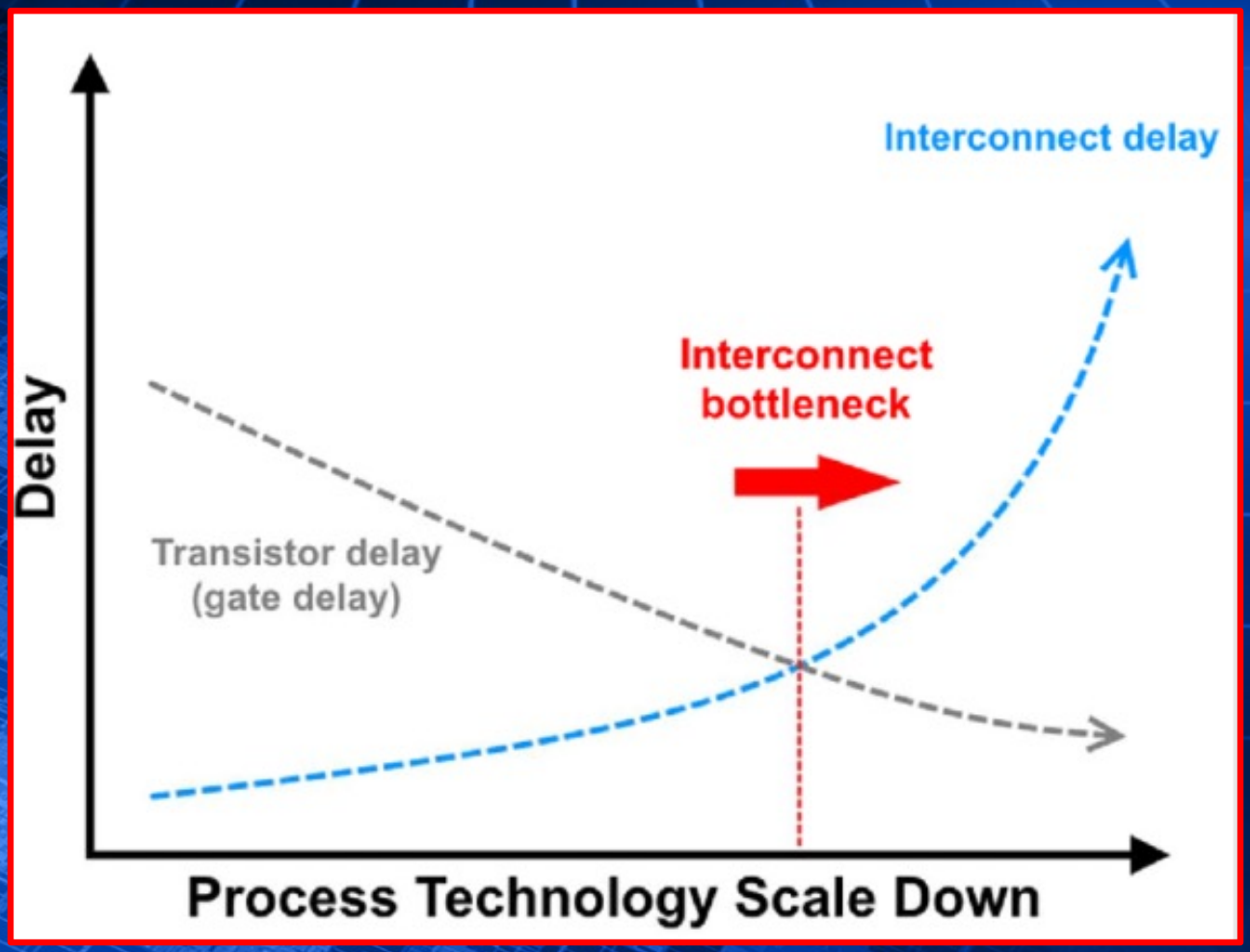
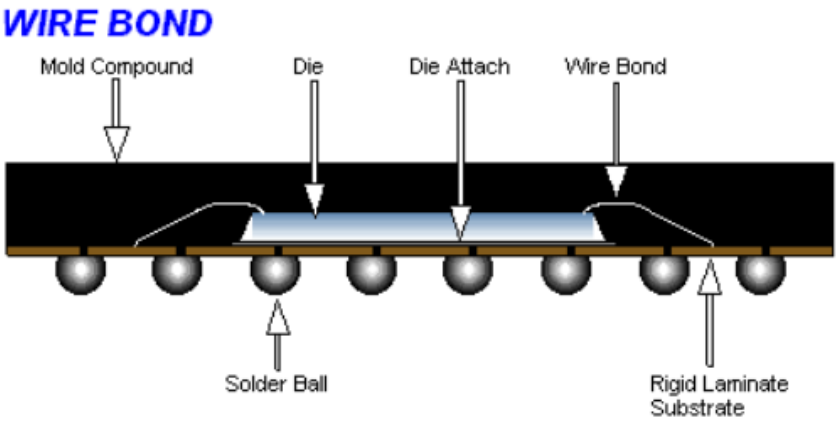
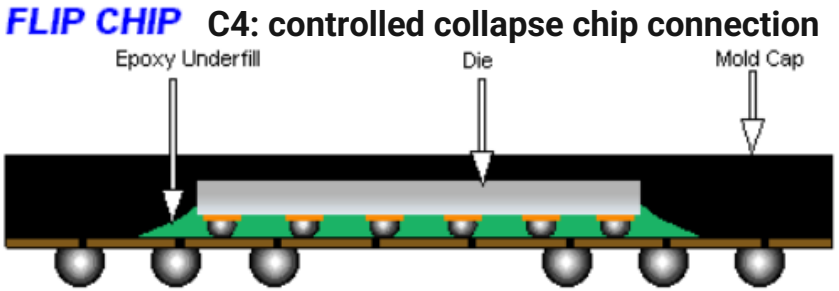
System In Package
SIP


Interconnect delay
Interconnect
bottleneck
Delay
Transistor delay
(gate delay)
Process Technology Scale Down

Develop a Technology to Produce an Infinitely “Large Die”

Melting point
Pb
327°C



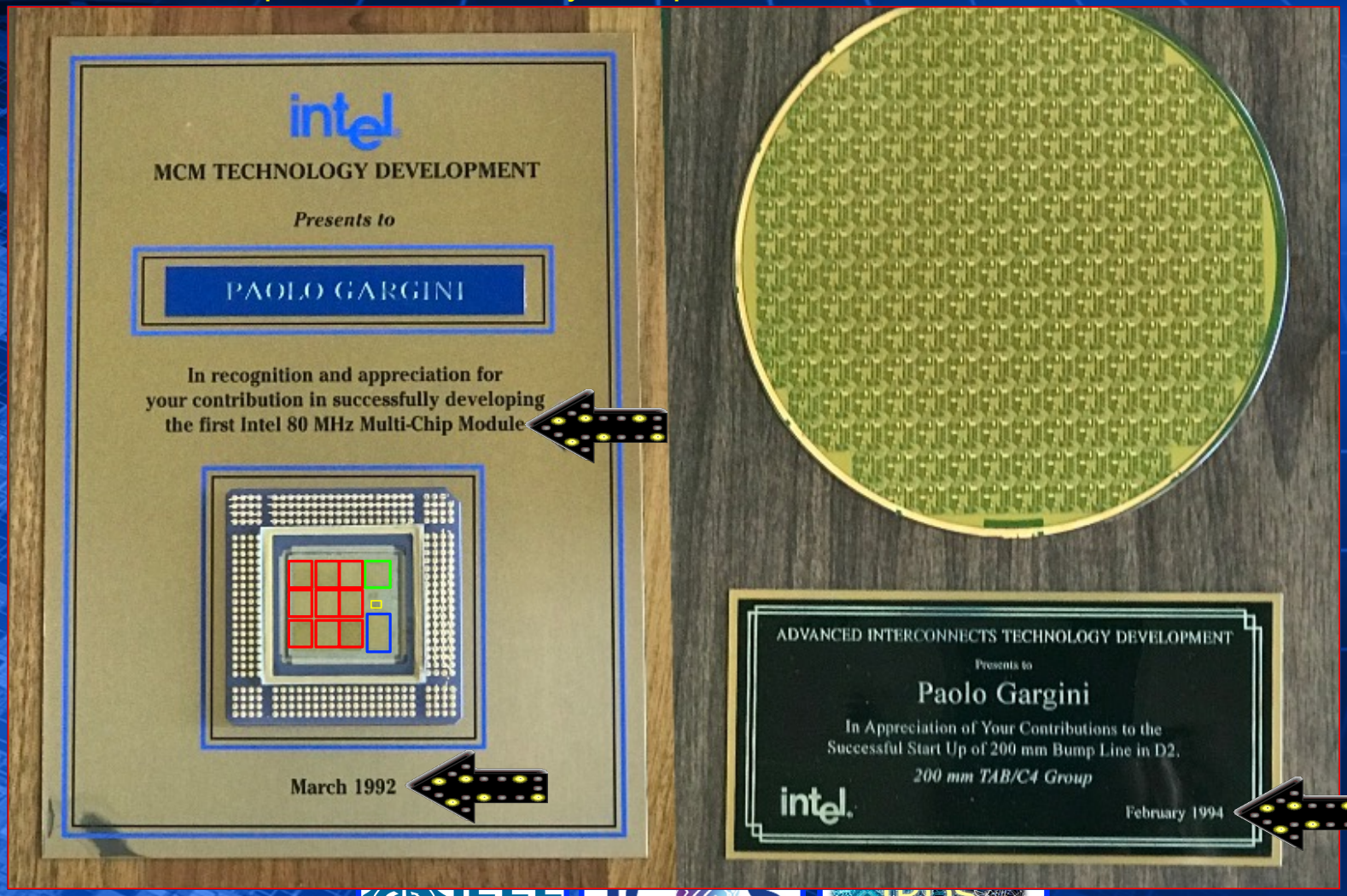


Wire Bond vs. Flip Chip

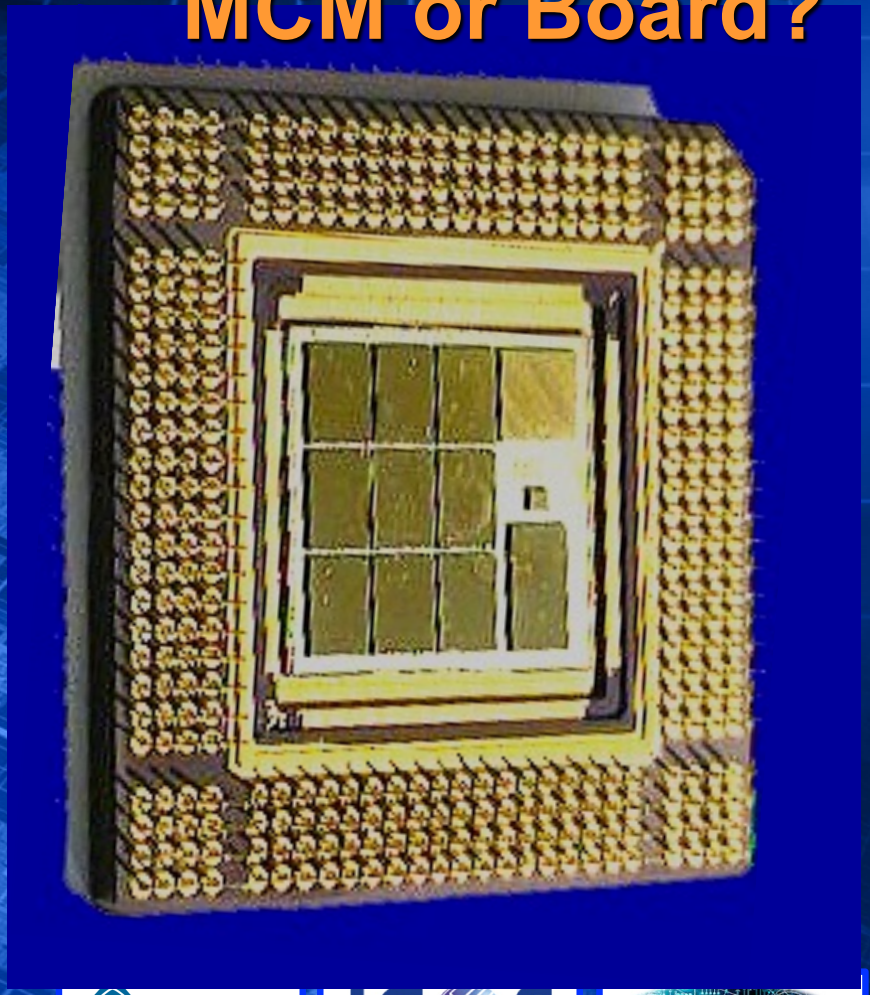
In the wire bond method (top), the die faces up and is attached to the package via wires. The flip chip (bottom) faces down and is typically attached via solder bumps similar to the larger ones that attach BGA packages to the printed circuit board (also shown here). *(Image courtesy of Amkor Technology, Inc.)*

Melting point
Sn
231°C

From co-evaporation to electrolytic deposition from solutions of metal salts



MCM or Board?



DRAMs

SRAM

Voltage Regulator

80486

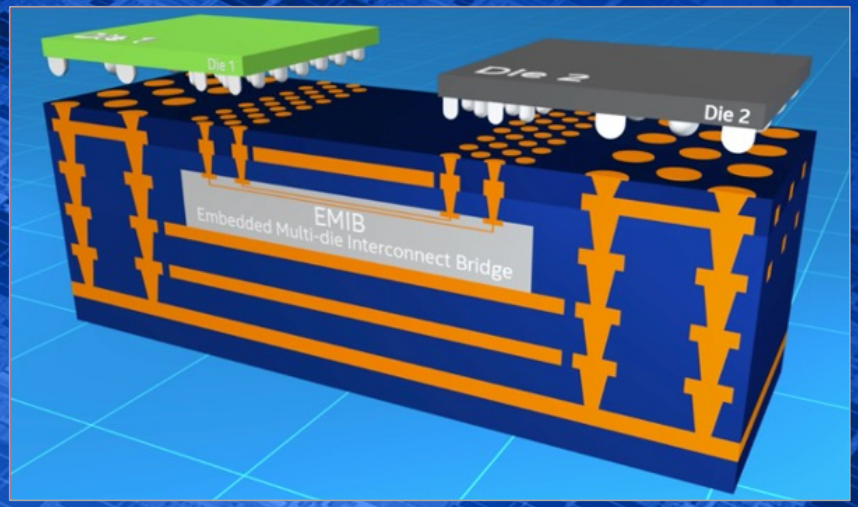
Intel Publications and Patents Guidelines

1968-1996

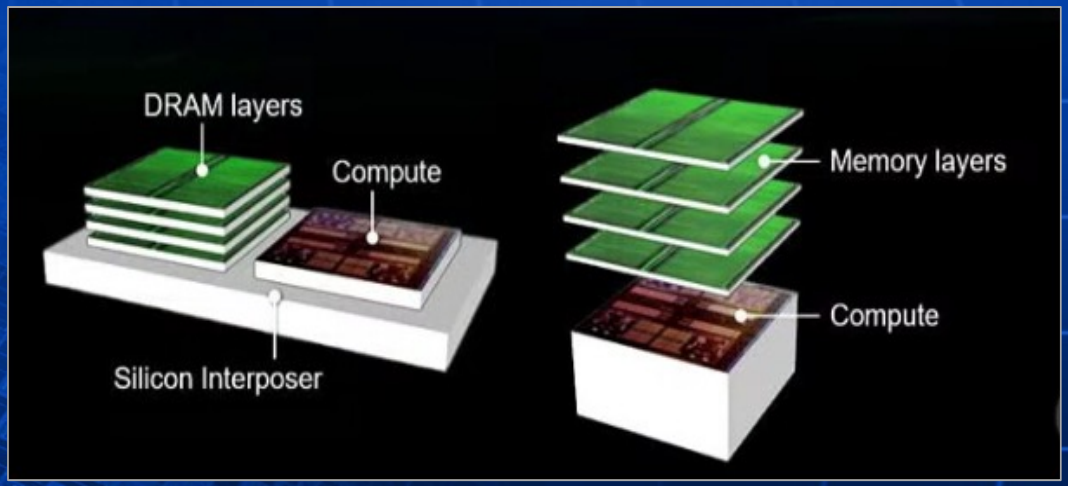
Write it on Silicon
NOT on Paper

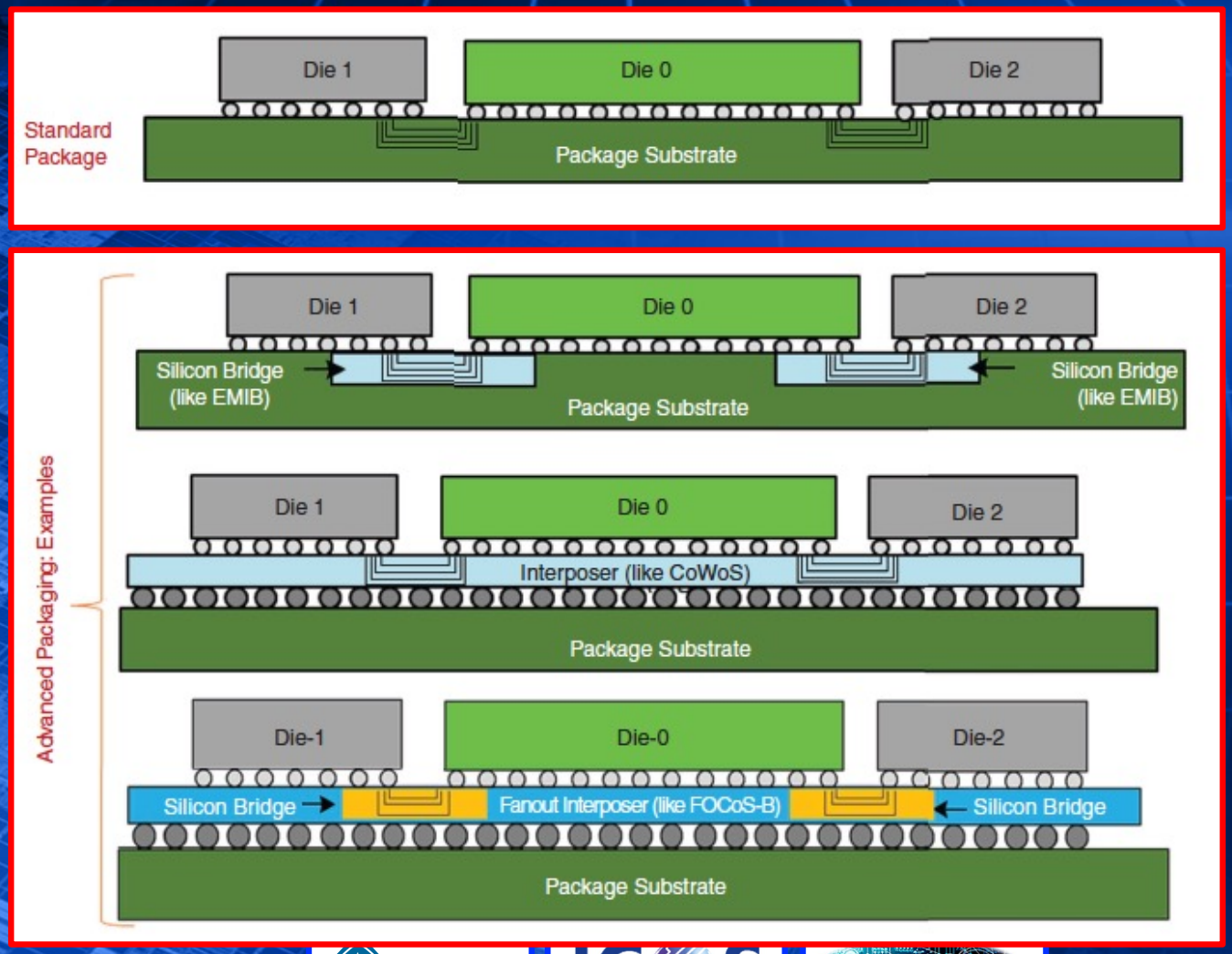
Gordon Moore

The Horizontal Approach

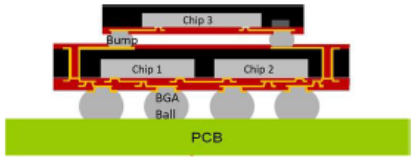
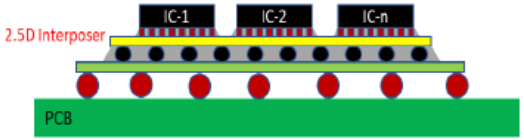
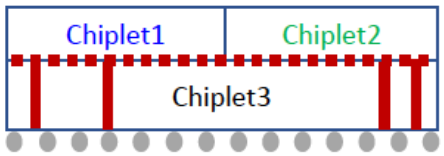


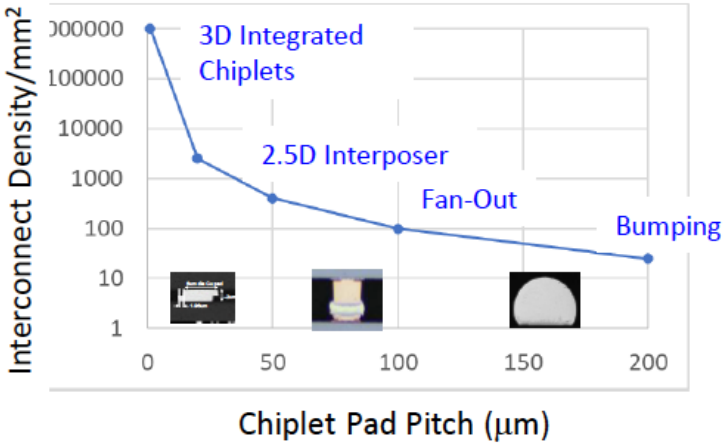
The Vertical Approach




Standard Package
Die 1
Die 0
Die 2
Package Substrate
Advanced Packaging: Examples
Die 1
Die 0
Die 2
Silicon Bridge (like EMIB)
Package Substrate
Silicon Bridge (like EMIB)
Die 1
Die 0
Die 2
Interposer (like CoWoS)
Package Substrate
Die-1
Die-0
Die-2
Silicon Bridge
Fanout Interposer (like FOCoS-B)
Silicon Bridge
Package Substrate

Multi Chiplet Heterogeneous Integration (MCHI) Platforms

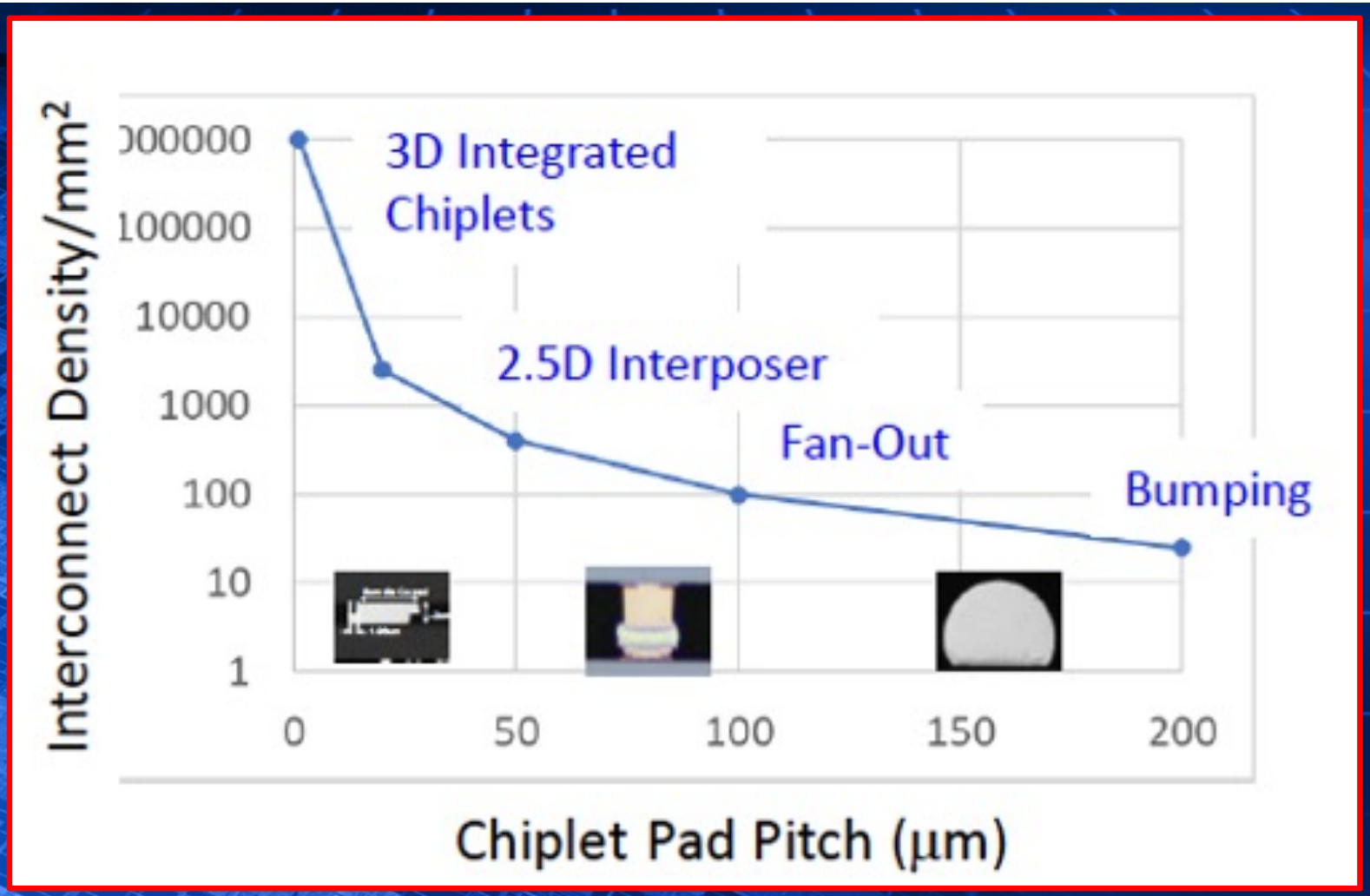
Target Applications.	Heterogeneous Integration Platforms
5G-Tx/Rx, mmWave Antenna, Automotive Radar AP+Memory, AR/VR.	Embedded High Density Fan-Out WLP 
Data Centre, HPC, AI, Chiplets	2.5D Interposer 
SOC Disintegration & reintegration, 3D Memory	3D-Integrated Chiplets 



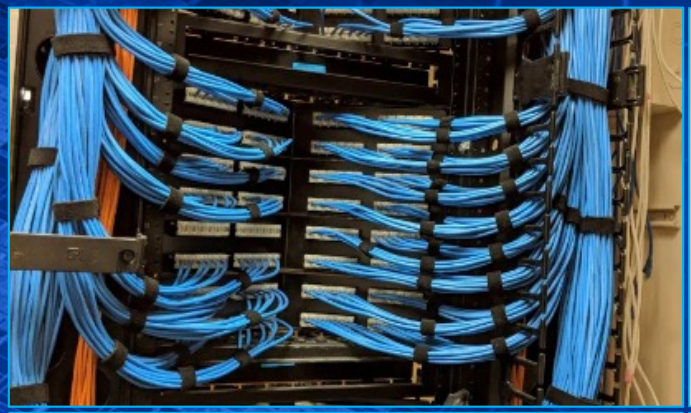
Inter-chiplet wiring density increases

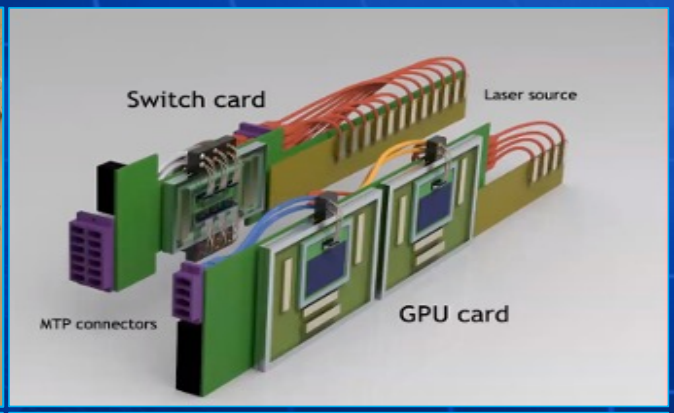
- 5x-10x from Bumping to FOWLP
- 10x from FOWLP to 2.5D Interposer
- >100x from 2.5D Interposer to 3DIC (hyb. Bonded)

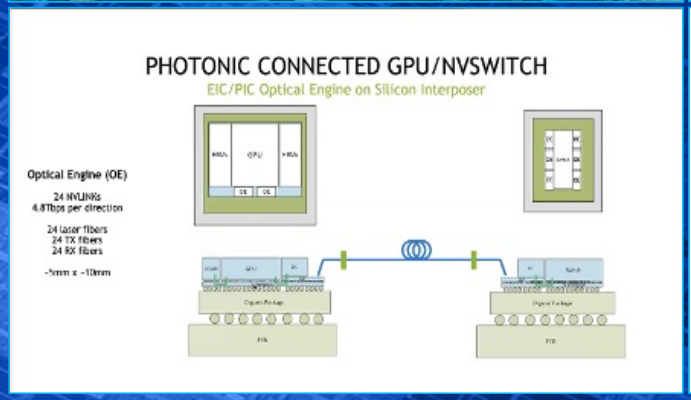
CHALLENGES: Package Architecture, Design, Materials, Process Optimization

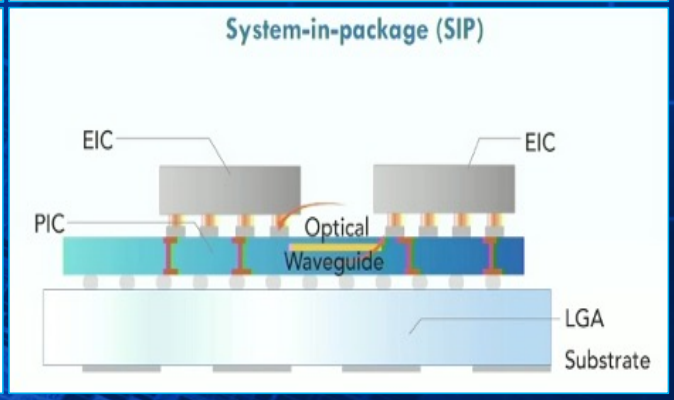

Interconnect Density/mm²
000000
100000
10000
1000
100
10
1
0
50
100
150
200
Chiplet Pad Pitch (µm)
3D Integrated Chiplets
2.5D Interposer
Fan-Out
Bumping

Evolution of fiber optics from data centers (meters) to board (centimeters) to package-to-package (millimeters) to chip-to-chip (tens of microns)





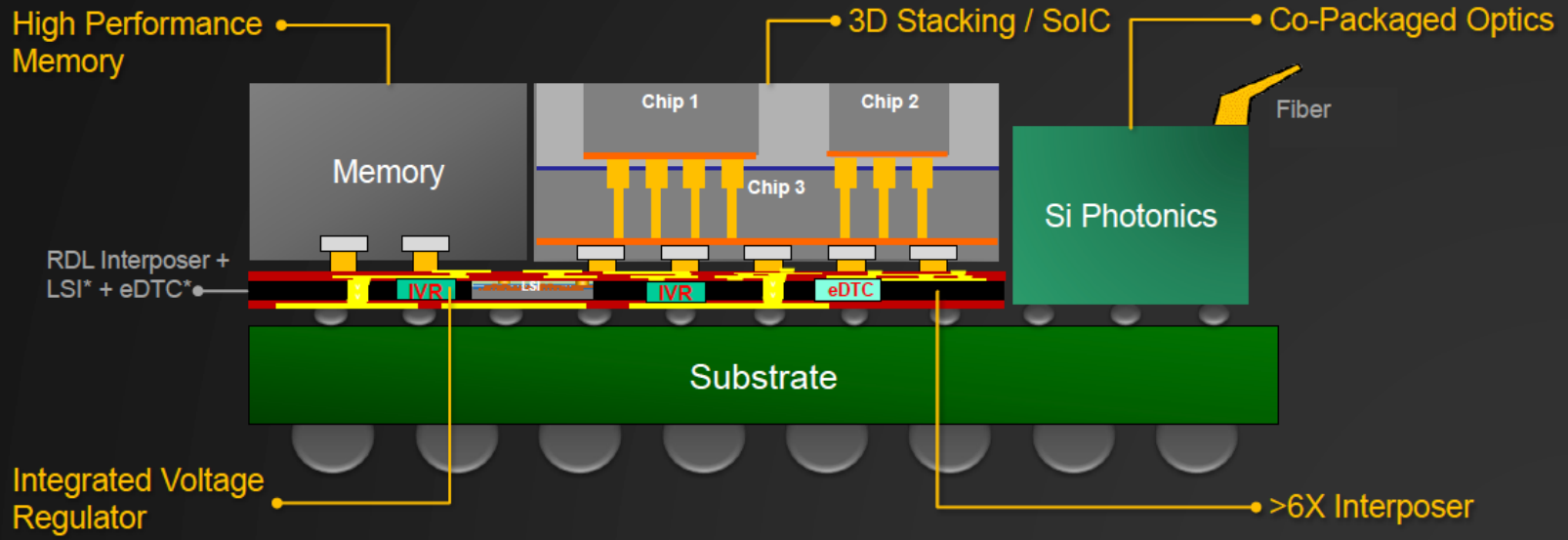




Sources: Fiber Broadband Association, NVIDIA, Lightelligence

Technology Platform for HPC / AI

TOMORROW

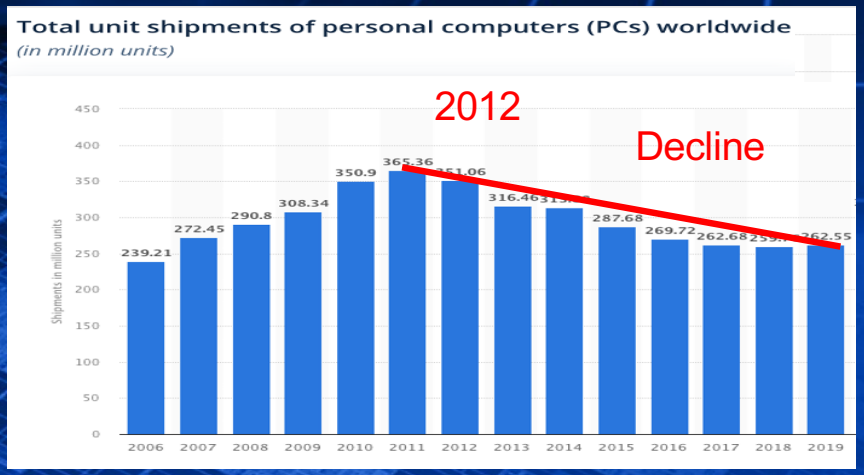


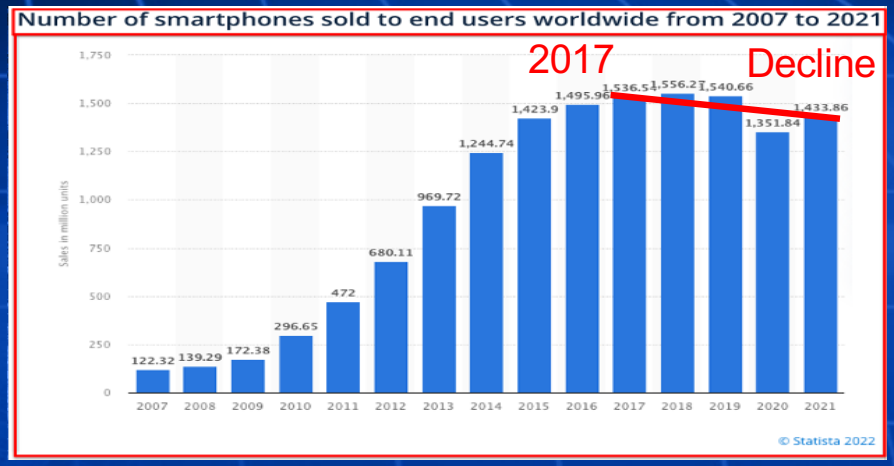
*: LSI: Local Silicon Interconnect; eDTC: embedded Deep Trench Capacitor

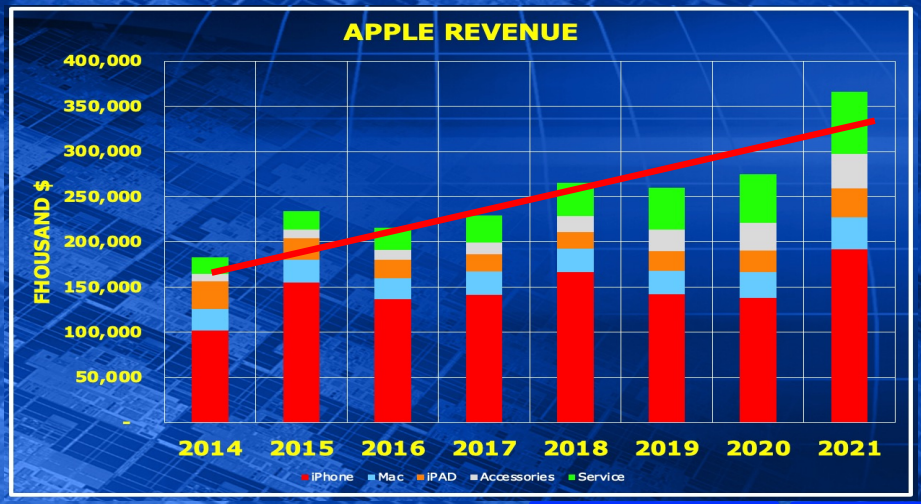
The New Electronics Industry

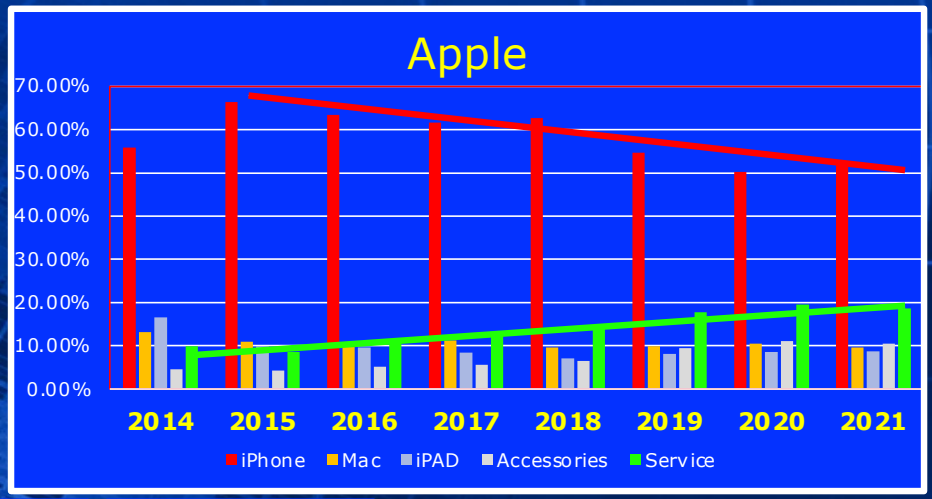
- 3D Transistors
- Beyond Silicon
- 3D Everything
- System In Package
- New Products
- New Architecture
- SOC: Endless Die Size
- SOC and SIP

What About products?


Total unit shipments of personal computers (PCs) worldwide
(in million units)
2012
Decline
Shipments in million units
239.21
272.45
290.8
308.34
350.9
365.36
351.06
316.46
287.68
269.72
262.68
262.55
2006 2007 2008 2009 2010 2011 2012 2013 2014 2015 2016 2017 2018 2019

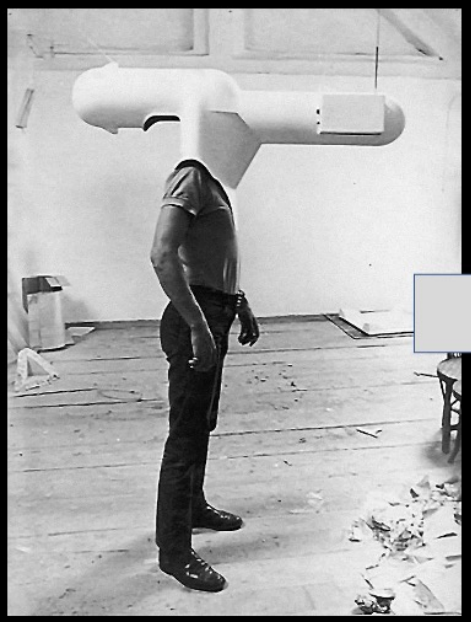

Number of smartphones sold to end users worldwide from 2007 to 2021
2017
Decline
Sales in million units
122.32
139.29
172.38
296.65
472
680.11
969.72
1,244.74
1,423.9
1,495.96
1,536.5
1,556.21
1,540.66
1,351.84
1,433.86
2007 2008 2009 2010 2011 2012 2013 2014 2015 2016 2017 2018 2019 2020 2021
© Statista 2022


APPLE REVENUE
FHOUSAND $
400,000
350,000
300,000
250,000
200,000
150,000
100,000
50,000
-
2014 2015 2016 2017 2018 2019 2020 2021
iPhone Mac iPAD Accessories Service

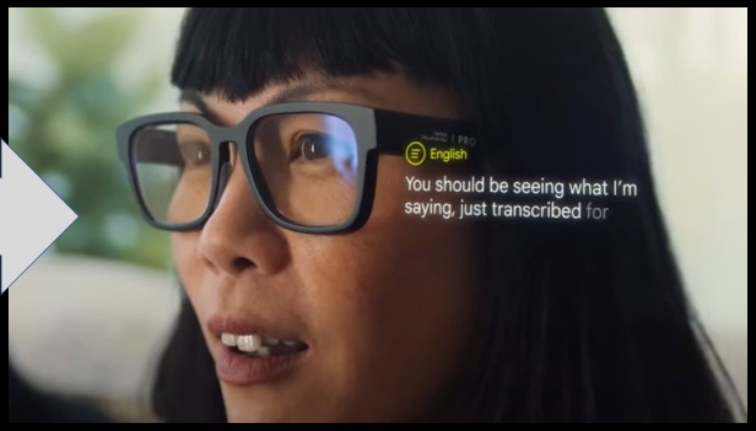

Apple
70.00%
60.00%
50.00%
40.00%
30.00%
20.00%
10.00%
0.00%
2014 2015 2016 2017 2018 2019 2020 2021
iPhone Mac iPAD Accessories Service

The Next Wave of Products

Flat and thin optical systems are key to enabling compact, transparent and light weight AR display architectures



Walter Pichler's TV helmet (1967)



Google monocular AR display glasses (Google I/O, May 2022)

https://www.istockphoto.com/search/2/image-film?page=13&phrase=ar%20glasses

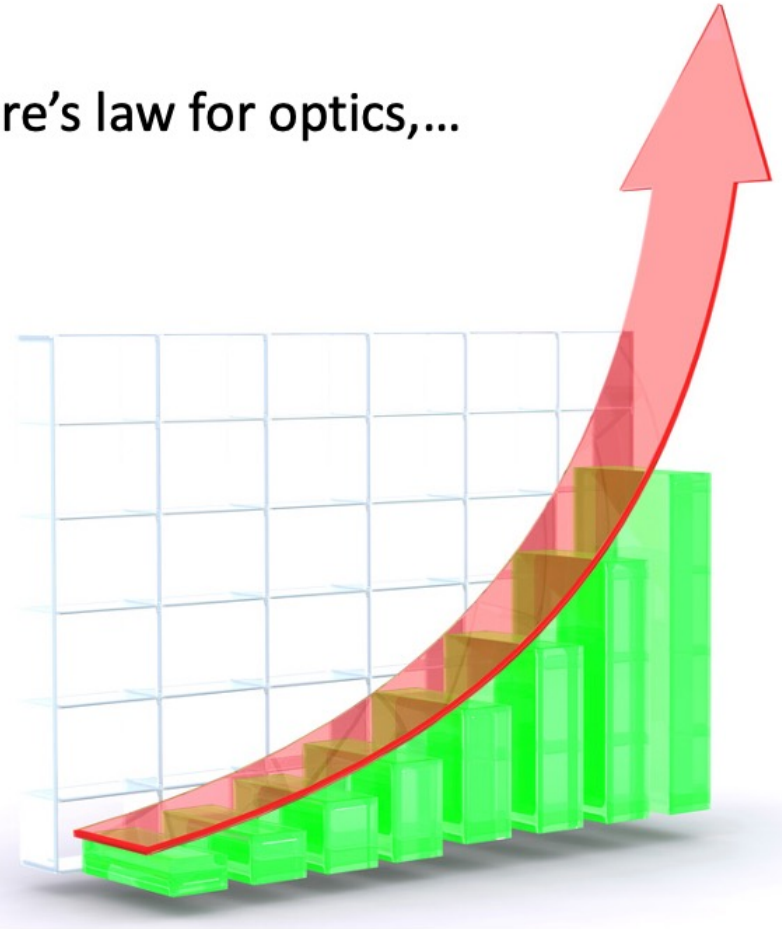
Ray-Ban and Facebook introduce Ray-Ban Stories, first-generation smart glasses

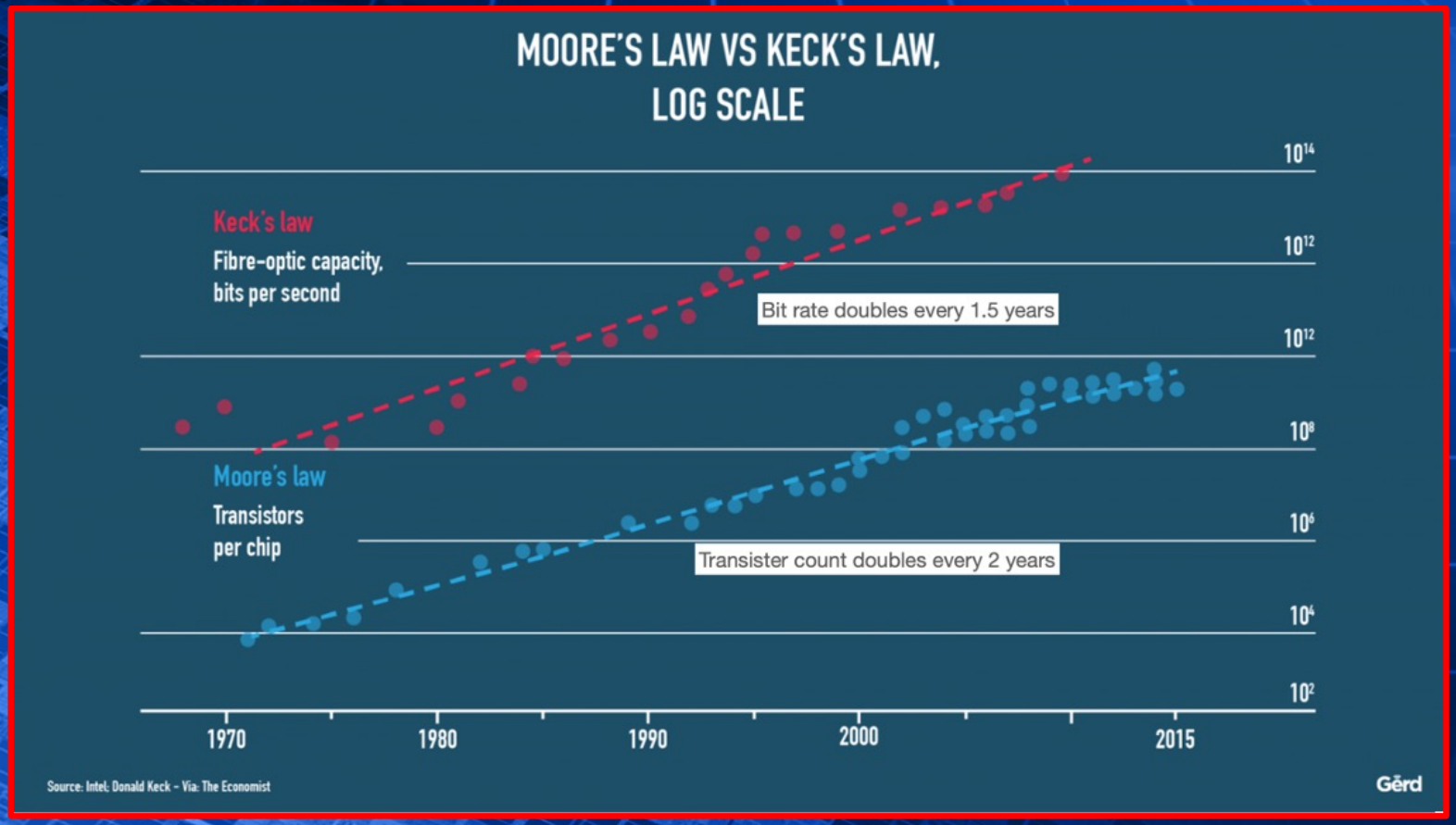
After promising smart glasses for years, Facebook's first glasses **are disappointingly** familiar. **These aren't AR glasses at all** They don't have displays in them. Instead, they're a blend of technologies that have already been in other glasses: they have cameras in them, and microphones, and speakers. They're headphones and camera-glasses in one, and that's about it.

Back to Basics

There might not be any Moore's law for optics,…

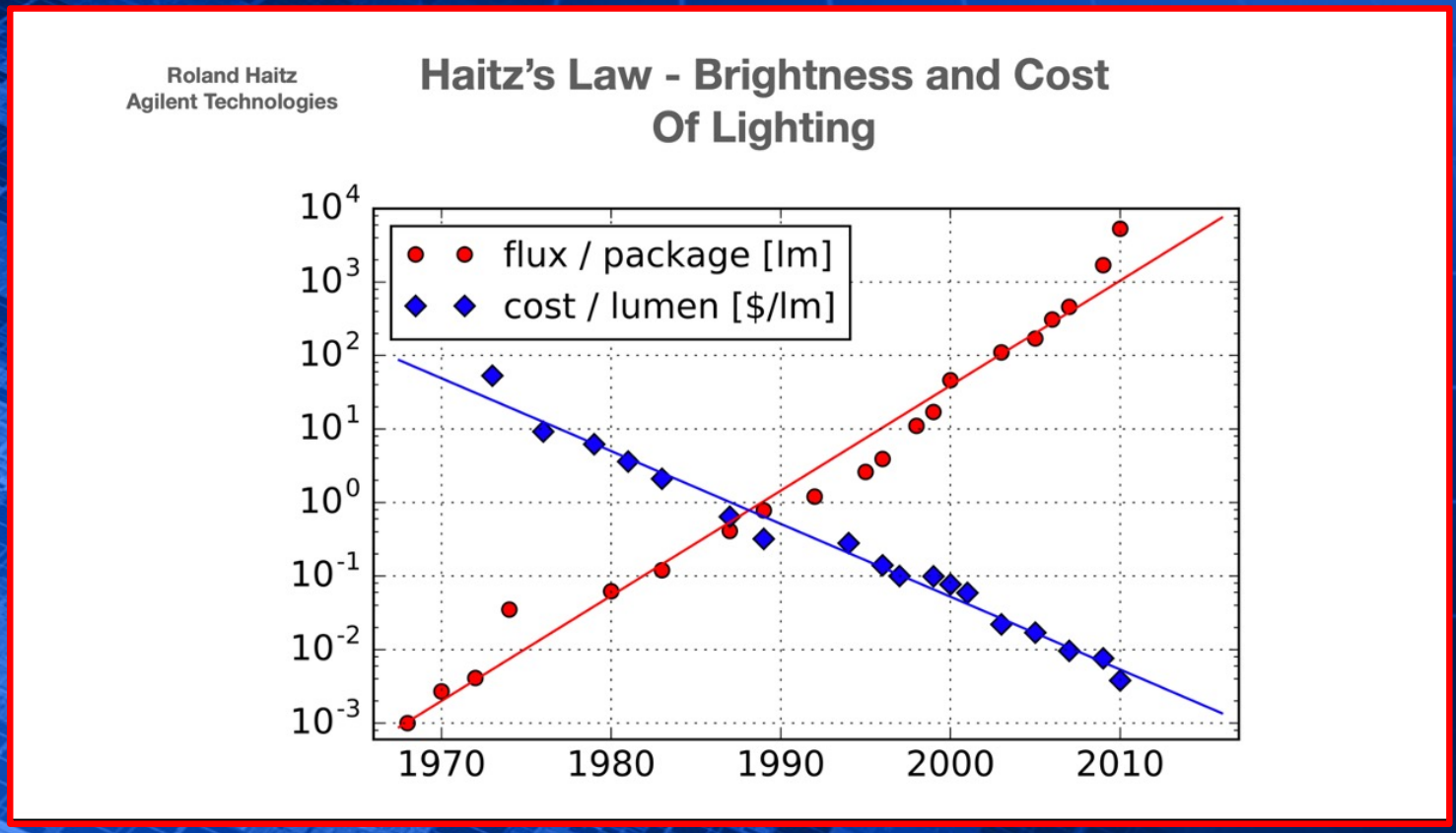
… but there are plenty of exponential growth laws in optics and photonics





Donald Keck invented fiber optics in 1970 at Corning

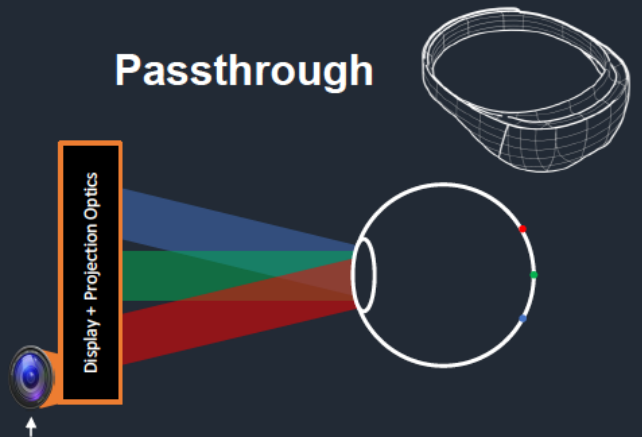
Haitz's law is an observation and forecast about the steady improvement, over many years, of light (LEDs).




alamy
PERSON
PERSON
PERSON
PERSON

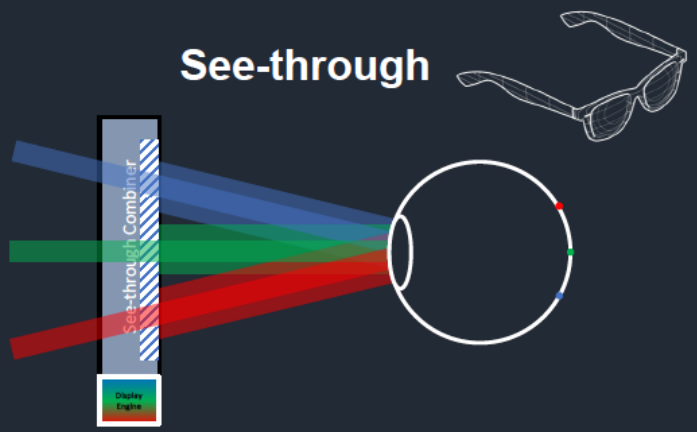
AR: Passthrough vs. See-through

Passthrough



Real world is captured through camera and re-displayed on screen together with other virtual content

See-through



Real world is seen through a combiner that displays virtual content as well as being transparent

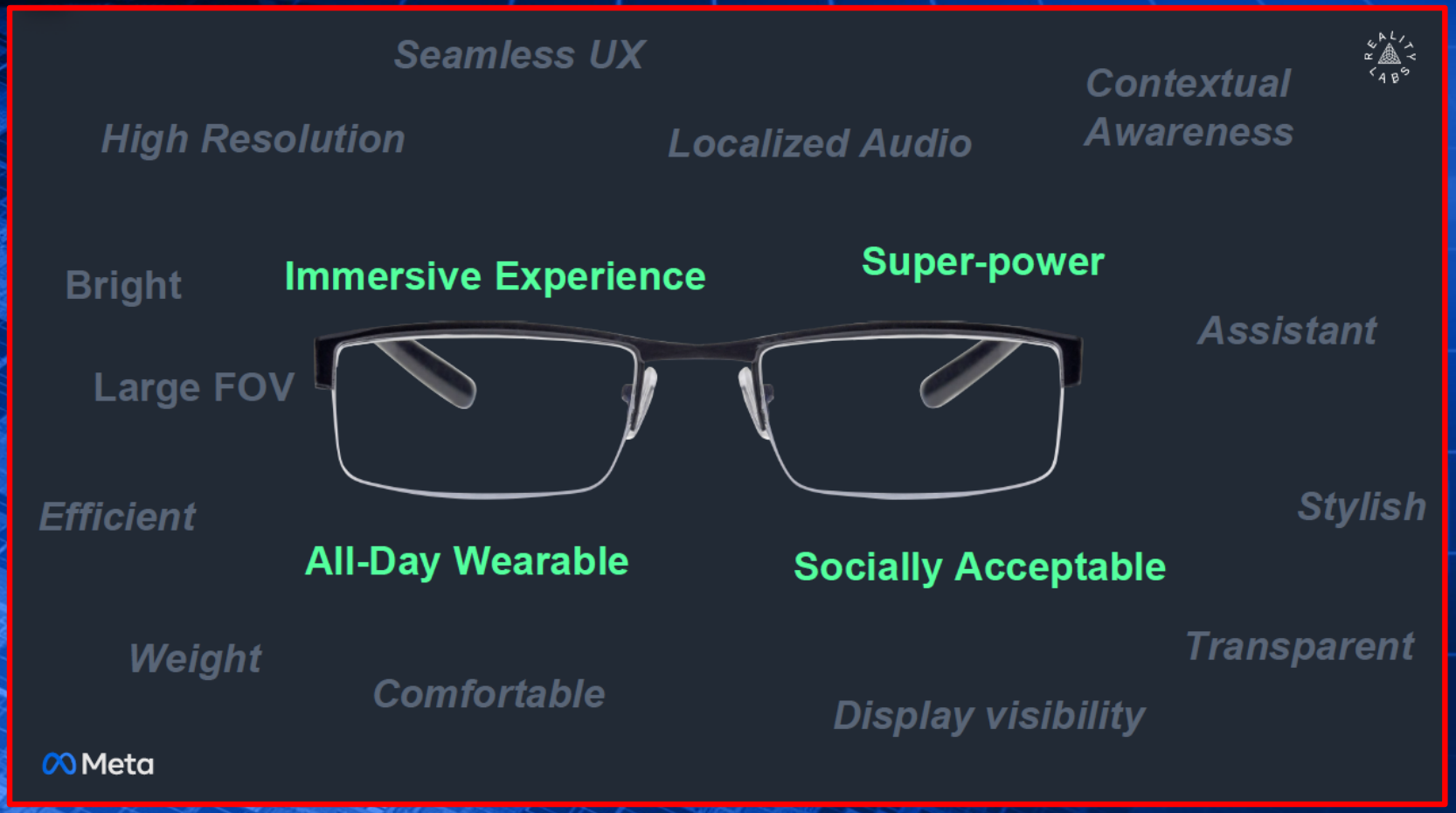
Meta

11

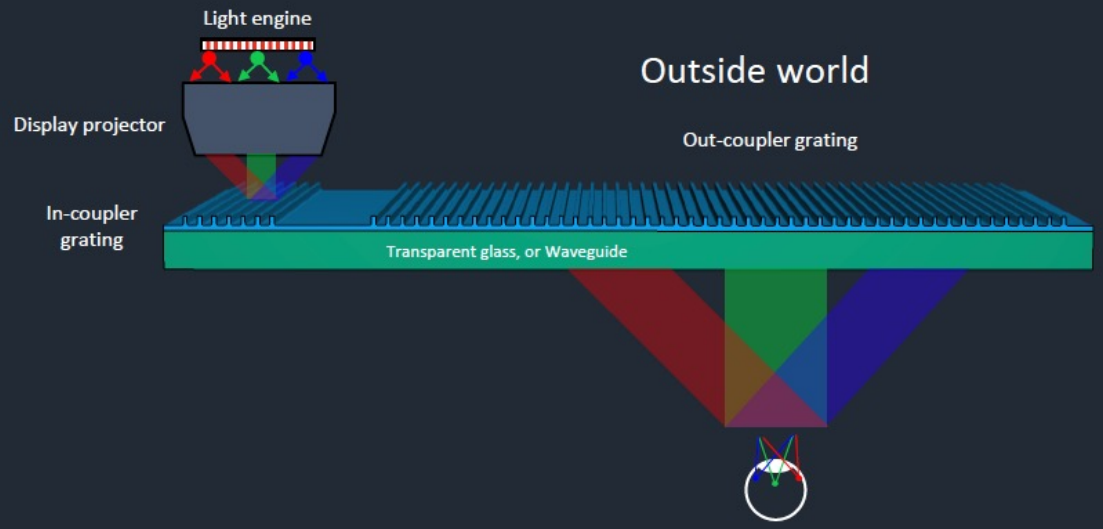
The Future: A true see-through augmented reality experience that's all-day wearable

Meta

9


Seamless UX
High Resolution
Localized Audio
Contextual Awareness
Bright
Immersive Experience
Super-power
Assistant
Large FOV
Efficient
Stylish
All-Day Wearable
Socially Acceptable
Weight
Transparent
Comfortable
Display visibility
Meta

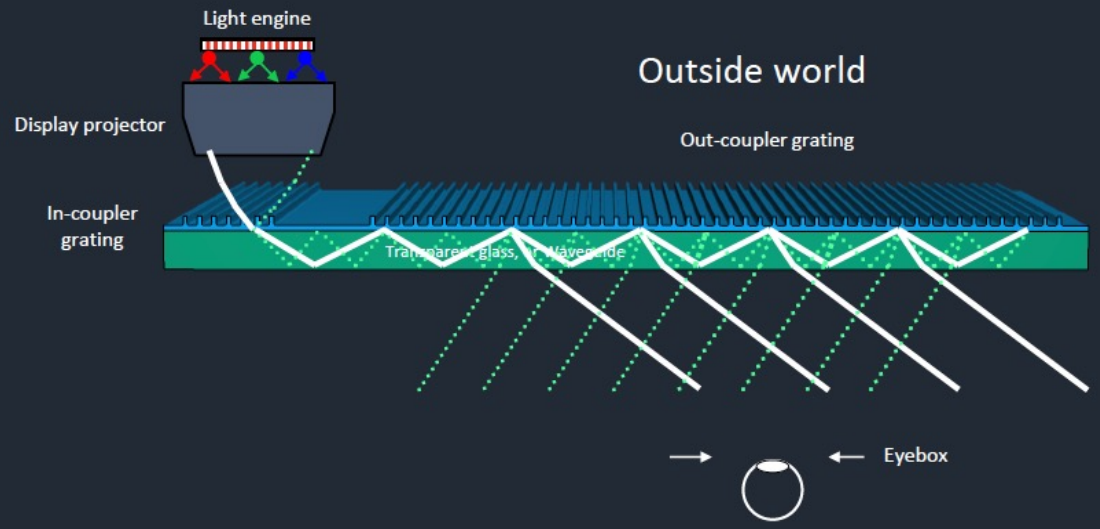
How to enable see-through AR? – Waveguide in AR Glass



Meta

14

How to enable see-through AR? – Waveguide in AR Glass



Meta

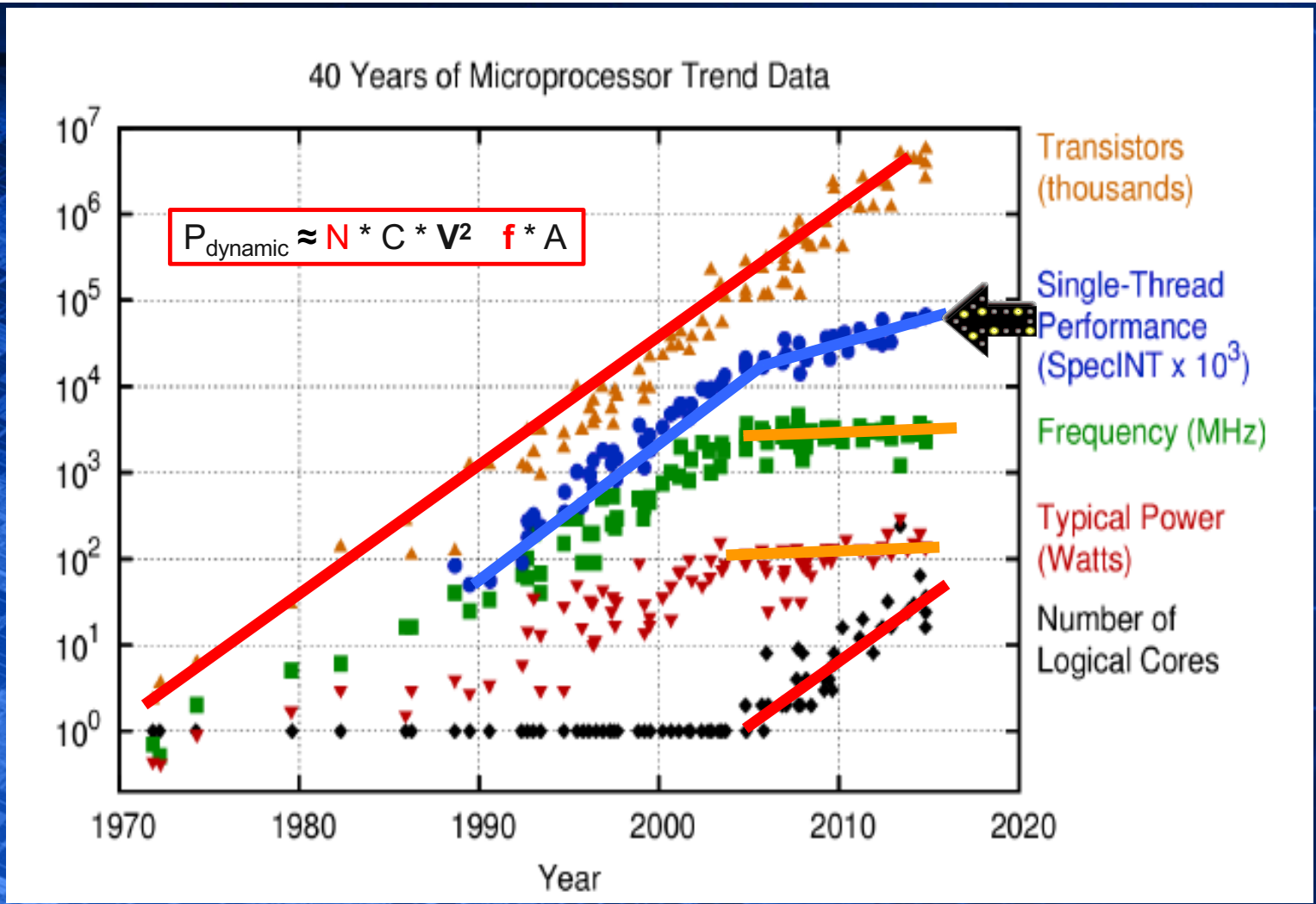
15


Rainfall
Connected
Location Map
Next ▶
Nitrogen in Soil
Humidity
25000 lux
Light Level
pH
NPK

The New Electronics Industry

- 3D Transistors
- Beyond Silicon
- 3D Everything
- System In Package
- New Products
- New Architecture
- SOC: Endless Die Size
- SOC and SIP

The Next Computing Architecture


40 Years of Microprocessor Trend Data
$P_{dynamic} \approx N * C * V^2 \quad f * A$
Transistors (thousands)
Single-Thread Performance (SpecINT x 10^3)
Frequency (MHz)
Typical Power (Watts)
Number of Logical Cores
10^7
10^6
10^5
10^4
10^3
10^2
10^1
10^0
1970
1980
1990
2000
2010
2020
Year

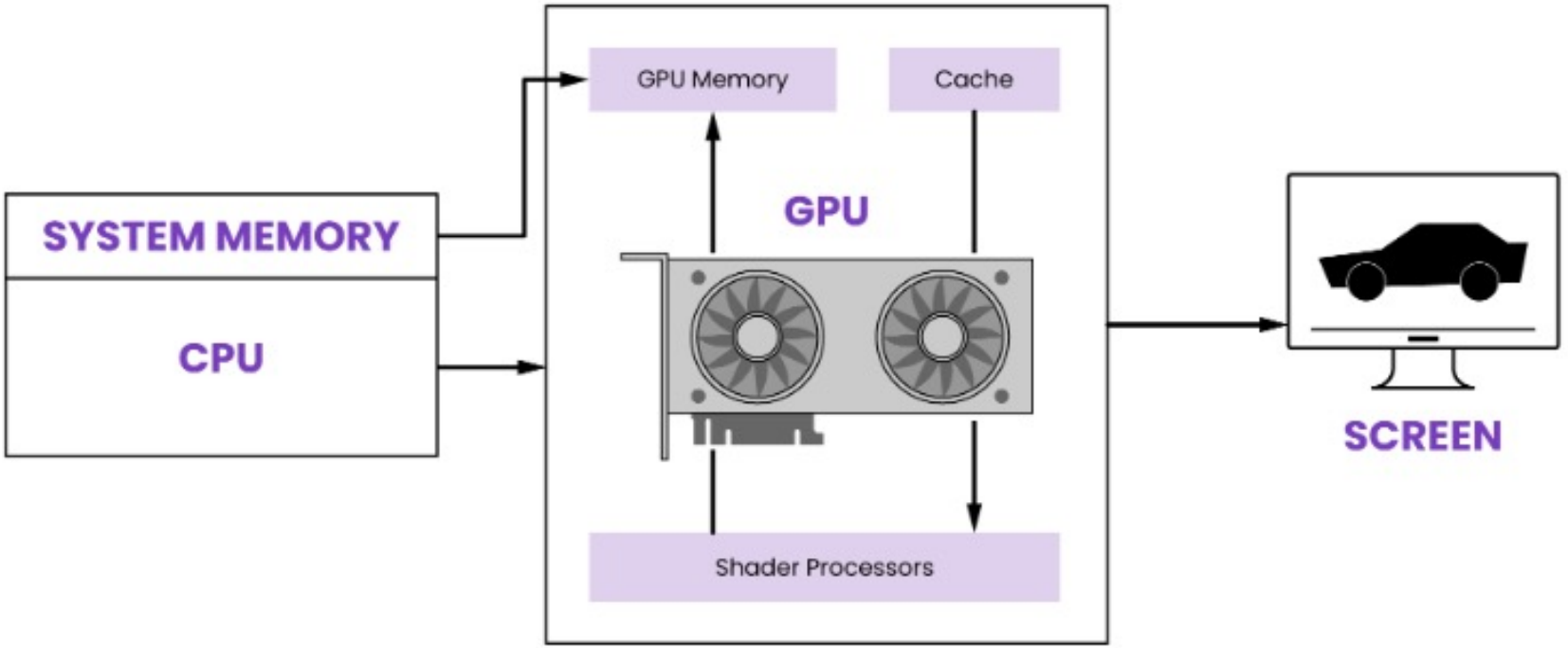
2009

Large-scale Deep Unsupervised Learning using Graphics Processors

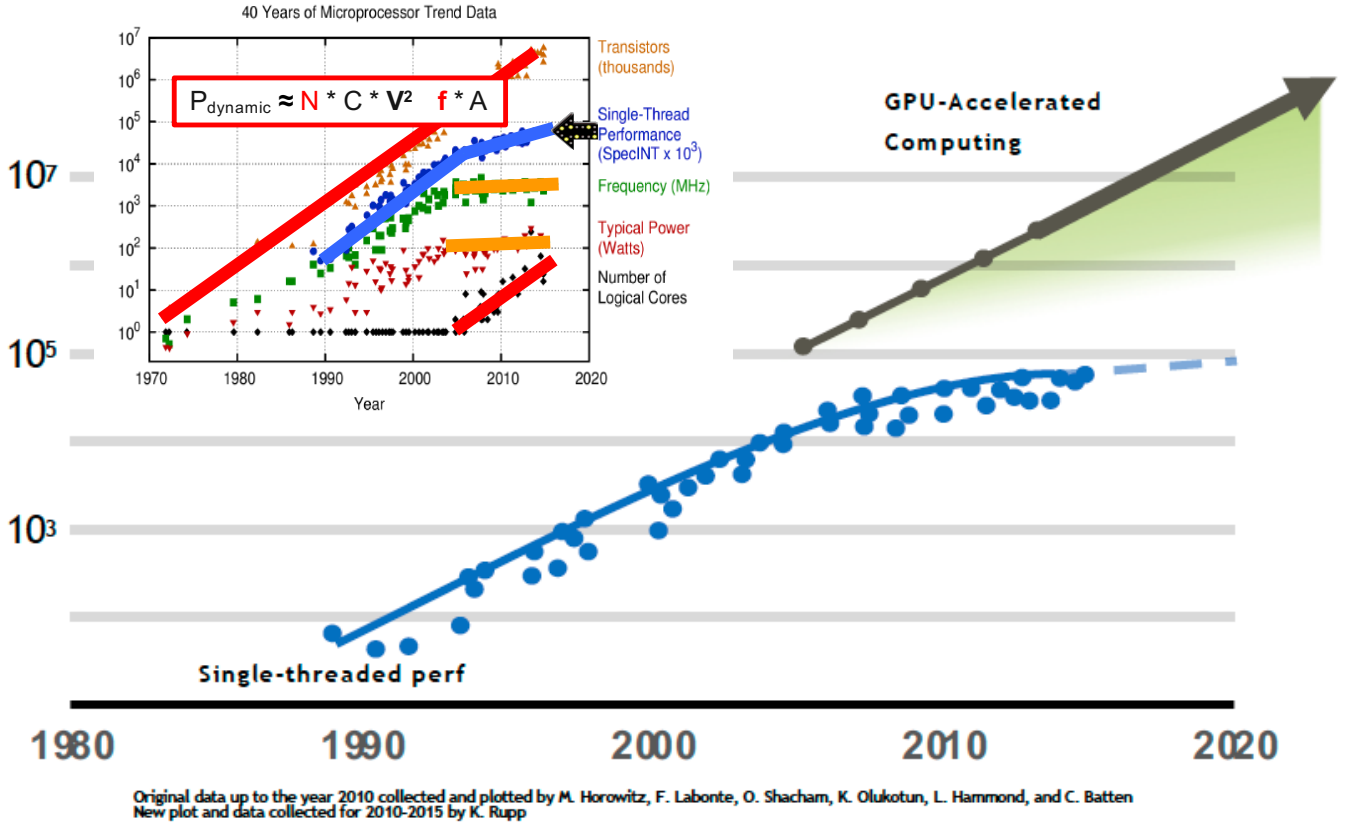
Rajat Raina RAJATR@CS.STANFORD.EDU
Anand Madhavan MANAND@STANFORD.EDU
Andrew Y. Ng ANG@CS.STANFORD.EDU
Computer Science Department, Stanford University, Stanford CA 94305 USA

7. Discussion

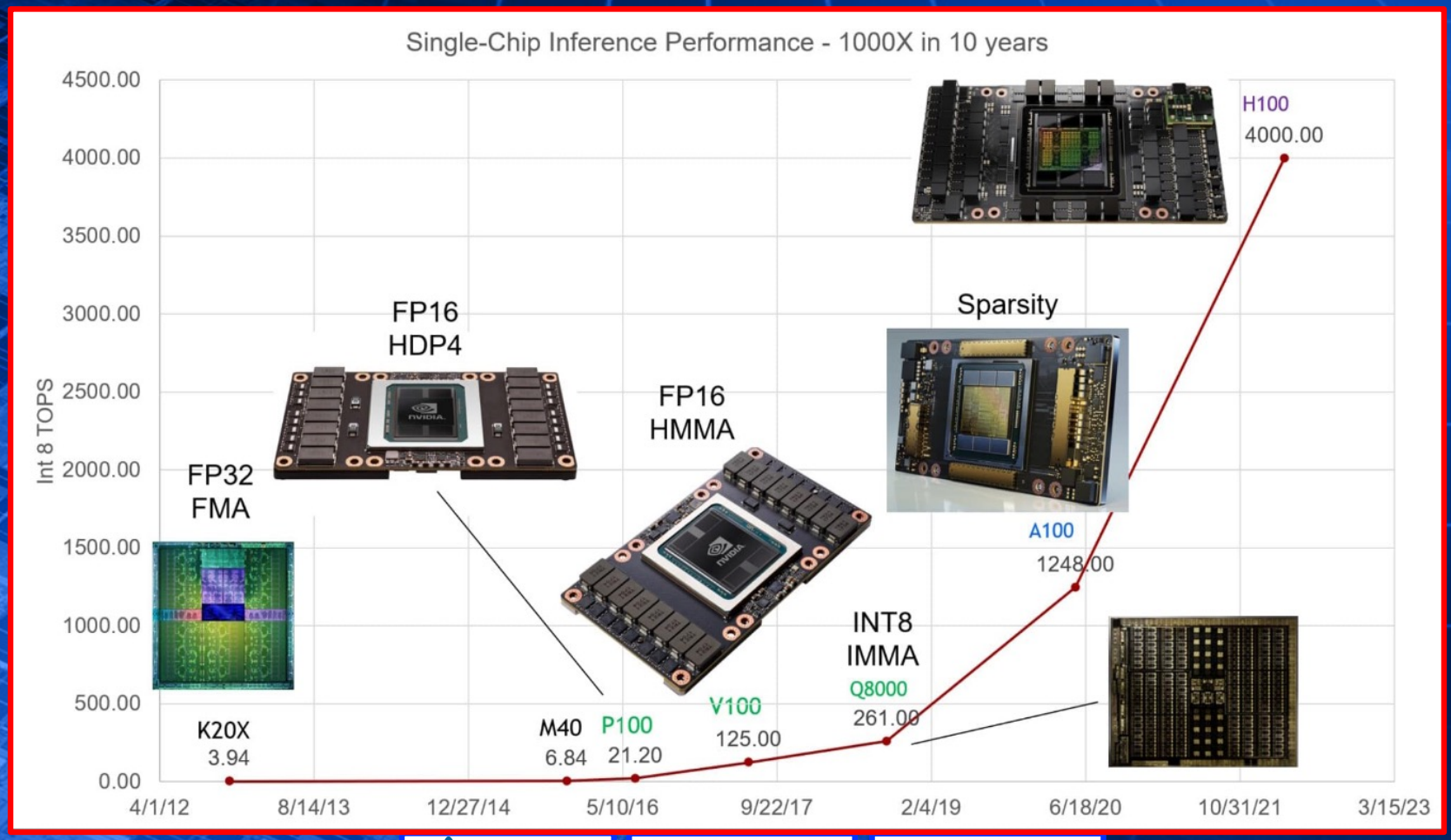
Graphics processors are able to exploit finer-grained parallelism than current multicore architectures or distributed clusters. They are designed to maintain thousands of active threads at any time, and to schedule the threads on hundreds of cores with very low scheduling overhead. The map-reduce framework (Dean & Ghe-


GPU Memory
Cache
GPU
SYSTEM MEMORY
CPU
Shader Processors
SCREEN

A Solution to the Architectural Problem



Courtesy W. Dally, NVIDIA

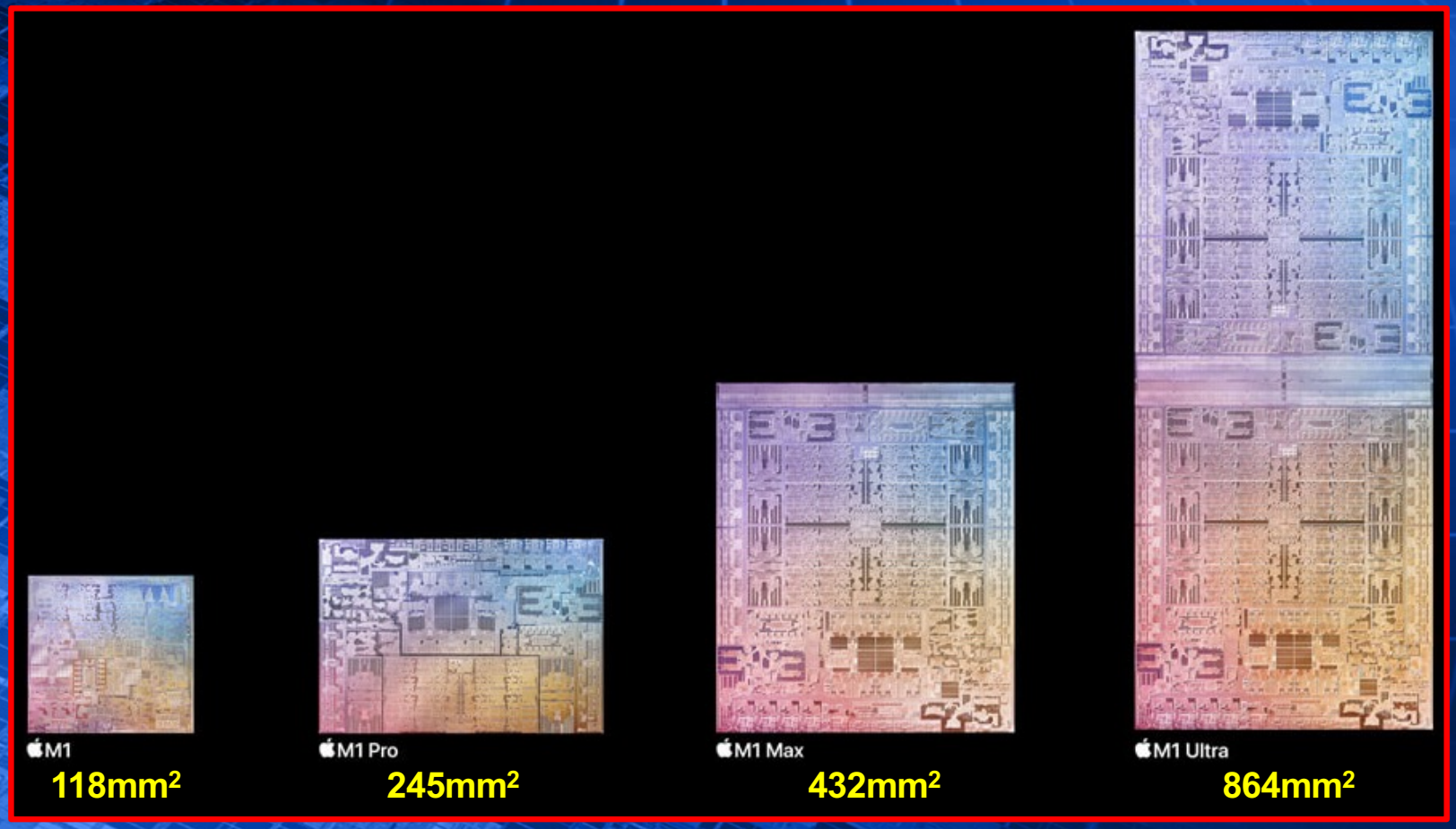

Single-Chip Inference Performance - 1000X in 10 years
Int 8 TOPS
4500.00
4000.00
3500.00
3000.00
2500.00
2000.00
1500.00
1000.00
500.00
0.00
4/1/12
8/14/13
12/27/14
5/10/16
9/22/17
2/4/19
6/18/20
10/31/21
3/15/23
FP32
FMA
FP16
HDP4
FP16
HMMA
Sparsity
INT8
IMMA
K20X
3.94
M40
6.84
P100
21.20
V100
125.00
Q8000
261.00
A100
1248.00
H100
4000.00

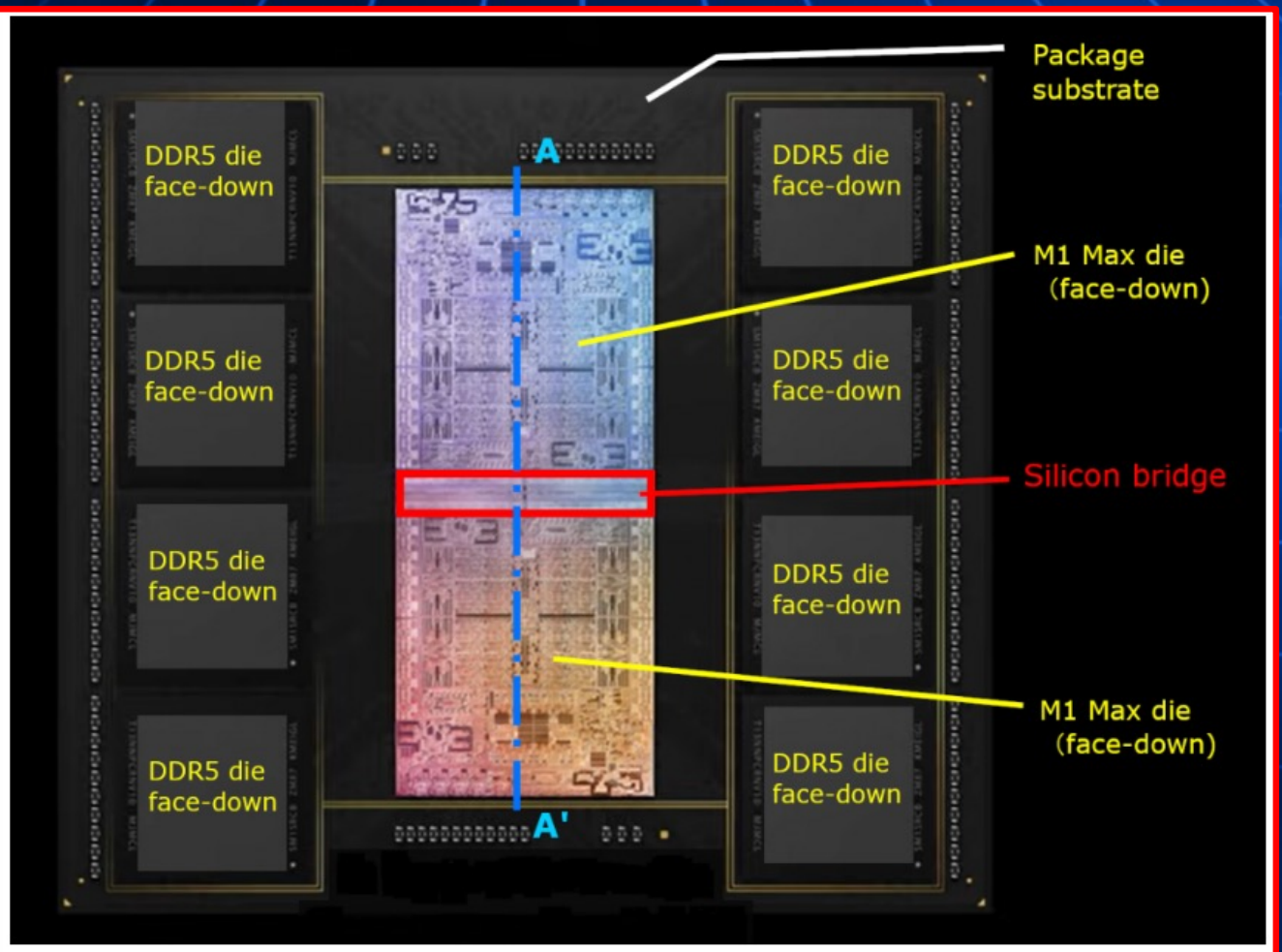
The New Electronics Industry

- 3D Transistors
- Beyond Silicon
- 3D Everything
- System In Package
- New Products
- New Architecture
- SOC: Endless Die Size
- SOC and SIP

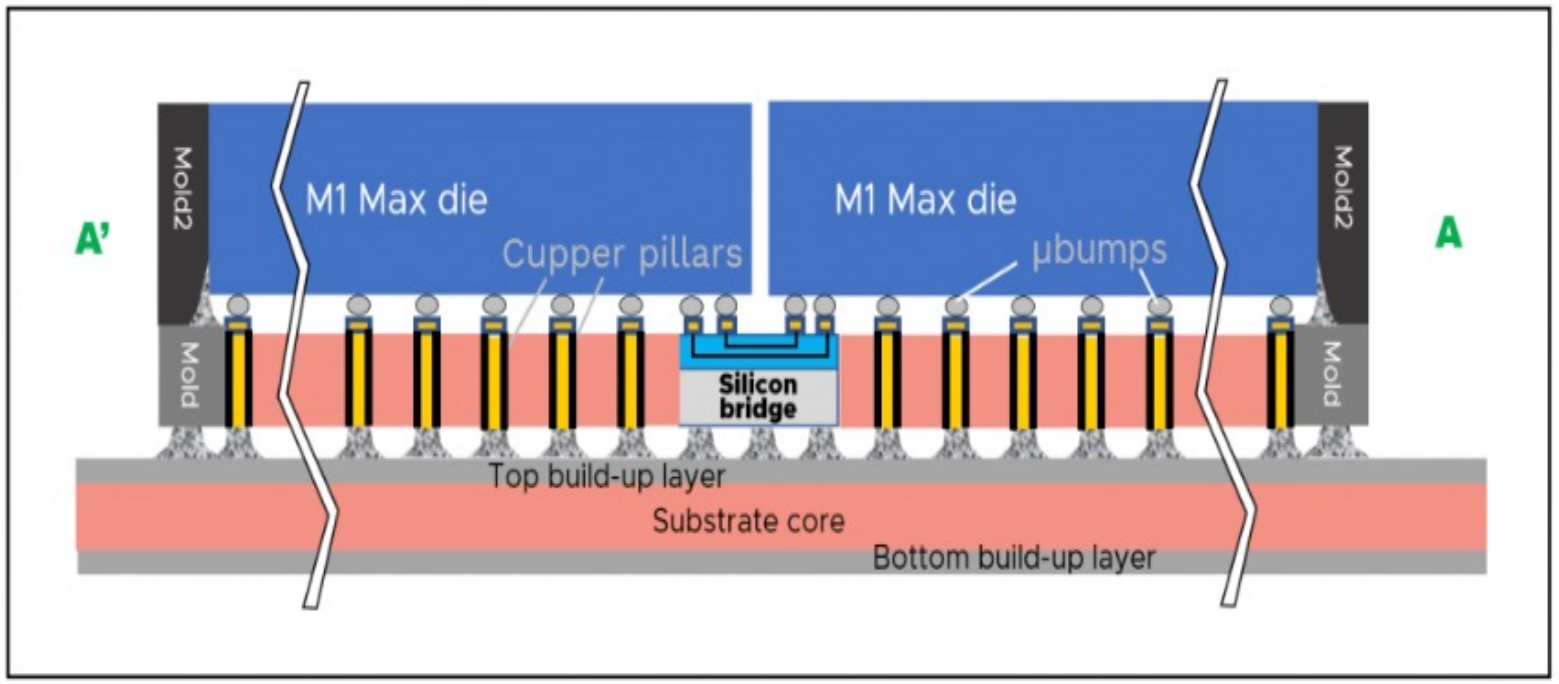
SOC
No Limits to Die Size

APPLE Chips



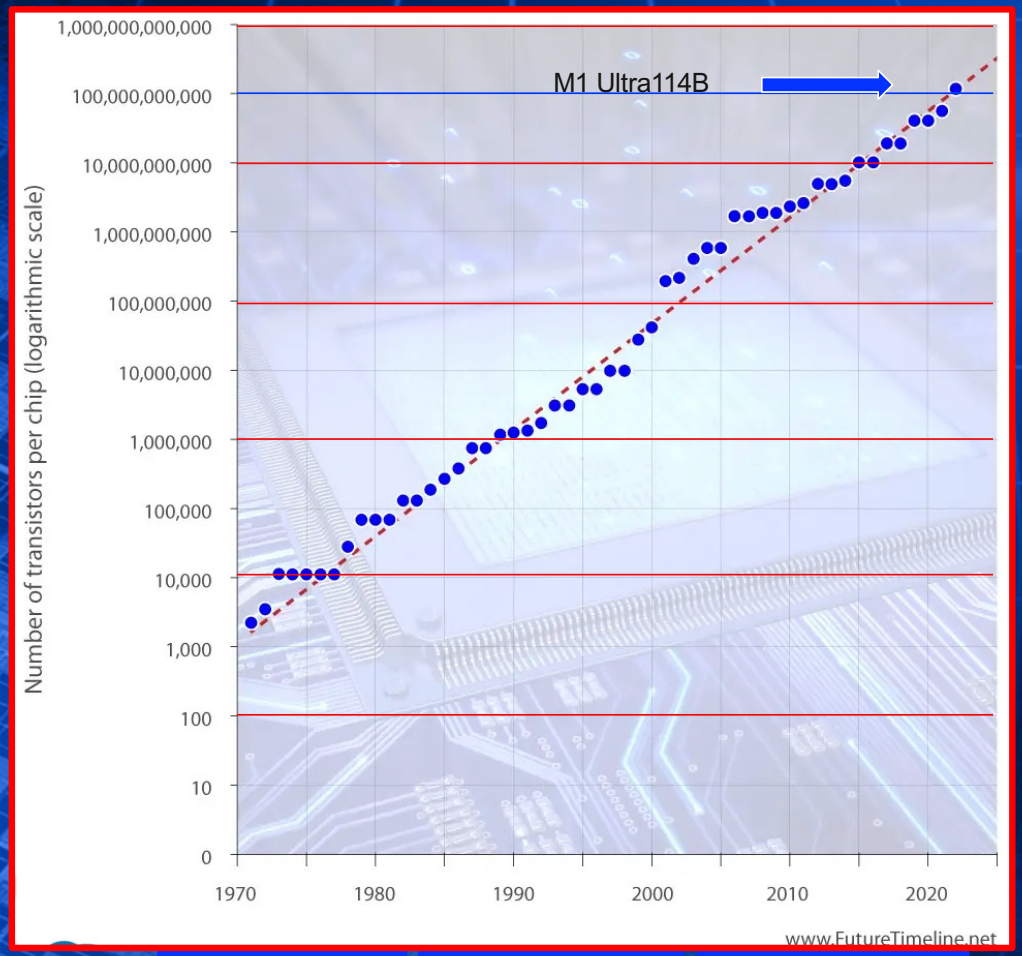


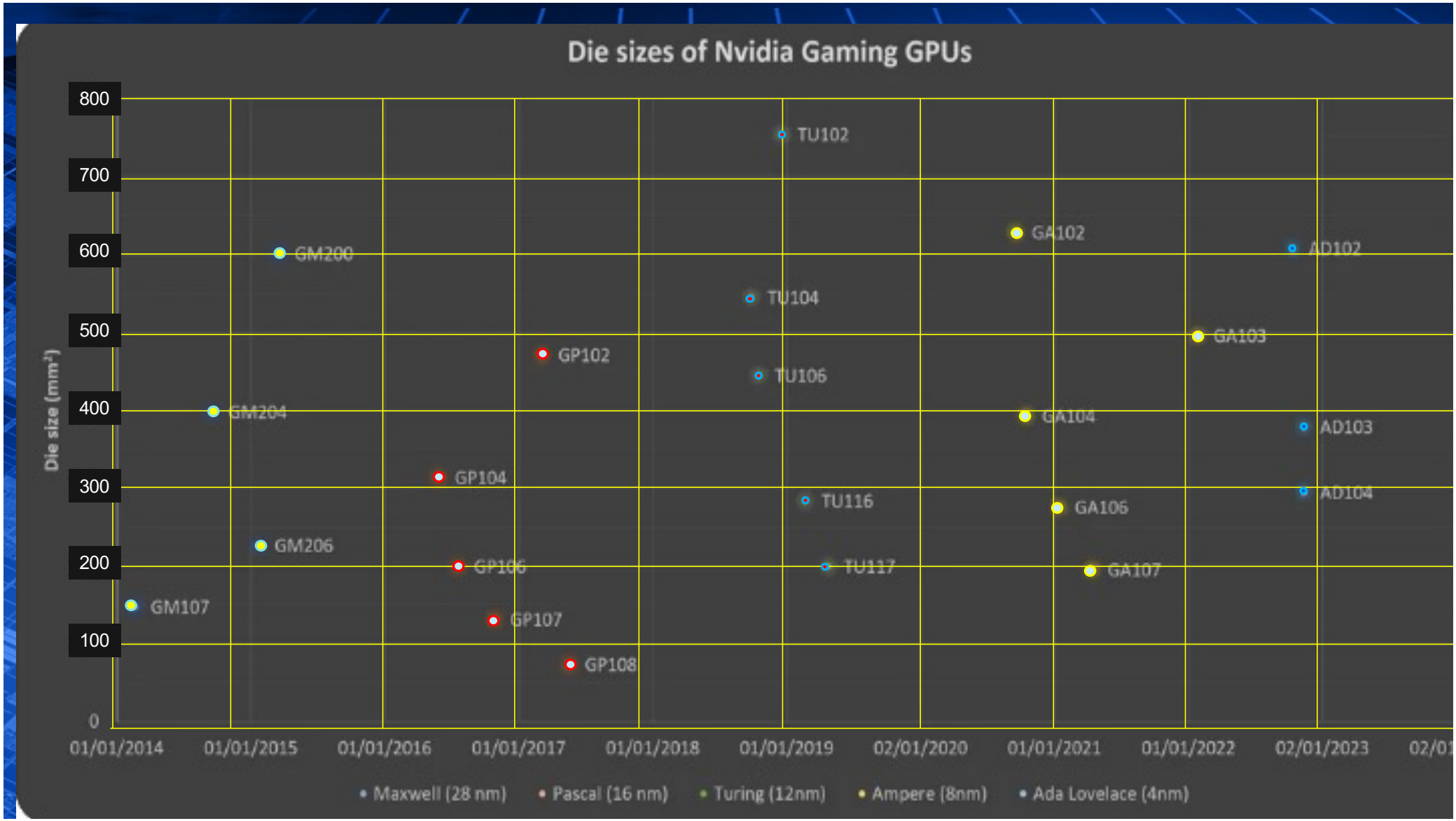
Interior Apple M1 Ultra package Illustration



Vertical cross-section of the M1 Ultra package

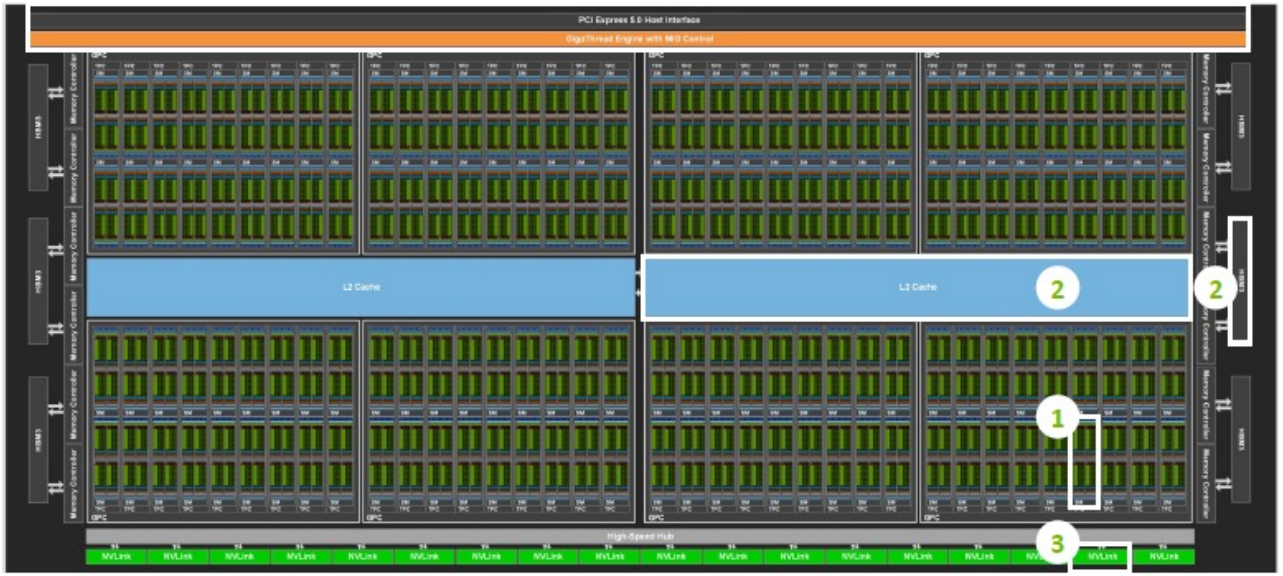
Over 100 Billion Transistors!




Die sizes of Nvidia Gaming GPUs
Die size (mm²)
800
700
600
500
400
300
200
100
0
01/01/2014
01/01/2015
01/01/2016
01/01/2017
01/01/2018
01/01/2019
02/01/2020
01/01/2021
01/01/2022
02/01/2023
GM107
GM206
GM204
GM200
GP108
GP107
GP106
GP104
GP102
TU117
TU116
TU106
TU104
TU102
GA107
GA106
GA104
GA103
GA102
AD104
AD103
AD102
Maxwell (28 nm)
Pascal (16 nm)
Turing (12nm)
Ampere (8nm)
Ada Lovelace (4nm)

NVIDIA Hopper GPU — Full Implementation

80B Transistors, 814mm² in TSMC 4N



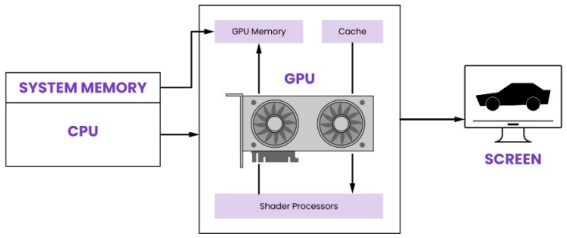
1. 144 SMs 2x Performance Per Clock 4th Gen Tensor Core Thread Block Clusters
2. New Memory System World's First HBM3e DRAM Larger 60MB L2
3. 4th Gen NVLink 900GB/s total BW New SHARP support NVLink Network

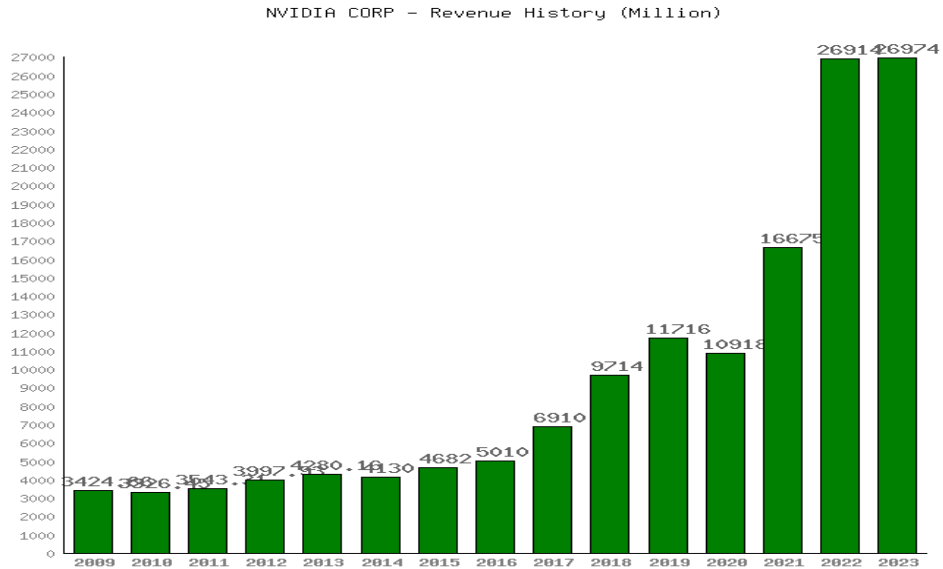
Technologies are Reaching 100M Users Faster than Ever

Source: https://www.visualcapitalist.com/threads-100-million-users/

Nvidia DGX H100	
Component	AI Server
CPU	$ 5,200
8 GPU + 4 NVSwitch Baseboard	$ 195,000
Memory	$ 7,860
Storage	$ 3,456
SmartNIC	$ 10,908
Chassis (Case, backplanes, cabling)	$ 563
Motherboard	$ 360
Cooling (Heatsinks+fans)	$ 463
Power Supply	$ 1,200
Assembly and Test	$ 1,485
Markup	$ 42,000
Total Cost	$ 268,495
DRAM BOM %*	2.9%
NAND BOM %	1.3%
Memory BOM %*	4.2%

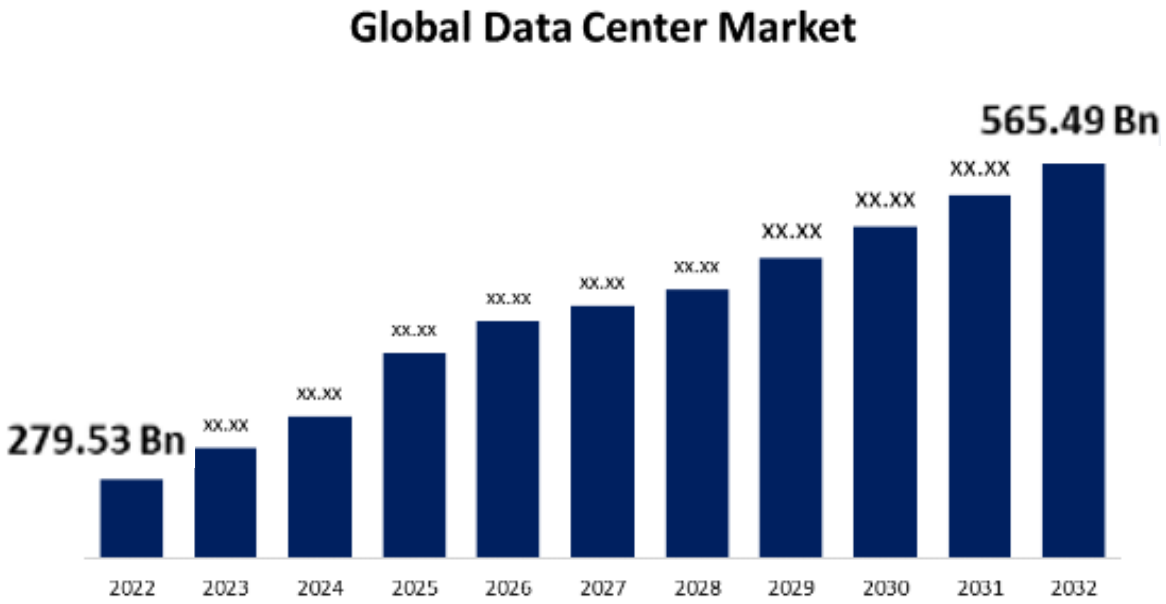
*HBM Costs are not included as they are part of the GPU. We have broken the Nvidia BOM below for subscribers.





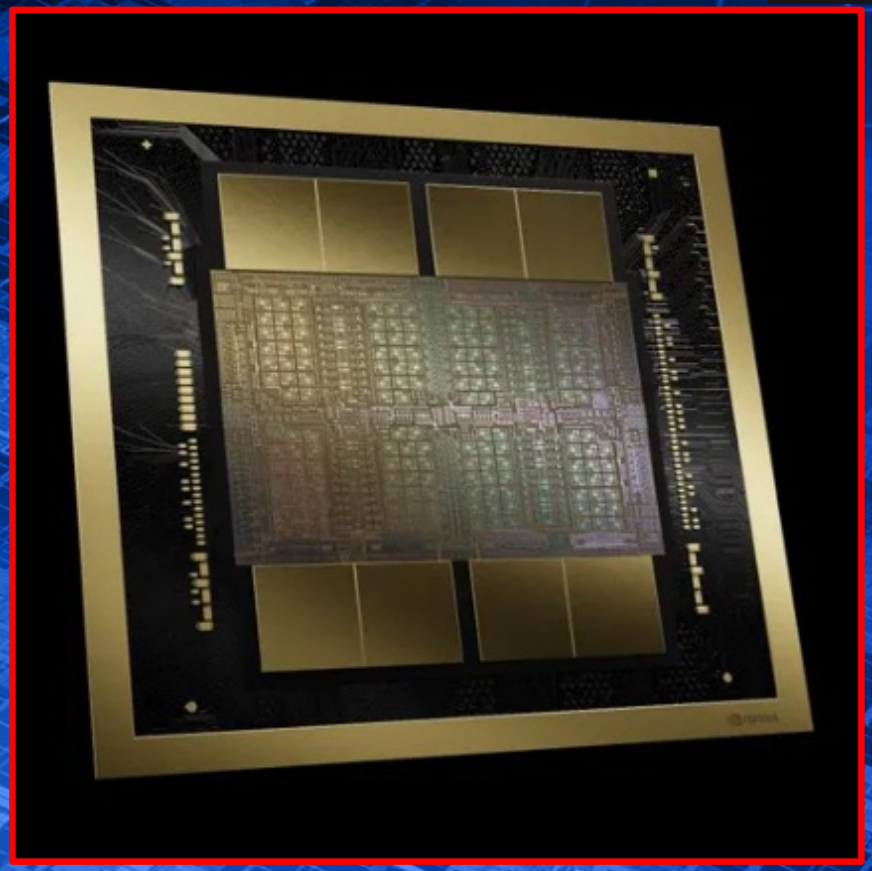
Global Data Center Market Insights Forecasts to 2032

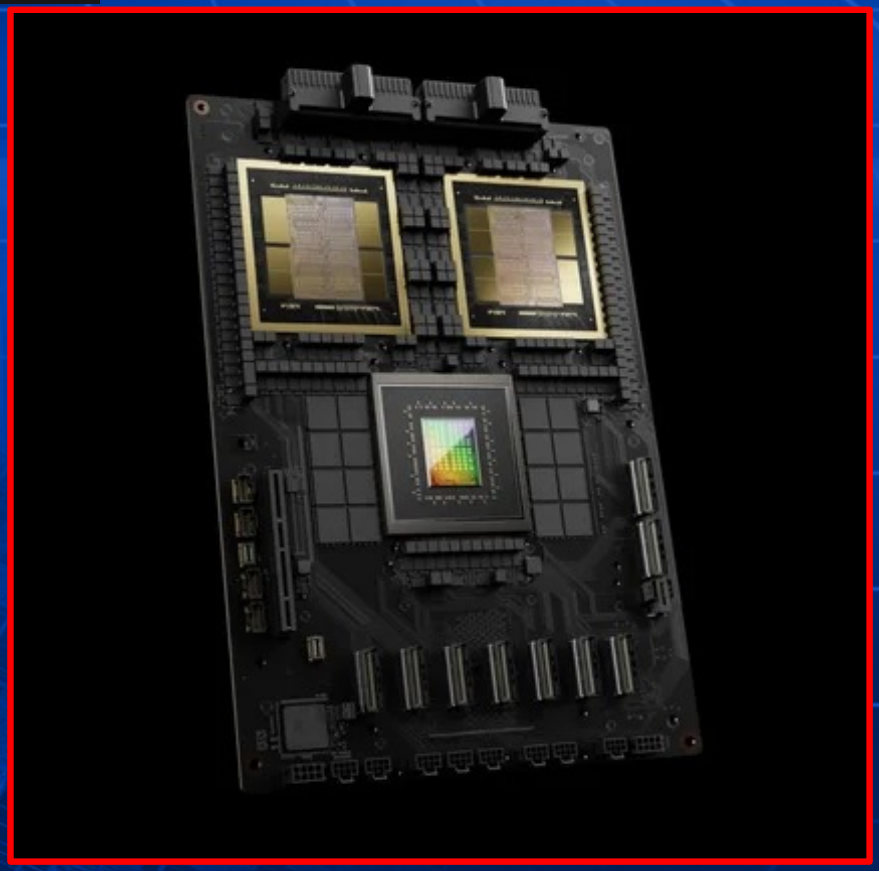
- The Global Data Center Market Size was valued at USD 279.53 Billion in 2022.
- The Market is Growing at a CAGR of 7.3% from 2023 to 2032
- The Worldwide Data Center Market Size is expected to reach USD 565.49 Billion by 2032
- Asia-Pacific is expected to Grow the fastest during the forecast period



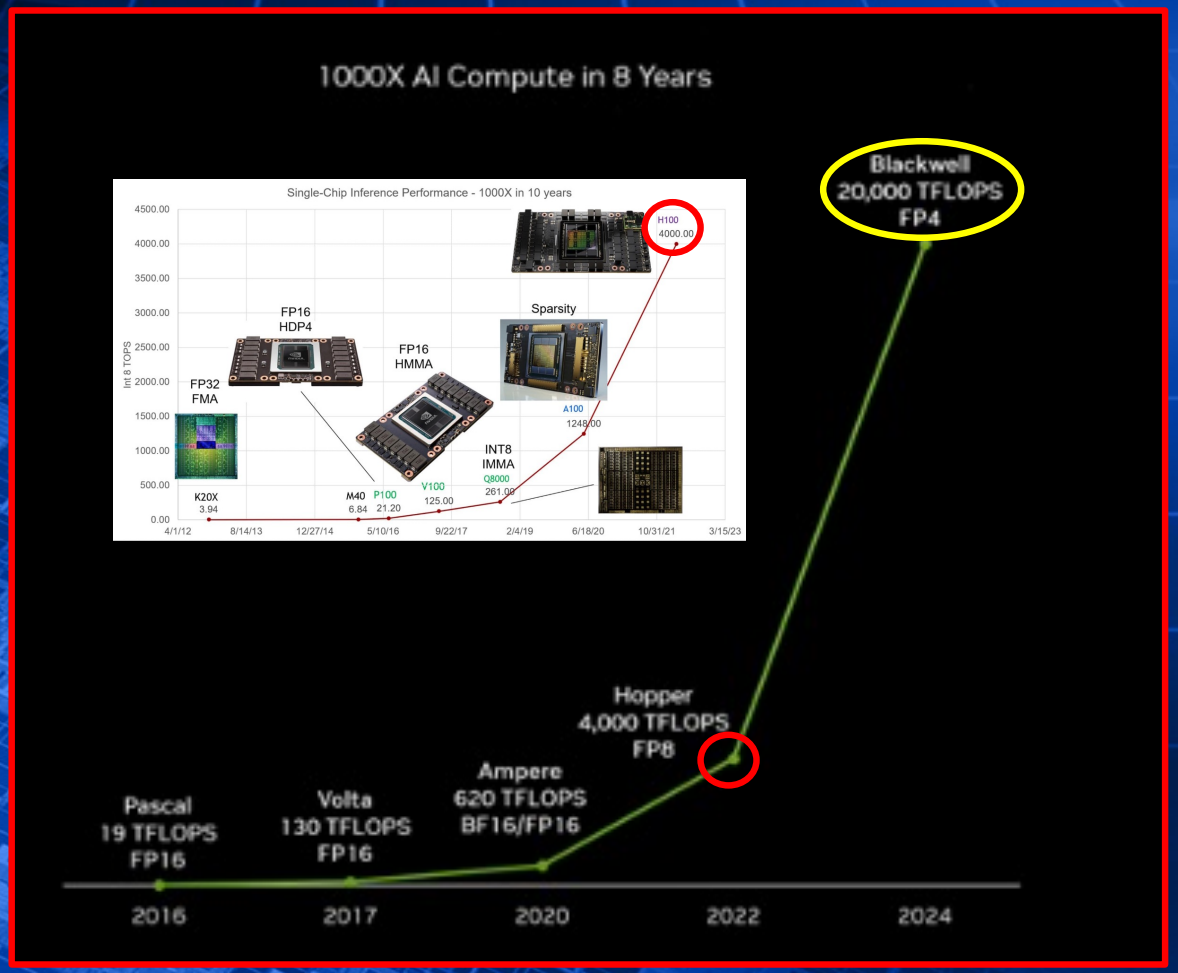
BLACKWELL

March 18, 2024

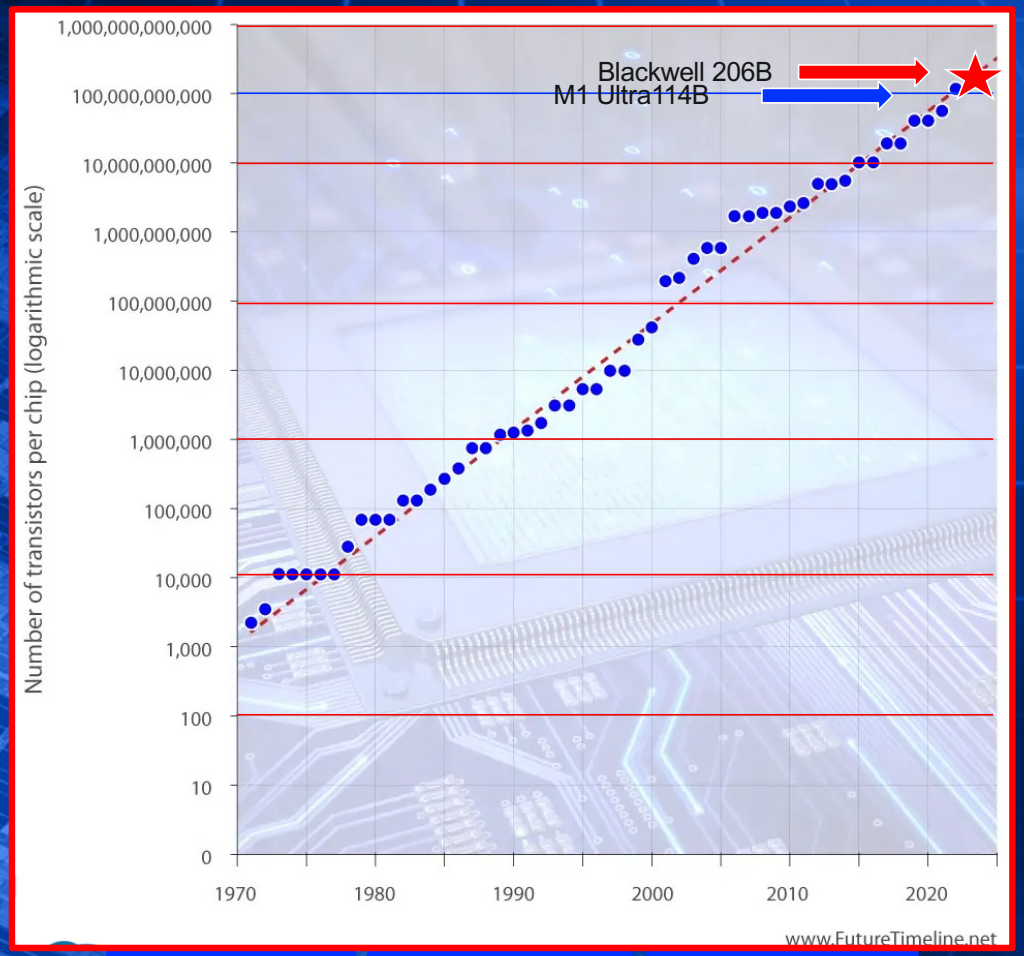




206 Billion Transistors, two 800mm^2 fused dice


1000X AI Compute in 8 Years
Single-Chip Inference Performance - 1000X in 10 years
Int 8 TOPS
4500.00
4000.00
3500.00
3000.00
2500.00
2000.00
1500.00
1000.00
500.00
0.00
4/1/12
8/14/13
12/27/14
5/10/16
9/22/17
2/4/19
6/18/20
10/31/21
3/15/23
FP32
FMA
FP16
HDP4
FP16
HMMA
Sparsity
INT8
IMMA
K20X
3.94
M40
6.84
P100
21.20
V100
125.00
A100
1248.00
Q8000
261.08
H100
4000.00
Blackwell
20,000 TFLOPS
FP4
Hopper
4,000 TFLOPS
FP8
Ampere
620 TFLOPS
BF16/FP16
Volta
130 TFLOPS
FP16
Pascal
19 TFLOPS
FP16
2016
2017
2020
2022
2024

Over 200 Billion Transistors!



4 TRILLION TRANSITORS

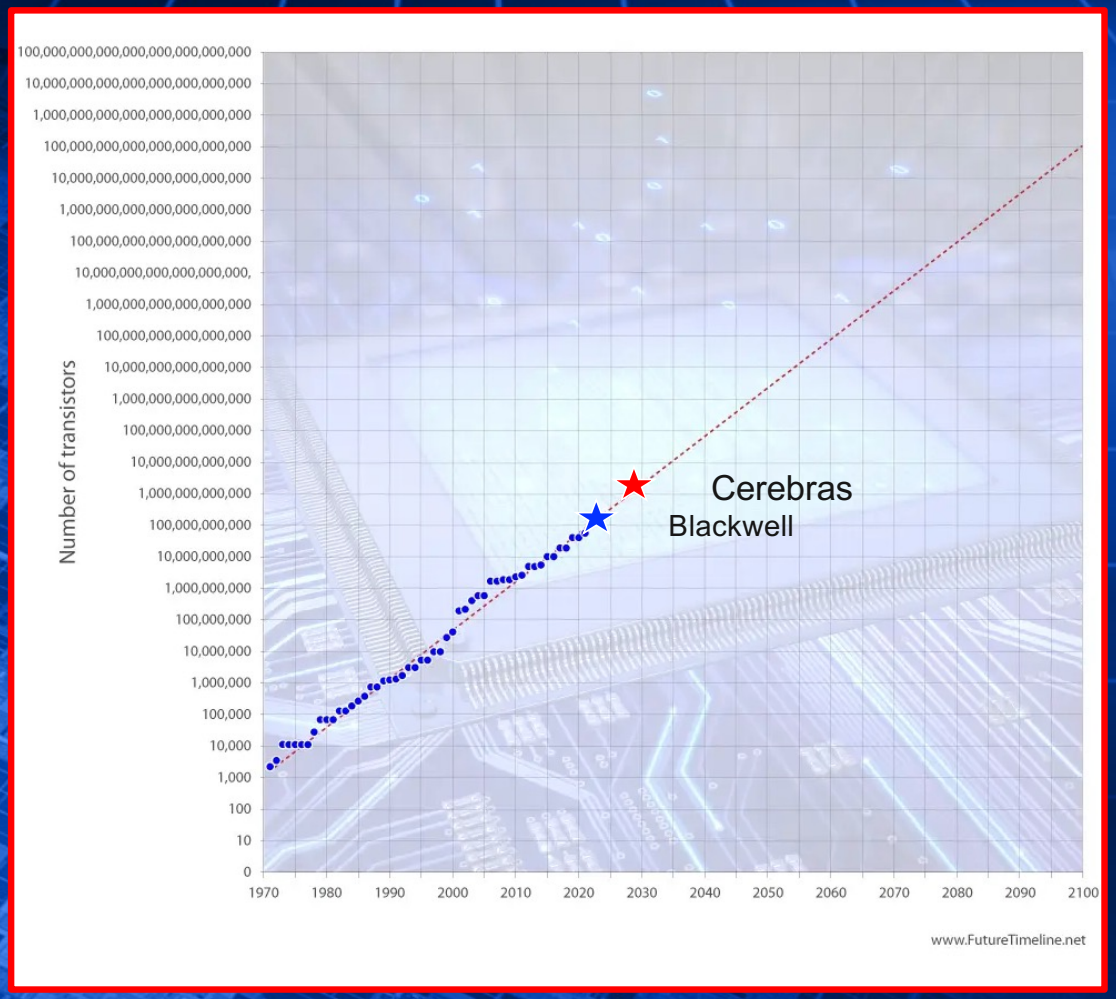
Andrew Feldman

900,000 AI-Optimized Cores 123x more cores	**44GB** On-Chip SRAM 1,000x more on-chip memory
214Pb/s Interconnect Bandwidth 45,000x more bandwidth	**21PB/s** Memory Bandwidth 12,800x more bandwidth
1.2Tb/s System I/O	**15RU** System Dimensions

There is no fundamental obstacle to achieving device yields of 100%. At present, packaging costs so far exceed the cost of the semiconductor structure itself that there is no incentive to improve yields, but they can be raised as high as is economically justified. No barrier exists comparable to the thermodynamic equilibrium considerations that often limit yields in chemical reactions; it is not even necessary to do any fundamental research or to replace present processes.

Only the engineering effort is needed

Gordon Moore, 1965


Number of transistors
100,000,000,000,000,000,000,000,000,000
10,000,000,000,000,000,000,000,000,000
1,000,000,000,000,000,000,000,000,000
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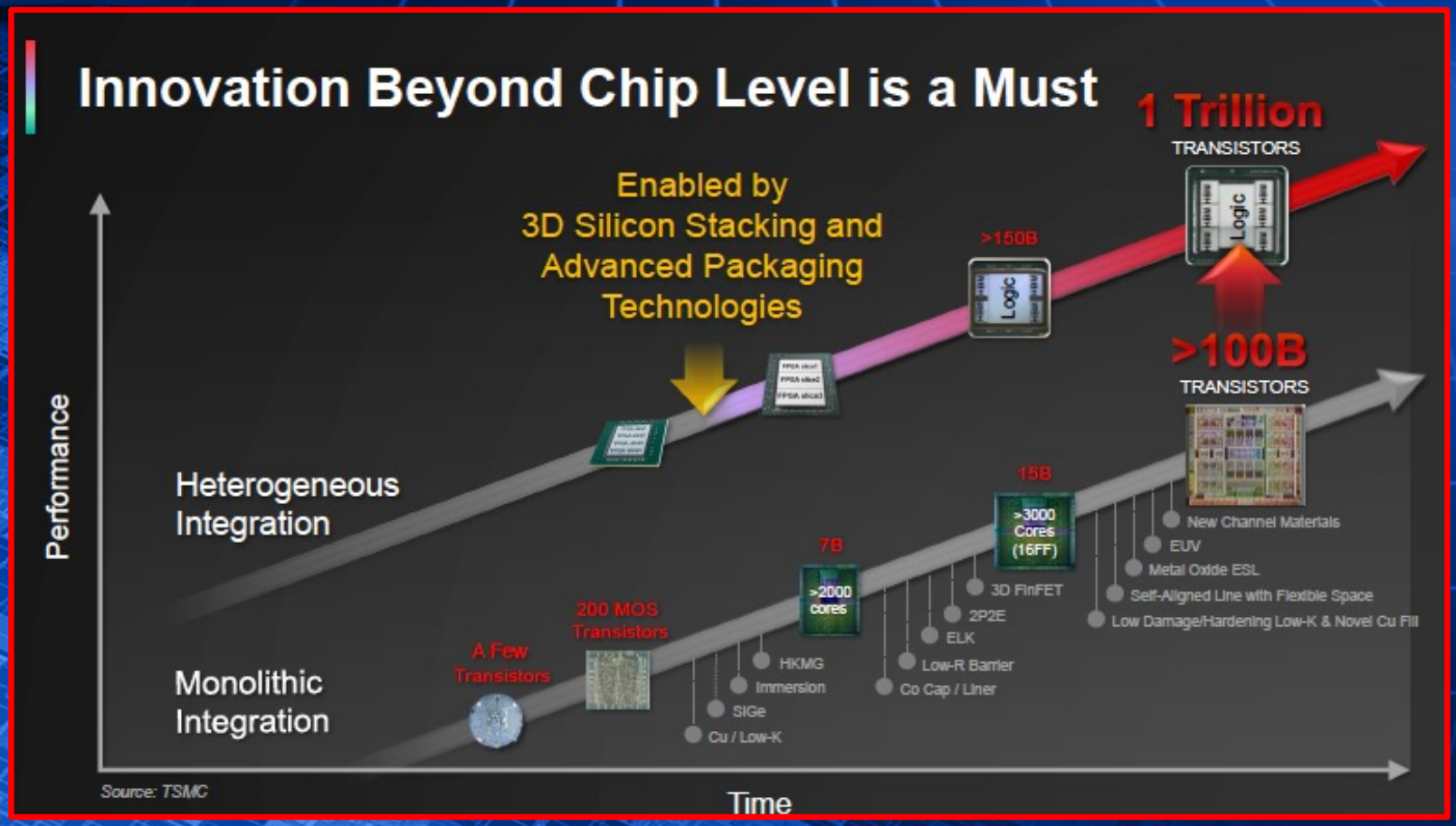
1970
1980
1990
2000
2010
2020
2030
2040
2050
2060
2070
2080
2090
2100
Cerebras
Blackwell
www.FutureTimeline.net

The New Electronics Industry

- 3D Transistors
- Beyond Silicon
- 3D Everything
- System In Package
- New Products
- New Architecture
- SOC: Endless Die Size
- SOC and SIP

SOC and SIP



Source: Kevin Zhang, Sr. VP of TSMC, February 19, 2024, ISSCC Plenary

1975

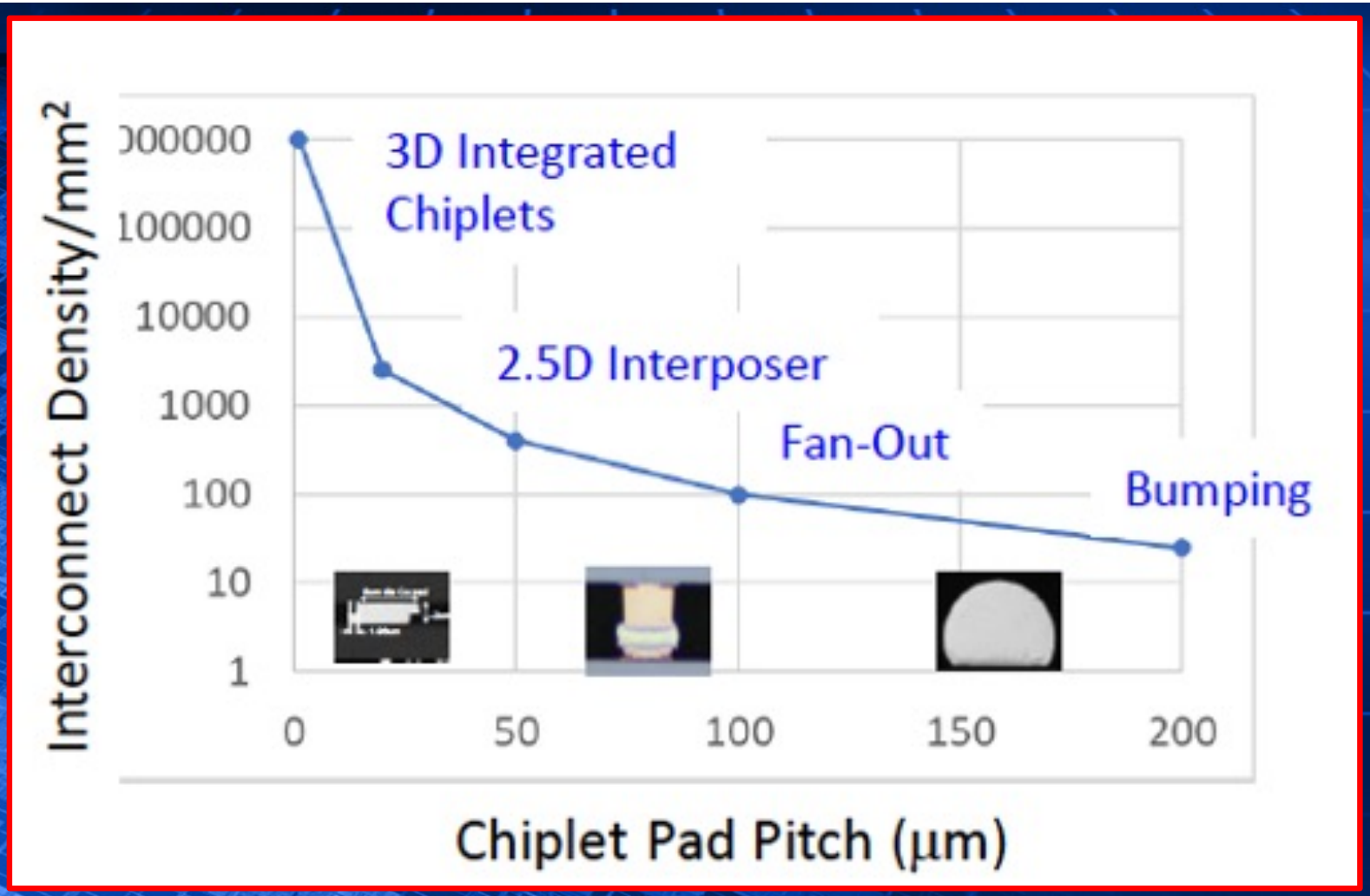
THE NUMBER OF TRANSISTORS PRODUCED IN AN INTEGRATED CIRCUIT CAN COST EFFECTIVELY DOUBLE EVERY 2 YEARS

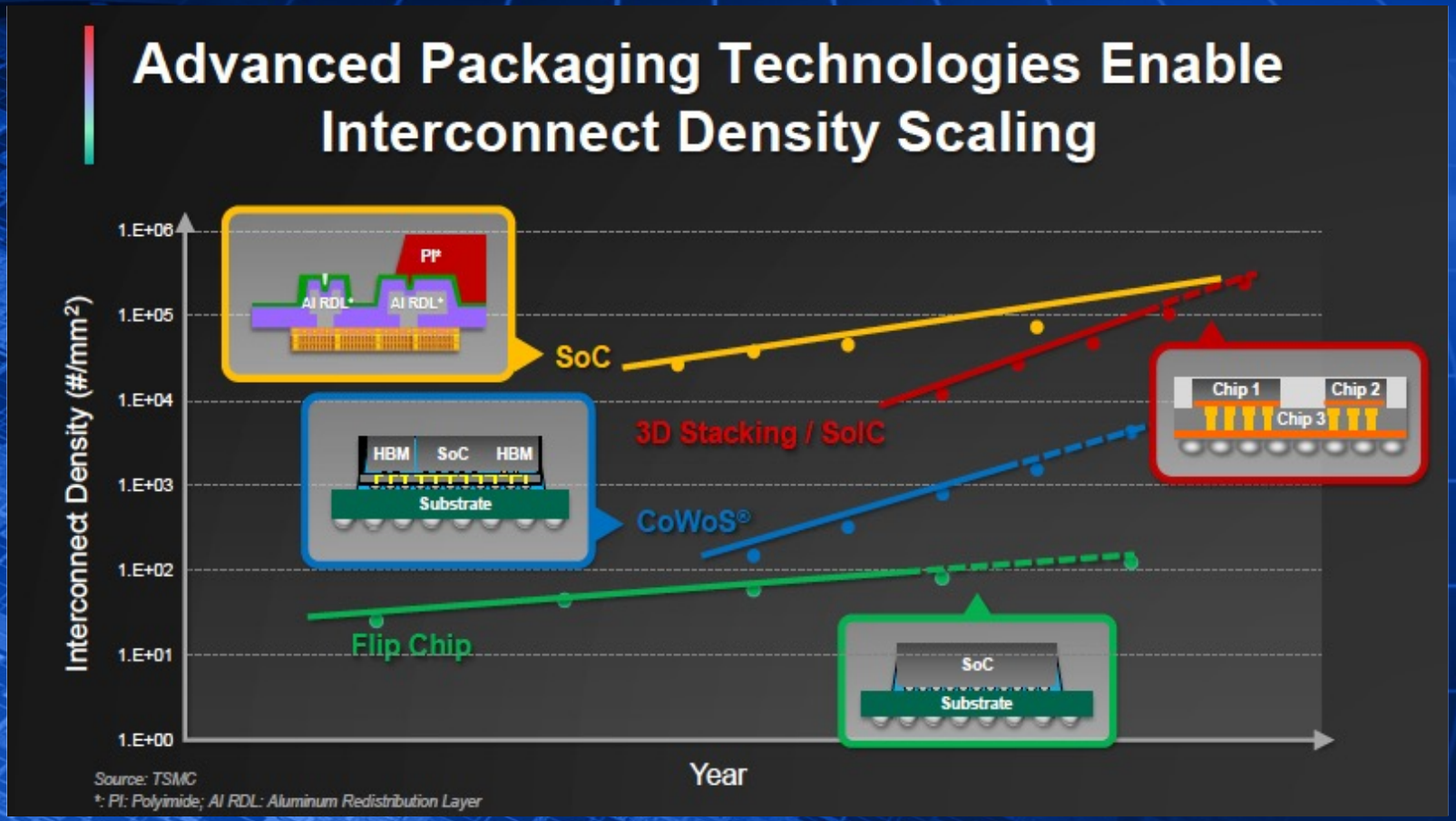
Gordon Moore

2020

THE NUMBER OF BITS PRODUCED IN AN INTEGRATED PACKAGE CAN COST EFFECTIVELY DOUBLE EVERY 2 YEARS

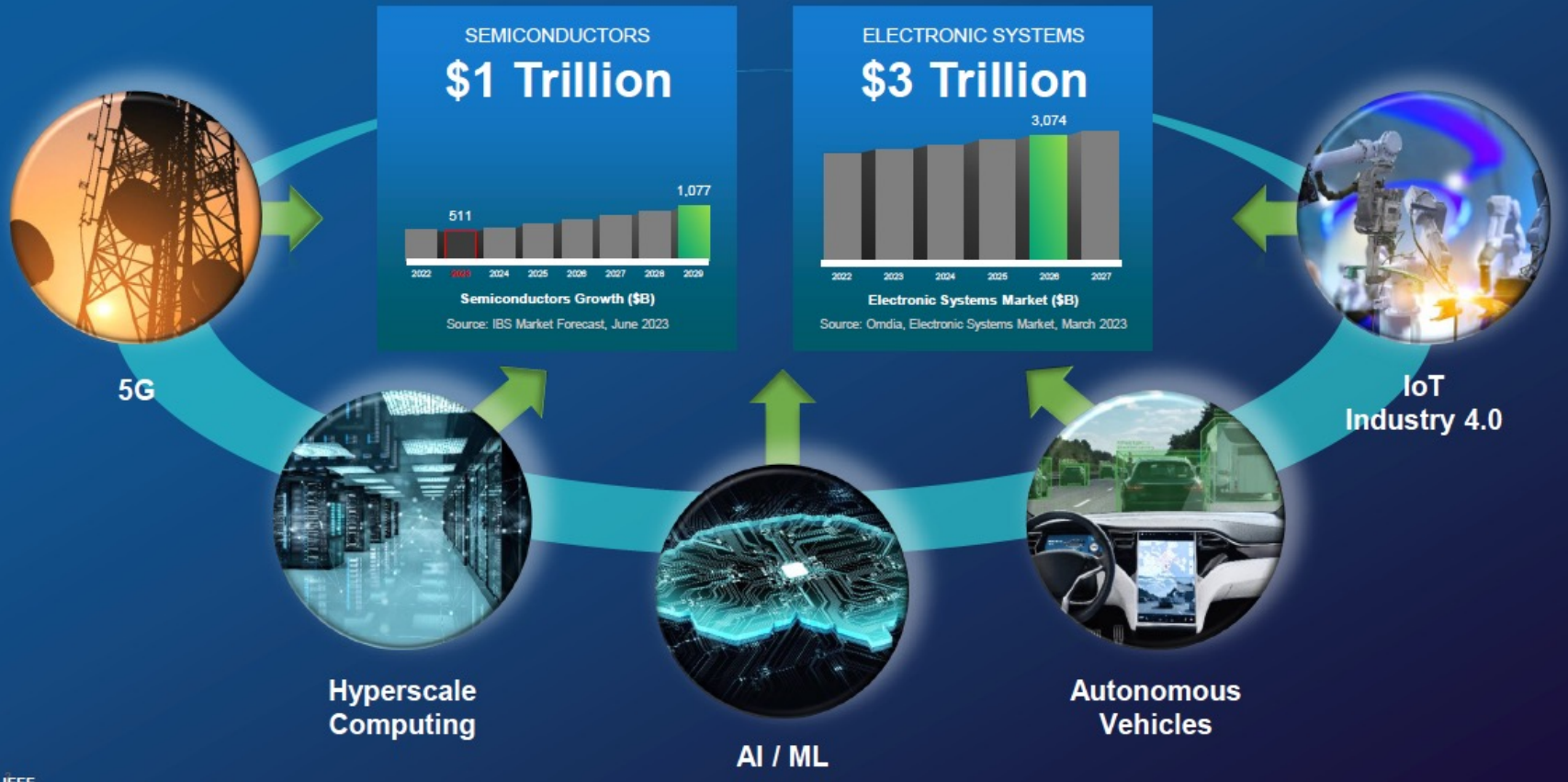
Paolo Gargini


Interconnect Density/mm²
000000
100000
10000
1000
100
10
1
3D Integrated
Chiplets
2.5D Interposer
Fan-Out
Bumping
0
50
100
150
200
Chiplet Pad Pitch (µm)



Source: Kevin Zhang, Sr. VP of TSMC, February 19, 2024, ISSCC Plenary

Generational Semiconductor Drivers



Conclusions

Transistor, Die, Package, Architecture, Products

- During the past 60 years the Electronics Industry has undergone and overcome 3 transformational inflection points
- In each case the Electronics Industry has created new semiconductors' devices and introduced new products that have transformed society
- The Electronics Industry is undergoing a top to bottom and bottom to top unprecedented revolution.
- SOC, SIP, GAA beyond silicon are all coming together to support unlimited possibilities
- AR/VR will give everybody a new "vision" of reality
- AI is going to make everybody omniscient
- Everything we have known will change in the new society