Emerging semiconductors meet new applications: security, multi-valued computing, and hazard monitoring

- Material-Device-Circuit Co-Consideration

Hocheon Yoo

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Head Professor of Graduate School
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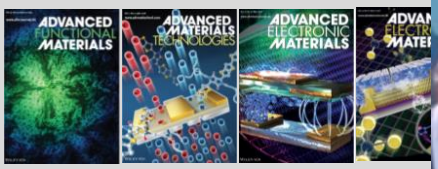
Gachon University

Homepage: https://sites.google.com/view/sdclab/

Introduction



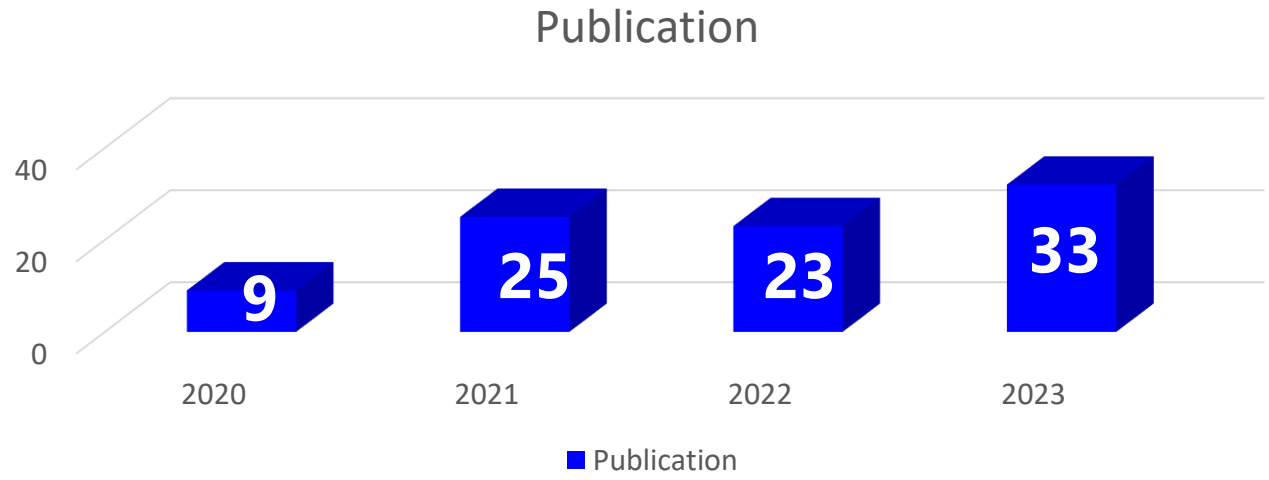
Postdoc, Northwestern Univ. (2019)
Ph.D., POSTECH (2018)
Visiting scholar, Holst Centre, Netherl
B.S., Hanyang Univ. (2014)

2022,2023)
Excellence, (2022, 2023)
21)
ard, (2021, 2023)

The SDC Research Lab develops
a material-device-process co-innovation approach.

Gachon Academic Top 1 (2022,203)
Gachon one of largest Lab (2022)


Gangnam
5 km
Gachon
Univ.
Gachon University,
Global Campus
COEX
L7 Gangnam
Ttukseom Hangang Park
Leeum Museum of Art
K-Star Road
Jamwon Hangang
Riverside Park
Garosu-gil
Gotomall Underground
Shopping Mall
Hilton Garden Inn
Seoul Gangnam
SaRang Church
Hangaram Arts
Center Museum
조효상점
Grocery store
Garak Market
Starfield City Wirye
SEONGSU-DONG
CHEONHO-DONG
GIL-DONG
PUNGNAP-DONG
SEONGNAE-DONG
DUNCHON-DONG
CHEONGDAM-DONG
SINCHEON-DONG
BOGWANGDONG
JAMWON-DONG
NONHYEON-DONG
BANPO-DONG
BANGI-DONG
GAMIL-DONG
SONGPA-GU
OGEUM-DONG
MACHEON-DONG
YEOKSAM-DONG
SAMJEON-DONG
GANGNAM-GU
GARAK-DONG
GEOYEO-DONG
SEOCHO-DONG
DOGOK-DONG
IRWON-DONG
SUSEO-DONG
MUNJEONG-DONG
GAEPO-DONG
JANGJI-DONG
SEOCHO-GU
CHANGGOK-DONG
TAEPYEONG-DONG
SINHEUNG-DONG
GWACHEON-DONG
SEOUL
GYEONGGI-DO



Energy Band Engineering by Remote Doping of Self-Assembled Monolayer Leads to High-Performance IGZO/p-Si Heterostructure Photodetectors. ***Advanced Materials,*** IF: 32.09

Vertically-Integrated Electronics: New Opportunities from Emerging Materials and Devices.
Nano-Micro Letters, IF: 23.655

A reconfigurable binary/ternary logic conversion-in-memory based on drain-aligned floating-gate heterojunction transistors.
Nature Communications, IF: 17.69

Machine Learning Attacks-Resistant Security by Mixed-Assembled Layers-Inserted Graphene Physically Unclonable Function.
Advanced Science, IF: 17.521

Vertically-Stacked, Low-Voltage Organic Ternary Logic Circuits Including Nonvolatile Floating-Gate Memory Transistors.
Nature Communications, IF: 17.69

Strengthening Multi-Factor Authentication through Physically Unclonable Functions. ***Advanced Science,*** IF: 17.52

Charge Transport Advancement in Anti-Ambipolar Transistors: Spatially Separating Layer Sandwiched between N-type Metal Oxides and P-type Small Molecules. ***Advanced Functional Materials,*** IF: 19.924

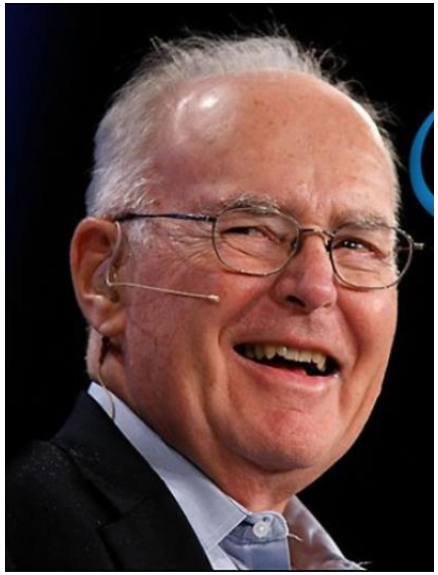
Nanoscale Channel Gate-Tunable Diodes Obtained by Asymmetric Contact and Adhesion Lithography on Fluoropolymers.
Small, IF: 15.153

Contributions of Light to Novel Logic Concepts using Optoelectronic Materials
Small Methods, IF: 15.367

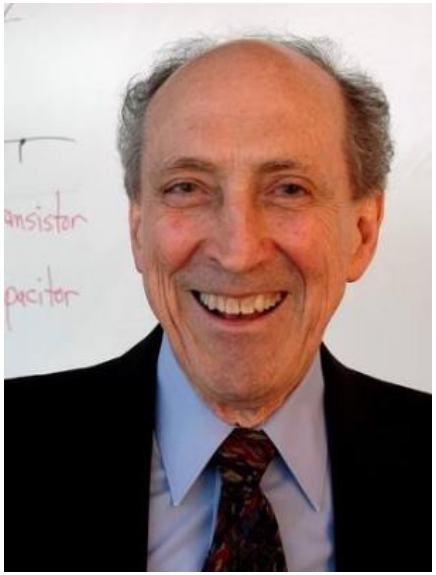
Boosting the Optoelectronic Properties of Molybdenum Diselenide by Combining Phase Transition Engineering with Organic Cationic Dye Doping. ***ACS nano,*** IF: 15.881

Unpredictably Disordered Distribution of Hetero-blended Graphene Oxide Flakes with Non-identical Resistance in Physical Unclonable Functions. ***Advanced Functional Materials,*** IF: 19.924

Background

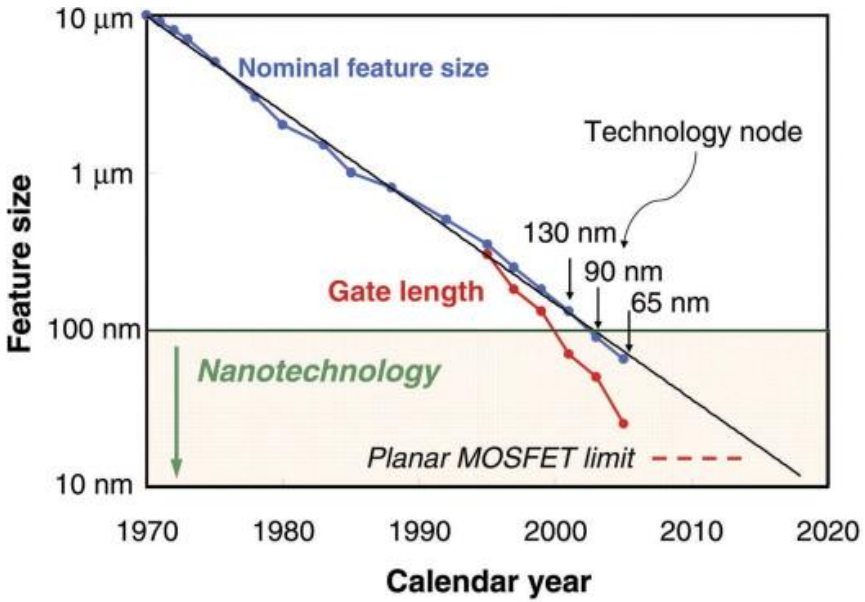


Gordon Moore



Robert Dennard

Thompson, Scott E., and Srivatsan Parthasarathy. Materials today 9.6 (2006): 20-25.



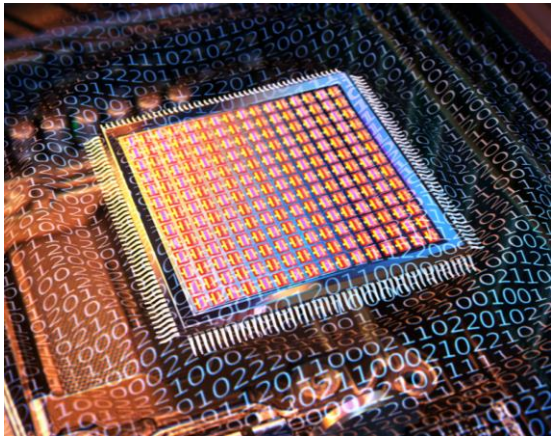
☺ **Lower power consumption**

☺ **Higher operating frequency**

☹ **Scaling limit** ➡

- **New Materials**
- **New Devices**
- **New Circuits**

Multi-valued logic

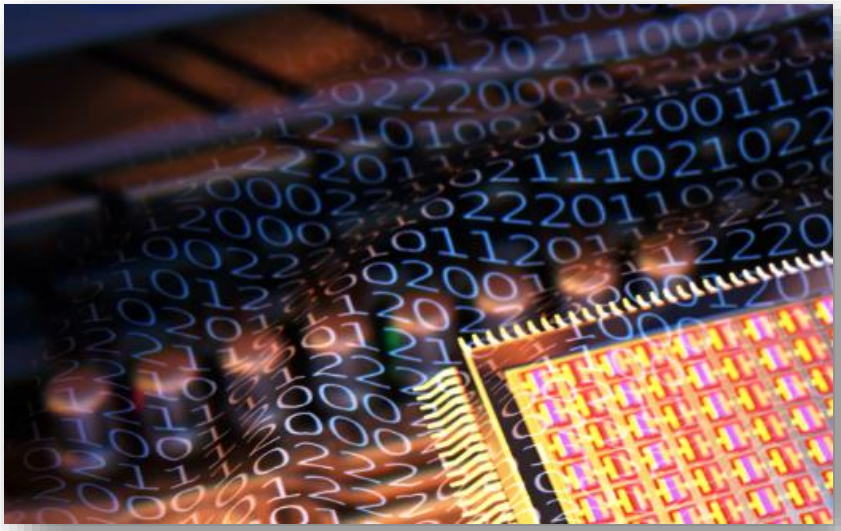


Security Devices

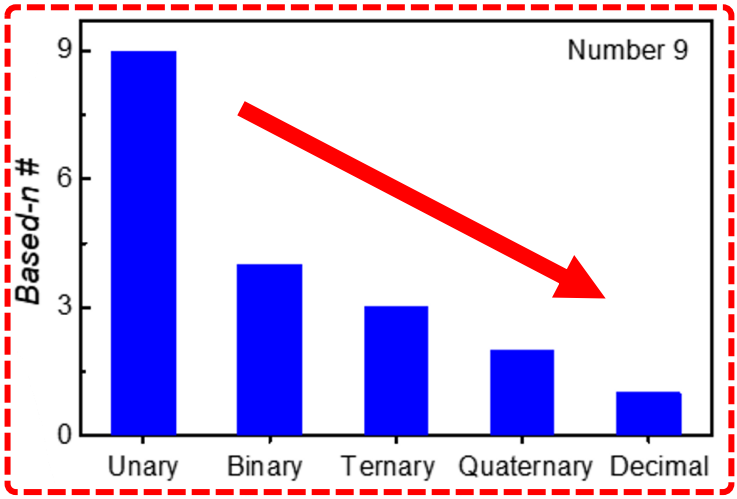
Multi-valued Logic

Binary

Ternary



Decimal	1	2	3	4	5	6	7	8	9
Binary	1	10	11	100	101	110	111	1000	1001
Ternary	1	2	10	11	12	20	21	22	100
Quaternary	1	2	3	10	11	12	13	20	21

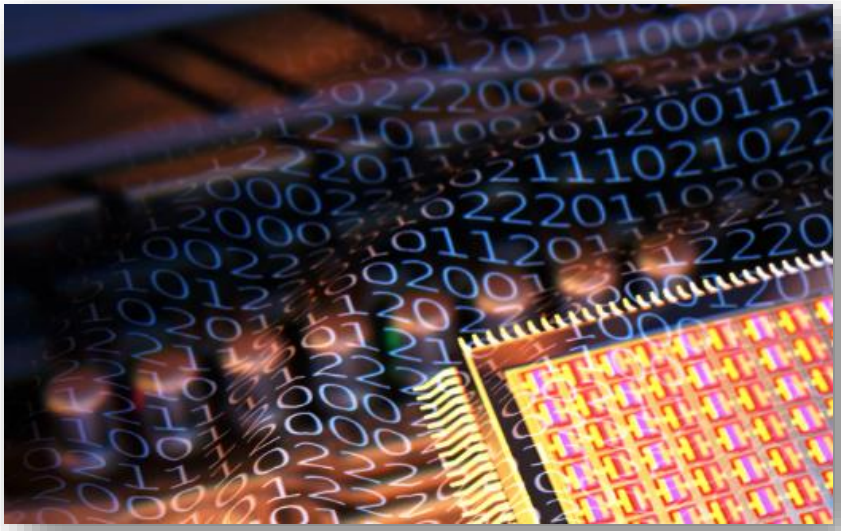


Hocheon Yoo, Chang-Hyun Kim, *Journal of Materials Chemistry C*, 2021

Multi-valued Logic

Binary

Ternary



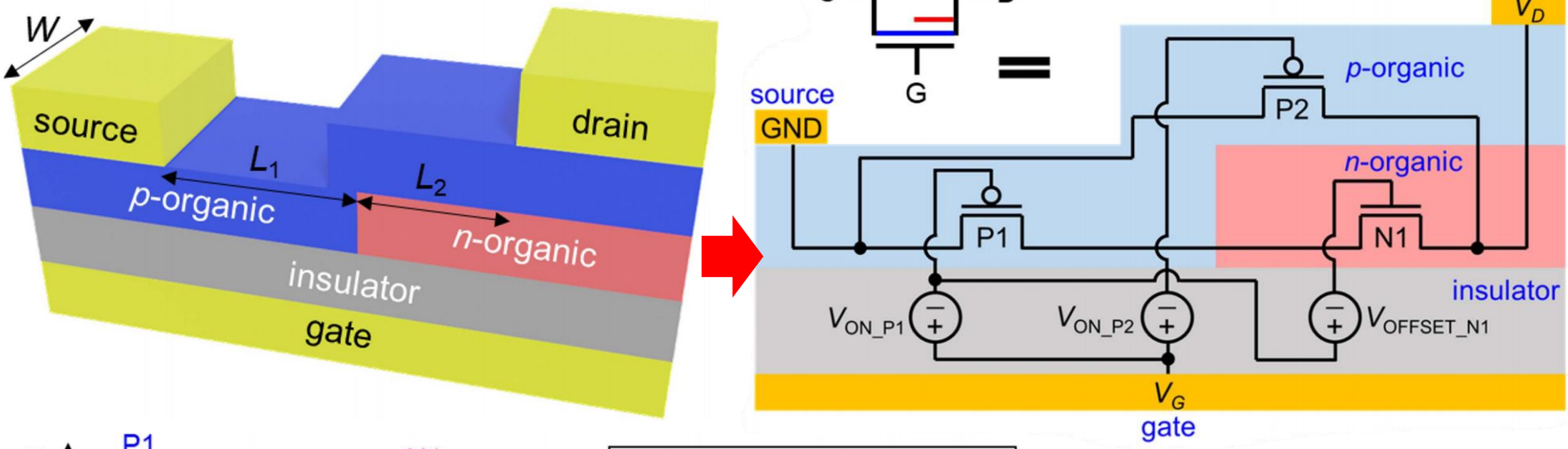
Higher Information Density

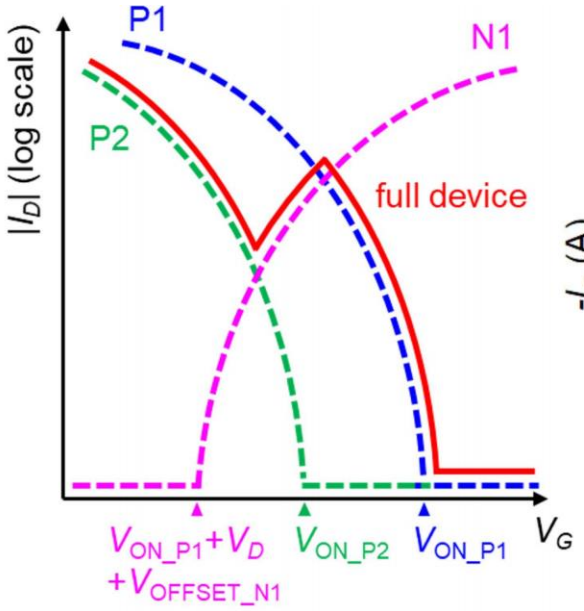
Reduced interconnect Lines

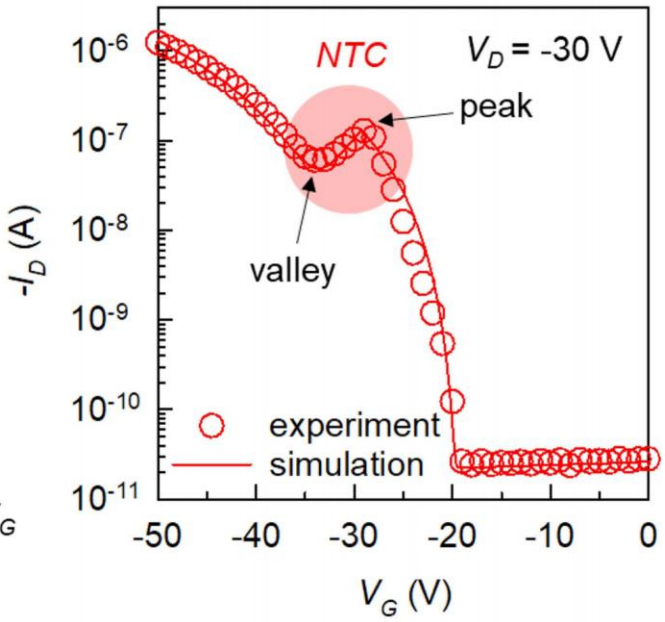
Lower Power Consumption

How to make ternary logic?

Multi-valued Logic







- **Peak/valley current**
- **NTC region**
- **Well-defined off-current**
- **Well-defined on-current**

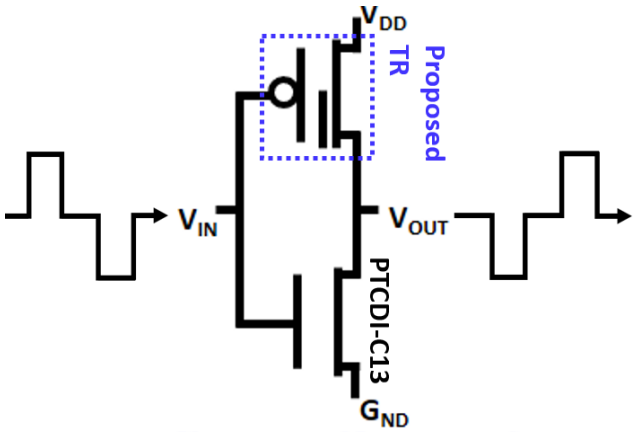
Hocheon Yoo, Chang-Hyun Kim *et al.*, *IEEE TED* (2022).

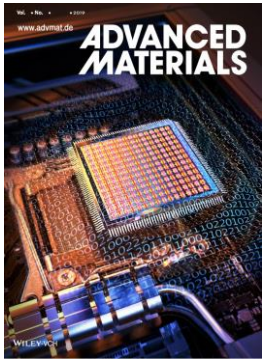
Multi-valued Logic

Logic = 2 (V_{DD}) → Logic = 1 (V_{DD}/2) → Logic = 0 (G_{ND})

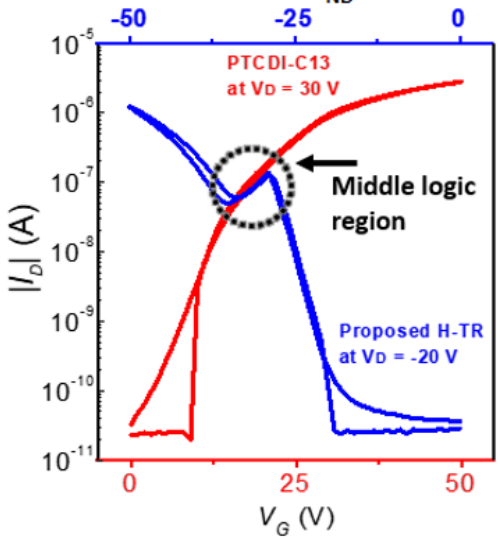
DC characteristic

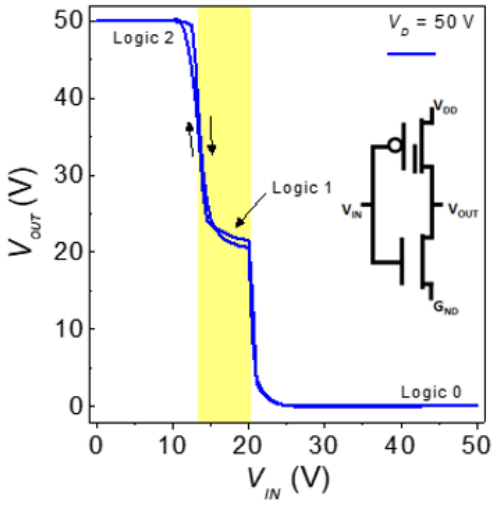
Transient characteristic





Front cover, July 2019





Three logic state (Logic = 2, 1, 0)

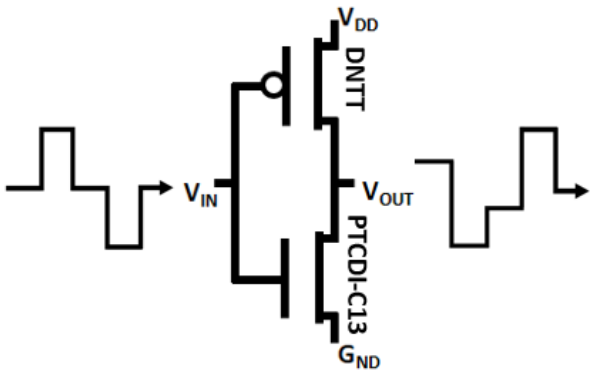
Hocheon Yoo *et al.*, ***Advanced Materials*** (2019) 1808265

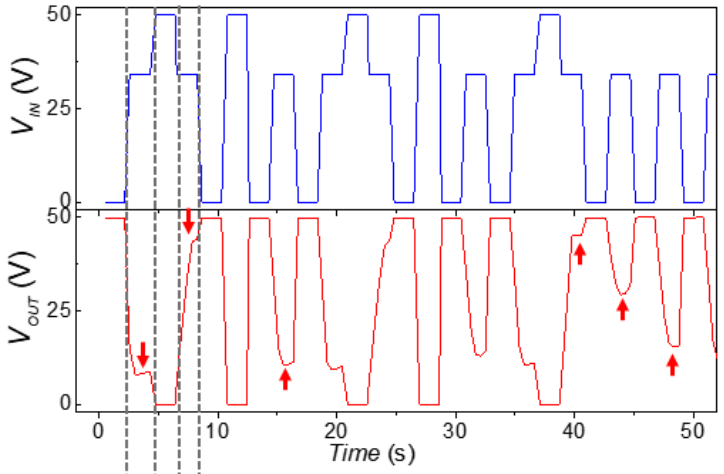
Multi-valued Logic

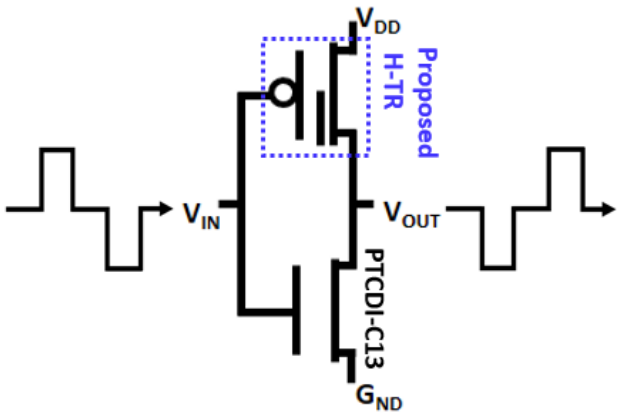
Logic = 2 (V_{DD}) → Logic = 1 (V_{DD}/2) → Logic = 0 (G_{ND})

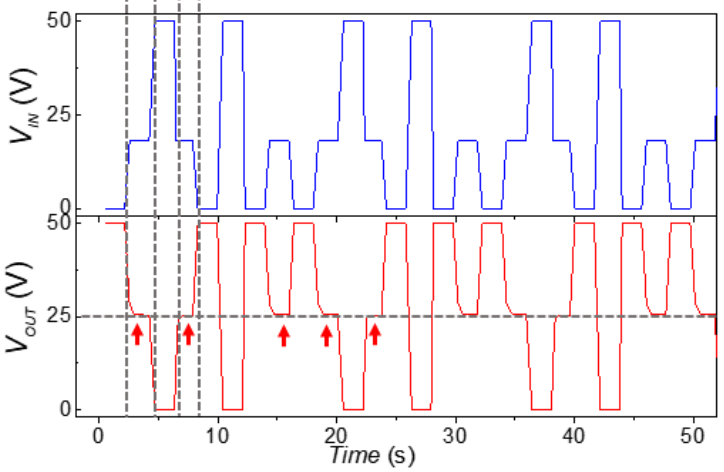
DC characteristic

Transient characteristic



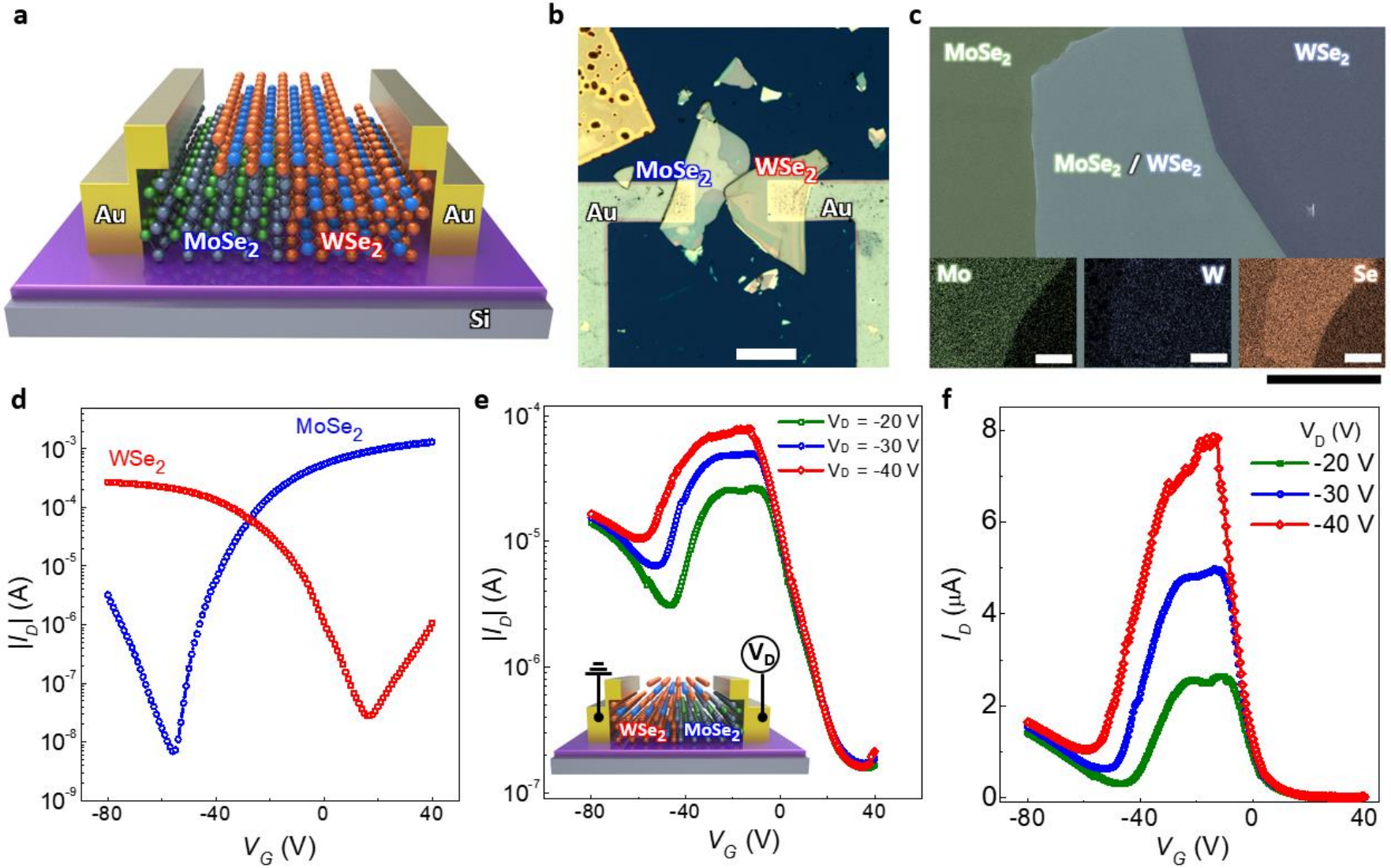






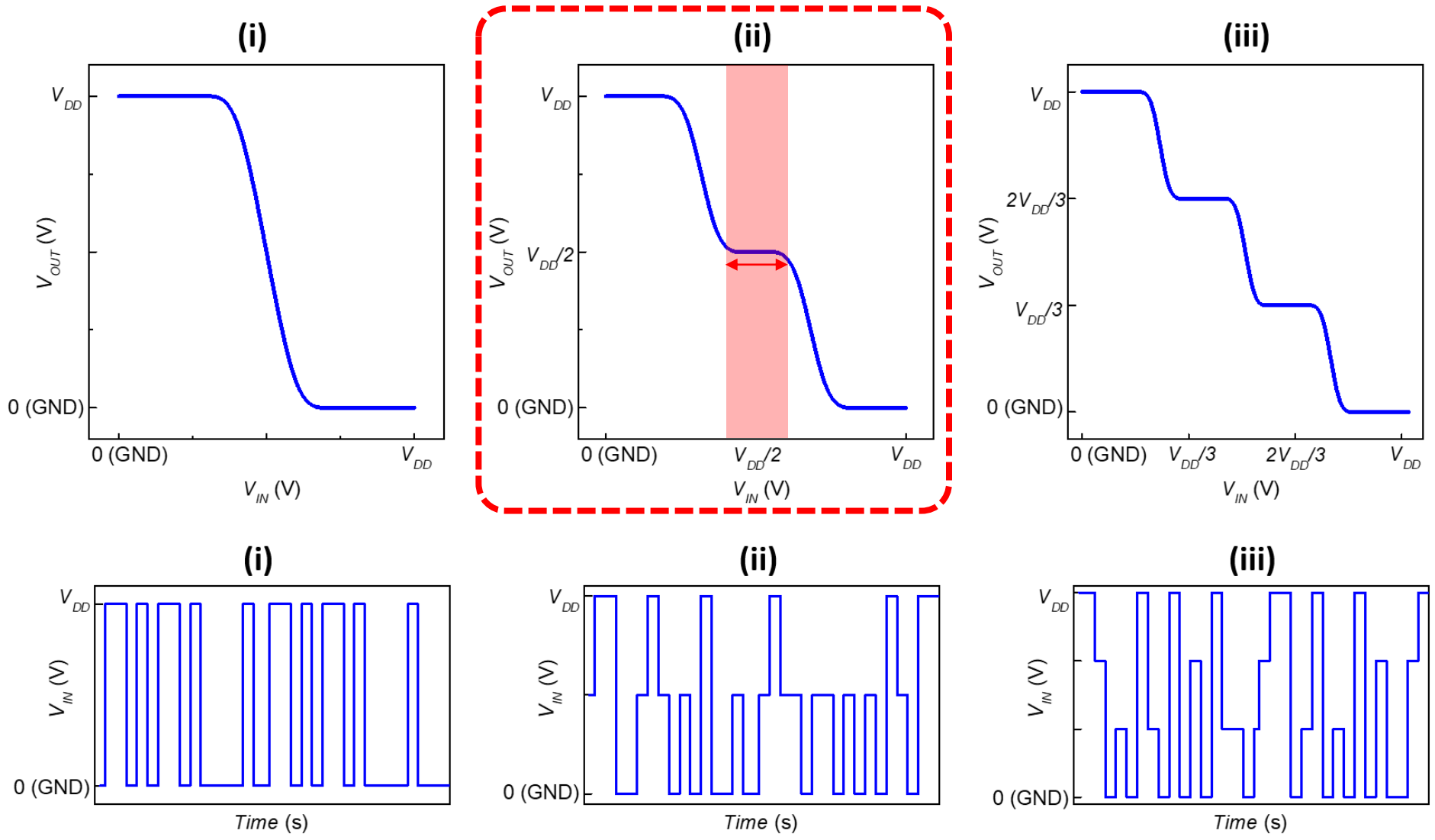
Hocheon Yoo *et al.*, ***Advanced Materials*** (2019) 1808265

Multi-valued Logic



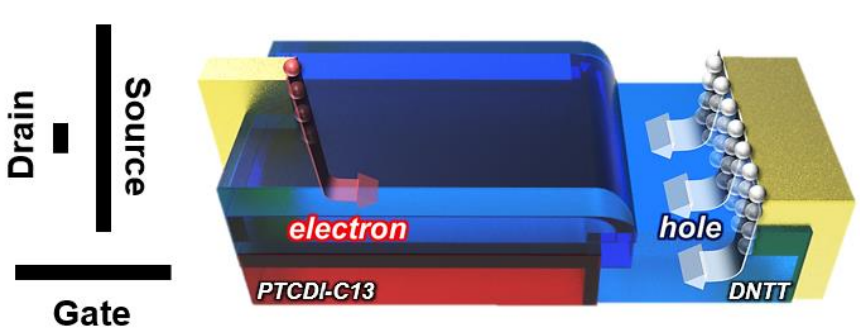
Unpublished results

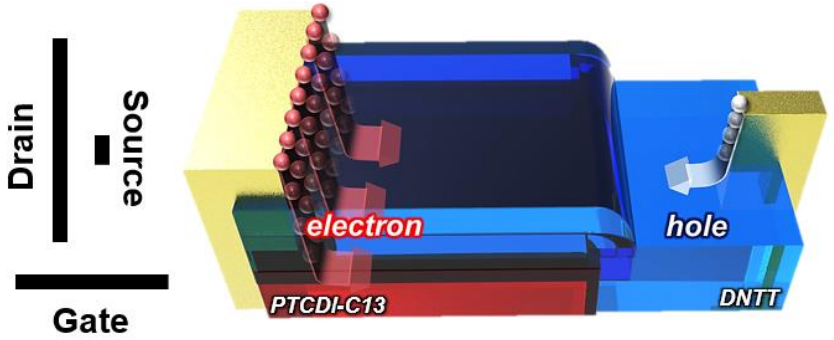
Multi-valued Logic

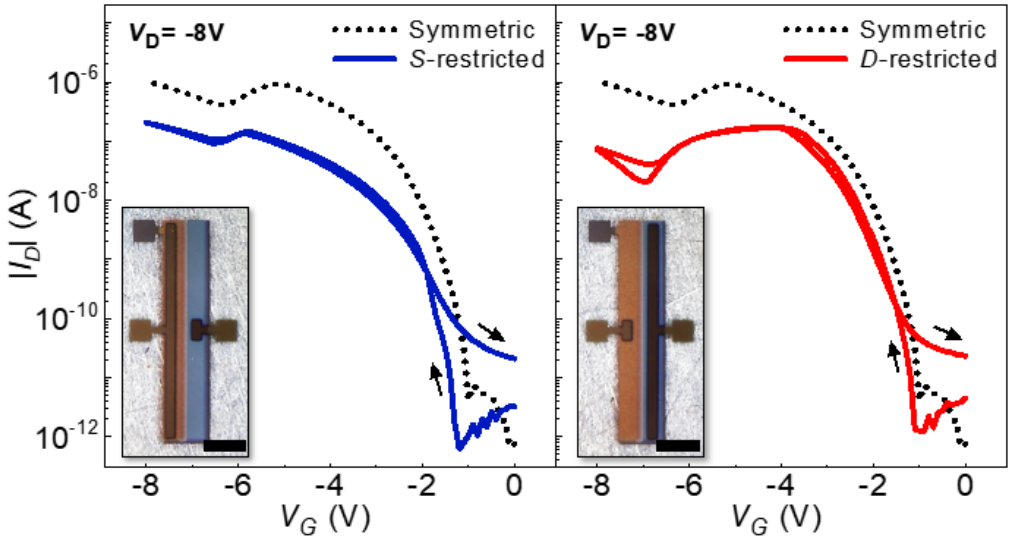


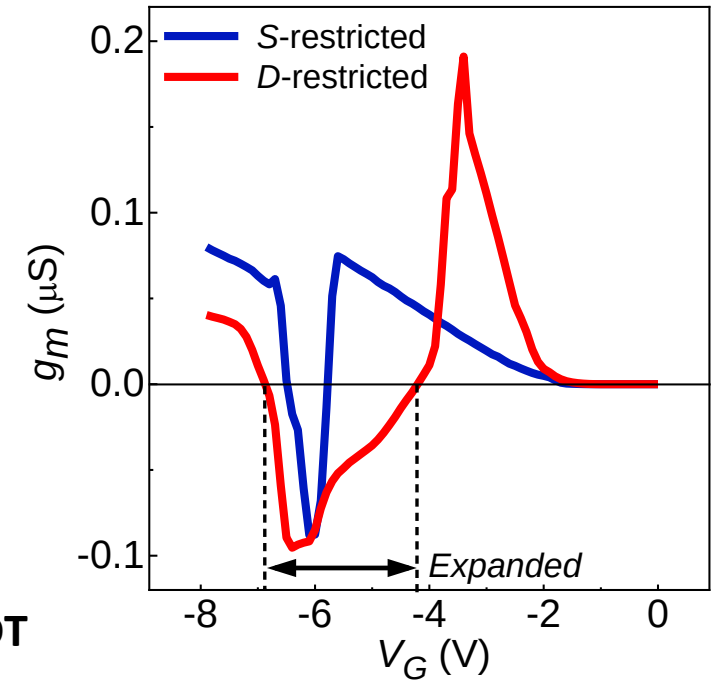
Hocheon Yoo, Chang-Hyun Kim, ***Journal of Materials Chemistry C***, 2021

NDT ternary circuits







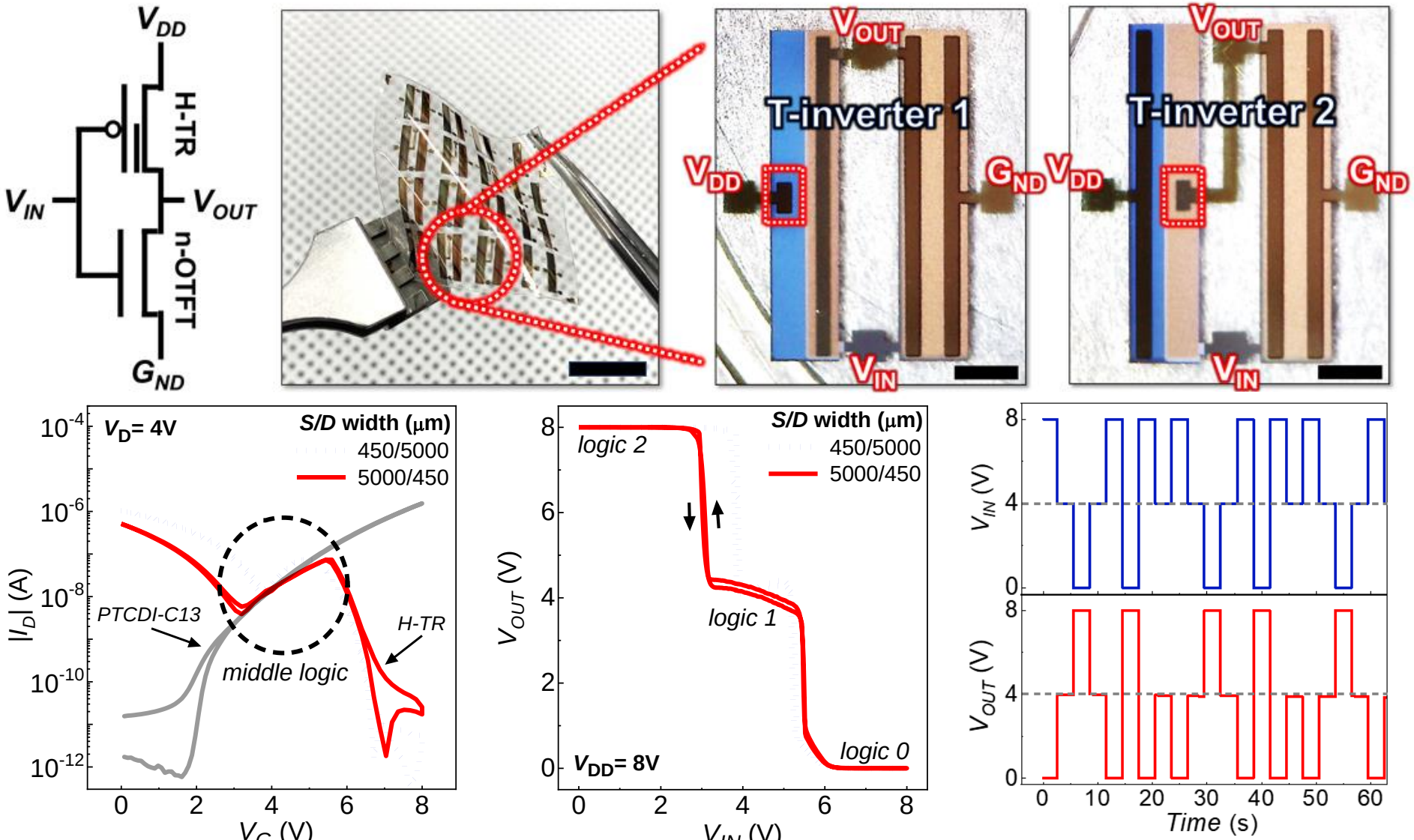


☺ **Asymmetric metal width scheme → Control of NDT**

☺ **Larger NDT ←→ Shorter NDT depending on the metal width ratio**

Chungryul Lee, Hocheon Yoo *et al.*, ***Small*** (2021)

NDT ternary circuits

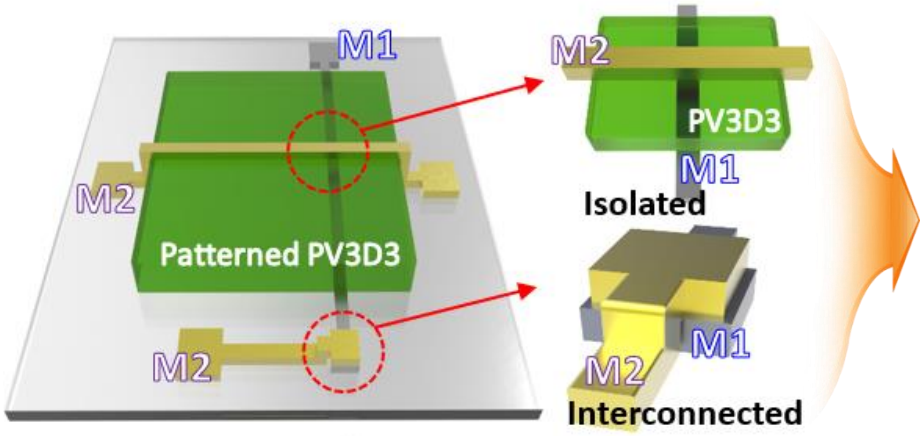


Flexible ternary circuits using asymmetric metal width transistors

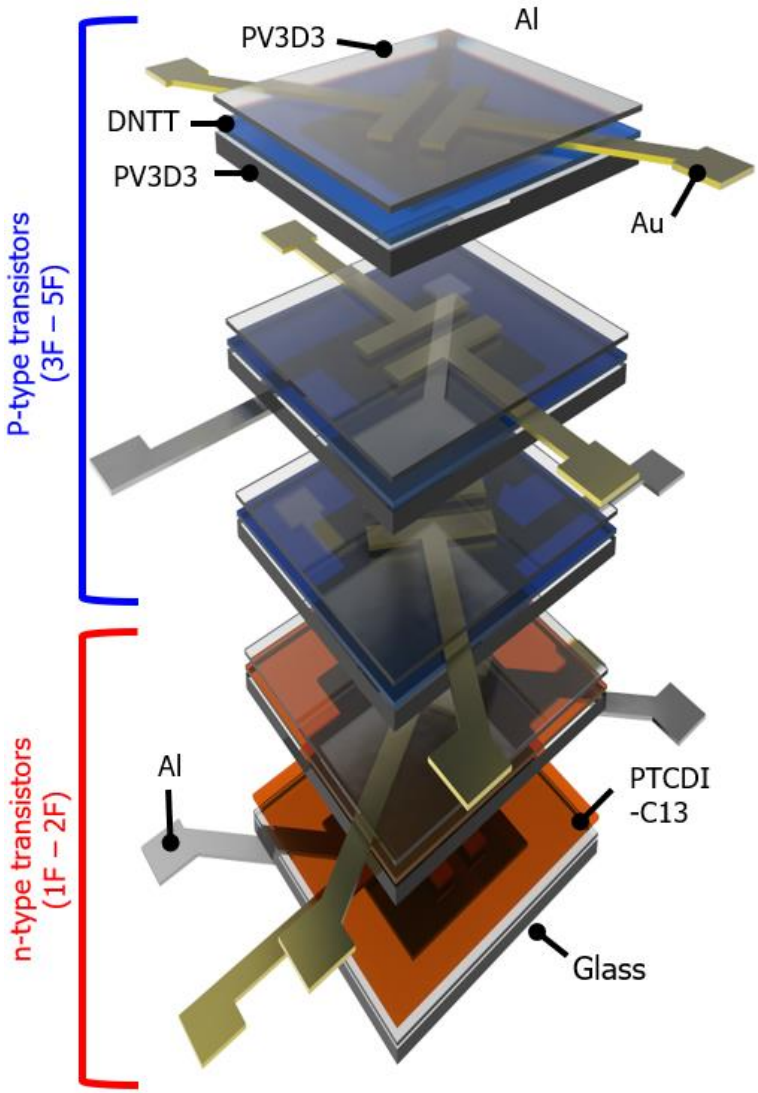
<u>**Chungryul Lee, Hocheon Yoo**</u> *et al.*, ***Small*** (2021)

Via-Hole-Less Metal Interconnects

Via-hole-less integration scheme



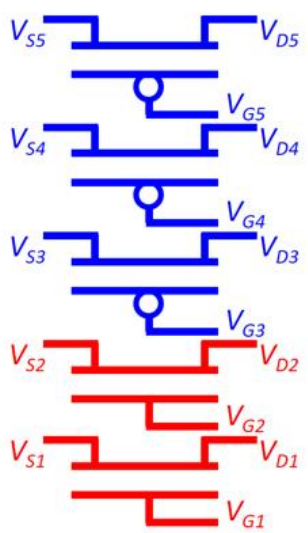
- Etching-free multilevel metal interconnect
- Solvent-free multilevel metal interconnect
- Simultaneous interconnection formation

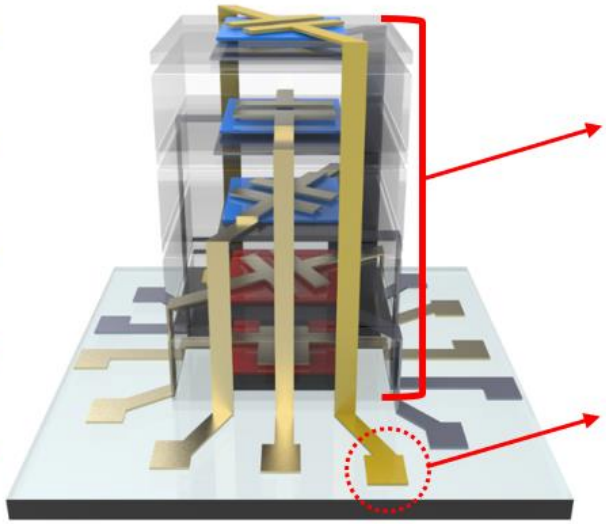


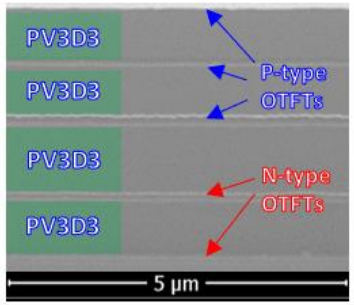
Hocheon Yoo, Hongkeun Park *et al.*, ***IEEE Electron Device Letters*** In progress

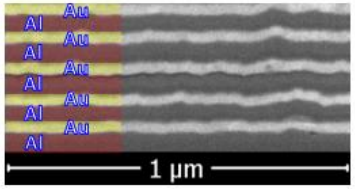
Hocheon Yoo, Hongkeun Park *et al.*, ***Nature Communications*** (2019) 10, 2424.

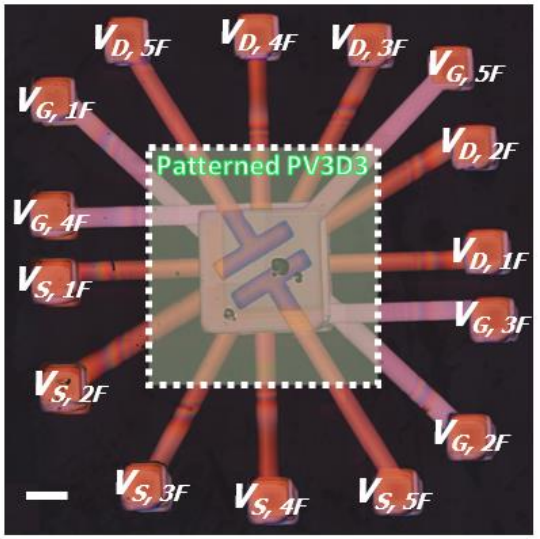
Via-Hole-Less Metal Interconnects

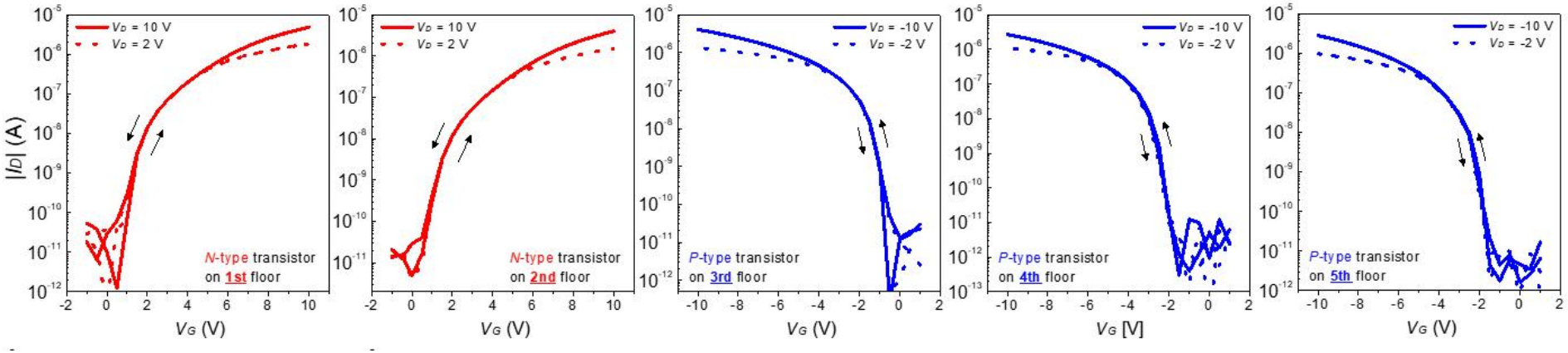












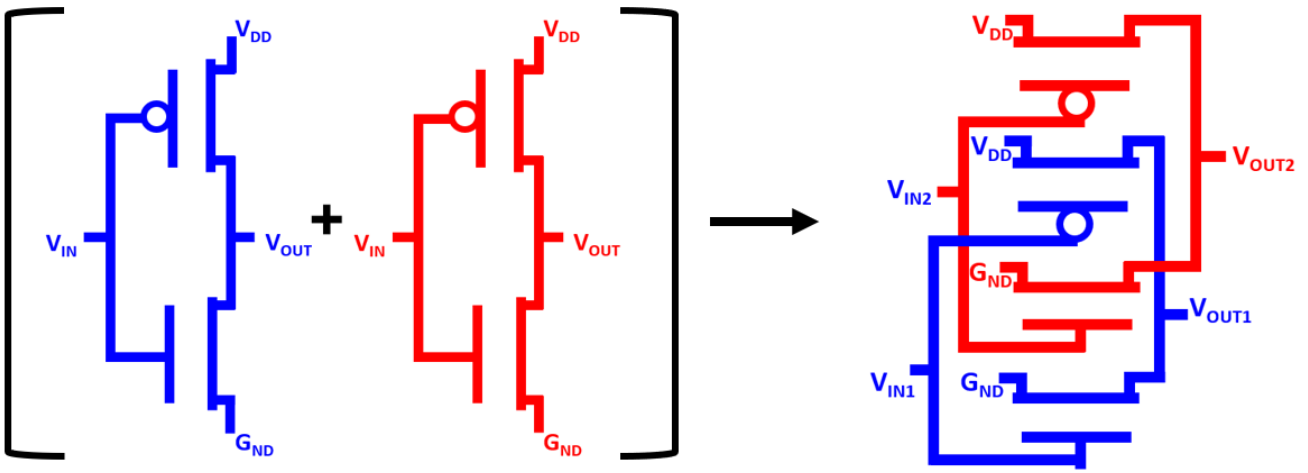
100% Yield

5-time higher density of devices

Highlighted in ***Nature Research Device & Materials Engineering Community***

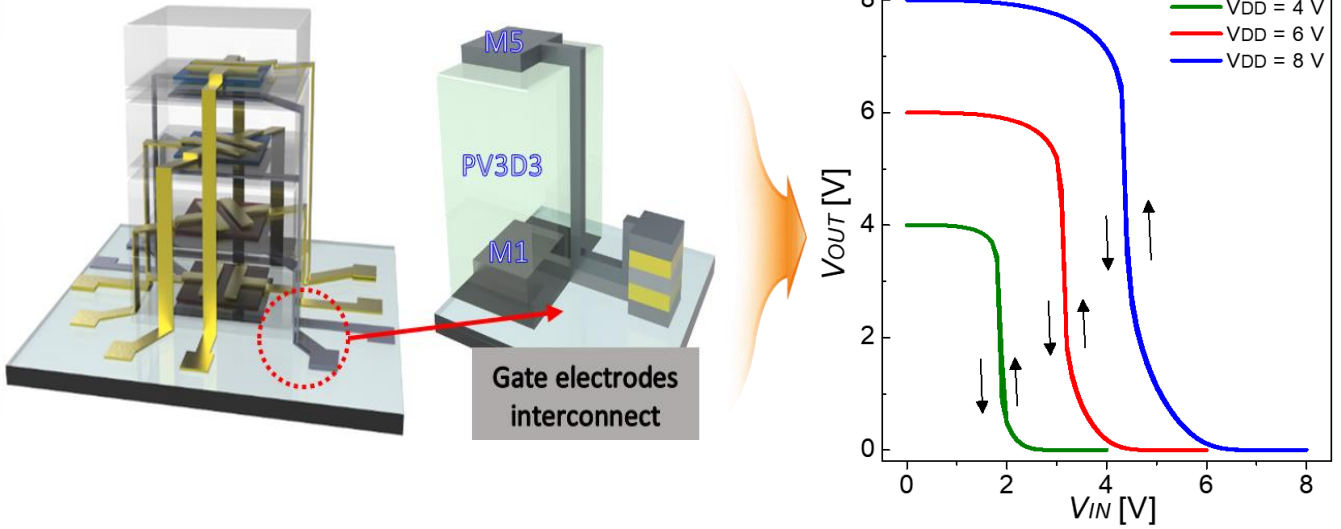
Via-Hole-Less Metal Interconnects

3D-Integarated Inverter Circuit



3D-Integarated NAND/NOR Circuit

Exclusive OR Circuit



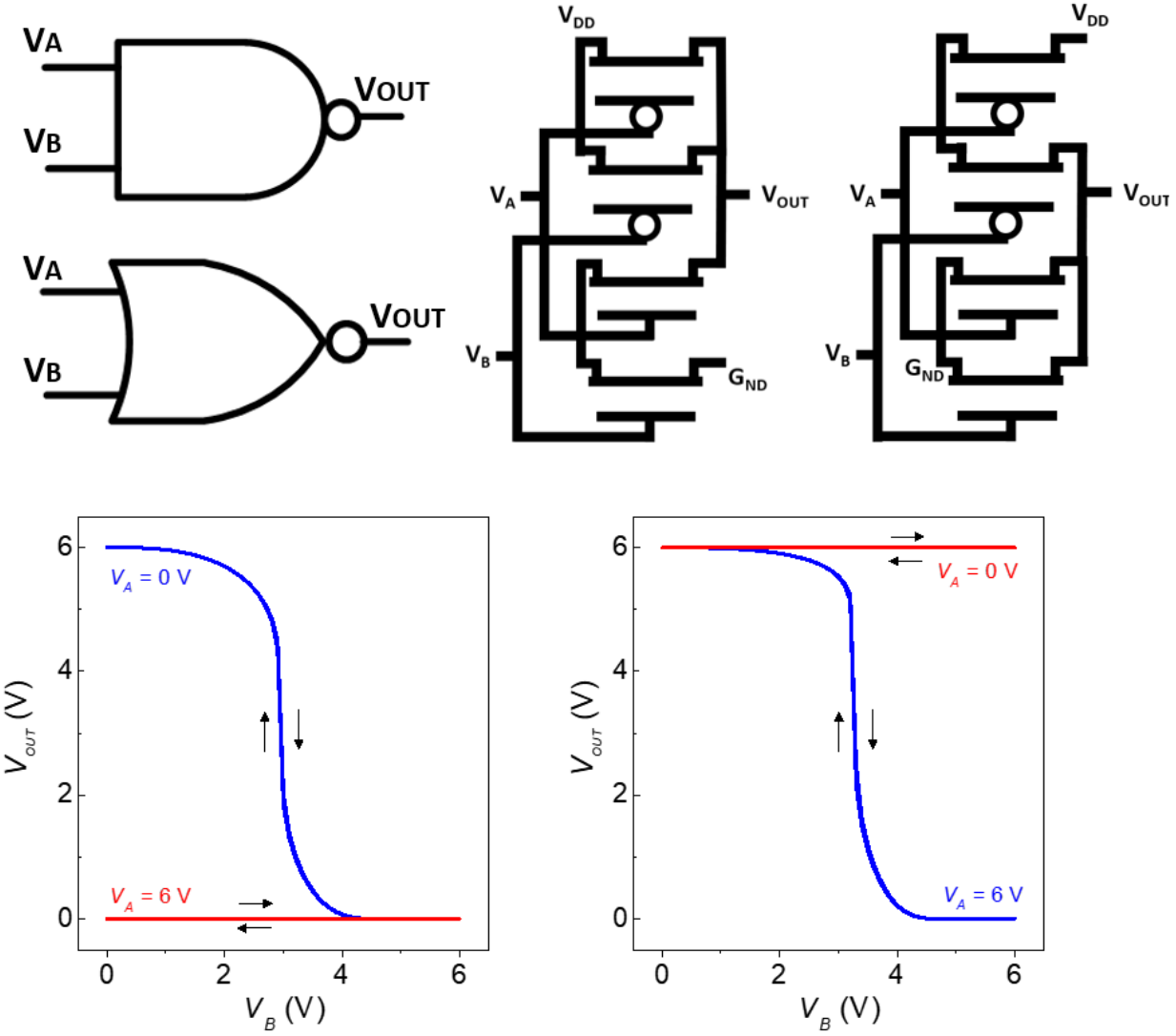
Hocheon Yoo, Hongkeun Park *et al.*, ***Nature Communications*** (2019) 10, 2424
Highlighted in ***Nature Research Device & Materials Engineering Community***

Via-Hole-Less Metal Interconnects

3D-Integarated Inverter Circuit

3D-Integarated NAND/NOR Circuit

Exclusive OR Circuit



Hocheon Yoo, Hongkeun Park *et al.*, ***IEEE Electron Device Letters***

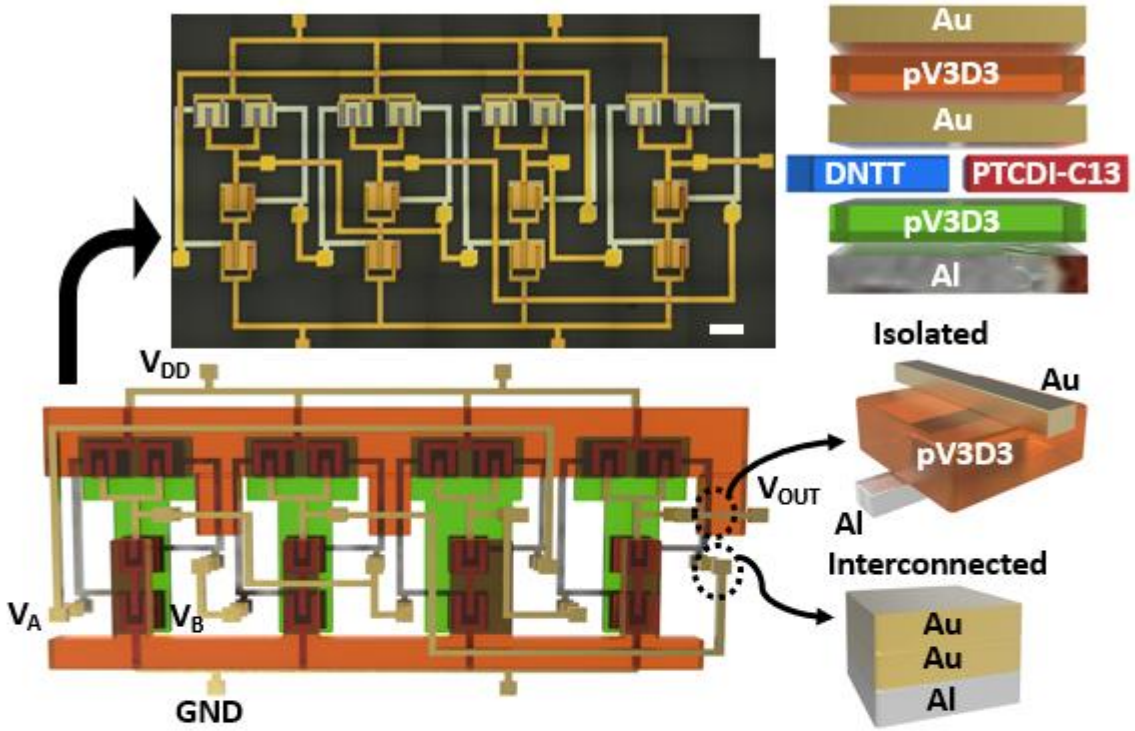
Hocheon Yoo, Hongkeun Park *et al.*, ***Nature Communications*** (2019) 10, 2424.

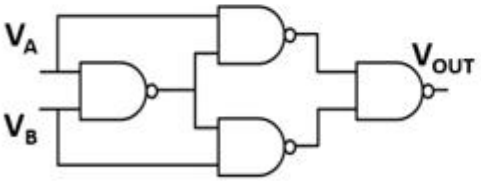
Via-Hole-Less Metal Interconnects

3D-Integarated Inverter Circuit

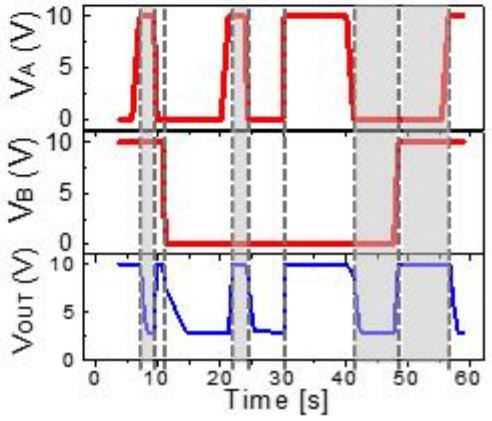
3D-Integarated NAND/NOR Circuit

Exclusive OR Circuit





V_A	1	1	0	0
V_B	1	0	0	1
V_{OUT}	0	1	0	1



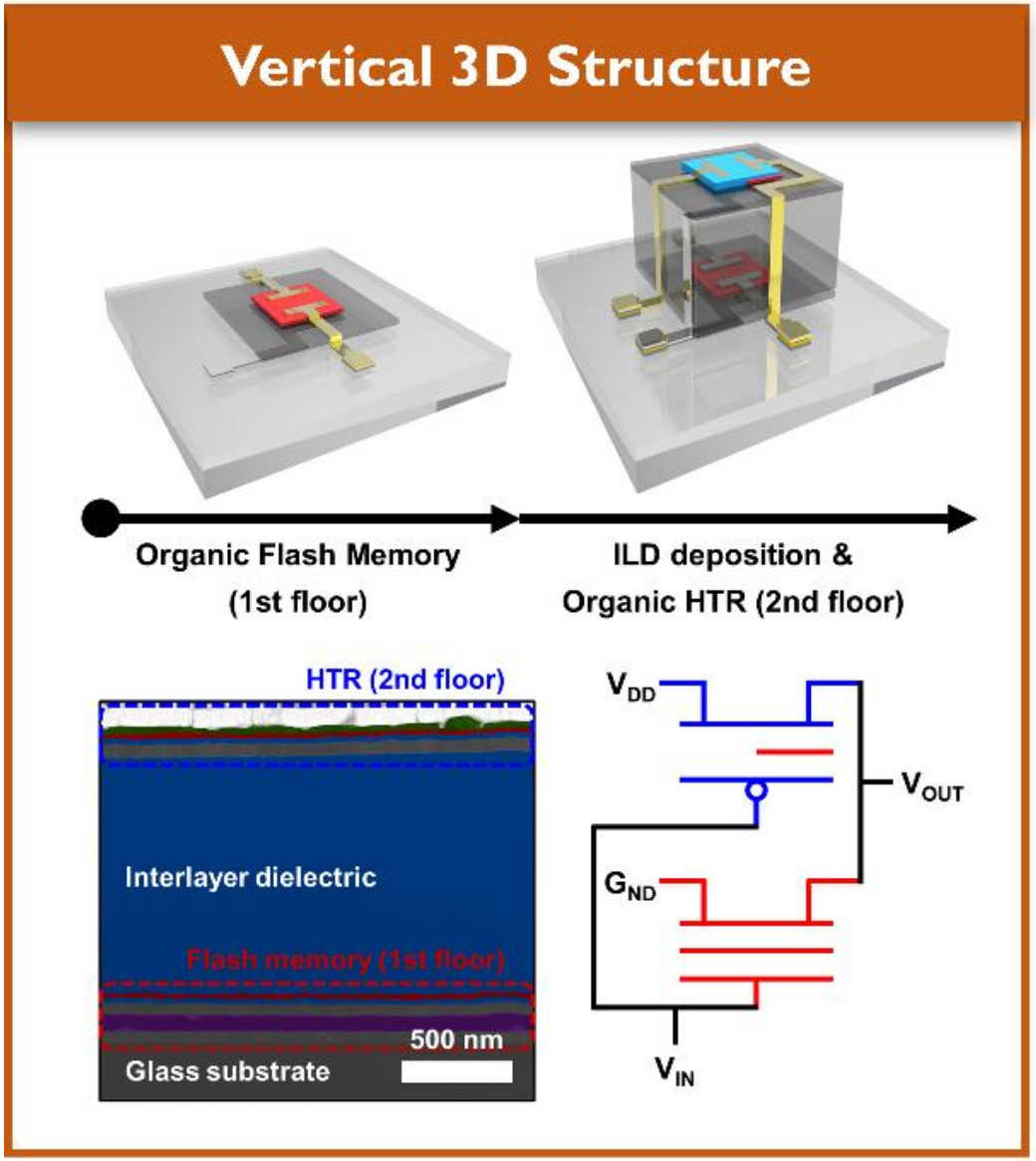
Hocheon Yoo, Hongkeun Park *et al.*, ***IEEE Electron Device Letters***

NDT ternary circuits

Vertically-Integrated MVL

Controllable MVL operation

MVL depending on memory states



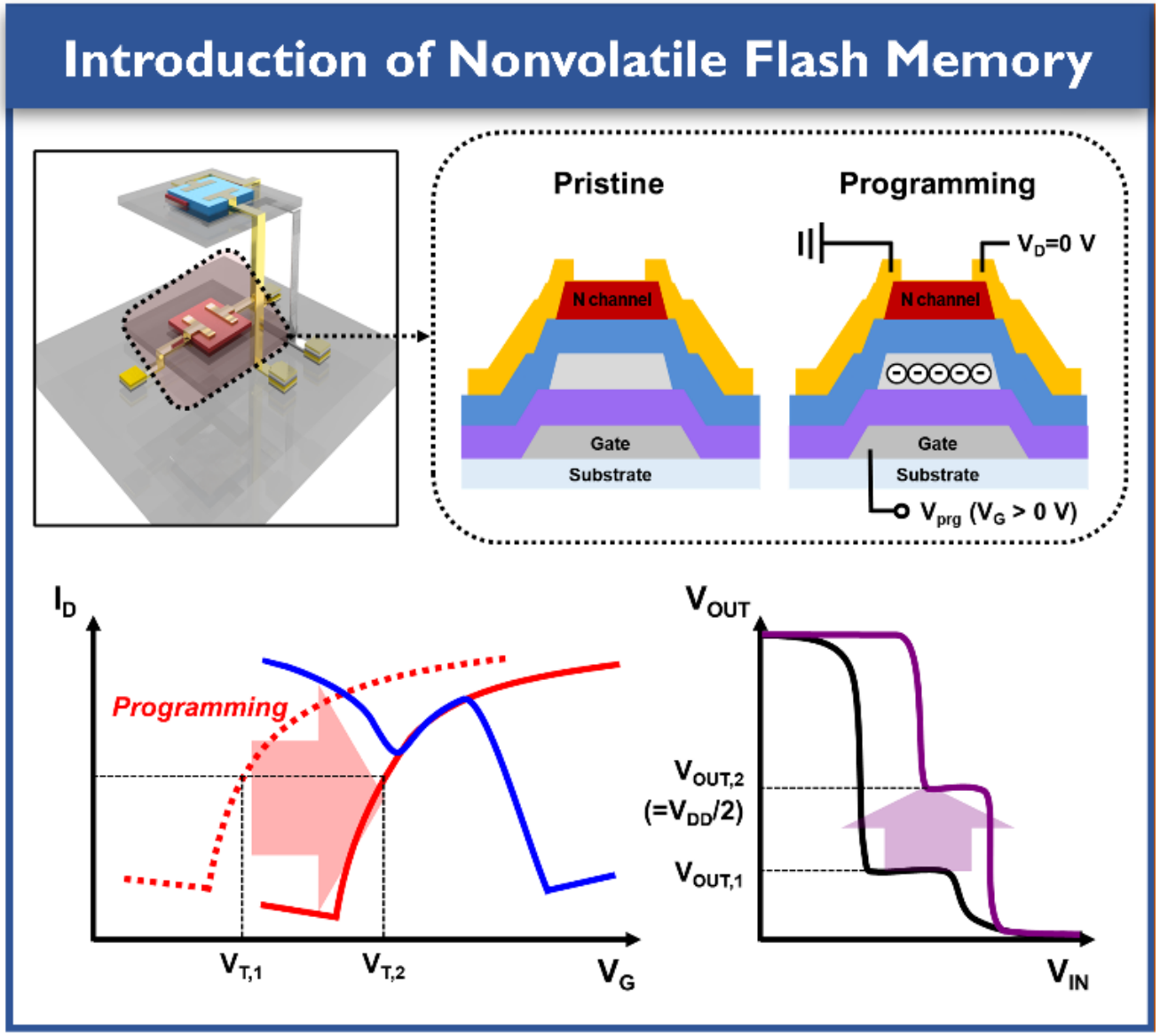
<u>**Junhwan Choi, Hocheon Yoo**</u> *et al.*, ***Nature Communications*** (2022)

NDT ternary circuits

Vertically-Integrated MVL

Controllable MVL operation

MVL depending on memory states



<u>**Junhwan Choi, Hocheon Yoo**</u> *et al.*, ***Nature Communications*** (2022)

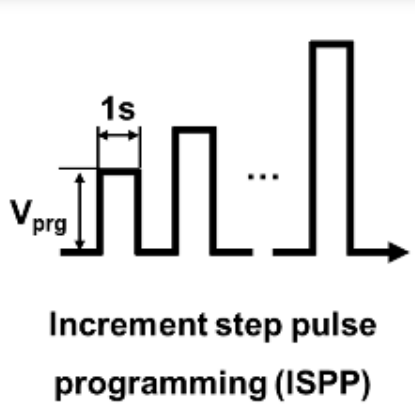
NDT ternary circuits

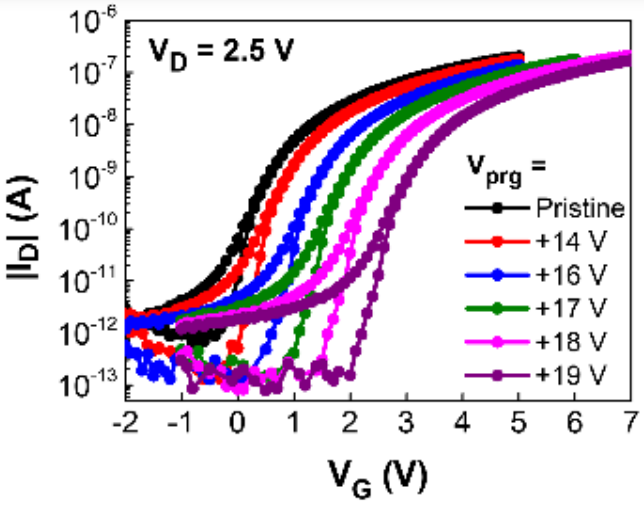
Vertically-Integrated MVL

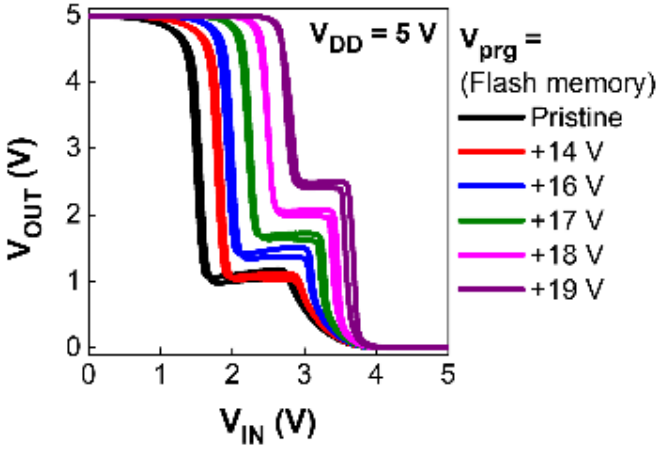
Controllable MVL operation

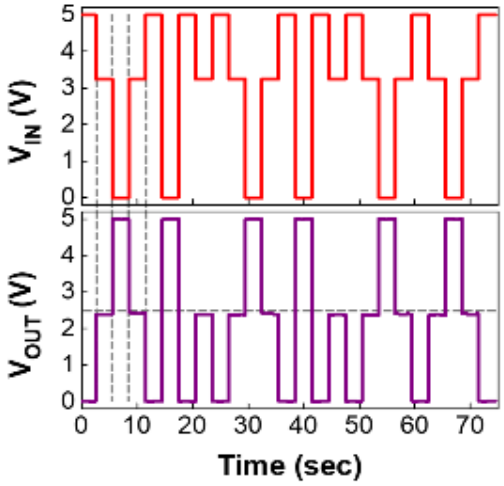
MVL depending on memory states

Controllable Intermediate Logic State



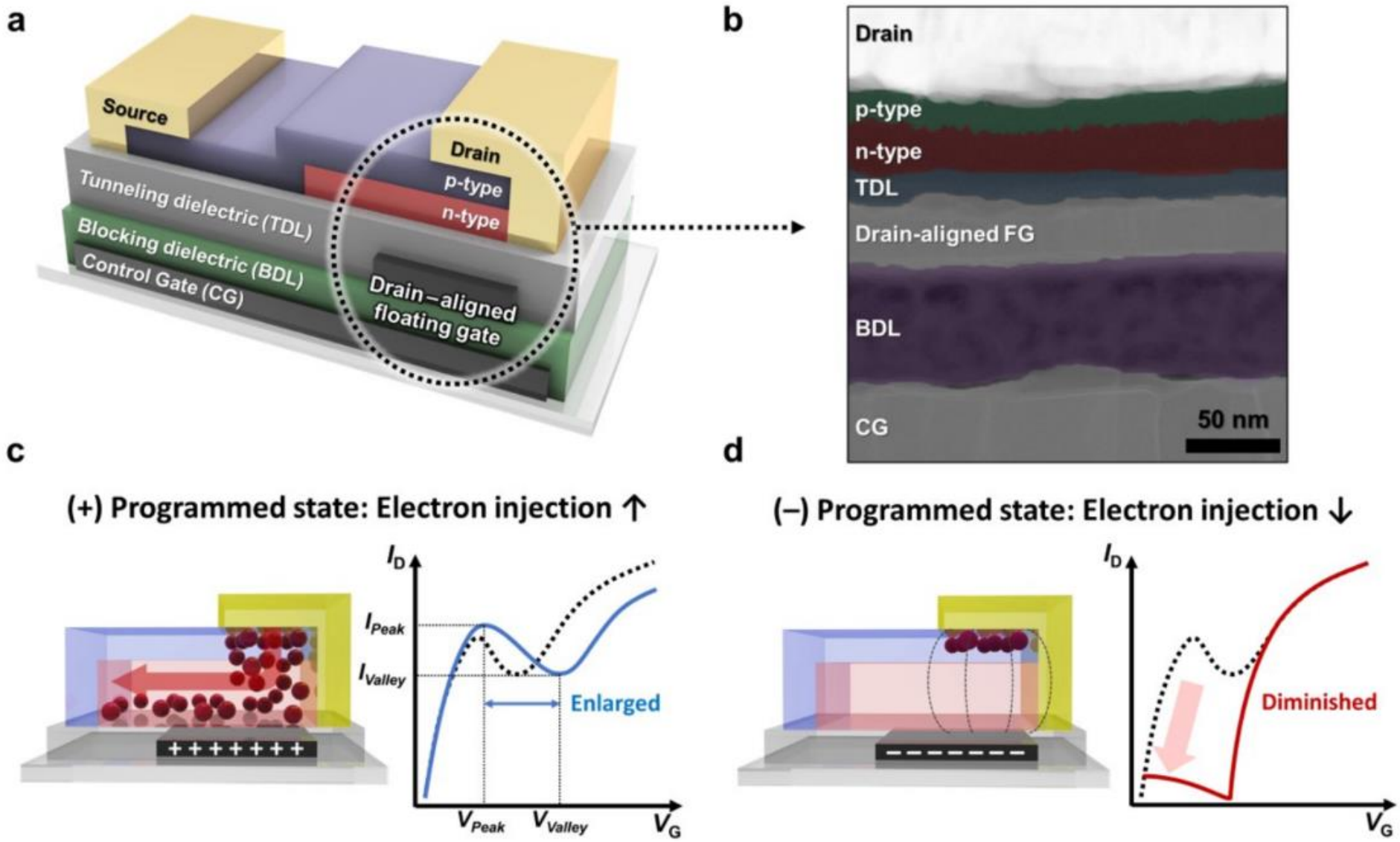






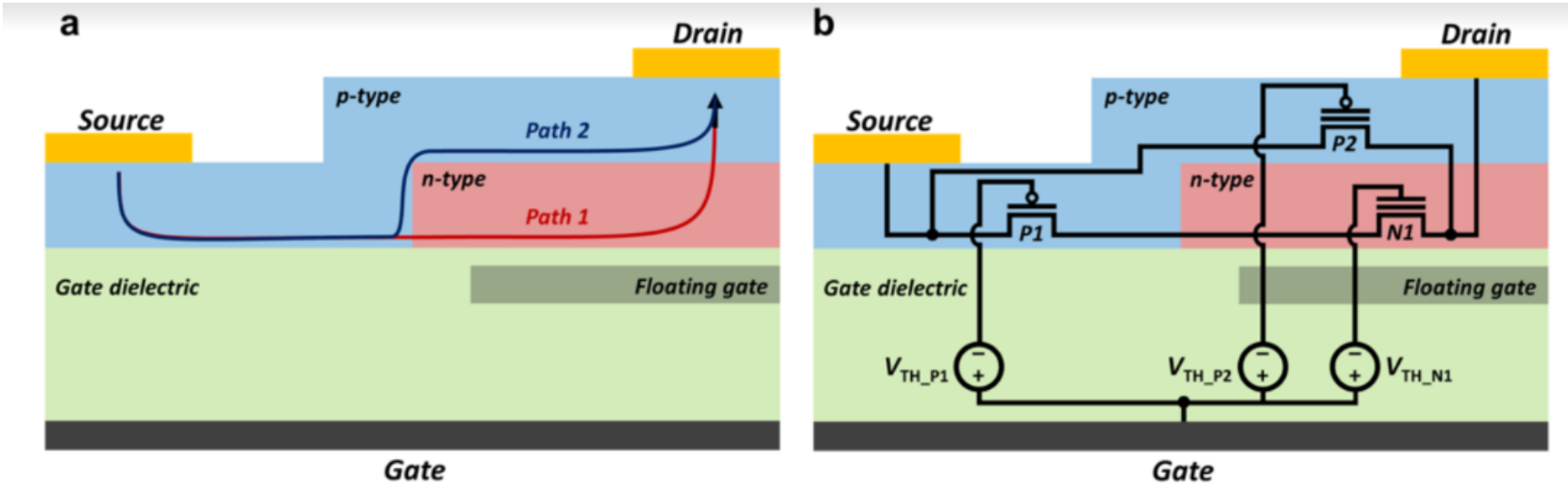
<u>**Junhwan Choi, Hocheon Yoo**</u> *et al.*, ***Nature Communications*** (2022)

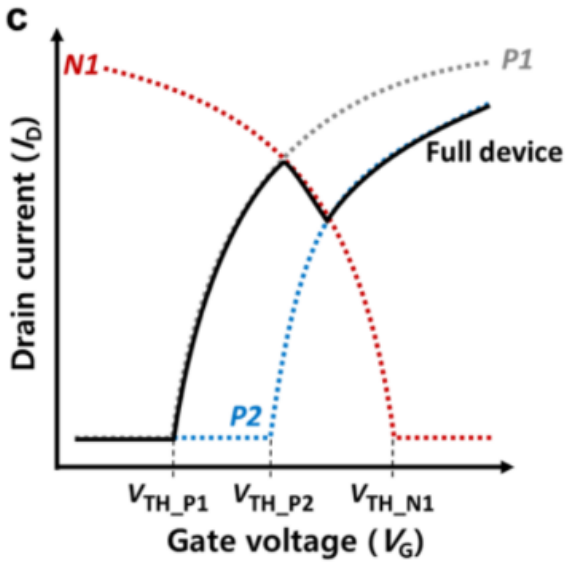
NDT ternary circuits



Nature Communications 14.1 (2023): 3757.

NDT ternary circuits





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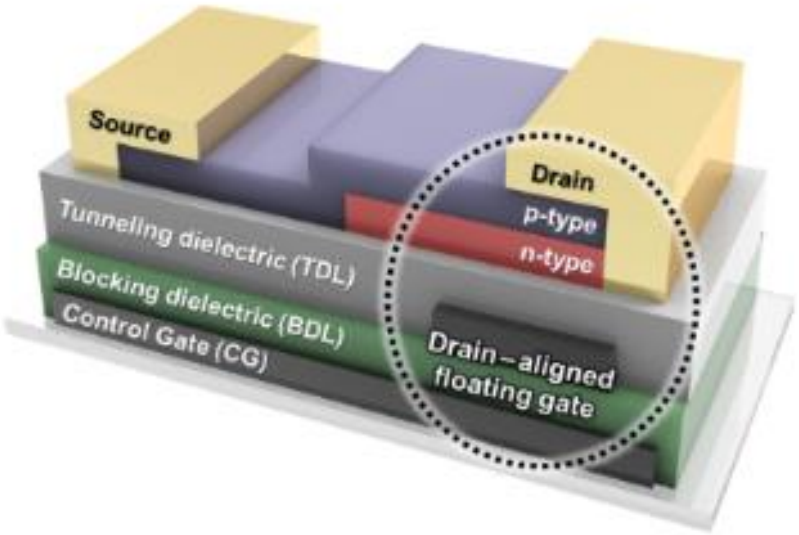
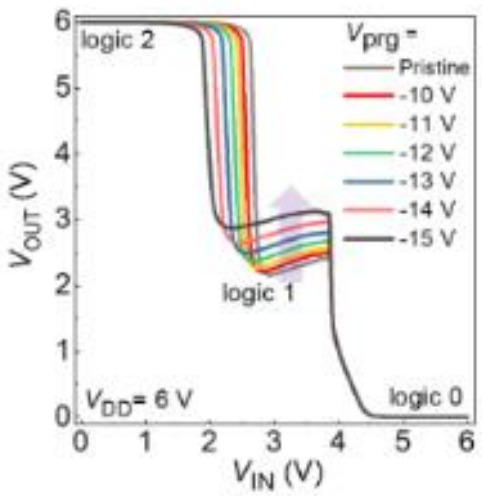
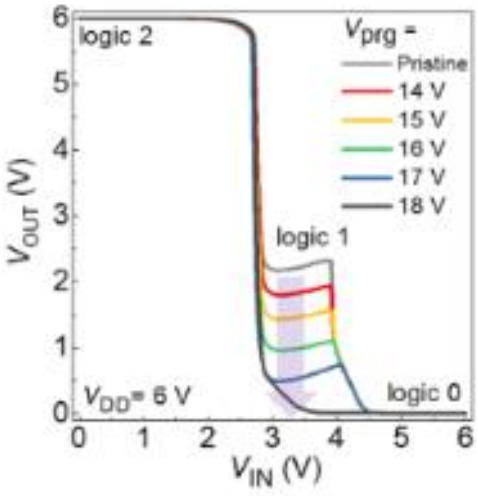
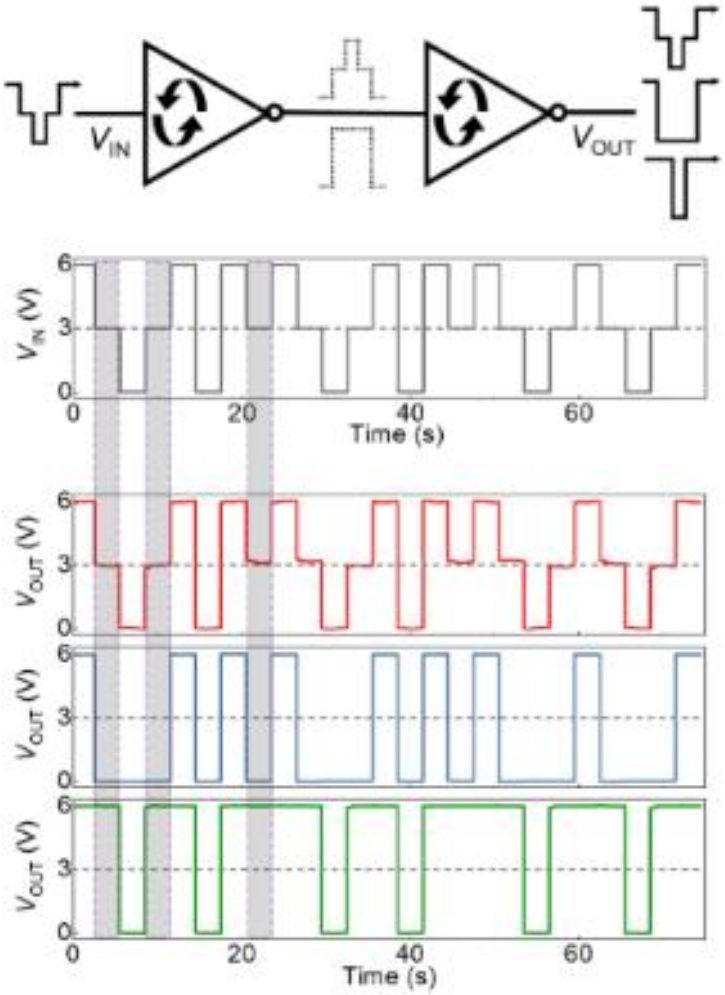
NDT ternary circuits



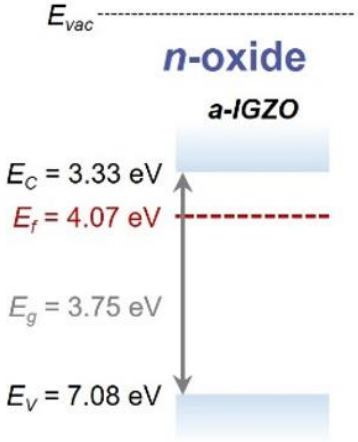


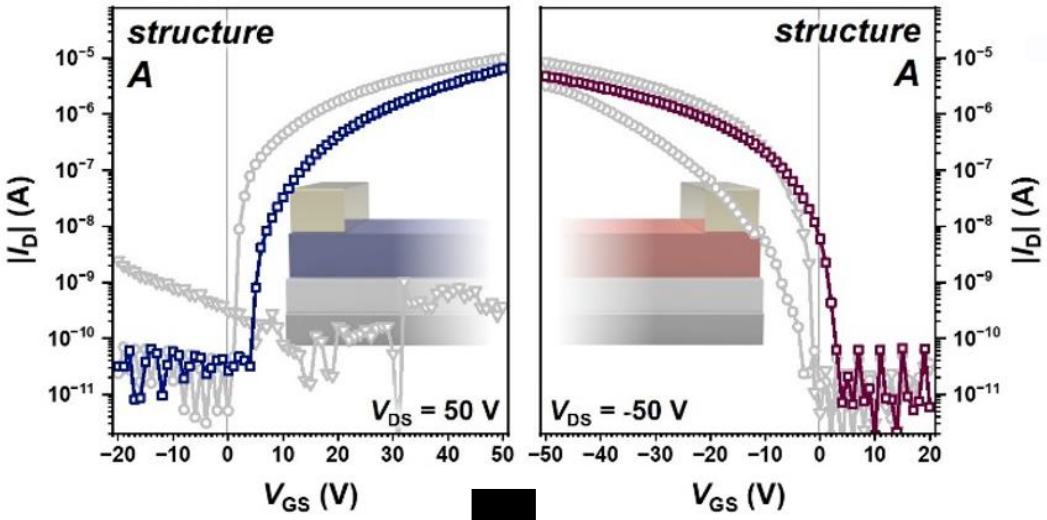


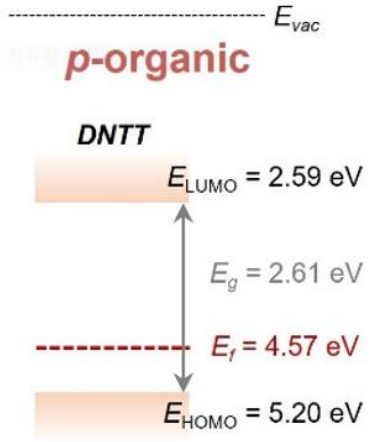


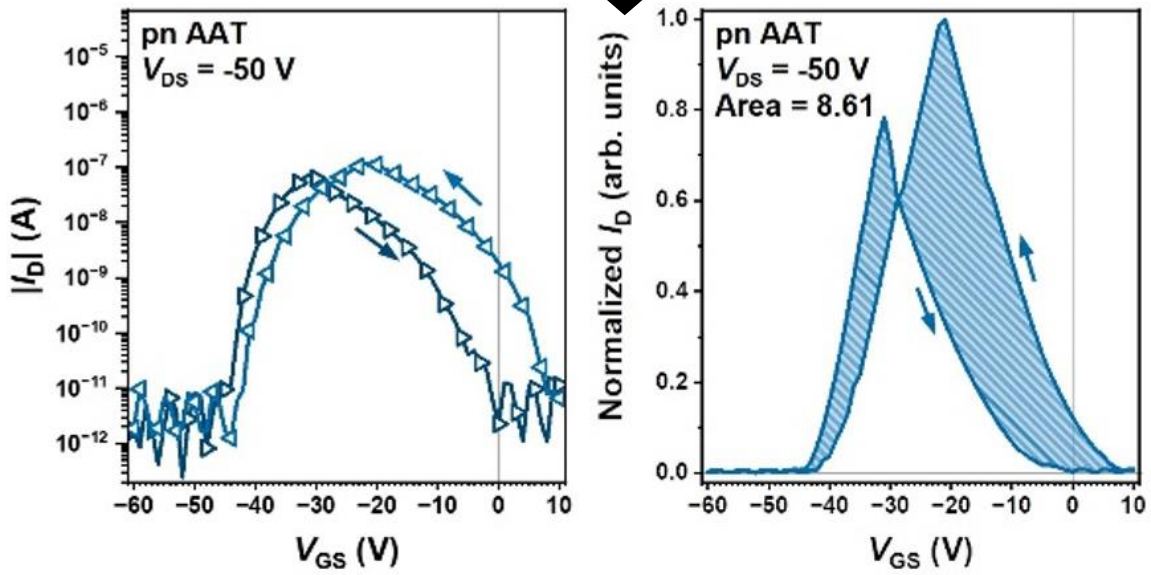
Nature Communications 14.1 (2023): 3757.

Anti-ambipolar transistors









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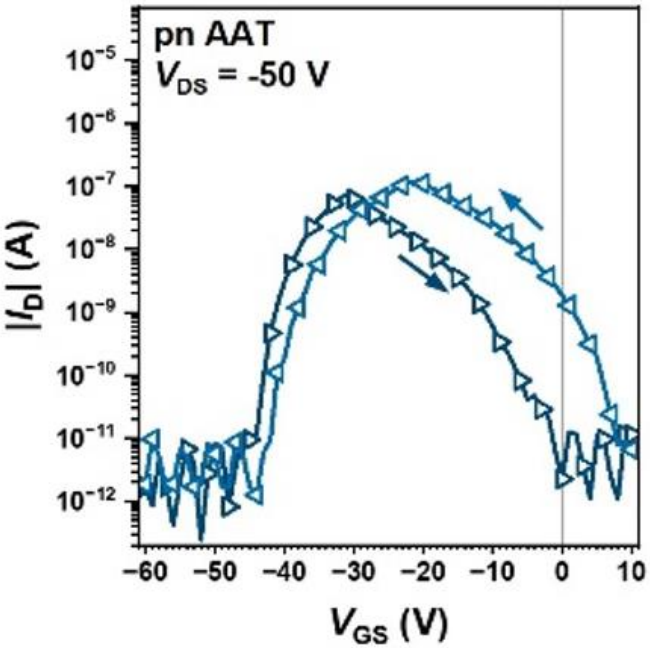
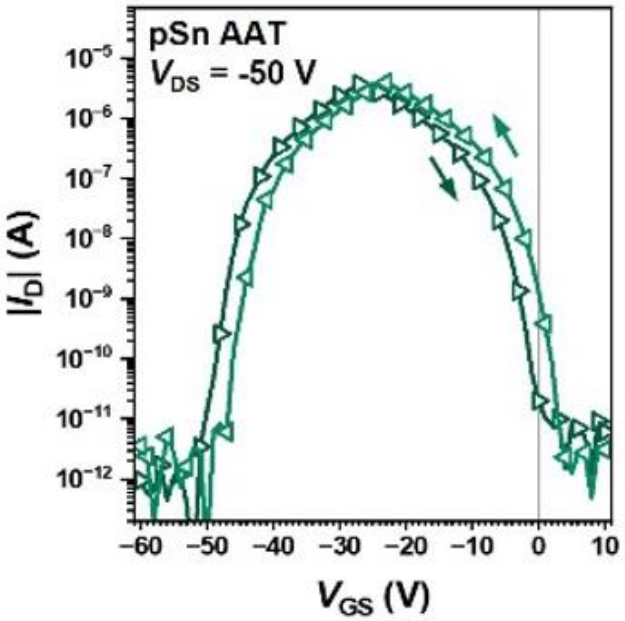
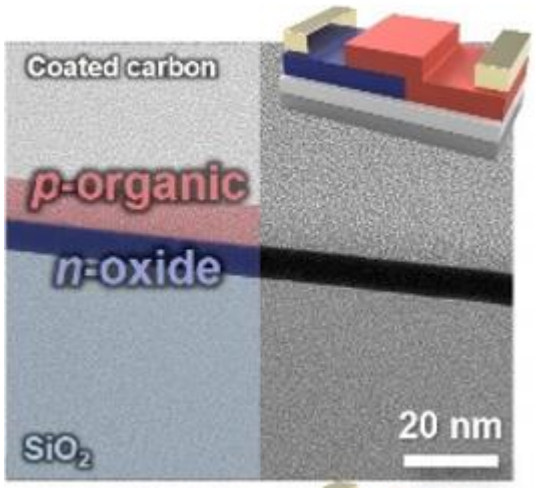
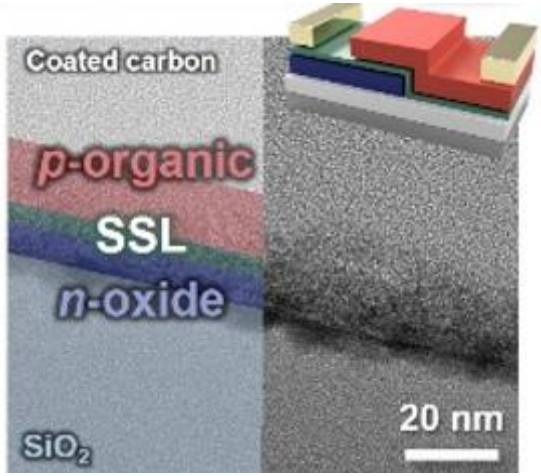
Anti-ambipolar transistors









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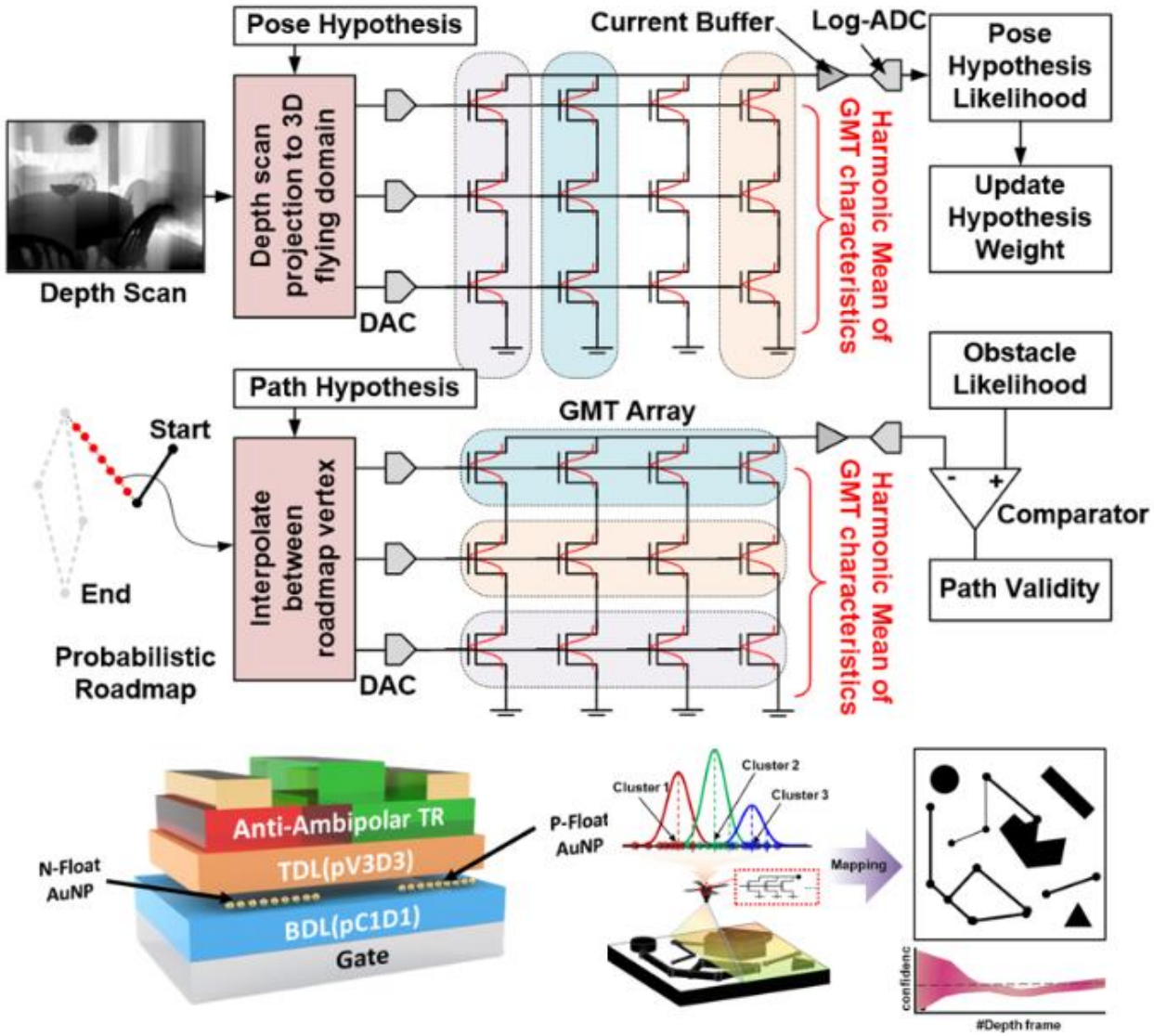
Probabilistic Reasoning with Gaussian Transistors



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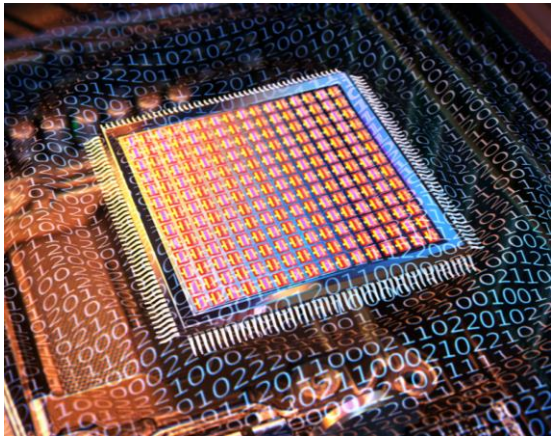
Multi-valued logic



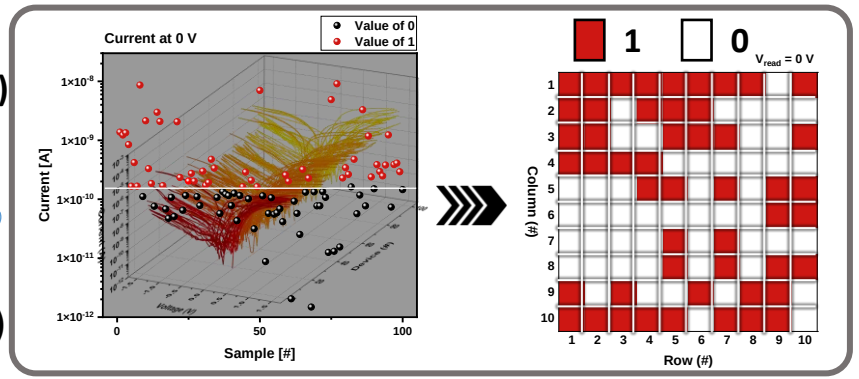
Security Devices

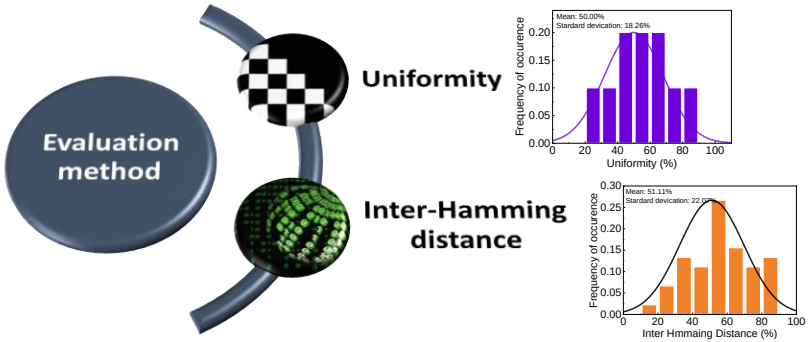
Physically Unclonable Functions

Physically Unclonable Functions

"The only function that cannot be replicated."

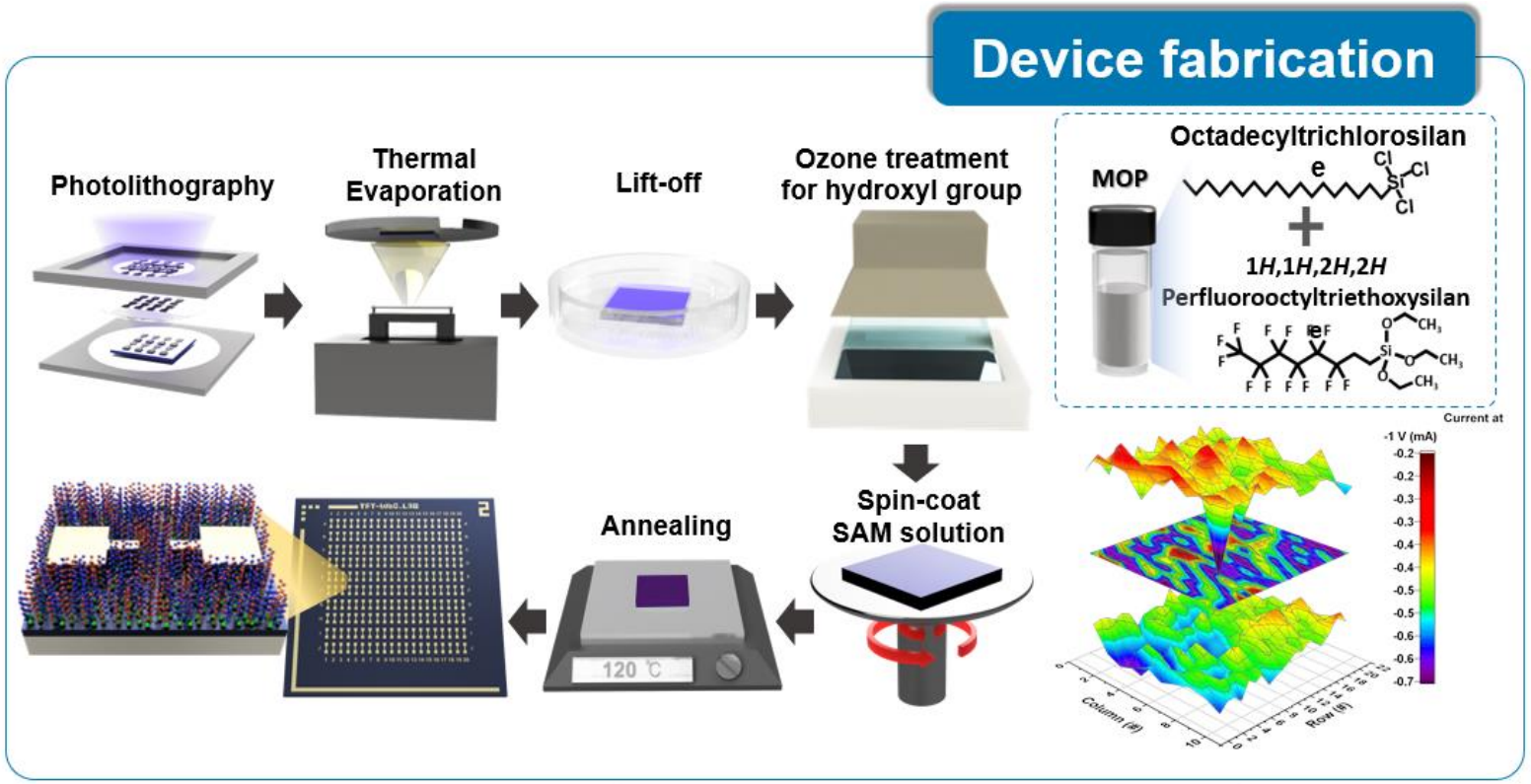
"Digital uniquely identifying fingerprints"

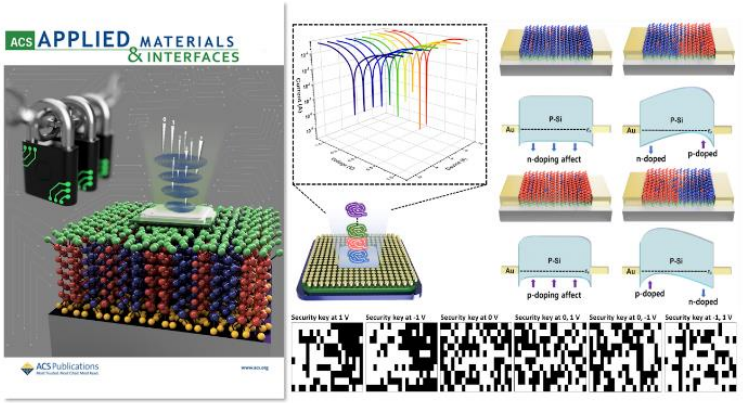


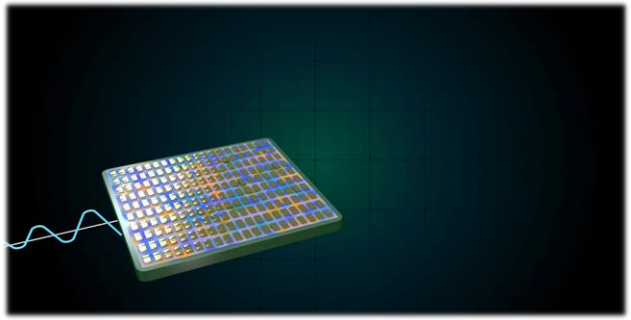


Indicator	Property	Ideal value
Uniformity	Each ratio of 0 and 1 in a dichotomously divided state	50 %
Inter-Hamming distance (HD)	Evaluation of unequal outputs for equal inputs of each device	50 %

Physically Unclonable Functions



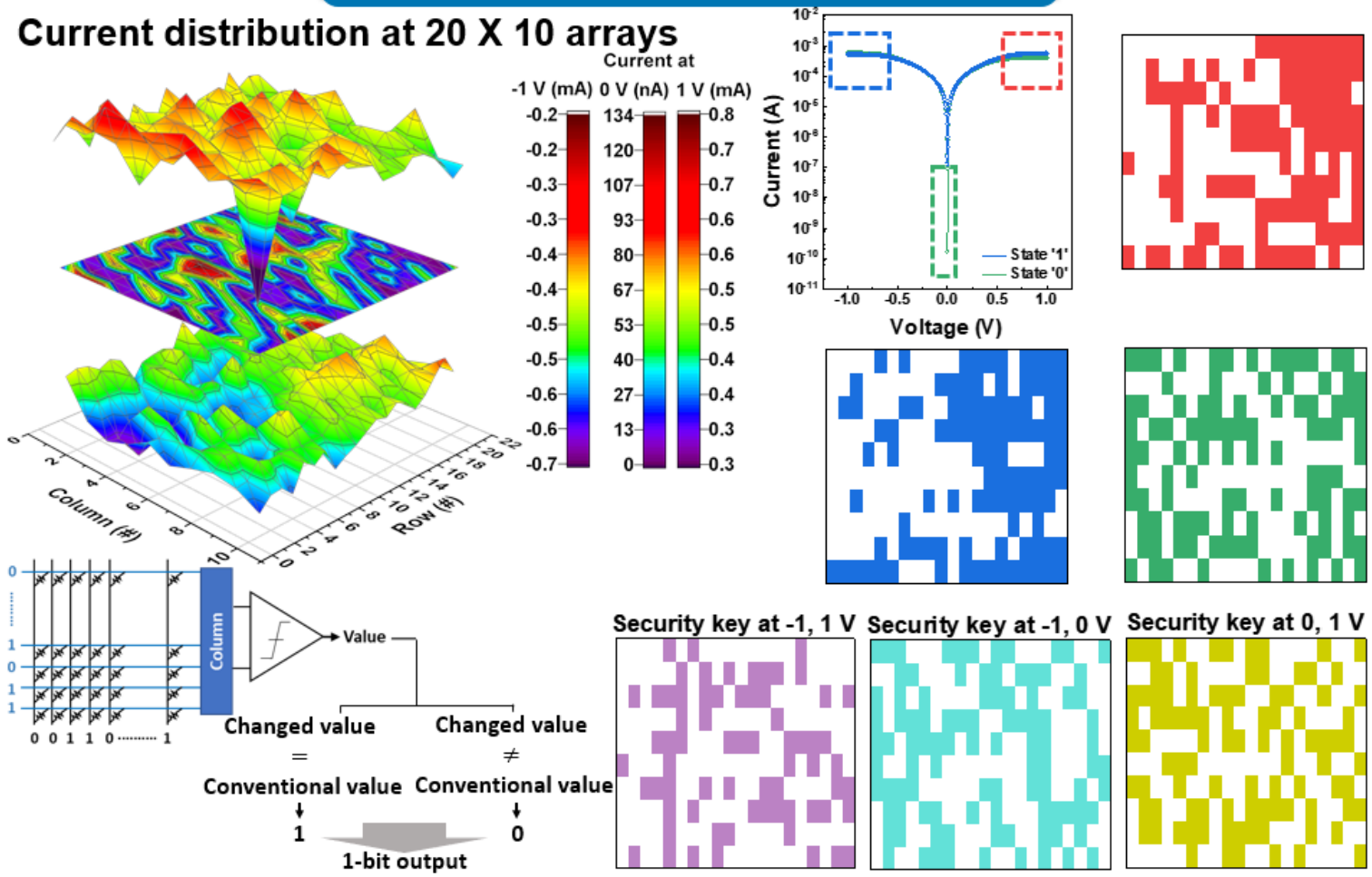




Subin Lee, ACS Applied Materials & Interfaces (2022)

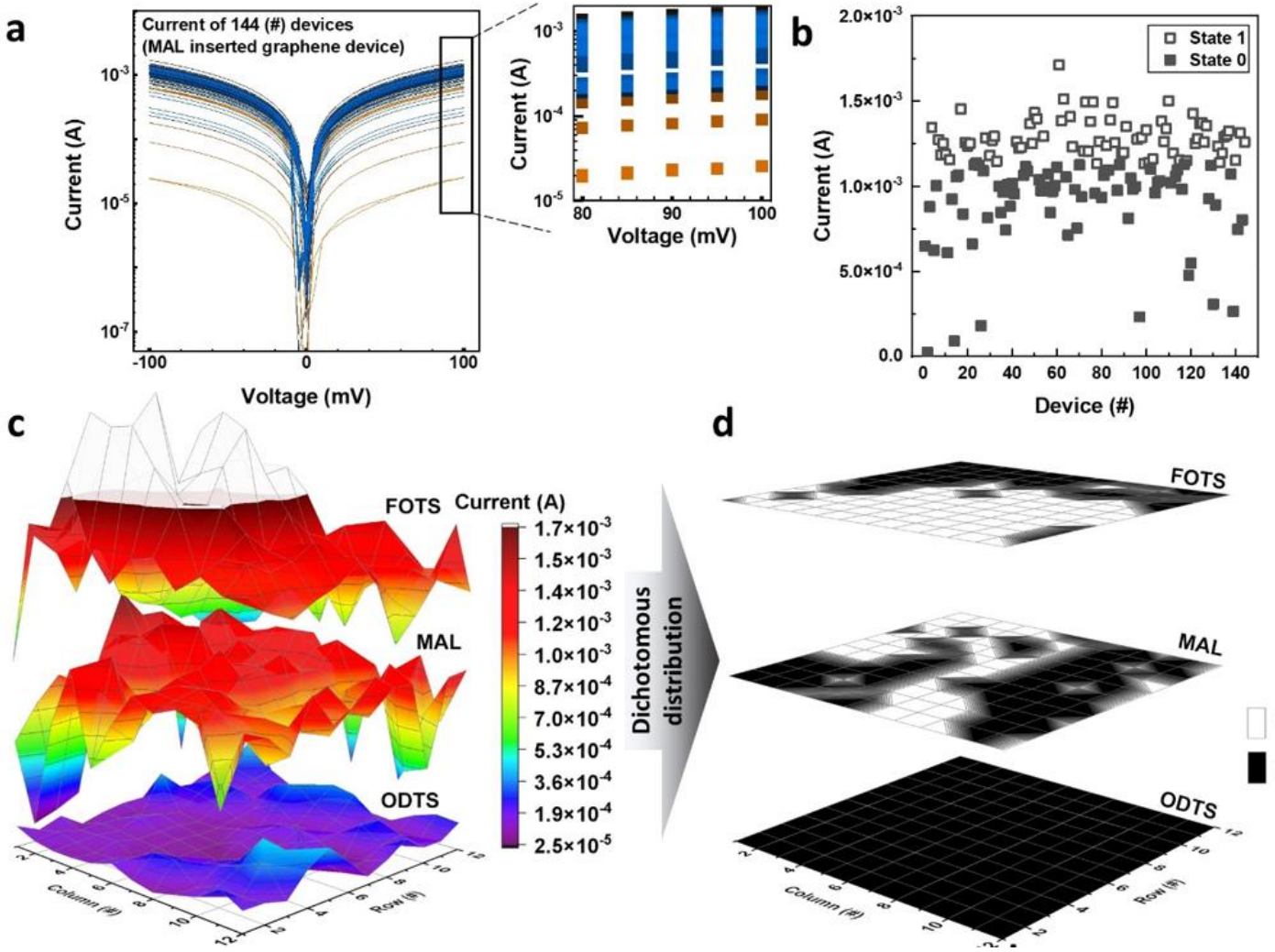
Physically Unclonable Functions

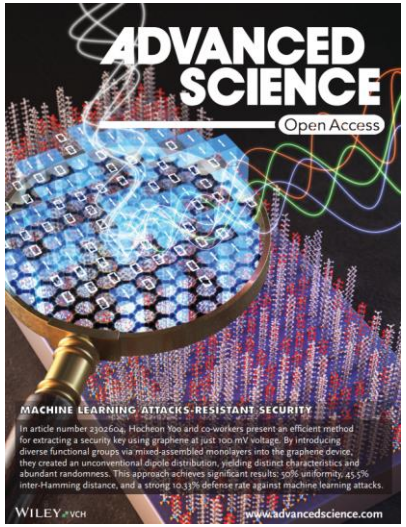
Generate security keys

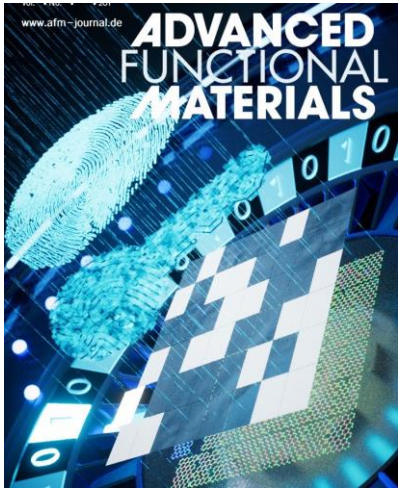


Subin Lee, ACS Applied Materials & Interfaces (2022)

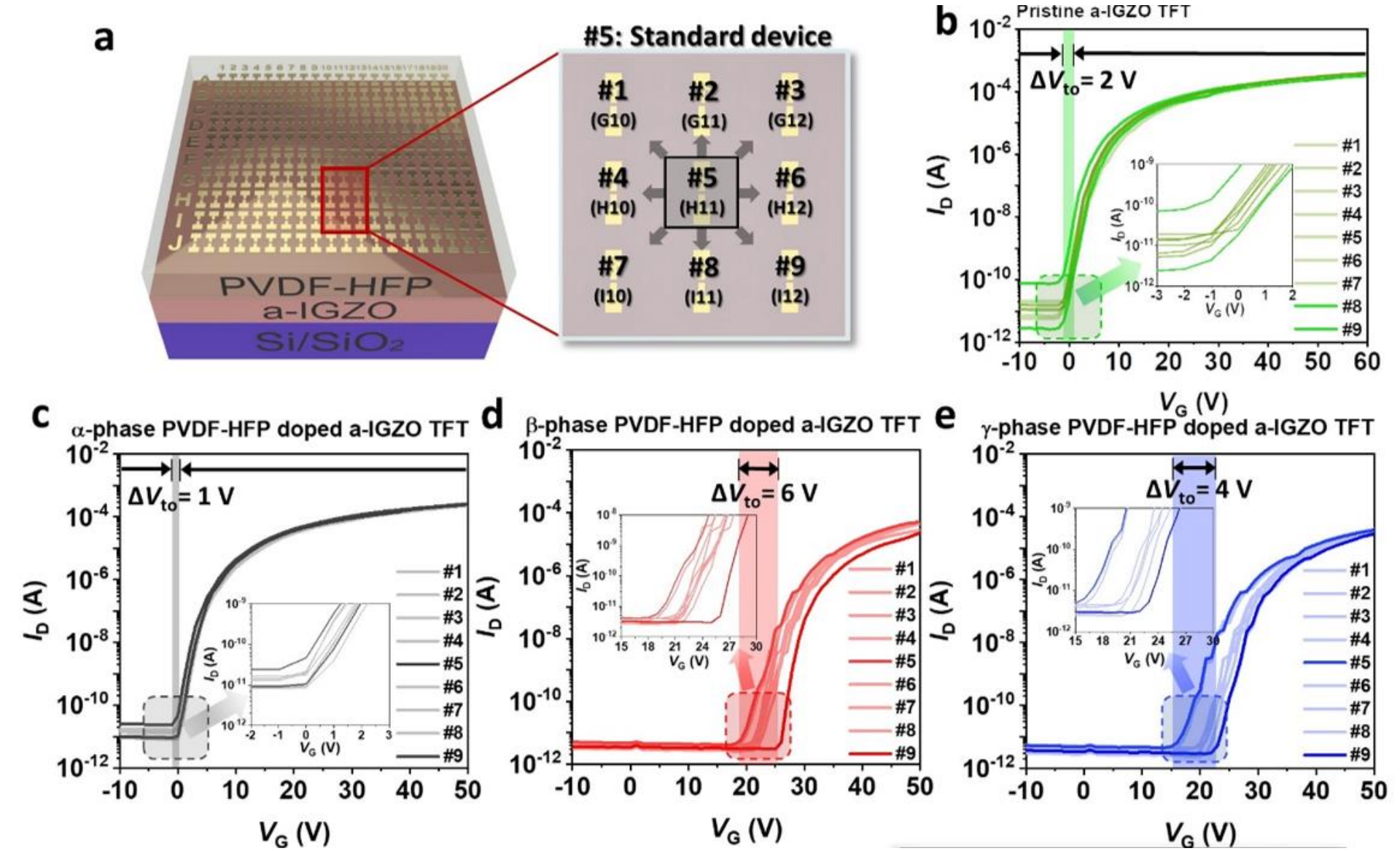
Physically Unclonable Functions







Advanced Science (2023), Advanced Functional Materials (2023)



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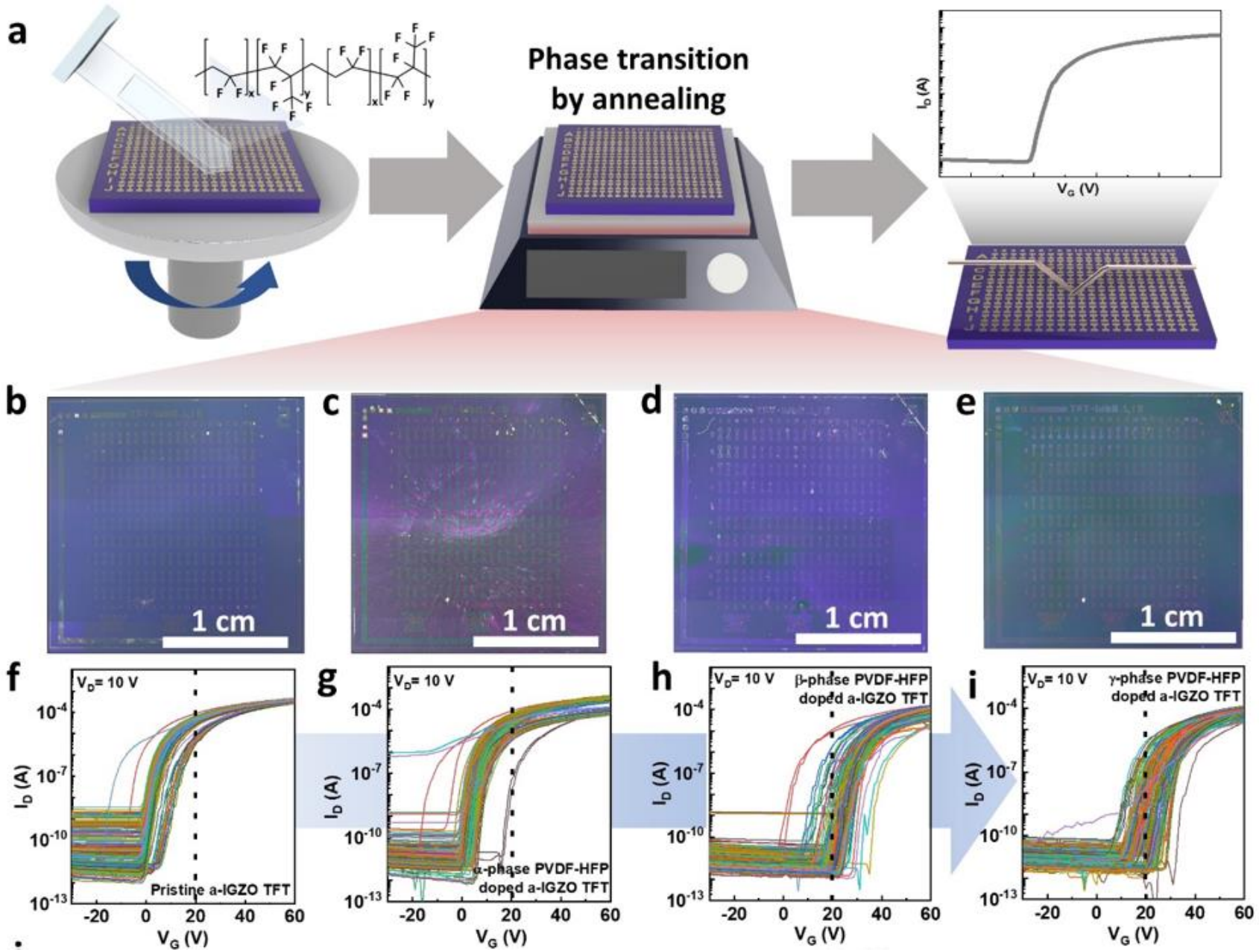

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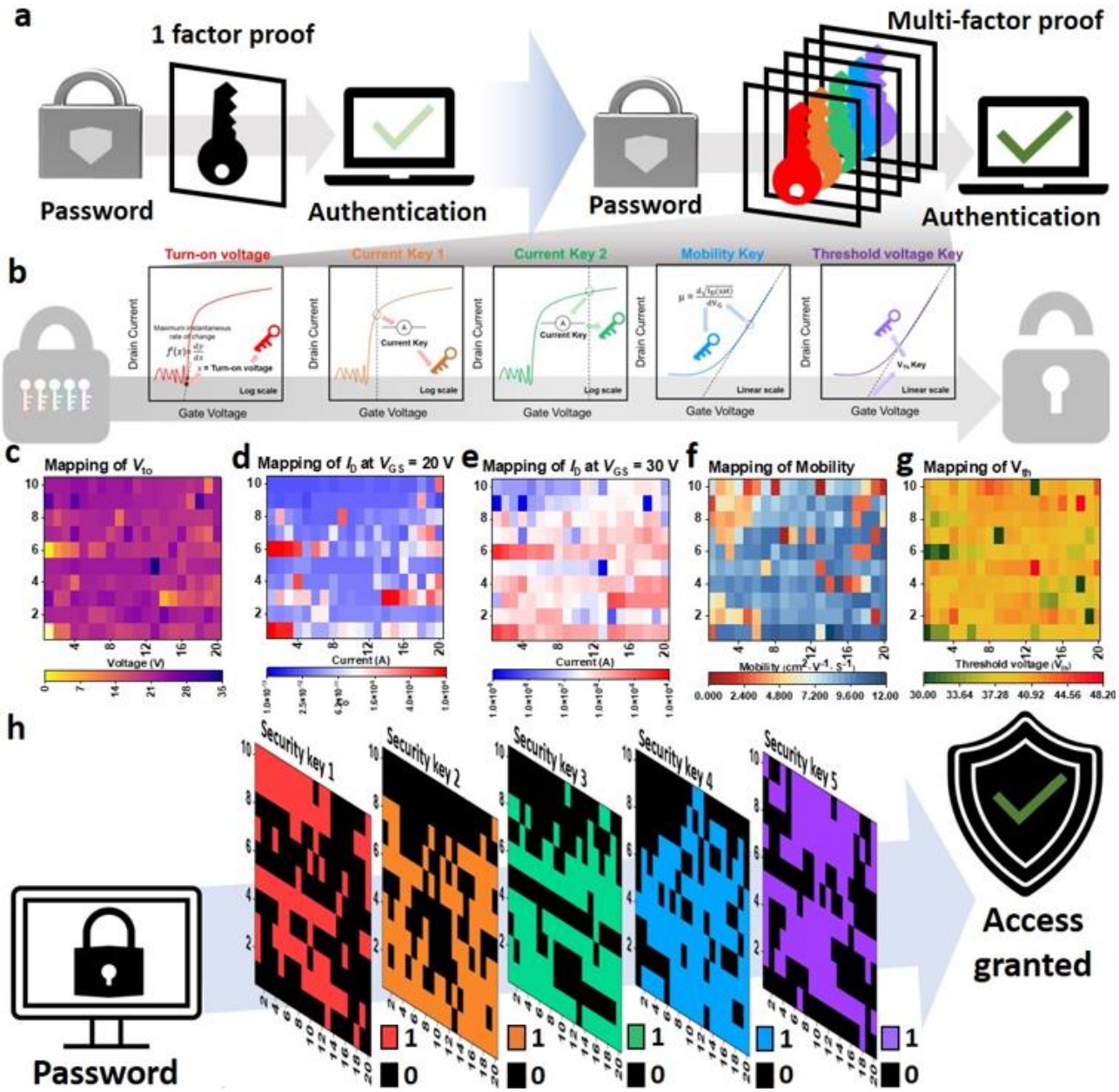
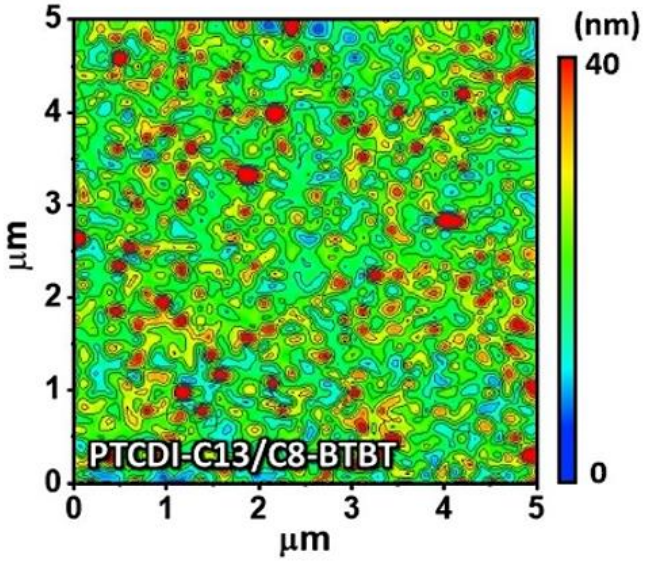
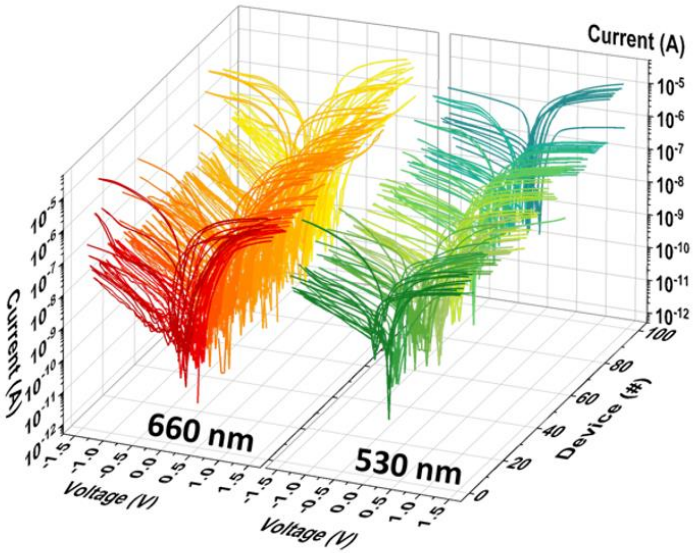
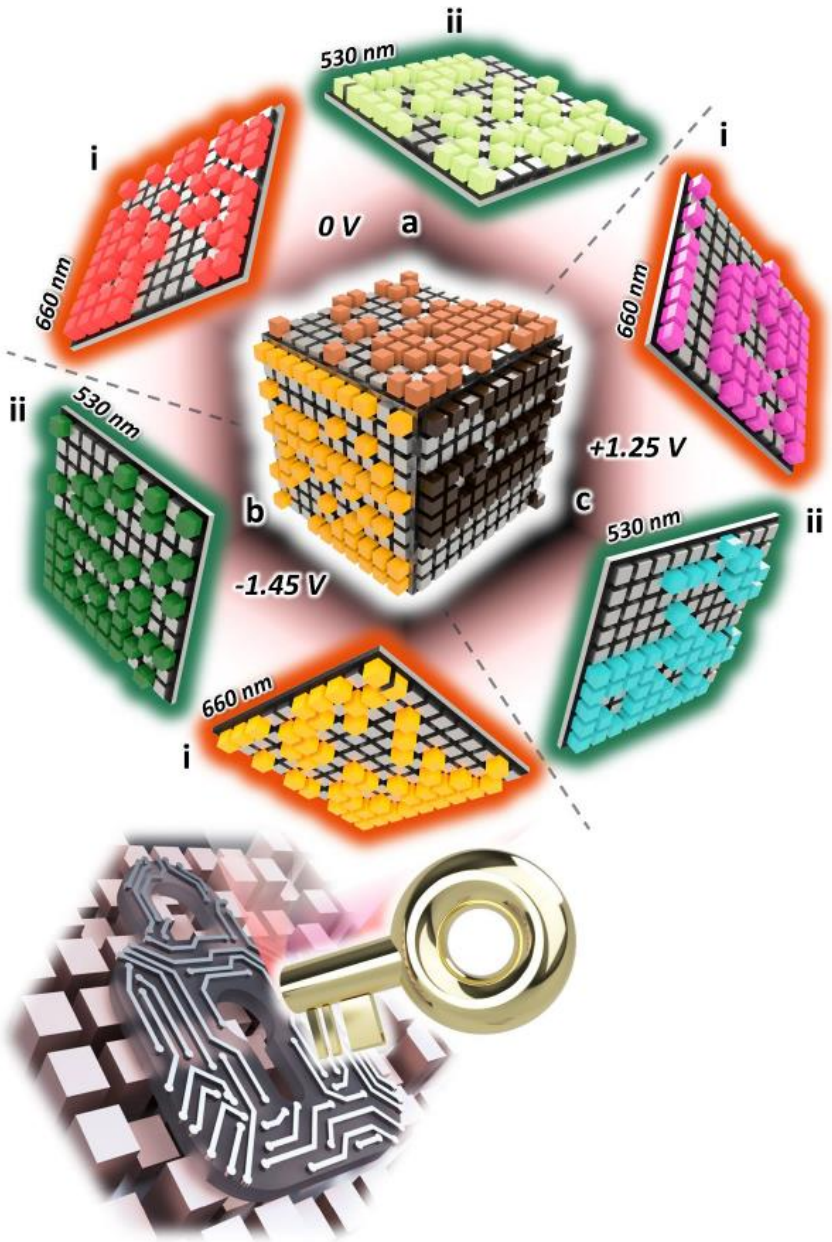


Just accepted last week, Advanced Science (2024)







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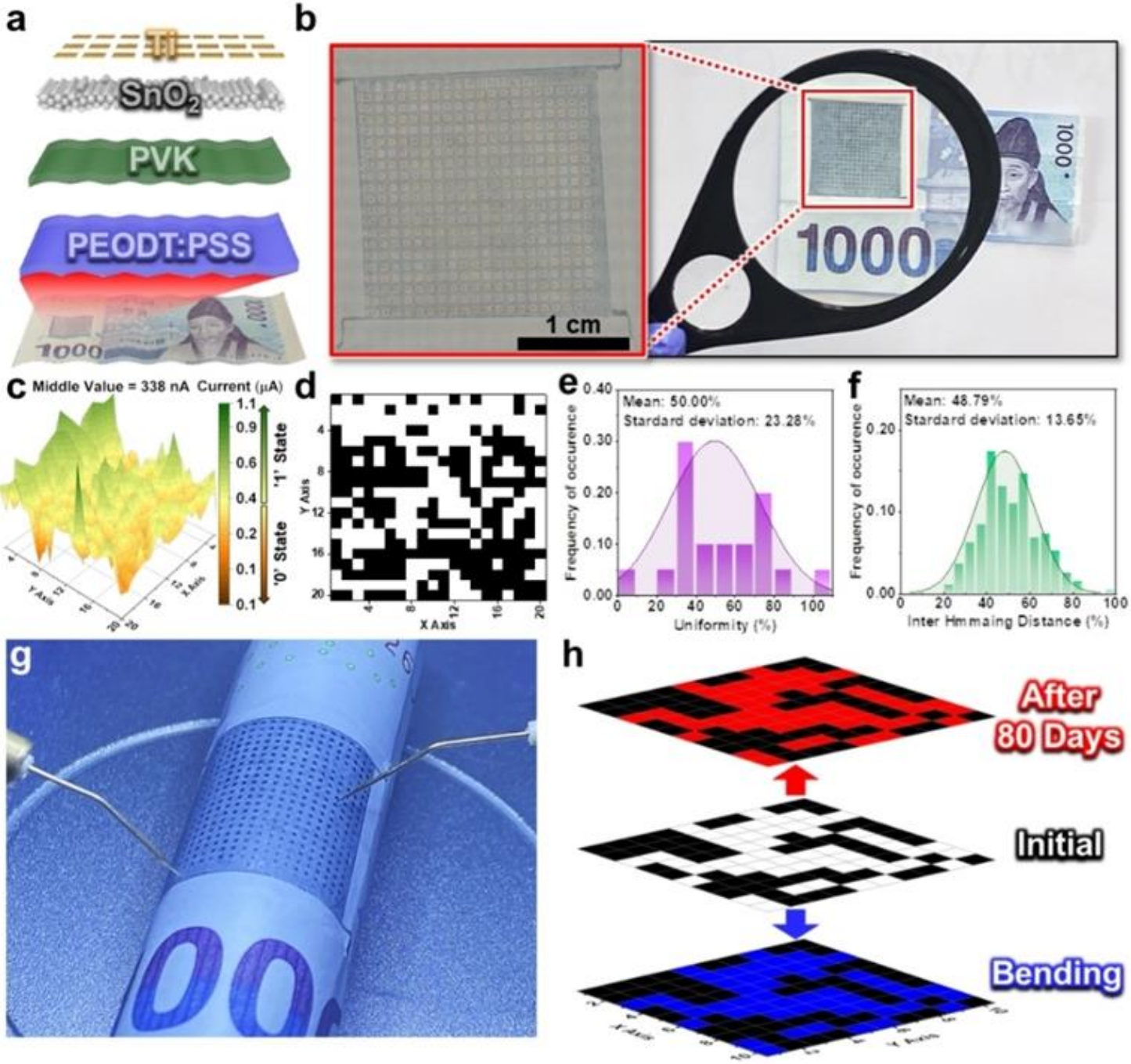
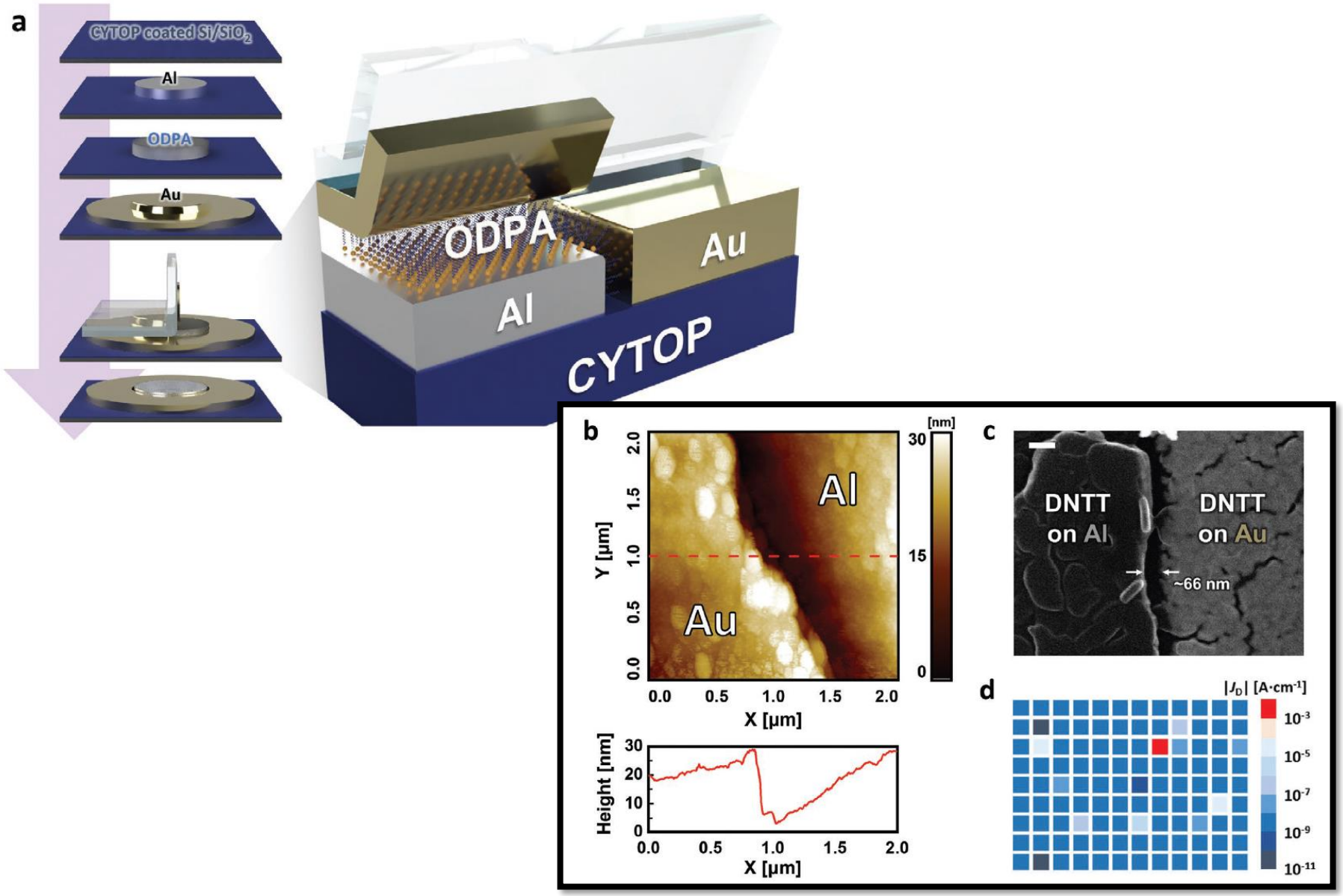


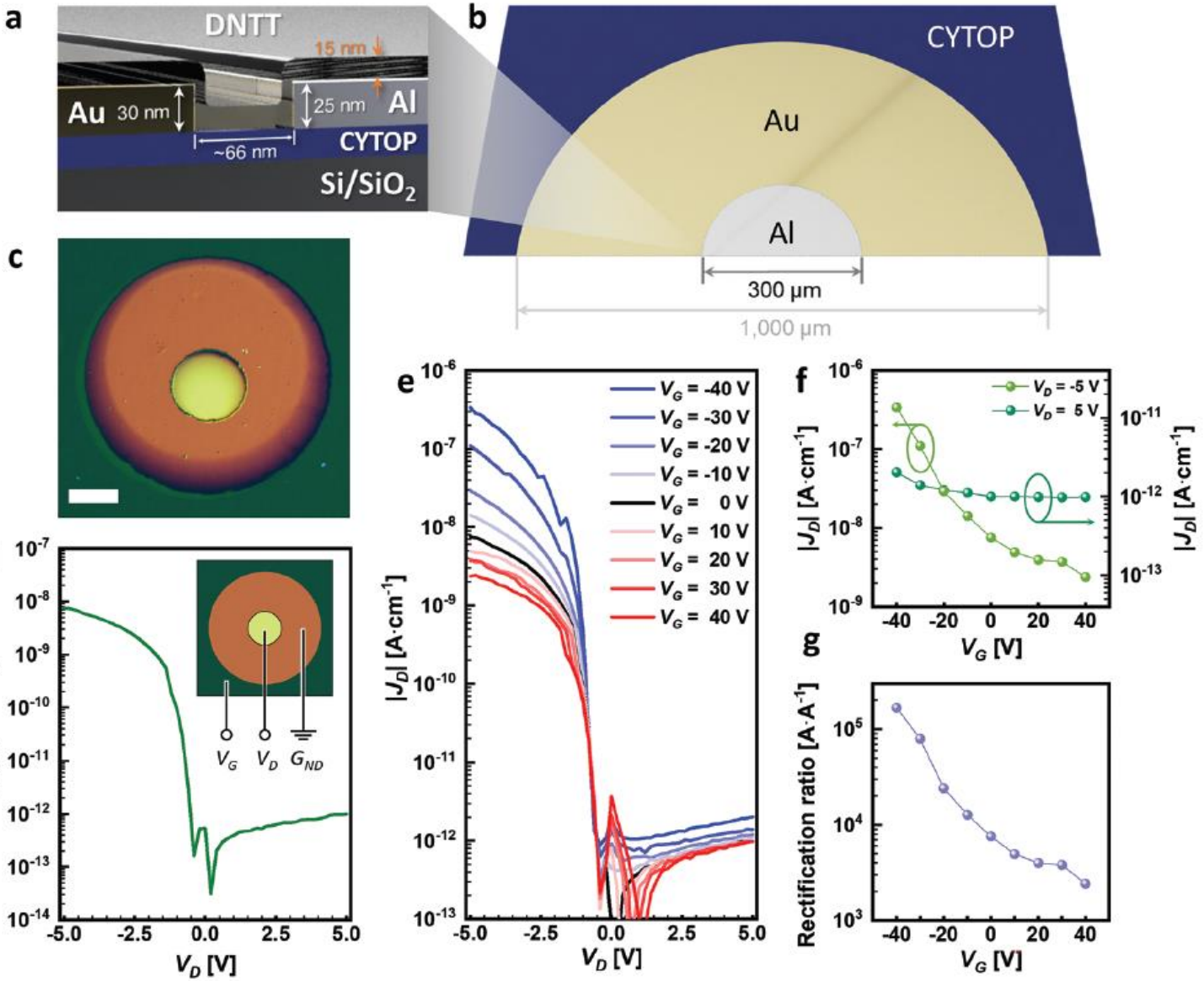
Unpublished results

Nanopattern by adhesion litho (tape)



Minseo Kim, Small (2023)

Nanopattern by adhesion litho (tape)



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Thank you very much for your attention!

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hyoo@gachon.ac.kr

Homepage: https://sites.google.com/view/sdclab/