WORKSHOP

EU – South Korea Joint Researchers Forum on Semiconductors

The Future of Semiconductors

Neuromorphic Computing, Advanced Functionalities, Heterogeneous Integration & Packaging

PROGRAMME

1st DAY

Morning

Coffee and Pastries 8h30

9h00 — OPENING AND POLICY SESSION *(Chair: Werner Steinhoegl)*

- **9h00** — **Introduction** *Werner Steinhoegl, Head of Sector CONNECT.A3/Francis Balestra, ICOS coordinator*
- **9h05** — **Welcome note** – Republic of Korea *Mr Jong-Ho Lee, Minister of MSIT*
- **9h15** — **Welcome note** – European Commission *Mrs Lucilla Sioli, Director CONNECT.A*
- **9h25** — **International Cooperation in the Chips Joint Undertaking** *Mr Jari Kinaret, Director Chips JU*
- **9h35** — **International Collaboration Programs of Korea in Semiconductor R&D** *Dr. Sang-Wan Ryu, Director of NRF (National Research Foundation of Korea)*
- **9h50** — **Presentation of EU-ROK Joint Call** *Yves Gigase, Head of programmes Chips JU*

Coffee break 10h05

10h35 — SESSION 1 – Advanced Functionalities/Heterogeneous Integration & Packaging *(Chair: Roel Baets)*

- **10h35** — **Electrochemical Calculations and Microstructural Analysis in Copper Electroplating to Fill Patterns at Various Feature Scales** *Hyojong Lee, Professor of Dong-A University*
- **11h00** — **Specialized microelectronics for in-memory computing, RF communication and quantum** *Jyrki Kiihamäki, VTT*
- **11h25** — **Integrated Photonics: Enabling the Progression of Digital Society** *Abdul Rahim, Photon Delta*
- **11h50** — **Digital technologies for Agri 4.0 applications** *Alan O'Riordan, Tyndall*
- **12h15** — **Silicon Carbide Electronics for Advanced Power, Sensing and System Integration** *Michael Jank, Fraunhofer IISB*

Lunch Break & Posters 12h40

Afternoon

SESSION 2 – Advanced logic and memories / Neuromorphic computing *(Chair: Francis Balestra/Danilo Demarchi)*

- **13h45** — **Innovative materials and devices for future logic and memory technologies** *Sujin Ahn, Vice President of Samsung Electronics*
- **14h10** — **Research on FD-SOI and non-volatile memory** *Olivier Faynot, CEA-LETI*
- **14h35** — **PIM use case - Cost effective LLM accelerator using AiM (SK hynix's PIM)** *Euicheol Lim, Vice President of SK Hynix*
- **15h00** — **Enabling new research paths with embedded PCM** *Andrea Redaelli, STMicroelectronics*
- **15h35** — **AI Semiconductor (On-Device AI) Present and Future** *Hoijun Yoo, Professor of KAIST (Korea Advanced Institute of Science and Technology)*
- **15h50** — **Emerging ferroelectric materials and devices for semiconductor applications** *Minhyuk Park, Professor of Seoul National University*

Coffee break & Posters 16h15

16h55 - **Advanced compute scaling: a new era of exciting innovations with nanosheet-based devices and increased interdisciplinary synergies** *Anabela Veloso, imec*

17h20 - **Large-Scale Synthesis of 2-Dimensional Transition Metal Dichalcogenide (TMDCs) by Low-Temperature Plasma and their Applications** *Taesung Kim, Professor of Sungkyunkwan University*

17h45 - **Electronic synapses enabled by epitaxial Hafnia-based ferroelectric field memristors on silicon** *Athanasios Dimoulas, National Center for Scientific Research DEMOKRITOS*

18h10 - **Mott memristor-based future computing** *Kyungmin Kim, Professor of KAIST*

18h35 - **Spintronics with complex spin texture** *Chanyong Hwang, Researcher of KRISS (Korea Research Institute of Standards and Science)*

19h00 - **Closing remarks** *Werner Steinhoegl, European Commission - Head of Sector CONNECT.A3*

Cocktail Dinner & Posters 19h10

End of day 1 20h30

2nd DAY

Morning

Coffee and Pastries 8h15

8h45

OPENING OF YOUNG RESEARCHERS SEGMENT

8h45 - **Introduction to Day 2:** *Werner Steinhoegl, Head of Sector CONNECT.A3/Francis Balestra, ICOS coordinator*

YOUNG RESEARCHERS' SESSION *(Chair: Jyrki Kiihamäki/Valeria Kilchytska)*

8h50

8h50 - **Emerging Semiconductors Meet Novel Capabilities: Multi-valued Logic, Security, and Hazard Monitoring** *Hocheon Yoo, Professor at Gachon University*

9h05 - **GaN Technology for Power Electronics Application** *Urmimala Chatterjee, imec*

9h20 - **Artificial Neuron Devices Fully Compatible with CMOS Technology for Neural Processing and Sensing in Neuromorphic Hardware** *Joon-Kyu Han, Professor of Sogang University*

9h35 - **Design ASIC architectures for generic, self-learning and reliable neuromorphic AI accelerators** *Martin Andraud, UCLouvain*

9h50 - **Tailoring memristors through metallization on amorphous materials** *Hanwool Yeon, Professor of GIST (Gwangju Institute of Science and Technology)*

Coffee break & Posters 10h05

10h45 - **Area-selective deposition and atomic layer etching as enabling technologies for the fabrication of 3-dimensional nanodevices**, *Adrie Mackus, Eindhoven University of Technology*

11h00 - **Topotactic engineering for oxide quantum materials** *Woojin Kim, Professor at Pusan National University*

11h15 - **Two-dimensional materials for next generaction non-volatile memories** *Jose Hugo Garcia, Institut Català de Nanociència i Nanotecnologia*

11h30 - **Electronic Eyes based on Flexible and Neuromorphic Optoelectronics** *Changsoon Choi, Researcher of KIST (Korea Institute of Science and Technology)*

11h45 - **2D Materials for Neuromorphic Computing** *Jimin Lee, RWTH Aachen University*

Lunch & posters 12h

End of Researchers Forum 14h

POSTERS SESSION

- **Powering the Future: High-Energy Efficiency Nanoelectronics for Advanced Neuromorphic Computing** *Qing-Tai Zhao, Forschungszentrum Jülich*
- **MoS2 growth and device technology; towards integration with multiplexed graphene sensors arrays** *Laura Remacha Gelabertó, Institut Català de Nanociència i Nanotecnologia*
- **Neuromorphic Computing: Latest activities at ELD and AMO** *Jan van den Hurk RWTH, Aachen University*
- **Smart Sensors and Systems as Enabling Technologies for Climate-Smart Agriculture** *Danilo Demarchi, Politecnico di Torino*
- **Patterned Multi-Wall Nanosheet FETs for Aggressive Scaling Beyond Forksheet FETs: Zero Gate Extension with Minimal Gate Cut Width** *Sanguk Lee, POSTECH*
- **Heterogenous integration of TMD-based memristors and memtransistors with Si CMOS for neuromorphic computating** *Francisco Gamiz, University of Granada*
- **Encapsulation and protection strategies for graphene-based solution-gated field-effect transistors towards high performing neural recording** *Anna Graf, ICN2*
- **Metal oxide-based structures for novel computing paradigm concepts** *Robert Mroczyński*, *Warsaw University of Technology*
- **Advancements in Neuromorphic Computing Using Silicon Nitride Memristors for IoT and Security** *Panagiotis Dimitrakis, NCSR Demokritos*
- **High Performance Chiplet-based PIM AI Semiconductor** *Jaehoon Chung / Jaewoong Choi, ETRI*
- **Smart systems integration for biomedical and environmental applications** *Bogdan Firtat, IMT Bucharest*
- **Advanced computing and functionalities in CROMA lab** *Alessandro Cresti, CNRS*
- **Full-Stack Neuromorphic Computing in Delft** *Moritz Fieback, TUDelft*
- **Neuromorphic sensing and computing at INL** *Bruno Romeira, INL*

ABSTRACTS AND SPEAKERS

OPENING AND POLICY SESSION

Jong-Ho Lee is the Minister of the Ministry of Science and ICT since 2022. Previously, he was Director at the Inter-University Semiconductor Research Center and Vice Dean for Planning and Strategy at the College of Engineering (Seoul National University). After his PhD in Electronics Engineering in 1993, he started his career as professor in several universities such as Wonkwang University, Kyungpook National University and Seoul National University. In 2017 he won the Kyung-Ahm Prize, Engineering and in 2015 he was awarded by the Order of Service Merit Green Stripes (Nokjo Geunjeong Medal).

Ms Lucilla Sioli is the Director for "Artificial Intelligence and Digital Industry" within Directorate-General CONNECT at the European Commission. She is responsible for the coordination of the European digitisation of industry strategy and for policy development in the areas of artificial intelligence (AI) and semiconductors. The directorate also supports R&D&I in key digital industrial technologies including microelectronics, photonics, robotics and AI. Lucilla holds a PhD in economics from the University of Southampton (UK) and one from the Catholic University of Milan (Italy) and has been a civil servant with the European Commission since 1997.

Jeonghyun Ryu is Ambassador Extraordinary and Plenipotentiary to the Kingdom of Belgium and the European Union and the Permanent Mission to the North Atlantic Treaty Organization. He started his career by joining the Ministry of Foreign Affairs (MOFA) in 1991 in which he worked as Deputy Director-General, South Asian and Pacific Affairs Bureau (2015), Director-General for South Asian and Pacific Affairs (2016) and Deputy Minister for Protocol Affairs (2021). In 2017, he was awarder with the Service Merit Medal.

Jari Kinaret received his M.Sc. degrees in Theoretical Physics and Electrical Engineering from the University of Oulu in Finland in 1986 and 1987, respectively. He then moved to the U.S. where he graduated with a Ph.D. in Physics from the Massachusetts Institute of Technology in 1992. After graduation he moved first to Denmark and then to Sweden, where he worked as Professor of Physics at the Chalmers University of Technology in Gothenburg. He is the initiator of the one billion euros Graphene Flagship project and served as its Director in 2013-2023 before moving to a new position in Brussels as the Executive Director of the Chips Joint Undertaking in October 2023.

- **International Collaboration Programs of Korea in Semiconductor R&D**
  Sang-Wan Ryu ~ NRF

Semiconductor is one of the strongest industries in Korea. As the industry has grown, we have developed our R&D activities in both basic science and advanced production technologies. At present, we are seeking closer international R&D cooperation to catch up with the ongoing internalization of the semiconductor chip manufacturing process. In this regard, the Korean governments have established Korea-EU and Korea-NSF(US) programs on advanced semiconductor chip, processing, and packaging technologies. In addition, we have announced a call for Korean researchers to propose international collaborative research projects on semiconductors, open to counterparts from all countries. We believe that our efforts to promote multinational collaborative research will lead to a stronger bond between countries in the semiconductor chip production network.

Sang-Wan Ryu holds various positions, including Director at the Division of Semiconductor & Display Technology, National Research Foundation of Korea since February 2024 and Professor at the Department of Physics, Chonnam National University since 2004. Previously, he served as a Senior Researcher at the Electronics and Telecommunication Research Institute and experienced as a Research Associate at the University of Southern California.

Dr. Yves Gigase is the Head of Programmes of the Chips Joint Undertaking. Prior to join the European institutions, he worked in companies active in optoelectronics, electronic consumer goods, epitaxy equipment, consulting, and telecommunication. He holds an Master in the Science of Engineering in Applied physics and a PhD in Optoelectronics, both from the University of Gent. He did two postdocs one at the IBM Research Labs in Zurich and one at the Optical Computing Systems Centre at the University of Colorado, Boulder.

Dr. Werner Steinhögl is Head of Sector in the Microelectronics and Photonics Industry unit of the European Commission in Brussels. He has been serving in the Communications Networks, Content and Technology (CONNECT) directorate general since 2005 in different positions. He has managed R&I support programs spanning from emerging quantum computing technologies over nano- technologies to safety-critical computing and cyber-physical systems. Since 2018 he has been in charge of the photonics public private partnership for research and contributed to the EU Chips Act. Since 2022 he deals also with international collaboration in the semiconductor area. Before joining the European Commission, he had worked as team leader for 6 years in the semiconductor industry at Infineon and Siemens in Munich, held various positions in corporate research and collaborated with R&D teams in the US. He holds a PhD in solid state physics acquired at the Max-Planck Institute for Fluid Dynamics in Göttingen, Germany, in 1998.

Francis Balestra, CNRS Research Director at CROMA, is Director Emeritus of the European SINANO Institute and President of IEEE Electron Device Society France, and has been Director of several Research labs. He coordinated several European Projects (NEREID, NANOFUNCTION, NANOSIL, etc.) that have represented unprecedented collaborations in Europe in the field of Nanoelectronics, and is currently coordinator of the Horizon Europe ICOS project dedicated to International Cooperation on Semiconductors with leading semiconductor countries. He founded and organized many international Conferences, and has co-authored more than 500 publications. He is member of several European Scientific Councils, of the Advisory Committees of International Journals and of the IRDS (International Roadmap for Devices and Systems) International Roadmap Committee, as representative of Europe.

SESSION 1 – ADVANCED FUNCTIONALITIES / HETEROGENEOUS INTEGRATION & PACKAGING

Chair: Roel Baets

Chair of the session
Roel Baets ~ imec

Roel Baets is an emeritus full professor at Ghent University and imec. For many years he has made contributions to research on integrated photonics (silicon, silicon nitride, III-V) and its applications in datacom/telecom as well as in medical and environmental sensing. He has founded and has chaired ePIXfab, the European Silicon Photonics Alliance, and continues to serve the silicon photonics community at large in advisory roles. He is a Fellow of IEEE, EOS and Optica. He has been recipient of amongst others the 2020 John Tyndall Award and the 2023 IEEE Photonics Award.

Electrochemical Calculations and Microstructural Analysis in Copper Electroplating to Fill Patterns at Various Feature Scales
Hyojong Lee ~ Dong-A University

This study covers the EBSD microstructure in connection with electrochemical analysis results at various feature scales. First, for mass transfer in aqueous solutions, copper ions, Cl-, and organic additives are known to have diffusion coefficients of ~10-10 m2s-1, which is estimated to have an average travel distance of ~10㎛ per second. In filling these nanoscale patterns, accumulation of accelerator due to competitive adsorption of organic additives and surface reduction is the main phenomenon. However, when the pattern scale is tens of microns or larger, the concentration gradient inside the pattern due to mass transfer can play an important role.

Hyojong Lee received the B.S. degree in metallurgical engineering from Seoul National University, Korea in 1997, and his M.S. and Ph.D degrees in Materials Science and Engineering from Seoul National University in 1999 and 2003, respectively. He is currently professor of Material Science and Engineering in Dong-A University of Pusan, Korea. He worked as a ULSI interconnect process engineer at Samsung Electronics and as a visiting researcher at Tohoku University in Japan, Caltech and NIST in the United States. He published over 70 papers and filed over 30 domestic and international patent applications. His current research interests include structure and properties of thin-films and

their crystallographic phenomena; In situ grain growth of Cu during recrystallization, stress-induced voiding, and hetero-epitaxial growth of GaN on sapphire substrate.

Specialized microelectronics for in-memory computing, RF communication and quantum
Jyrki Kiihamäki ~ VTT

Specialised microelectronics uses new materials and manufacturing processes that enable completely new functionalities compared to mainstream microelectronics. They can also improve the efficiency of existing functionalities lowering power consumption and increasing computing power. VTT's focuses in specialized microelectronics include microelectromechanical systems (MEMS), radio frequency (RF) technologies, photonics and quantum technologies. In this presentation, we show examples of (i) materials, device, process and application development for neuromorphic computing, (ii) micromachined 3D integration of RF devices for THz frequency range and (iii) advanced quantum sensors and electronics.

Dr. Jyrki Kiihamäki has worked for 35 years at VTT, Technical Research Centre of Finland, currently as a Co-Creation Manager at the Microelectronics and Quantum Technologies research area. He has led the silicon-on-insulator (SOI) MEMS and the MEMS teams 2006-2012. After that he has been in strategic research management positions. He is VTT representative at Aeneas and EPoSS industry associations and a member of Xecs TEG.

Integrated Photonics: Enabling the Progression of Digital Society
Abdul Rahim ~ PhotonDelta

Integrated photonic technologies enable the large-scale production of low-cost photonic chips that can perform complex photonic functions in an energy-efficient manner. This technology has become indispensable for the datacom/telecom industry, where millions of PIC-based high-speed transceivers act as the backbone of today's data centres and the internet. With the rise of AI and high-performance computing, the microelectronics industry has shown a growing interest in integrated photonics, where this technology could boost the semiconductor industry's growth. Additionally, the continuous maturity of photonic IC technology and its versatile nature make it a strong candidate to revolutionize various other markets, including quantum, healthcare, agrifood, and mobility. This presentation will cover various use cases of photonic integration technologies and their impact on the digital transformation of our society in a sustainable manner.

Abdul Rahim received a double master's degree in electrical engineering with emphasis on Photonics in 2008 from the Royal Institute of Technology, Sweden and Ghent University, Belgium. In 2014, he earned his PhD from Technische Universitaet Berlin, Germany. His research focuses on silicon photonics for optical communication. He also holds a degree in innovation management and entrepreneurship from HEC Paris. Abdul Rahim has held research positions at Larid Technologies in Sweden, The Leibniz Institute for High-Performance Microelectronics (IHP) in Germany, and The Institut National de la Recherche Scientifique (INRS) in Canada. From 2015 to 2024, Abdul Rahim managed ePIXfab - the European silicon photonics alliance. Currently, he is managing the ecosystem of PhotonDelta, which is a growth accelerator for integrated photonics. Abdul Rahim has published >30 publications in prestigious international conferences and journals.

Digital technologies for Agri 4.0 applications
Alan O'Riordan ~ Tyndall

With the global population expected to grow to over 9.6 billion by 2050 it is a projected that a 50-60 % increase in food production will be required. A key challenge then, going forward, will be to sustainably close the food gap. This must be achieved against the backdrop of climate change & desertification, labour shortages and competition for energy, land & resources. It is clear then, that addressing this challenge will require the development of more efficient and sustainable food production techniques and processes. To this end, new technologies, that are fit for purpose, are urgently required to digitise the entire food chain. This convergence between the Internet of Things (IoT) and the agri-food industry requires sensor systems and technologies that provide real time data to producers and processers; required for rapid, but informed, decision making. In this talk, some of the digital technologies being developed by Tyndall to address the sustainability issues, by focusing on specific use cases, will be presented.

Alan O'Riordan is a Senior Research Fellow at the Tyndall National Institute. He received his BSc in Analytical Chemistry in 1995 and a PhD in Chemistry (Nanotechnology) in 2005. He has graduated 15 PhDs and 3 MSc. students and currently leads a team of 2 staff members, 6 post Docs, 7 PhD students focused on developing smart sensors and systems for Sustainable Agri-food and Environmental applications. The Group is developing two complementary sensor technologies on silicon chip substrates that employ (i) nanoelectrochemistry and (ii) Surface enhanced Raman Spectroscopy detection mechanisms that providing highly sensitive, selective and reliable measurements. A key foundation of his research focus is to ensure its relevance and real-life deployment through collaborative co-development. To this end he has competitively won multiple research projects worth circa ~€17M in total research funding to the PI. This has resulted in multiple invited and keynote talks on Agri 4.0 at major conferences (IEEE ESTC and ECS-ICMS conferences), he leads the EU team's contribution on Smart Sensor Systems for the IEEE International roadmap on Devices and Systems - More than Moore white paper. He has published over 100 peer reviewed publications, one patent granted "Nanowire Electrode Sensor" EU & US (US 20140145709) and won the Enterprise Ireland Gold Medal for Most Innovative Technology Emerging from Third Level (National Ploughing Contest 2016/2022). He is a Steering Committee member of the Royal Society of Chemistry – Electroanalytical Sensors and Systems Group and a core steering committee member of EPoSS SSI conferences 2021-2023.

Silicon Carbide Electronics for Advanced Power, Sensing and System Integration
Michael Jank ~ Fraunhofer IISB

The wide bandgap semiconductor Silicon Carbide offers unique potentialities for operation of devices and systems at harsh conditions. Power devices and high-temperature environments are the most common examples. Fraunhofer IISB offers research, development and prototyping for MOS and bipolar power devices, CMOS-integrated sensing and control solutions as well as dedicated discrete sensor solutions for advanced application requirements.
The presentation will showcase the research and development portfolio and selected examples from international cooperation. We will finally put future fields of interest forward for discussion towards joint project approaches. The IISB service and prototyping portfolio can be accessed via EUROPRACTICE and ASCENT+.

Michael Jank earned a diploma in Electrical Engineering and a PhD with a thesis on Silicon CMOS process integration from Friedrich-Alexander-Universität Erlangen-Nuremberg (FAU).

After his doctorate in 2006, he started a research group on thin-film materials and systems at Fraunhofer Institute for Integrated Systems and Device Technology IISB. His research includes electronic materials, electron devices and semiconductor processing including sensors as well as assembly and interconnect technologies. Michael has a proven track record in regional, national and European projects both in application-oriented funding schemes as well as in basic research.

Since 2023 he is heading the Research and Development on Semiconductor Devices and Processes at IISB, focusing on Silicon Carbide and Silicon devices for power electronics. He is reviewer for a range of scientific journals, conferences and research programs related to his field of expertise. Further, he is teaching at FAU on Nanoelectronics, Power Semiconductor Devices and Flexible Electronics.

SESSION 2 – ADVANCED LOGIC AND MEMORIES / NEUROMORPHIC COMPUTING

Chair: Francis Balestra (part 1) / Danilo Demarchi (part 2)

- **Innovative materials and devices for future logic and memory technologies**
  Sujin Ahn ~ Samsung Electronics

Artificial intelligence and smart devices have brought about an unprecedented revolution in our society. Semiconductors play a crucial role in this revolution, being at the core of many computing device innovations. These transformative trends of AI and smart devices will continue to open up explosive growth opportunities for the semiconductor community.
However, there are compelling technical challenges to fully grasp its growth potential. It has become even more challenging to meet the requirements such as Power, Performance and Area (PPA), while continuously scaling the physical dimensions of semiconductor devices below 10 nm. To address these challenges, technical innovations in terms of device structures, materials, processes and equipment as well as strong global research collaboration are essential. After reviewing the evolution of the semiconductor technologies over the past 50 years, I will identify today's technical challenges and discuss promising innovative technologies for future logic and memory.

Sujin Ahn is a corporate EVP and the head of Advanced Technology Development Office at Samsung Semiconductor R&D Center. She is currently in charge of research and development of Samsung's future innovative memory, logic devices and advanced packaging. She has more than two decades of technology leadership driving innovation at Samsung, such as PRAM, STT MRAM, and CTF Nand Flash R&D from 1999 to 2013. She made a significant contribution to the commercialization and mass production of VNAND Flash at the Memory Business as well as R&D from 2014 to 2023.
Dr. Ahn received the B.S., M.S., and Ph.D. degrees in Electrical and Electronics Engineering from Pohang Science and Technology in Korea in 1993, 1996, 1999 respectively. She has published 50 papers at international conferences and SCIE, and holds 40 domestic and international patents. She served as an executive committee member in IEDM Society from 2014 to 2018, and is working as an IEEE Journal review since 2007.

Dr. Ahn was dedicated at the forefront of Samsung's innovative technology R&D such as CTF Nand Flash, VNAND, and STT MRAM from 1999 to 2013. She was promoted to vice president in 2014 and led the research and development of VNAND from 2014 to 2018. She made a significant contribution to the commercialization and mass production of VNAND at the Memory Business from 2018 to 2020 and served as the head of the Flash Process Architecture Team at the Memory Business from 2020 to 2023.

Research on advanced FD-SOI and non-volatile memories technologies
Olivier Faynot ~ CEA-Leti

World's digitalization induces a tremendous increase of data generation, close to 500 Zetabyte by 2030. This data deluge leads to a dramatic increase of energy consumption, not sustainable on a medium term. Technological breakthrough must be developed in order to significantly improve (by a factor of 1000) the Power efficiency of electronic.
This paper will detail all the ongoing developments on FD-SOI technology and also Non-Volatile memories, and will highlight how those developments will impact Energy efficiency. Resistive Memories can be coupled with Neuromorphic architectures, in order to explore new paradigms and open new opportunities for the future of computing.

Olivier Faynot received the M.Sc and Ph.D. degrees from the Institut National Polytechnique de Grenoble, in 1991 and 1995, respectively. His doctoral research was related to the characterization and modeling of deep submicron Fully Depleted SOI devices fabricated on ultrathin SIMOX wafers. He joined LETI (CEA-Grenoble, France) in 1995, working on Partially Depleted and Fully Depleted SOI technologies development in the frame of Industrial Partnerships.
From 2008 to 2017, he managed various teams focussed on advanced CMOS, memories and 3D technology integration and was assigned on manufacturing sites to implement FDSOI technologies. During that period, he was engaged in the transfer to production of 28nm and 22nm FDSOI technologies with industrial partners. Those technologies are now available in production. From 2017 to 2019, he managed the Patterning department at CEA-LETI, within the Silicon Technology division. Since 2019, he is managing the whole Silicon Component division at CEA-Leti. He is author and co-author of more than 300 scientific publications in journals and international conferences, and was successively in the committees of the main international Semiconductors conferences like International Electron Device Meeting (IEDM), the symposium on VLSI Technology, the IEEE International SOI conference, the EUROSOI network, the Solid State Device and Materials (SSDM) conference and the International S3S conference. He received the 'Général Férié' award in 2012 and the 'Electron d'Or' award with CEA-Leti, ST Microelectronics and SOITEC in 2017.

PIM use case - Cost effective LLM accelerator using AiM (SK hynix's PIM)
Euicheol Lim ~ SK Hynix

AI chatbot service has been opening up the mainstream market for AI services. But problems seem to exist with considerably higher operating costs and substantially longer service latency. As the generative AI model size continued to increase, memory intensive function takes up most of the service operation. That's why even latest GPU system does not provide sufficient performance and energy efficiency. To resolve it, we are introducing shorter latency and operating cost-effective generative AI accelerator using AiM (SK hynix's PIM) We'd like to introduce how to reduce service latency and decrease energy consumption through AiM, as well as explain the architecture of AiMX, an accelerator using AiM.

Euicheol Lim is a Research Fellow and leader of Memory Solution Product Design team in SK Hynix. He received the B.S. degree and the M.S. degree from Yonsei University, Seoul, Korea, in 1993 and 1995, and the Ph.D. degree from Sungkyunkwan University, suwon, Korea in 2006. Dr.Lim joined SK Hynix in 2016 as a system architect in memory system R&D. Before joining SK Hynix, he had been working as an SoC architect in Samsung Electronics and leading the architecture of most Exynos mobile SoC. His recent interesting points are memory

and storage system architecture with new media memory and new memory solution such as CXL memory and Processing in Memory.

Enabling new research paths with embedded PCM

Andrea Redaelli ~ STMicroelectronics

In the last years, embedded PCM has been moved from emerging to a mainstream memory in the microcontroller roadmap for technology nodes below 28nm. The developed capability to master the technology, the reliability and the yield is enabling the use of ePCM for additional research programs in more advanced fields like in-memory computing and neuromorphic computing. In the talk, a brief review of the key innovations required to bring to maturity the technology will be illustrated as well as the opportunities to fully exploit the potential of PCM devices.

Andrea Redaelli received the Laurea and Ph.D. degrees in electronic engineering from the Politecnico di Milano, Italy. During the Ph.D., he worked on Phase Change Memories in the Department of Electrical and Electronic Engineering (Politecnico di Milano). From 2008 to 2013 he worked on 45 and 26 nm PCM technology developments, firstly as a Numonyx employee and then joining Micron Technology. His work areas included memory array architecture definition, design of test structures, process integration, cell modelling and cell electrical testing. He was also the coordinator of a European funded project under FP7 named PASTRY on low power PCM development. From 2014 to 2020, Andrea worked on 3DXpoint technologies, in charge of the cell development at the most advanced scaled nodes. Since 2020, Andrea is a fellow in STMicroelectronics, leading the cell development of embedded PCM technologies. Andrea is author and co-author of more than 70 papers and more than 140 US patents, resulting in a h-index of 30 according to google scholar.

AI Semiconductor (On-Device AI) Present and Future

Hoijun Yoo ~ KAIST

Recently, Deep Neural Networks are widely used for Mobile and Edge devices need more AI services because of the huge interest in On-Device AI.
Low power CNPU and reconfigurable DNPU which can accelerate both CNN (Convolutional Neural Network) and RNN (Recurrent Neural Network) will be introduced. UNPU with“Dynamically Reconfigurable Processor” architecture will be explained.
The On-Device AI will implement not only the inference but also learning on a chip. Even DRL chip will be introduced for the object tracking applications are implemented with low-power and high-performance for autonomous vehicles and intelligent robots.
Finally, the future direction of AI SoC will be explained along 3 directions, Spatial Computing, PIM (Processing In Memory) and Neuromorphic Chips. A few examples of each research, especially ultra-low power LLM acceleration example, will be introduced and conclusions will be made.

Prof. Hoijun Yoo is the Dean of KAIST AI Semiconductor Graduate School, ICT Chair professor of Department of Electrical Engineering at KAIST, Director of National PIM Semiconductor Design Research Center, KAIST IT Convergence Research Institute, and SDIA (System Design Innovation and Application Research Center). He was 2008 IEEE Fellow and was the plenary speaker of ISSCC 2019. His current research interests are Bio Inspired Intelligent SoC Design, Wearable Computing and Wearable Healthcare. He published more than 200 papers, and wrote 5 books including “Mobile 3D Graphics SoC” (2010, Wiley) and "Biomedical CMOS ICs"(2011, Springer).
He is the Steering Committee Chair of IEEE A-SSCC, and a member of the executive committee of Symposium on VLSI. He was the elected AdCom Member of IEEE SSCS (2021-2023),

TPC Co-Chair of ISWC 2010, IEEE Distinguished Lecturer('10-'11), and Asia Chair of ISSCC('10-'11). He was TPC Chair of ISSCC 2015, Vice Chair of ISSCC 2014, Technology Direction Sub-Committee Chair of ISSCC 2013, a member of Executive Committee of ISSCC 2008-2015 and recognized as the top 4 paper-contributor for 2004-2013 ISSCCs, top 10 paper contributor for 1954-2013 ISSCCs and top 5 paper contributor for 1954-2023 ISSCCs. From 2003 to 2005, he was the full time Advisor to the Minister of Korean Ministry of Information and Communication for SoC and Next Generation Computing. Dr. Yoo received the National Medal for his contribution to Korean Memory Industry in December of 2011, the Korean Scientist of the Month Award in Dec. 2010, KAIST Best Research Award in 2007, KAIST Best Academic Award in 2019, and KAIST Best Achievement Award in 2022. He received Best paper awards of IEEE ISCAS 2021 and 2023, Best paper aAwards of IEEE AI-CAS 2019 and 2022, and Outstandong Paper Award of 2022 CICC. He received Best Design Award of 2001 ASP-DAC, and Outstanding Design Awards of A-SSCCs 2005, 2006, 2007, 2010, 2011, 2014, 2020, 2021, 2023, and Best Demo Award of ISSCC 2016, 2017, 2019, 2020 and 2024.

- **Emerging ferroelectric materials and devices for semiconductor applications**
  Minhyuk Park ~ Seoul National University

Fluorite-structured ferroelectrics are recognized as promising candidates for electronic devices in both present and future computing systems due to their compatibility with complementary metal oxide semiconductor technology and scalable dimensions. [1-3] Atomic layer deposition facilitates the uniform formation of sub-10-nm thick films on 3D nanostructures, enabling the integration of nanoelectronic devices on an extensive scale. Despite these advantages, challenges persist in device performance, encompassing endurance, device-to-device variation, and the intricate balance between operational speed and longevity, necessitating urgent solutions for practical applications. These challenges are intricately linked to material issues arising from defects, ranging from intrinsic factors like oxygen vacancies to extrinsic elements such as residual impurities and interfacial chemistry at ferroelectric/metal and ferroelectric/semiconductor interfaces. [4-7] The polycrystalline nature, coupled with a weak preferred orientation, contributes significantly to pronounced device-to-device variations. Notably, mobile charged defects, including oxygen vacancies, impact polarization switching kinetics and overall device operational speed. This presentation comprehensively reviews the current material challenges in fluorite-structured ferroelectrics, drawing insights from previous studies to address these concerns and unlock the full potential of these materials in electronic device applications.

Minhyuk Park, an associate professor at Seoul National University's Department of Materials Science and Engineering, has made significant contributions to emerging fluorite-structured ferroelectrics like hafnia and zirconia. His research, conducted at Seoul National University, NaMLab gGmbH, and Pusan National University, focuses on elucidating mechanisms behind the formation of metastable ferroelectric phases, exploring energy-related applications such as supercapacitors and energy harvestors, and studying ferroelectricity in fluorite-structured nanolaminates and superlattices. With over 110 coauthored papers in peer-reviewed journals, including prestigious ones like Nature Reviews Materials and Advanced Materials, Park's work has been cited over 10,000 times with an h-index of 54, showcasing his academic impact. Recognitions include being selected as a POSCO Science Fellow in 2020 and receiving two SK-Hynix Awards at the Korean Conference on Semiconductors. Park was also a Humboldt Postdoctoral Fellow and has been acknowledged as an emerging investigator in several journals, including Nanoscale and Journal of Materials Chemistry C. He received the Ferroelectrics Young Investigator Award from IEEE UFFC society in July 2023.

- **Advanced compute scaling: a new era of exciting innovations with nanosheet-based devices and increased interdisciplinary synergies**

Anabela Veloso ~ imec

The need for increased computing keeps growing at an ultra-fast speed, required to support an ever larger and wider range of applications. Logic standard-cell shrinkage remains at the core of the compute roadmap. Its momentum is expected to carry on by introducing new device architectures (e.g., nanosheet-based FETs in single-level and 3D-stacked configurations), materials, scaling boosters like backside-power-delivery and an overall move towards increased use of both wafer-sides. Adoption of system-technology-co-optimization (STCO) can further enable new scaling paths with more versatile/hybridized platforms for enhanced-system-performance. We will discuss key advances, sustainability-aware innovations, and increased interdisciplinary synergies that are shaping the roadmap.

Anabela Veloso received a Ph.D. from INESC-IST-Lisbon University, Portugal in 2002. Since 2001, she has been working at imec, in Leuven, Belgium, where she is a principal member of technical staff. Currently, her main research interests are in the areas of advanced CMOS device physics, integration, characterization, and technology, with recent focus on the exploration of scaled nanowires/nanosheets-based FETs (with lateral or vertical transport), logic with functional backside, and overall novel device schemes that also take into consideration possible new options for transistor engineering and connectivity by using both wafer sides. She has authored or co-authored more than 200 papers published in peer-reviewed international conference proceedings and technical journals, presented 26 invited conference talks, and has been (co-) inventor of more than 23 filed/granted patents. She has also been serving in several conference committees including IEDM, SSDM, ECS Meeting, IIT, and the Symposium on VLSI Technology and Circuits.

- ### Large-Scale Synthesis of 2-Dimensional Transition Metal Dichalcogenide (TMDCs) by Low-Temperature Plasma and their Applications
  ### Taesung Kim ~ Sungkyunkwan University

The growing interest in transition metal dichalcogenides (TMDCs) stems from their potential synergies with other 2D materials in heterostructures, which can lead to advancements in next-generation electronic devices. However, the practical utilization faces challenges due to limited synthesis processes, including high temperatures, poor controllability, and low yield. In response, my research group has focused on plasma-enhanced chemical vapor deposition (PECVD) for 2D TMDC synthesis since 2015. The fabrication of heterogeneous 2D TMDCs and structural polymorphs by optimizing plasma characteristics has been explored. These materials have been applied to enable next generation devices, such as photoreactive functional devices, neuromorphic devices, and etc.

Dr. Taesung Kim received his Bachelor's in Mechanical Engineering from Seoul National University, Korea in 1994. He received his Master's, and Ph. D. in Mechanical Engineering from University of Minnesota, USA in 1998 and 2002, respectively. He joined Seagate Technology in 2002 and worked as Sr./Staff Engineer in Recording Head R&D.

Since 2005 Dr. Kim has been a professor in the School of Mechanical Engineering and SKKU Advanced Institute of Nanotechnology (SAINT), Sungkyunkwan University in Suwon, Korea. In 2014, he was appointed as SKKU Young Fellow and started working for SKKU Research & Business Foundation as a Vice President. During 2019 and 2020, he worked as a Vice President of Admission and he is currently a dean of College of Engineering starting 2023. His research interests include 2-D material synthesis using plasma process, optical fiber sensors, semiconductor fabrication process (CMP, cleaning and contamination control), and atmospheric/indoor aerosol control.

Electronic synapses enabled by epitaxial Hafnia-based ferroelectric field memristors on silicon
Athanasios Dimoulas ~ NCSRD DEMOKRITOS

A new ferroelectric field effect memristor is presented, comprising epitaxial Hf0.5**z**r0.5O2 ferroelectric with epitaxial SrTiO3-**δ** semiconductor bottom electrode, monolithically integrated on silicon. The memristor shows pair pulse facilitation and spike timing dependent plasticity in the 1 mV -100 ns range at very low programming voltage of 2V - 0.4 V, in compatibility with CMOS. The estimated energy consumption of less than 10 fJ per programming event is comparable to biological synapses. The device is good candidate for analog in-memory computing in dense and large cross bar AI accelerator arrays power consumption is a big concern (N. Siannas et al., https://doi.org/10.1002/adfm.202311767).

Athanasios Dimoulas is Research Director at NCSR-DEMOKRITOS in Athens. After receiving his PhD, he served as post doc at the U. Groningen, CALTECH and U. Maryland College Park. He is founder and head of Epitaxy and Surface Science Lab (ESSL) of the Institute of Nanoscience and Nanotechnology since 1999. He has received an ERC advanced grant and several Marie Curie and FET grants. Dr. Dimoulas had a Chair of Excellence appointment at CEA and the U. Grenoble Alpes in years 2016-2018. He has a background in high mobility channels (e.g. Ge) for advanced CMOS and his current interests focus on Hafnia-based ferroelectric memristors for use in edge AI applications. He is currently participating in EU CL4 projects FIXIT and CONCEPT on ferroelectric neuromorphic devices. He has also been appointed as director of the project ARSYF of the Romanian Recovery and Resilience Plan for the development of Neuromorphic technologies.

Mott memristor-based future computing
Kyungmin Kim ~ KAIST

Mott memristor is a very intriguing device that exhibits electrical characteristics through the dynamic interaction of heat and current. Here, heat shows dynamic behavior in both temporal accumulations via heat capacity and spatial transportation via heat diffusion, enabling the coupling of memristor devices when arranged in arrays, which can be utilized in computing. Additionally, the thermal behavior of memristors inherently involves stochasticity, leading to probabilistic behavior. Such thermal coupling and stochastic behavior offer a solution to NP-hard problems that conventional computers find challenging to address. In this presentation, various computing devices using Mott memristors will be introduced, including TRNG, probabilistic computing, and thermal computing, and their future potential is discussed.

Professor Kyungmin Kim is an Associate Professor in the Department of Materials Science and Engineering at the Korea Advanced Institute of Science and Technology (KAIST) since 2017. He earned his B.S. degree in 2003 and his Ph.D. degree in 2008 from Seoul National University, Seoul, Korea. From 2011 to 2013, he worked at Samsung Electronics in Korea, and from 2014 to 2017, he worked at Hewlett Packard Labs of Hewlett Packard Enterprise in Palo Alto, California, USA. His research covers a wide range of areas related to next-generation semiconductor technology. This includes exploring new semiconductor materials and processing techniques, post-von Neumann computing technologies such as neuromorphic computing, reservoir computing, and probabilistic computing, as well as semiconductor packaging technology.

- **Spintronics with complex spin texture**
  Chanyong Hwang ~ KRISS

A magnetic skyrmion is a particle-like topological spin texture, where the forming nots are key parameters to hold its topology. Especially, it has drawn a lot of attention for its potential use in spintronic devices. From memory to logic devices, its manipulation (creation, deletion, movement) with pure electric external variables are most demanding. Recently we have shown several unique methods for the generation and manipulation of this magnetic skyrmion based on the detailed skyrmion formation process. With these methods, we can demonstrate several skyrmionic devices such as skyrmion racetrack memory, skyrmion transistor, and skyrmion neuromorphic device.

Chanyong Hwang received his BS in 1985 from the physics department of Seoul National University. He went to the graduate school of the physics department of the University of Wisconsin at Madison, and obtained his PhD in 1990. After his degree, he joined the Korea research institute of Standards and Science. Now, he is leading the quantum spin team at Quantum Technology Institute. His research covers several areas such as spintronics, spin dynamics, quantum spintronics, 2D materials, and quantum materials.

YOUNG RESEARCHERS' SESSION

Chair: Jyrki Kiihamäki (part 1) / Valeria Kilchytska (part 2)

- **Chair of the session**
  Valeria Kilchytska ~ UCLouvain

Dr. Valeria Kilchytska is Senior Researcher, Logistic Director assuring scientific lead of the Welcome Electrical Characterization Platform at UCLouvain. She received PhD degree in semiconductor and dielectric physics from Kyiv University, Ukraine in 1997. She joined UCLouvain in 2002. Her research interest are characterization, simulation and modelling of advanced devices with a focus on wide frequency band, noise, performance assessment as well as cryogenic, high-temperature and radiation behavior. She has authored or co-authored >300 scientific papers and conference contributions. She is a reviewer for numerous scientific journals and a TPC member of several conferences. She is a Deputy Director of SINANO Institute.

- **GaN Technology for Power Electronics Application**
  Urmimala Chatterjee ~ imec

GaN technology can drive the high frequency operation for power circuits beyond today's limit that facilitates to build a smaller, lighter and more cost-effective solution compared to its other silicon alternatives. This talk will give you a brief of IMEC's different GaN technology platforms for the discrete power devices. Besides this will also cover the aspects of monolithic integration in this technology. In order to fully utilize the fast-switching capability of GaN technology, monolithically integrated GaN power IC is beneficial. For instance, integration helps to reduce the gate ringing, switching loss which in-turn makes a smooth highly efficient circuit.

Dr. Urmimala Chatterjee received her bachelor's degree on Electronics Engineering from West Bengal, India and master's degree from NTU-TUM, Munich, Germany. After that she pursued her PhD in ESAT, KU Leuven on smart power converter design for Photovoltaic application. Before joining IMEC, she works few years in Thales, Belgium on discrete circuit design for satellite and space application. Presently in IMEC she is working in GaN power electronics, mainly responsible for GaN IC activities and device design.

Artificial Neuron Devices Fully Compatible with CMOS Technology for Neural Processing and Sensing in Neuromorphic Hardware

Joon-Kyu Han ~ Sogang University

Neuromorphic hardware, inspired by the structure and principles of the human brain, can significantly reduce the energy consumption of AI functions by eliminating von Neumann bottlenecks. In particular, a spiking neural network (SNN) has received considerable attention due to its remarkable energy efficiency.[1] This presentation introduces the fully CMOS compatible single transistor-based artificial neuron devices for SNN. They are co-integrated with artificial synaptic devices in both 2-dimensional and 3-dimensional structures to construct a complete neuromorphic system. Additionally, artificial sensory neuron devices, which simultaneously perform sensor and neuromorphic functions are introduced, greatly reducing energy consumption in sensor systems by in-sensor computing.

Dr. Joon-Kyu Han is Assistant Professor in System Semiconductor Engineering and Department of Electronic Engineering at Sogang University. His research focuses on (1) neuromorphic device & system and (2) nano CMOS for logic & memory. He graduated Summa Cum Laude from Korea Advanced Science and Technology (KAIST) in 2017 with a Bachelor of Science in Electrical Engineering. He obtained his Master's and Ph.D. in Electrical Engineering at the KAIST in 2019 and 2023, respectively. He received Ph.D. Dissertation Award at KAIST College of Engineering. He was a postdoctoral researcher at Seoul National University and visiting scholar at Harvard University from 2023 to 2024. He is the author/co-author of 68 peer-reviewed articles including Science Advances, Advanced Materials, Advanced Science, Advanced Functional Materials, Nano Letters, etc. He received Excellent Paper Awards from Samsung Electronics in 2021 and 2022.

Design ASIC architectures for generic, self-learning and reliable neuromorphic AI accelerators

Martin Andraud ~ UCLouvain

Developing the next generation of AI accelerators faces several challenges, among them the explosion of model sizes, particularly deep neural networks (DNNs) and transformers. Although we develop more efficient hardware accelerators, specifically neuromorphic or in-memory computing architectures, they chase always more massive computational costs. To tackle this, I propose the design of more generic and reliable ASIC architectures. Generic, because a single AISC architecture can accelerate various emerging and less computationally intensive models (compressed or sparse DNNs, probabilistic models, etc.), and reliable, because the accelerator contains various self-calibration and self-learning abilities to function optimally across multiple tasks and operating conditions.

Martin Andraud is currently an assistant professor in UCLouvain, Belgium, and a visiting professor in Aalto University, Finland. He obtained his PhD in 2016 from Grenoble Alpes University, France, in 2016, working on AI-based self-calibration of analog and RF circuits. He then did his postdoctoral studies between 2016 and 2019 successively with TU Eindhoven, The Netherlands, and KU Leuven, Belgium, working on embedded intelligence for heavily resource-constrained sensor nodes. From 2019 to 2023, he joined Aalto University, Finland, where he built his research team focusing on AI accelerators and intelligence for edge devices. He moved to UCLouvain in 2024 to extend his activities. His research interests are at the interface between hardware and software for AI, covering the development of novel embedded AI applications (using probabilistic models) and the design of generic and efficient ASICs for AI acceleration (digital, mixed-signal in-memory computing, time-based).

Tailoring memristors through metallization on amorphous materials

Hanwool Yeon ~ GIST

The origin of memristive switching lies in the dynamic modulation of the conduction channel in nanometer-thick resistive mediums, and promising properties of memristors (e.g., analog switching) have been reported over 15 years. However, it should be highlighted that a single memristor, exhibiting all the promising performances simultaneously, does not exist due to a paradox in the switching dynamics. To address the performance dilemma and produce application-tailored memristive devices, material innovations for engineering the conduction channel are indispensable. In a 10-minute presentation, I will introduce my group's strategies to engineer the switching channel through metallization technologies, thereby addressing the dilemmas.

Professor Hanwool Yeon is an assistant professor at Gwangju Institute of Science and Technology (GIST) in the School of Materials Science and Engineering. He received B.S., M.S. and Ph.D. from Seoul National university, all in Materials Science and Engineering. He is a recipient of the 14th POSCO Science Fellowship. His group is developing a unique metallization technology termed SMART metallization for the advancement of semiconductor technologies, including in-memory computing, heterogeneous integration, and edge devices.

Area-selective deposition and atomic layer etching as enabling technologies for the fabrication of 3-dimensional nanodevices

Adrie Mackus ~ Eindhoven University of Technology

With the advancement of logic and memory relying on the vertical stacking of devices, atomic layer deposition (ALD) and atomic layer etching (ALE) are essential techniques for the processing of materials on such 3-dimensional devices structures. To eliminate alignment issues when patterning the 100+ layers of future devices, there is a need for self-aligned fabrication approaches involving novel area-selective ALD processes. In this contribution, applications of selective ALD and ALE processes will be discussed, as well as several strategies for achieving selectivity in deposition and etching.

Adrie Mackus (1985) is an associate professor in Applied Physics at Eindhoven University of Technology, TU/e. He earned his M.Sc. and Ph.D. degrees (both with highest honors) in Applied Physics from TU/e in 2009 and 2013, respectively. Adrie worked as a postdoc at the department of Chemical Engineering at Stanford University in 2014-2016. His current research encompasses thin film deposition and etching for applications in nanoelectronics, with a focus on selective processing for bottom-up fabrication. Adrie chaired the 2nd Area Selective Deposition workshop (ASD2017) in Eindhoven in 2017. In 2020 he was awarded a Starting Grant from the European Research Council (ERC) based on a proposal entitled "*From the bottom-up: a physico-chemical approach towards 3D nanostructures with atomic-scale control*".

- **Emerging Semiconductors Meet Novel Capabilities: Multi-valued Logic, Security, and Hazard Monitoring**
  Hocheon Yoo ~ Gachon University

Since its proposal by Dr. Dawon Kahng and Dr. Mohamed M. Atalla in 1959, the metal-oxide-semiconductor field-effect transistor (MOSFET) has played a crucial role in modern electronic devices. With over 1.36 trillion MOSFETs manufactured since its commercialization in 1960, it has found widespread use in processors, image sensors, memories, and various other applications. However, the scaling of MOSFETs is currently encountering physical limitations, leading to challenges such as low process yields (around 70%) and problems arising from short-channel effects. As a result, there is an increasing demand for next-generation semiconductor devices. In this talk, we present an approach called "Material-Device-Application Co-Consideration" for the development of new applications. This approach involves bottom-up processes that leverage emerging materials. Specifically, we will focus on our recent efforts in the development of multi-valued logic (MVL) by controlling negative differential transconductance (NDT). We will also discuss the utilization of atomically-thin graphene and self-assembled monolayers in the creation of physically unclonable functions (PUFs) for information security. Furthermore, we will explore deep ultraviolet (DUV) region (280 nm – 200 nm)-based emerging applications: (i) partial discharge detection, (ii) flame sensing for fire monitoring and (iii) blood component identification. These topics will be covered in-depth during the presentation.

Hocheon Yoo received the Ph.D. degree from the Department of IT Engineering, Pohang University of Science and Technology (POSTECH), Pohang, South Korea, in 2018. In 2019, he was a Postdoctoral Researcher with Northwestern University Materials Research Center, Evanston, IL, USA. He is currently an Associate Professor of electronic engineering with Gachon University, Seongnam, Republic of Korea. His current research interests include new semiconductor materials, neuromorphic devices, thin-film circuits, and sensors for healthcare and biomedical applications.

- **Two-dimensional materials for next generation non-volatile memories**
  Jose Hugo Garcia ~ Institut Català de Nanociència i Nanotecnologia

The increasing global demand for powerful and efficient electronic devices promoted semiconducting industry and research as a critical sector worldwide. Despite the astonishing improvement of nanofabrication control engineering of silicon-based devices, many other candidates are scrutinized for novel semiconducting applications, such as terahertz emission, ultralow power spintronic systems and, and neuromorphic devices. In this presentation, I will introduce 2D materials as interesting platform for semiconducting devices and express their relevance in the field of spin-orbit torque memories. Specifically, I will present how one can exploit

crystalline interfaces to achieve superior memories compared to traditional STT-RAM technologies.

José H. Garcia, a Senior Researcher at ICN2, brings a decade of expertise in theoretical simulations of quantum electronic devices using low-symmetry materials. He currently leads the ERC Starting Grant project AI4SPIN, focusing on unlocking the potential of electronic structures databases through advanced quantum transport calculations, heuristic optimization, and AI to develop next-generation memories. Garcia is the principal developer of the LINQT code on the LSQUANT platform, enabling linear-scaling quantum transport across various models. His work extends to creating algorithms now integral to other quantum transport software. Garcia has managed research teams and contributed significantly as PI and Co-PI on multiple projects.

Electronic Eyes based on Flexible and Neuromorphic Optoelectronics
Changsoon Choi ~ KIST

Machine vision technologies enable mobile and humanoid robots to detect and identify surrounding objects. To achieve error-free execution of such tasks, mobile robots necessitate high-performance imaging and data processing capabilities, especially in compact design and energy-efficient architecture. Here, we introduce electronic eyes featuring high-performance imaging and data processing capabilities. First, we developed the bio-inspired cameras that emulate the structural features of biological eyes, offering a compact form factor ideal for high-mobility robotics. Second, we introduce machine vision sensors capable of performing image signal processing at the sensory level via in-sensor computing techniques, without resource-intensive computations, thereby enhancing data processing efficiency.

Changsoon Choi received his B. S. degree (2012) from the Department of Material Science and Engineering at the Seoul National University and his M. S. degree (2014) and his Ph. D. degree (2020) from the School of Chemical and Biological Engineering at the Seoul National University. He worked in John A. Paulson School of Engineering and Applied Sciences, Harvard University as a postdoctoral research associate (2020-2021). He is currently a senior research scientist of Center for Opto-Electronic Materials and Devices, Post-silicon Semiconductor Institute (PSI), Korea Institute of Science and Technology (KIST). His research interests include bio-inspired optoelectronics and in-sensor computing for machine vision applications.

2D Materials for Neuromorphic Computing
Jimin Lee ~ RWTH Aachen University

The talk will start with the potential impact of two-dimensional (2D) materials across various fields of future microelectronics, such as the continuation of “device scaling” (i.e. Moore’s Law), the enhancement of functionality, and the implementation of neuromorphic computing [1]. Secondly, I will give an overview of recently initiated large-scale research projects funded by German government for the development and utilization of neuromorphic hardware for artificial intelligence. Finally, I will present recent experiments and results on 2D material-based neuromorphic devices [2]-[5]. This work has been funded by the German Federal Ministry of Education and Research (BMBF) through NeuroSys (03ZU1106AA) and NEUROTEC II (16ME0399/16ME0400).

Jimin Lee is currently a Ph.D. student in Electrical Engineering at RWTH Aachen University. She received her B.Sc. in Materials Science and Engineering from Yonsei University in 2012. She then worked as a materials process engineer at Samsung Electronics Co. LTD from 2012 to 2018. She received her M.Sc. in Materials Science from RWTH Aachen University, Aachen, Germany in 2021. Her current research interests focus on the fabrication, characterization, and mechanism of the 2D material-based memristive devices for neuromorphic computing applications.

- **Topotactic engineering for oxide quantum materials**
  Woojin Kim ~ Pusan National University

In this talk, I will present the latest advances in quasi-two-dimensional oxide quantum materials synthesized through topotactic reduction reactions in thin film heterostructures [1,2]. These materials can enter diverse quantum states, such as Jahn-Teller ordering and unconventional superconductivity, depending on their d-electron filling states. Given the tunability of quantum phenomena, topotactic engineering offers a promising material platform that could contribute to the designing of innovative quantum devices for future computation and information technology.

Woojin Kim received his Ph.D. degree from the Department of Physics, Seoul National University, Korea in 2019. After completing his Ph.D., Woojin Kim started a four-year postdoctoral fellowship at the Applied Physics Department at Stanford University, USA. He is currently an Assistant Professor at the School of Materials Science and Engineering, Pusan National University. His research interests include exotic and emergent phenomena in transition metal oxides (magnetism, metal-insulator transition, superconductivity, and topological phenomena); Atomic scale synthesis of heterostructure of quantum materials; Novel devices and energy materials research on freestanding oxide heterostructure.

POSTERS SESSION

- **Powering the Future: High-Energy Efficiency Nanoelectronics for Advanced Neuromorphic Computing**
  Qing-Tai Zhao ~ Forschungszentrum Jülich

We focus on CMOS devices for neuromorphic computing, including ferroelectric and FDSOI nanometer transistors as artificial synapses/neurons. Ferroelectric devices are demonstrated high potential as artificial synapses and neurons. Furthermore, we develop a capacitorless SOI-FETs memory unit, functioning down to 4 K with high energy efficiency, to facilitate neuromorphic-quantum computing applications.

Qing-Tai Zhao completed his PhD in Physics at Peking University, China, in 1994, and subsequently joined the Institute of Microelectronics at the same university, where he focused on research of SOI materials and devices. In 1997, he was awarded as a Humboldt Research Fellow and started his research in Forschungszentrum Juelich, Germany, where he currently leads a group on the research of nanoelectronic devices. His primary research focuses on Si-Ge-Sn based high mobility devices and technology, FDSOI and nanowire devices,

ferroelectric transistors and 1T-DRAM devices for neuromorphic computing and cryogenic electronics for quantum computing.

- **MoS2 growth and device technology; towards integration with multiplexed graphene sensors arrays**
  Laura Remacha Gelabertó ~ Institut Català de Nanociència i Nanotecnologia

2D semiconductors are of paramount importance for *More Moore* and *More-than-Moore* applications. This poster presents an overview of the technology challenges for developing efficient and reliable MoS_2 Field Effect Transistors (FETs), towards the monolithic integration of MoS_2 FETs with multiplexed graphene sensors on flexible probes for biomedical applications.

Laura Remacha Gelabertó obtained a Bachelor's and Master's degree in Nanoscience from Universitat Autònoma de Barcelona in 2022 and 2023, respectively.
Bachelor's and Master's degree thesis at the Insitut Català de Nanociència i Nanotecnologia supervised by Prof. Jose Antonio Garrido and Dra. Elena del Corro. The Bachelor's focused on the metal-organic chemical vapour deposition of MoS_2. The Master's on the device technology and microfabrication at wafer scale.
JAE intro ICU of 7 months in 2022 at Institut de Ciència de Materials de Barcelona with the Nanostructured Materials for Optoelectronics and Energy Harvesting group, investigating the self-assembly of gold nanoparticles and nanostructuration of polymers.

- **Neuromorphic Computing: Latest activities at ELD and AMO**
  Jan van den Hurk ~ RWTH Aachen University

The chair of Electronic Devices (ELD) at RWTH Aachen University and AMO GmbH work together at the forefront of neuromorphic computing to provide next-generation hardware for artificial intelligence. Both organizations are active in the Cluster4Future NeuroSys and the joint project NEUROTEC to bring neuro-inspired computing hardware to life.

Dr.-Ing. Jan van den Hurk is the deputy head of the Chair of Electronic Devices (ELD) at RWTH Aachen University. He is an alumnus of RWTH Aachen University, University College Cork and AMO GmbH with a strong background in microelectronic engineering and material science. During his doctorate, he started to investigate memristive systems under the direction of Prof. Ilia Valov and Prof. Rainer Waser. As a lead process engineer and lab manager at AIXTRON SE he gained valuable experience with South Korea's semiconductor industry. In spring 2023 he joined Prof. Max Lemme's chair.

- **Smart Sensors and Systems as Enabling Technologies for Climate-Smart Agriculture**
  Danilo Demarchi ~ Politecnico di Torino

Smart Sensors and Systems for Climate-Smart Agriculture are enabling technologies for a more controlled quality production and optimisation of the resources, improving food quality and environment respect. They bring the functionalities for eco-friendly, circular and practical solutions, generating the needed information and control along the whole food value chain.

Danilo Demarchi is full Professor at Politecnico di Torino, Department of Electronics and Telecommunications. Visiting Professor at EPFL Lausanne (2019) and at Tel Aviv University (2018-2021). Visiting Scientist (2018) at MIT and Harvard Medical School. Author and co-author of 5 patents and more than 350 scientific publications in international journals and peer-reviewed conference proceedings. Leading the

eLiONS (electronic Life-Oriented iNtelligent Systems) Laboratory of Politecnico di Torino and coordinating the Italian Institute of Technology Microelectronics group at Politecnico di Torino (IIT@DET). Working on Micro&Nano Electronics, Smart Systems and IoTs for the AgriFood Value Chain and for BioMedical Devices.

- **Patterned Multi-Wall Nanosheet FETs for Aggressive Scaling Beyond Forksheet FETs: Zero Gate Extension with Minimal Gate Cut Width**
  Sanguk Lee ~ POSTECH

Power-performance-area (PPA) improvement is a major challenge for logic devices. We propose patterned multi-wall nanosheet FETs (MW-NSFETs) for advanced nodes beyond forksheet FETs (FSFETs). It features gate-all-around (GAA) channels, wrap-around contact (WAC), and self-aligned gate edges with minimal gate expansion and gate cut margins.

Sanguk Lee received a B.S. degree in electrical engineering from Kyungpook National University, Republic of Korea, in 2021 and received an M.S. degree from Pohang University of Science and Technology (POSTECH) in 2023. He is currently pursuing a Ph.D. degree in electrical engineering from POSTECH. His research interests include technology computer-aided design (TCAD) simulation of logic devices (FinFETs, nanosheet FETs, forksheet FETs, vertical-transport FETs, and CFETs); advanced node device benchmarking; design technology co-optimization (DTCO).

- **Heterogenous integration of TMD-based memristors and memtransistors with Si CMOS for neuromorphic computing**
  Francisco Gamiz ~ UGR

Two-dimensional (2D) materials offer promising prospects beyond the conventional von Neumann computing architecture paradigm. We suggest implementing and demonstrating the functionality of neuromorphic systems using memristive devices—both memristors and memtransistors—constructed from 2D materials. These devices would be integrated on the back-end of Si CMOS control/driver circuits.

Francisco Gamiz (ORCID 0000-0002-5072-7924) graduated with Honors in Physics (National Award of the Spanish Ministry of Education) in 1991 at UGR and obtained the Ph.D. degree (Extraordinary Award) in 1994. Prof. Gamiz coordinated the European projects EUROSOI and EUROSOI+ in EU-FP6 & FP7. The outcome of EUROSOI projects is the EUROSOI-ULIS conference series, a forum for discussing nanoelectronic technology since 2005 in Europe. Also, in 2004, he participated in the SINANO Network of Excellence, the precursor of the current SINANO Institute, bringing together the most important actors in European Nanoelectronics. Prof. Gamiz is member of the Governing Board of SINANO. He has participated in European industrial projects with CATRENE or ECSEL labels: REACHING-22, PLACES2BE, and H2020-WAYTOGO-FAST. In 2015, Prof. Gamiz coordinated the EU-project REMINDER, with the participation of Korean researchers. Since November 2021, Prof. Gamiz has been the Head of the Research Center for Information and Communication Technologies, CITIC-UGR, and Head of the PERTE-Chip University Chair at UGR. Prof. Gamiz is a member of the Science Academy of Granada.

- **Encapsulation and protection strategies for graphene-based solution-gated field-effect transistors towards high performing neural recording**
  Anna Graf ~ ICN2

Graphene offers the potential for miniaturization and integration of neural interfaces into advanced biomedical devices. By modifying substrate interface and optimizing microfabrication processes, this work aims at enabling high-fidelity neural recordings using graphene-based field-effect transistors, with application in brain-computer interfaces for monitoring and treatment of neurological disorders.

Anna Graf is a doctoral student of Jose A. Garrido's Advanced Electronics Materials and Devices group at ICN2 working in the field of graphene-based solution-gated field-effect transistors technology (gSGFET) for biomedical applications, within La Caixa INPhINIT fellowship. She holds BEng and MEng degrees in Chemistry and Materials Engineering from WUST in Poland, and an MSc in MMRES from BIST and UPF in Spain, with the research focused on biomaterials for photonics and graphene oxide-based electrodes, respectively. She completed research stays at the University of Oulu, exploring new materials for efficient photocatalysis, and at ICIQ, investigating spin-crossover hybrids for molecular switches.

Metal oxide-based structures for novel computing paradigm concepts
Robert Mroczinski ~ Warsaw University of Technology

This work summarizes the recent results devoted to the materials engineering, optimization, and subtle characterization of structures and devices based on ultrathin oxide materials. Those materials fabricated employing low-temperature methods show great potential in new concepts for logic and memory devices, e.g., neuromorphic or brain-inspired computing, as possible candidates for emulating artificial synapses and constructing artificial neural networks.

A graduate of the Faculty of Electronics and Information Technologies of the Warsaw University of Technology (WUT). His research concerns technology, characterization, and diagnostics of materials, structures, and semiconductor devices. He participated in several research internships, including at the University of Michigan (USA), Brandenburg University of Technology (Germany), Fraunhofer MOEZ/IZI (Germany), Dresden University of Technology (Germany), IBM Thomas J. Watson Center and Sommers (USA). He also participated in a didactics internship in the course of the Ministry of Science and Education programme "Master of Didactics" at Ghent University (Belgium), as well as "Leaders in University Management" at University of Munich (Germany). Moreover, he spent a month as Visiting Professor at KyungPook National University (South Korea). Since 2021, he has been the head of the Microelectronic and Nanoelectronic Devices Division at WUT, while in June 2023 elected to the Governing Board of the SINANO Institute.

Advancements in Neuromorphic Computing Using Silicon Nitride Memristors for IoT and Security
Panagiotis Dimitrakis ~ NCSR Demokritos

Here, we demonstrate our latest advances in Silicon Nitride (SiN) memristors for RRAMs, neuromorphic and IoT edge computing. The usefulness of our CMOS-compatible SiN device technology in unconventional computing paradigms is disclosed. Novel security and multi-state logic circuits are proposed. Simulations verify performance and power optimization prospects impacting advancements in IoT hardware.

Dr. Panagiotis Dimitrakis, a graduate of the University of Athens (BSc 1995, MSc 1998), specializes in nonvolatile memories (PhD, 2006). With extensive experience in process design and device fabrication, he contributed to various national, bilateral and European projects integrating new materials like 2D with CMOS technology. Presently, he leads projects developing memristive devices for neuromorphic and quantum computing, and works on heterogeneous integration GaN RF circuits on Si for 5G. He is Director of Research at NCSR "Demokritos" and senior member of IEEE. A prolific author and editor, Dr. Dimitrakis's research focuses on novel memory devices, and nanoelectronics enriching the field since 2017.

High Performance Chiplet-based PIM AI Semiconductor
Chung Jaehoon / Choi Jaewoong, ETRI

The chiplet-based design is a viable solution for designing an AI processor since it provides much higher performance with lower cost, compared to IP-based design. We have implemented a chip with a chiplet architecture that integrates 2 NPUs and 8 HBM3s for petaflops-scale performance.

Jaehoon Chung received his B.S. and M.S. degree in computer engineering from Korea University, Seoul, Rep. of Korea in 2015 and 2017, respectively. Since 2017, he has been with Electronics and Telecommunications Research Institute (ETRI), Daejeon, Rep. of Korea, and is currently a senior member of the research staff. His current research interests include Processing-in-Memory architecture, Artificial Intelligence (AI) processor design, and low-power design.

Jaewoong Choi received his B.S. in electrical engineering from Hanyang University, Seoul, Rep. of Korea in 2017, and the M.S. degree in electronic engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejeon, Rep. of Korea in 2019. Since 2021, he has been with Electronics and Telecommunications Research Institute (ETRI), Daejeon, Rep. of Korea, an is currently a member of the research staff. His current research interests include structure of neural networks accelerator and digital signal processing.

Smart systems integration for biomedical and environmental applications
Bogdan Firtat, IMT Bucharest

This paper presents innovative ideas and technology approaches for integrating smart systems in two showcases. 1 - Implantable interfaces to dually link peripheral nerves with neural-based prostheses for control and feedback; 2 – Portable platform for air monitoring, with self-powered ultra-sensitive sensors array and AI-based detection algorithms.

Bogdan Firtat is electronics engineer with a PhD in Microsystems. He has 24 years of experience in semiconductors and micro/nano systems design, simulation and modelling for mechanical, chemical and biological microsensors, micro and nanofluidic devices development and integration. Bogdan has a broad experience as a project and program manager, leading several KDT-JU / CHIPS-JU projects, as well as various European R&I consortia.

Advanced computing and functionalities in CROMA lab
Alessandro Cresti, CNRS

We illustrate the main activities and interests of CROMA lab in the domain of advanced computing and functionalities. Our focus is on transistors and memories, multiphysics transducers, optoelectronic devices and photonics with applications in low-power devices, energy harvesters, biology and health, and neuromorphic computing.

Alessandro Cresti received his doctorate in physics at the University of Pisa, Italy, in 2006. Since 2011 he has been a researcher CNRS at CROMA lab, France. He developed full-quantum tools for simulating transport in nanostructures, with particular focus on both basic and applied aspects of 2D materials.

Full-Stack Neuromorphic Computing in Delft
Moritz Fieback, TUDelft

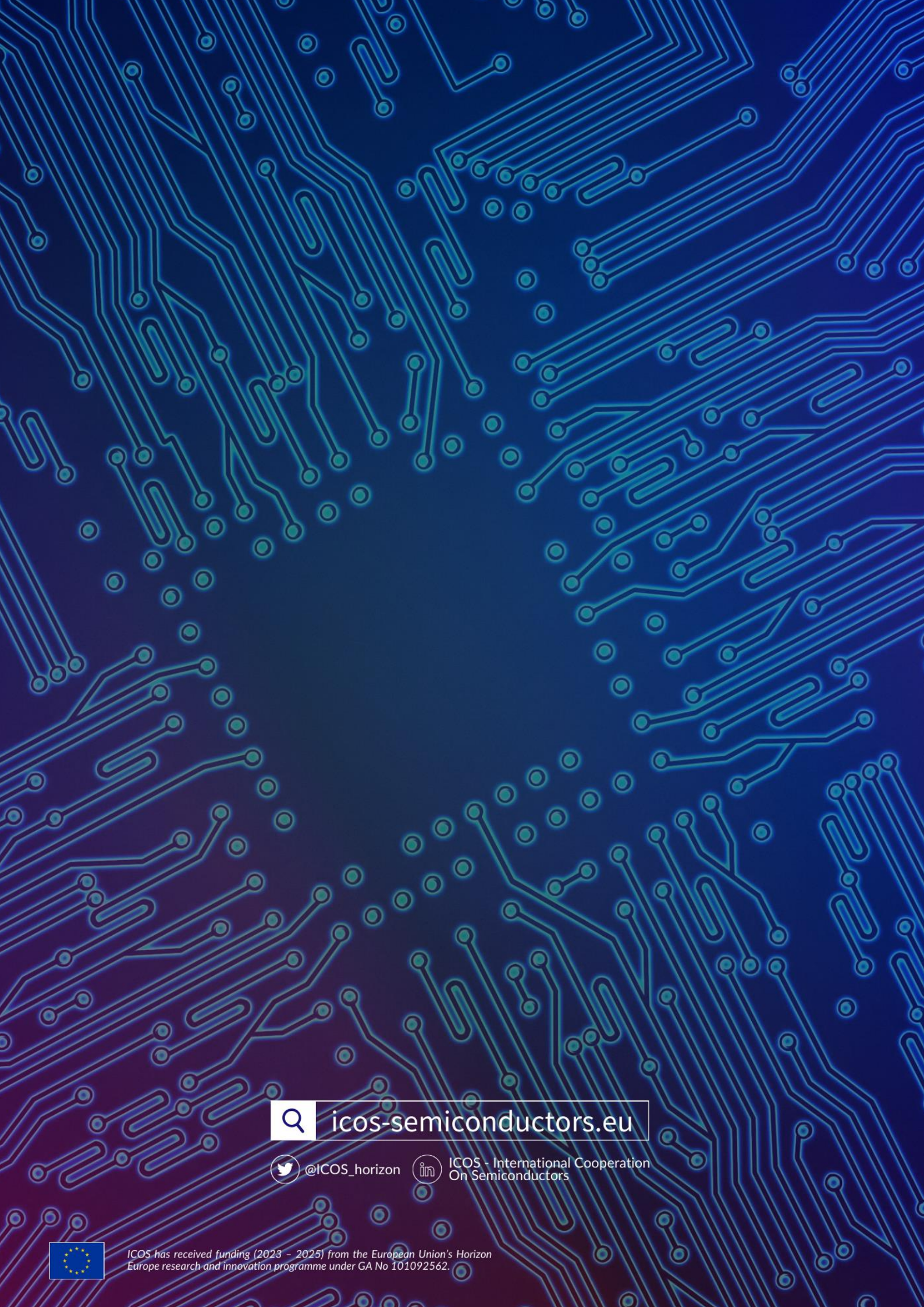
Computer Engineering in Delft targets the invention, design, prototyping and demonstration of disruptive computing, targeting a broad range of energy-constrained applications, including AI. To maximise the computational efficiency of our computing engines, we address the entire design stack from devices, via circuits and architectures, to applications, while also considering dependability.

Moritz Fieback received his PhD degree from Delft University of Technology in the Netherlands in 2022. Currently, he is working as an assistant professor in the same university. His research interests include testing of AI accelerators, focussing on device and defect modeling of emerging memories. He has co-authored over 40 articles and won 3 best paper awards.

Neuromorphic sensing and computing at INL
Bruno Romeira, INL

Advances in power-efficient neuromorphic nanodevices and its advanced integration are required for edge computing nanosystems. INL develops microelectromechanical, spintronic, nanophotonic, and nanophononic systems for neuromorphic sensing and computing applications. Here, we show examples using (i) nanophotonic sensory oscillator neurons, (ii) synapses and neurons based on spintronic nano-oscillators, and iii) heterogeneous integration with CMOS.

Bruno Romeira received his PhD in physics at the University of the Algarve (Portugal), jointly with the University of Glasgow (UK) and the University of Seville (Spain). He then held a postdoc at the University of Ottawa (Canada), and a Marie Skłodowska-Curie Fellowship at Eindhoven University of Technology (The Netherlands). He is currently a staff researcher at the International Iberian Nanotechnology Laboratory (Portugal).
His interests include semiconductor physics, quantum electronics, nanophotonics, and neuromorphic devices. He has participated in several European projects in the neuromorphic field, including the H2020-FET-OPEN project "ChipAI" (Coordinator, 2019-2022) and the Horizon Europe project "InsectNeuroNano" (PI, 2023-).



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