Patterned Multi-Wall Nanosheet FETs for Aggressive Scaling: Zero Gate Extension with Minimal Gate Cut Width

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I. Motivation

- Forksheet FETs (FSFETs) allow for aggressive scaling of cell height by introducing the dielectric walls between the N/P-type devices.
- However, their electrical performance is lower than that of NSFETs due to one side of the channel and S/D inevitably interfacing with the wall.
- Additionally, one of the gate edges that is not aligned with the wall still requires sufficient gate cut (GC) and gate extension (GE) margins.
- We propose patterned multi-wall NSFETs (MW-NSFETs) featuring 1) gate-all-around (GAA) channel, 2) wrap-around contact (WAC), 3) self-aligned gate edges with minimal GC, and 4) confined S/D.

II. Simulation Design and Methodology

- The MW-NSFETs were thoroughly analyzed using Synopsys TCAD.

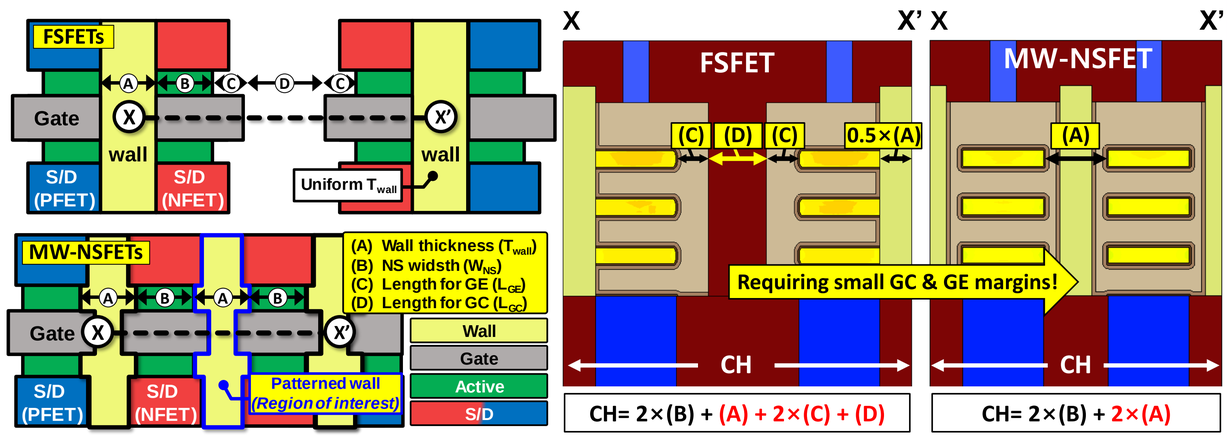

Figure 1. (left) The schematic comparison between the FSFETs and MW-NSFETs. **(right)** Cross-sectional view along the X-X' cut line of MW-NSFETs and FSFETs.

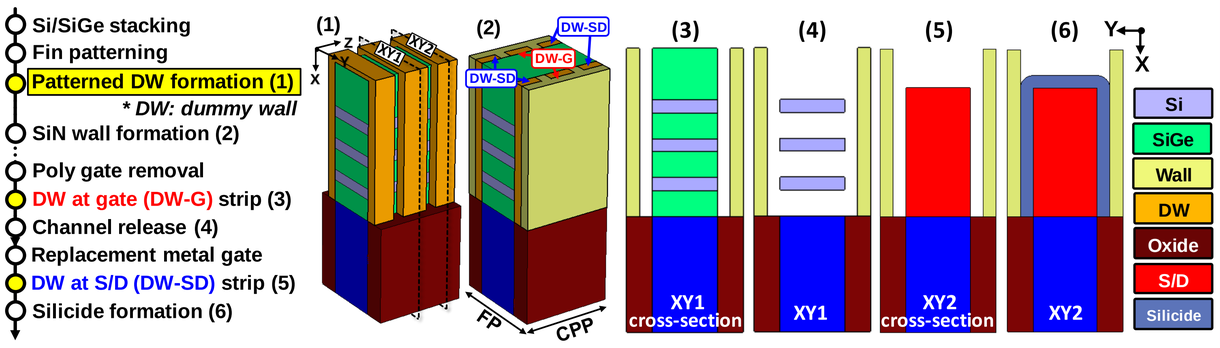

Figure 2. Process flow of MW-NSFETs, and cross-sectional view of main process (1)-(6).

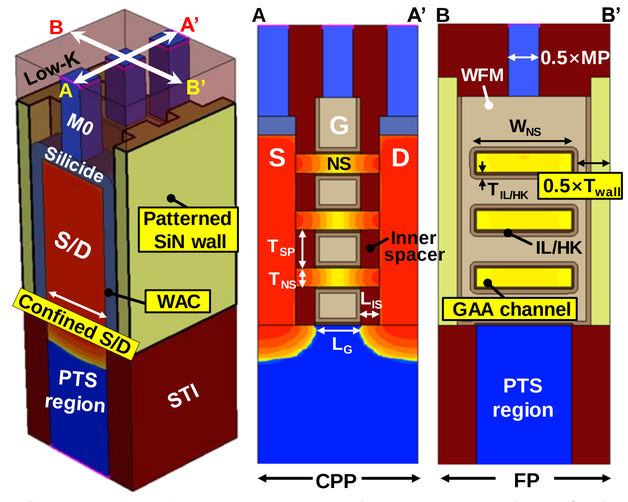

Table 1. Geometric parameters for MW-NSFETs

Parameters	Values	Parameters	Values
Contact poly pitch (CPP)	42 nm	Spacing layer thickness (T_{SP})	10 nm
Fin pitch (FP) MW-NS/FS	45/54 nm	Inner spacer length (L_{IS})	5 nm
Metal pitch (MP)	16 nm	IL/HK thickness (T_{IL}/T_{HK})	0.6/1.1 nm
Gate length (L_G)	12 nm	S/D doping	5×10^{20} cm^{-3}
NS width (W_{NS})	25 nm	PTS doping	2×10^{18} cm^{-3}
NS thickness (T_{NS})	5 nm	Gate cut length (L_{GC})	18 nm
Wall thickness (T_{wall})	20 nm	Gate extension length (L_{GE})	10 nm

Figure 3. 3D structure and cross-sectional view (A-A', and B-B') of MW-NSFETs.

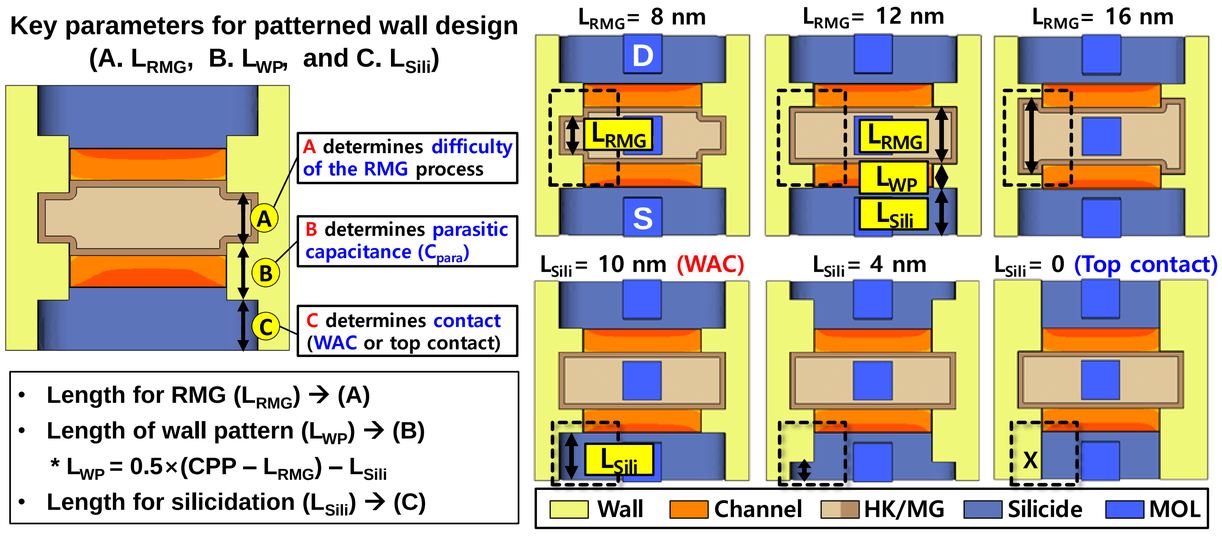

Figure 4. (left) Key factors for patterned wall. **(right)** Patterned wall according to L_{RMG} & L_{Sili}.

III. Results and Discussion

- A. Optimized wall patterns considering DC/AC characteristics

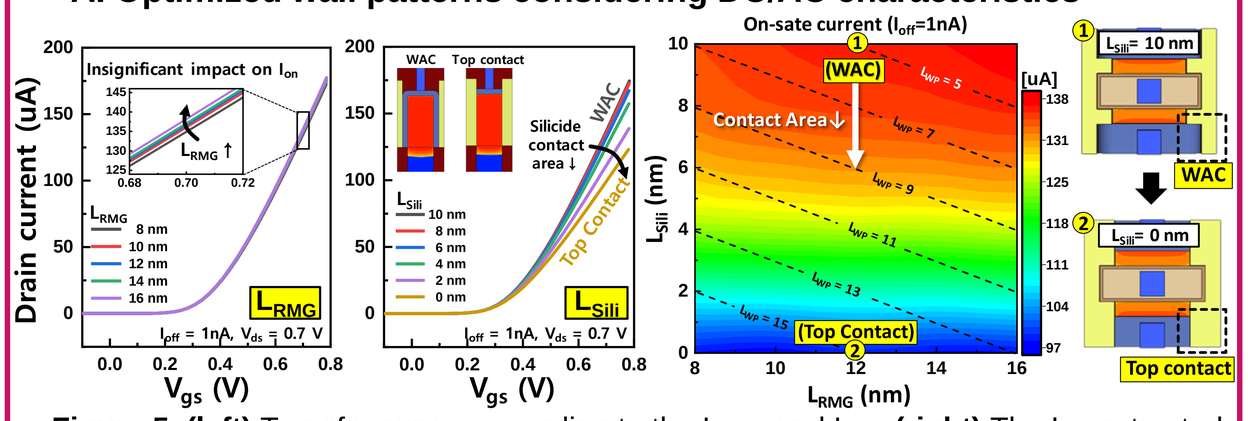

Figure 5. (left) Transfer curves according to the L_{RMG} and L_{Sili}. **(right)** The I_{on}, extracted at V_{gs}=V_{ds}=0.7 V, for different wall patterns at the same I_{off} (=1 nA).

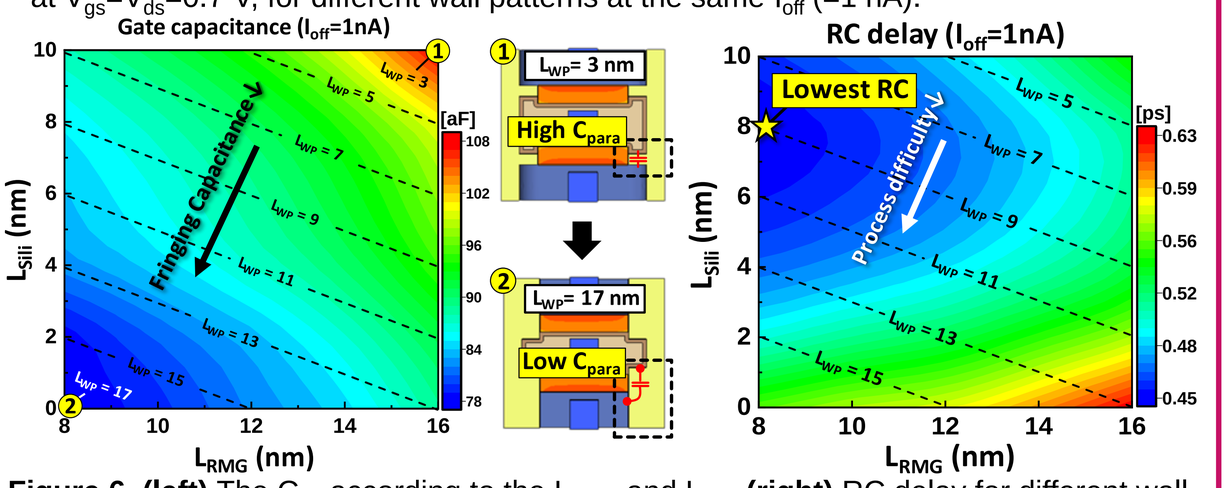

Figure 6. (left) The C_{gg} according to the L_{RMG} and L_{Sili}. **(right)** RC delay for different wall patterns. The lowest RC delay was observed when L_{RMG} = L_{Sili} = 8 nm, and L_{WP} = 9 nm.

- B. DC/AC performance conparison of FSFETs and MW-NSFETs

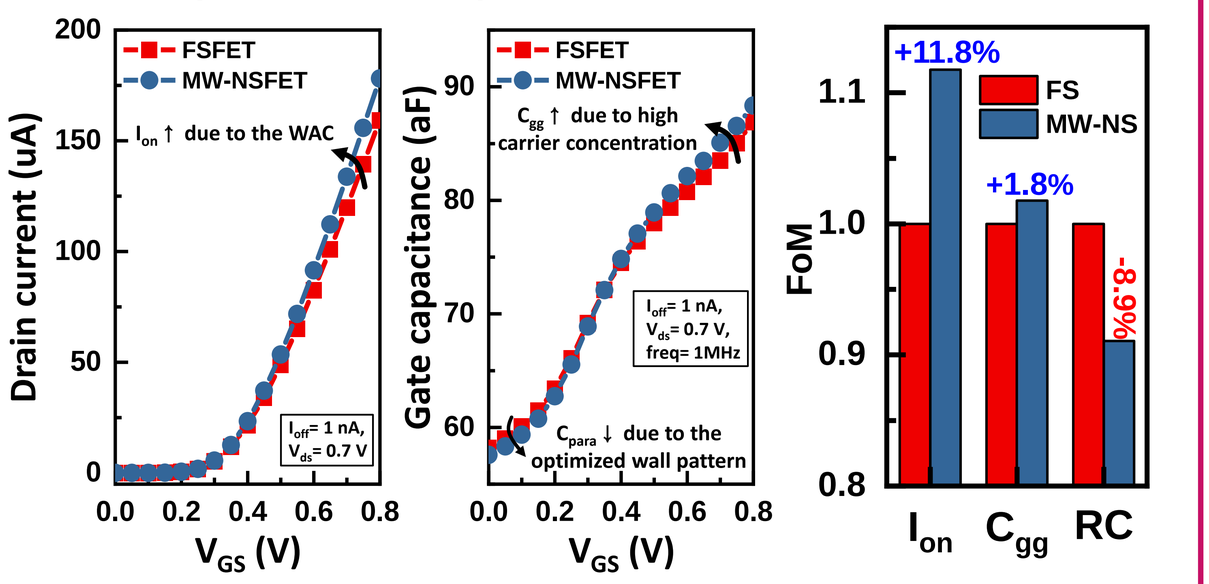

Figure 7. (left) Drain current and C_{gg} to the V_{gs} for MW-NSFETs and FSFETs. **(right)** Normalized FoM (I_{on}, C_{gg}, and RC delay) between FSFETs and MW-NSFETs.

- C. Impact of wall mask misalignment on RC delay

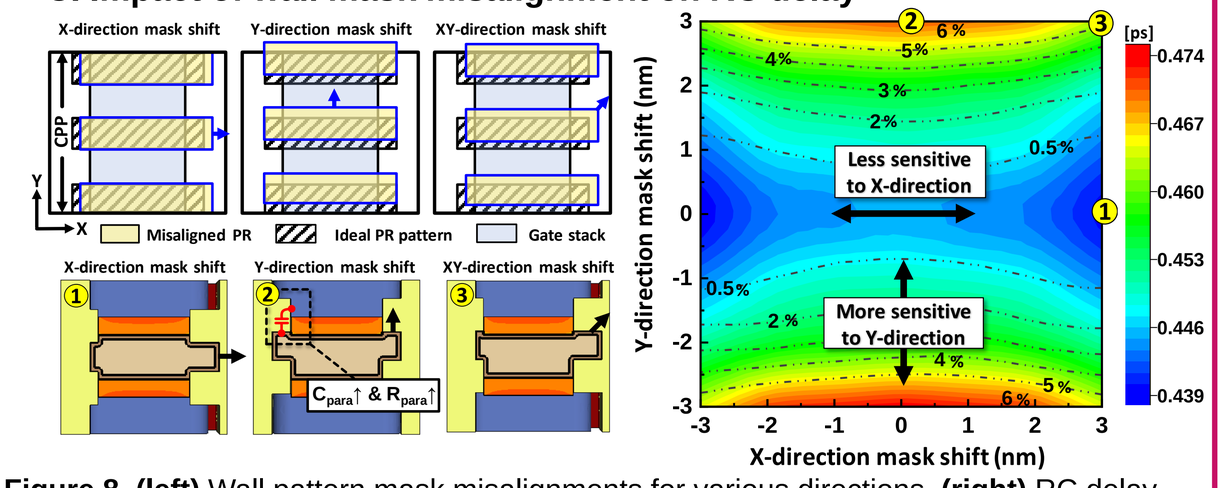

Figure 8. (left) Wall pattern mask misalignments for various directions. **(right)** RC delay due to mask misalignment. The dashed lines indicate the percentage change of the RC delay due to the misalignments compared to the RC delay with well-aligned.

IV. Conclusion

- The optimal wall pattern was L_{RMG} = L_{Sili} = 8 nm (at L_{WP} = 9 nm) (Fig. 6).
- Compared to the FSFETs, I_{on} improved by 11.8% and C_{gg} increased by 1.8%, which resulted in 8.9% lower RC delay thanks to the optimal wall design (Fig. 7).
- Controlling Y-direction misalignment was critical than in X-direction (Fig. 8).
- MW-NSFETs are expected to be used for logic applications beyond FSFETs.