



EU - SOUTH KOREA – Joint Researchers Forum
on Semiconductors



Specialized microelectronics for in-memory computing, RF communication, and quantum technologies

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VTT Technical Research Centre of Finland Ltd.,
Microelectronics and Quantum Technologies

The logo for VTT, consisting of the letters "VTT" in white on an orange square background.

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EU – SOUTH KOREA - Joint Researchers Forum
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Name

Contents

- Some basic facts about VTT
- Materials, device, process and application development for neuromorphic computing
- Microacoustics for 6G
- Micromachined 3D integration of RF devices for THz frequency range
- Advanced quantum sensors and electronics

VTT – *beyond the obvious*

VTT is a visionary research, development and innovation partner for companies and society and one of the leading research organisations in Europe.

Our role is to promote the utilization and commercialization of research and technology in business and society. Through science and technology, we turn global challenges into sustainable solutions for business and society in a responsible way.

261 M€
turnover and other
operating income

2,213
employees

43%
of the net turnover
from abroad

32%
a doctorate or a
licentiate's degree

Establishment year
1942

Steered by Ministry
of Economic Affairs
and Employment

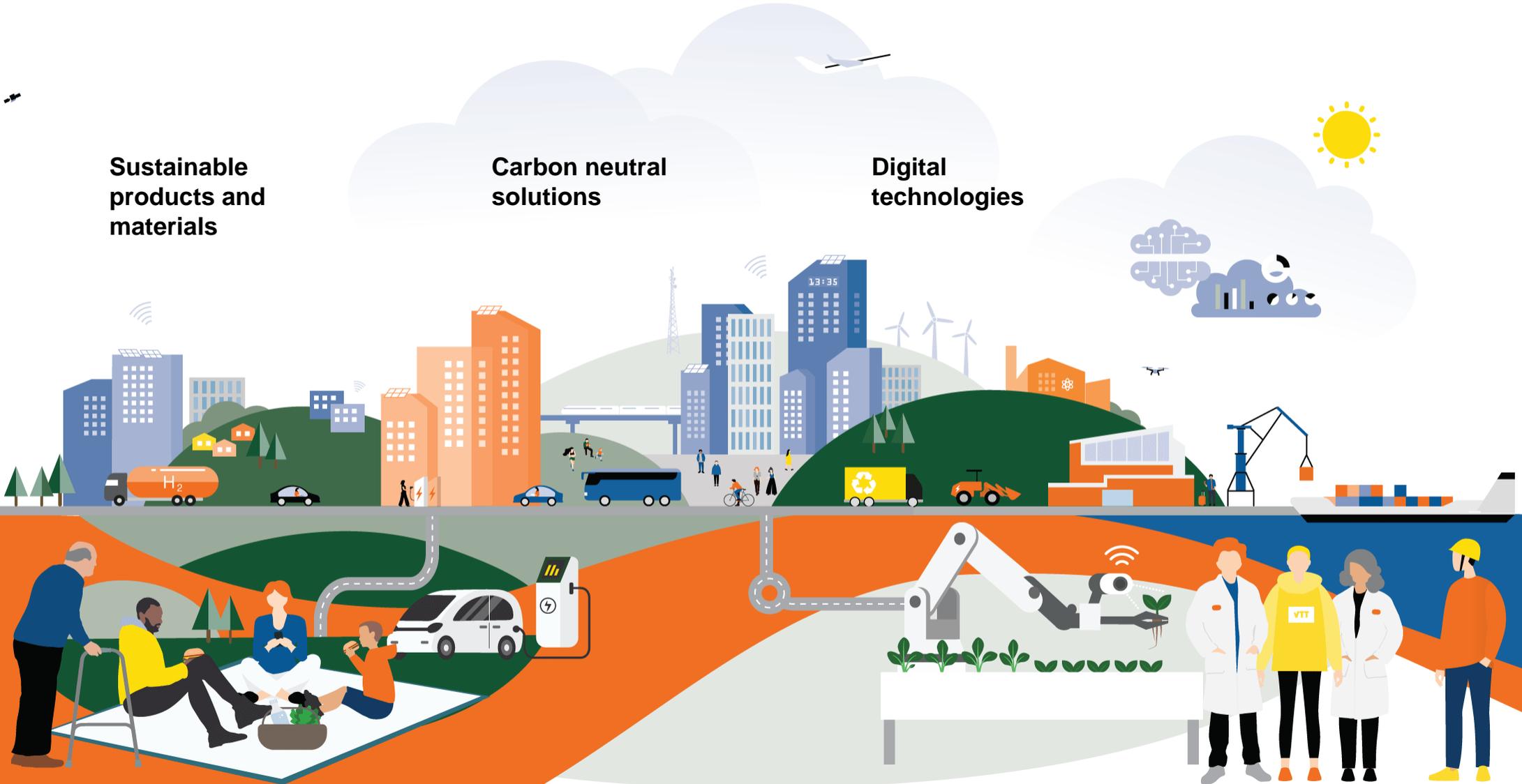
<https://www.vttresearch.com/en>

We create solutions in three business areas

**Sustainable
products and
materials**

**Carbon neutral
solutions**

**Digital
technologies**



Digital technologies

We create cutting-edge digital technologies and identify future opportunities to solve global challenges

Scaling up quantum

Specialised microelectronics

Integrated flexible electronics

Personalised health and wellness

Photonics sensing

Secured connectivity

New space

Defence & security

We innovate tomorrow's solutions together with our customers and partners



We enable the development of a high-performing and sustainable digital society



Micronova: the Finnish microelectronics ecosystem hub



Applied research and development



Basic research and education

20+

private companies using Micronova facilities

- Micronova infrastructure including clean rooms and measurement facilities
- Public and jointly funded Business Finland and EU projects
- Contract research and development

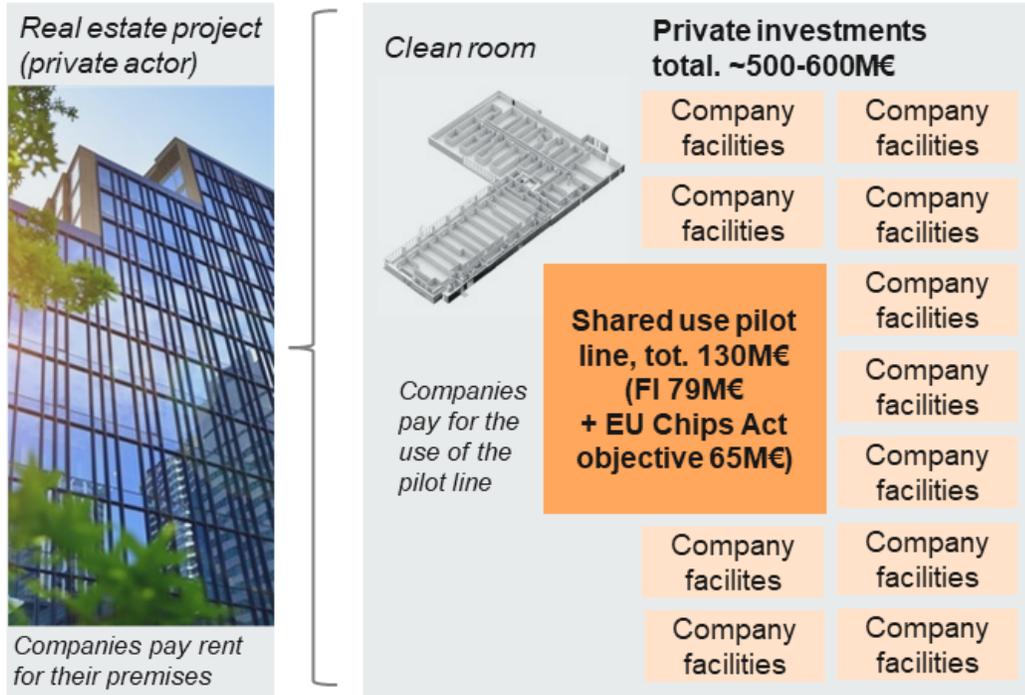


Main cleanroom characteristics

- Total area 2 600 m²
- Cleanroom classification ISO 4...ISO 6
- Temperature 21 °C ± 0,5 °C, relative humidity 45% ± 5
- Wafer size 150mm, to be moved -> 200mm 2025

Kvanttinova boosting EU's competitiveness on more-than-Moore Chips

Companies committed to the project

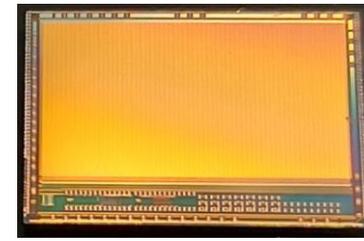


Focus and expected impact

- ✓ Pilot line for small volume manufacturing and scale-up in more-than-Moore technologies
- ✓ EU added value created by complementarity and natural interfaces with other main European pilot lines as well as synergies with EU quantum flagship
- ✓ Strengthening collaboration between research and business
- ✓ Creating new business, jobs and attracting new talent

Materials, device, process and application development for neuromorphic computing

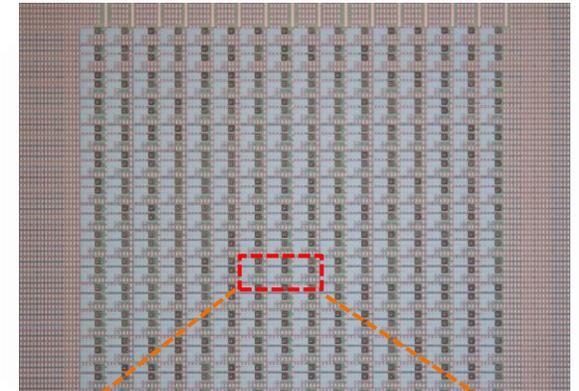
Neuromorphic computing



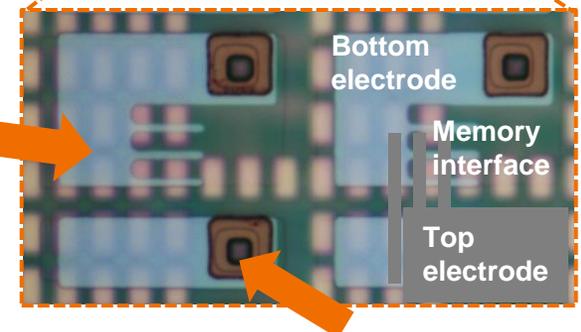
Neuro-IC chip

- To reduce power consumption in computing (analog computing) and data transfer (edge computing)
- Analog/mixed-signal neuromorphic chips for over 25 years
 - Recurrent Neural Net for **channel decoder**
 - Associative Neural Net for **robotics**
 - Cellular Neural Net for **image processing**
 - Hopfield Net for solving **optimization problems**
- VTT is developing a platform that includes:
 - BEOL compatible metal oxide transistors
 - HfZrO and AlScN ferroelectric computational units
 - Filamentary switching resistive memories
 - Nanoscale MΩ resistors
- Materials by ALD and reactive sputtering processes
- Post-CMOS integration

Integrated post-CMOS array of ferroelectrical transistors for analog in-memory computations



TiN developed with <111> phase to act as crystallization template for ALD grown ferroelectrical hafnium-zirconium-oxide

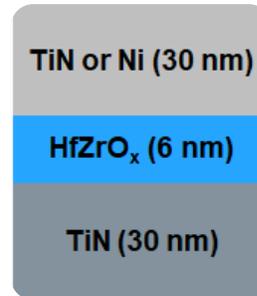


Via connects the CMOS front-end with back-end ferro-electrical capacitor to create a ferro-gated transistor

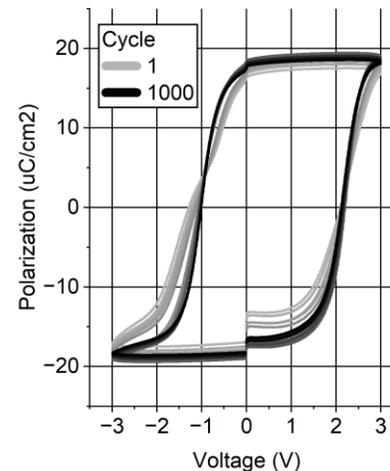
BEOL Compatible Ferroelectric HZO Integration

- For FeFETs, annealing is typically performed with a top-electrode (TE) that is later removed^{1,2}
- Adding and removing the TE adds complexity and may cause damages and interface issues if not adequately removed³
- TE-less annealing often results in a P_R of $\sim 1\text{-}2 \mu\text{C}/\text{cm}^2$ instead of the state-of-the-art $20\text{-}30 \mu\text{C}/\text{cm}^2$
- VTT have results showing that we can engineer the ferro-electrical phase transformation without a TE and that it highly depends on the initial BE TiN-stress
- Depending on the specific HZO-stack, we achieve a P_R up to $20 \mu\text{C}/\text{cm}^2$ for a scaled stack (6 nm thick HZO films shown here)
- The method gives opportunity to integrate a 2D or thin film semiconductor for BEOL FeFET implementations
- We switch our devices at different voltages up to 100M+ cycles with $20 \mu\text{s}$ pulses (pulse time limited by equipment, data not shown here as not published)

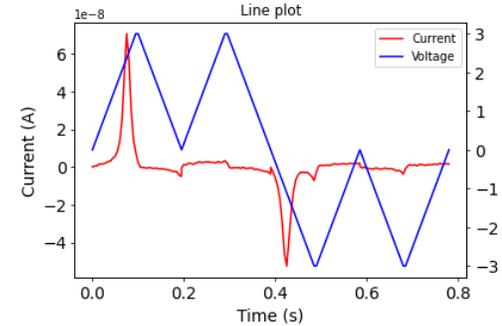
Our FE-stack



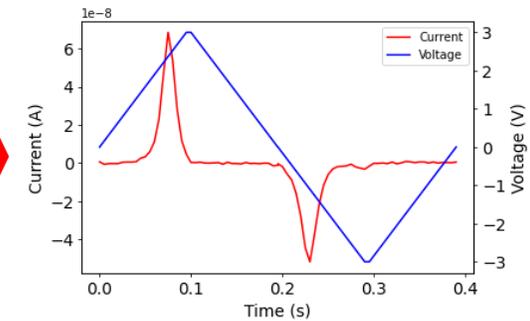
TiN/HZO/Ni-stack



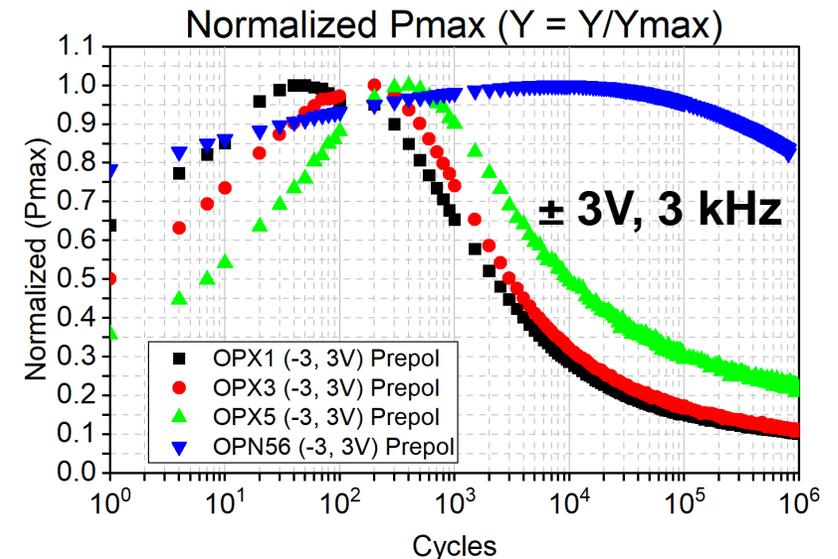
Raw PUND data



Extracted switching current



Comparison of different TiN/HZO/TiN-stacks



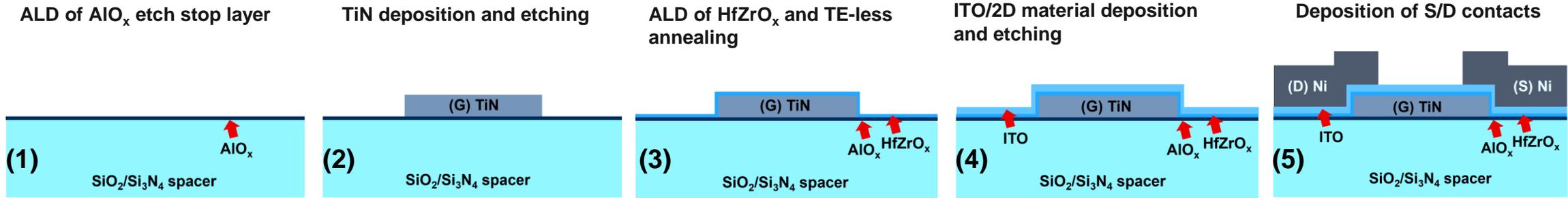
Preliminary VTT results not published

[1] Z. Liang et al (Key Laboratory, China), IEDM 2021

[2] M. Hoffman et al (Berkeley, NaMLab, TU Dresden), APL 2022

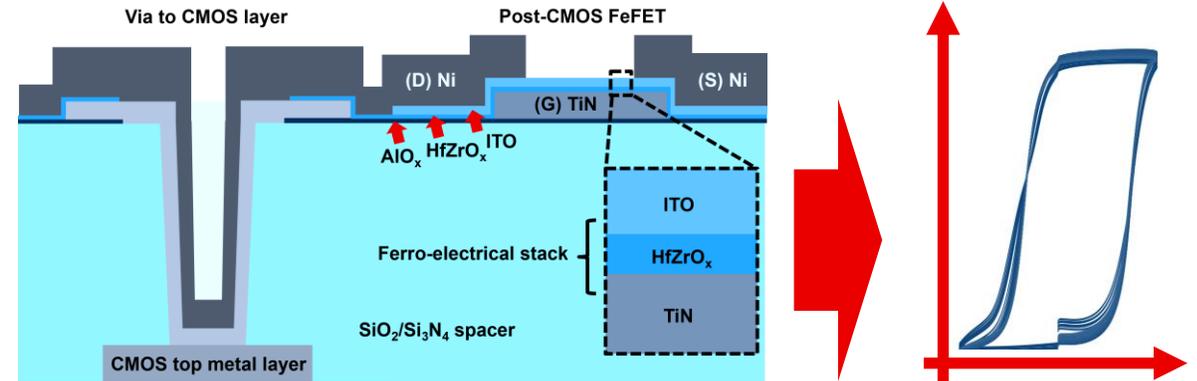
[3] R. Athle et al (Lund U), AEM 2022

VTT FeFET Process Flow

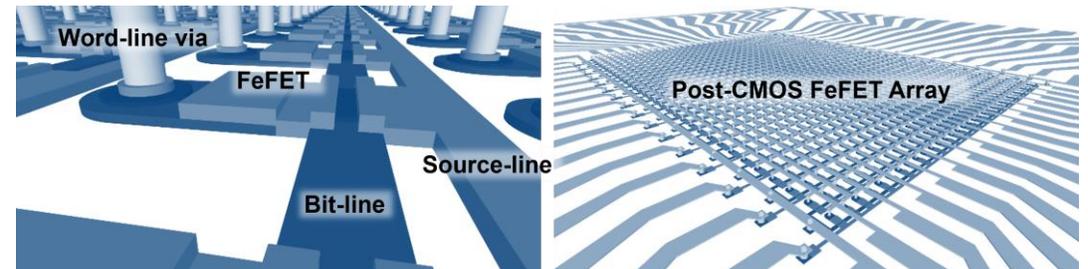


- (1) **ALD of AlO_x etch stop layer**
 - Protecting the underlying front-end spacer
- (2) **TiN deposition and etching**
 - Deposition of our optimized sputtered TiN film where we can control stress
- (3) **ALD of HfZrO_x and TE-less annealing**
 - A process developed for a resulting strong remanent polarization without the need of a top-electrode during annealing
- (4) **ITO/2D material deposition and etching**
 - The fabrication is independent of the semiconducting material such that it is possible to deposit conductive oxides or 2D-semiconductors post anneal
- (5) **Deposition of S/D contacts**
 - The fabrication scheme is very low complexity, enabling possibility for low-cost, high yield, and multiple layers

The full integration showing both FeFET and front-end CMOS-via

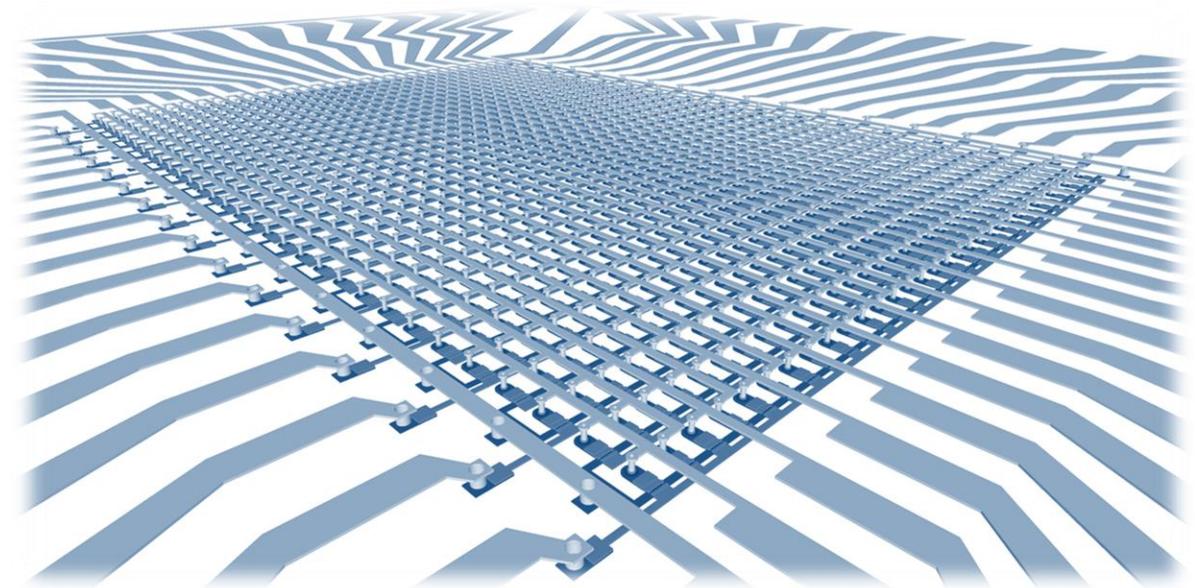


Dense array can be realised without the need of vias



Summary and Conclusions

- Electrical data shows promising ferroelectric polarization for our unique method to achieve TE-less annealing
- Close collaboration between circuit designers and device developers gives opportunity to make large functional systems
- We have circuit designs and developed fabrication schemes for both sensors and memories for post-CMOS integration on 200 mm wafers
- Our long-term goal is to build a 3D-platform that can utilize different types of sensory input for on-chip classification
- **Acknowledgements:** Patrik Eskelinen, Oscar Kaatranen, Kimmo Rutanen, Olli-Pekka Kilpi, Arto Rantala, Jacek Flak



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A decorative geometric pattern covers the left side of the slide. It features a repeating arrangement of hexagonal shapes in various shades of blue (light, medium, and dark) and black. Some of the hexagons are highlighted with a bright orange color, creating a complex, three-dimensional optical illusion effect.

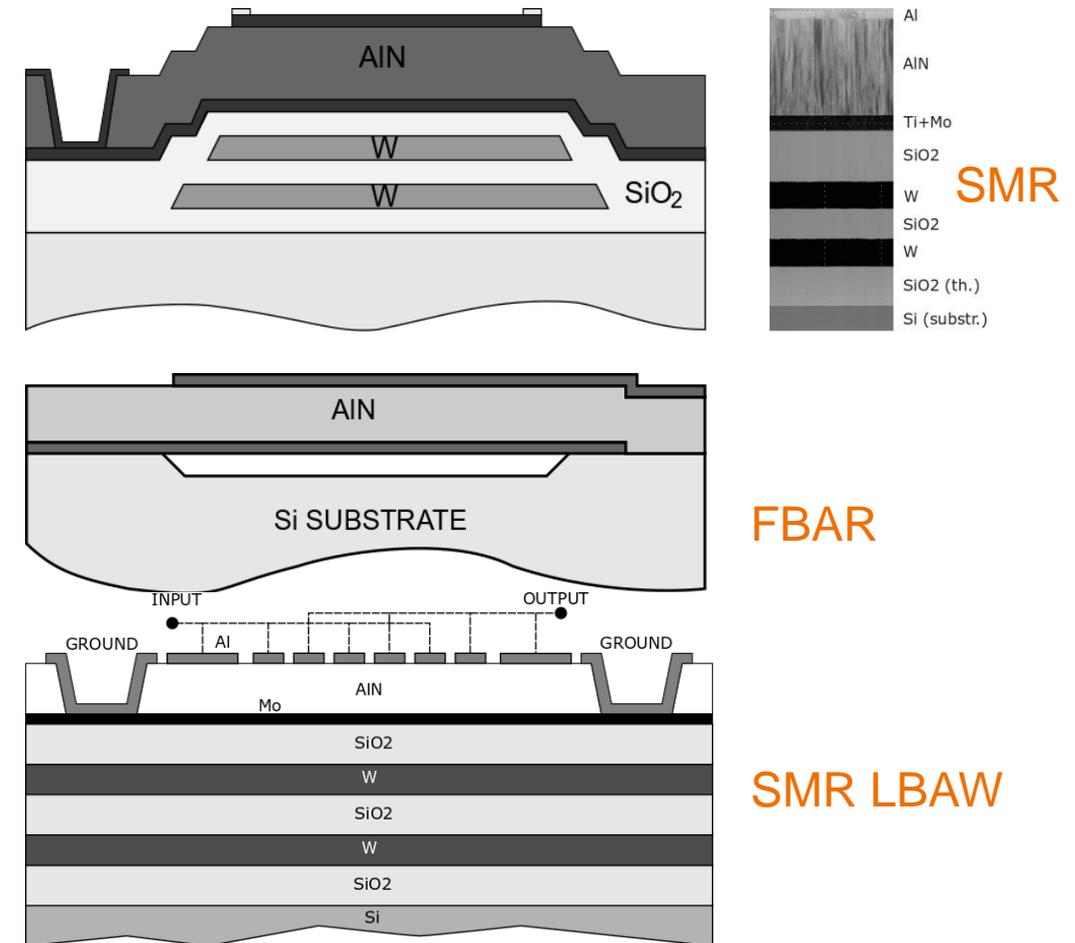
Microacoustics for 6G

Thin Film BAW development

- Long experience in GHz range thin film BAW devices since 1990's
- Material & process development
- Acoustic & RF design, modelling method & tool development
- BAW, LBAW, Lamb-wave, SAW and POI-based device design and prototyping

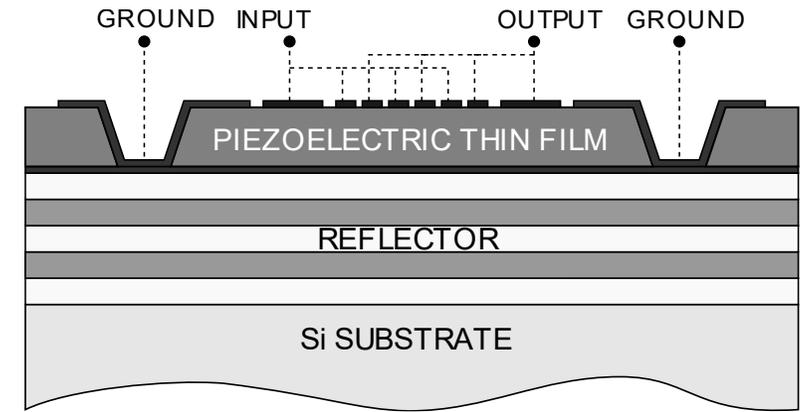
Prototype manufacturing

- Advanced piezoelectric thin film deposition processes
- Surface micromachined and monolithic device process platforms
 - FBAR & SMR
- IPD process platform for RF applications
- i-line stepper lithography
- Mainly 150 mm processing, moving to 200 mm
- RF characterization
- Materials:
 - Sputtered AlN, $Sc_xAl_{1-x}N$ x from $< .1$ to > 0.3
 - Focus at the moment $x=0.3$ optimization. Moving to higher x studies
 - Electrode systems
 - Ti-Mo, AlN-Mo, Al-W multilayers
 - SMR reflector layers
 - SiO₂, W, TiW

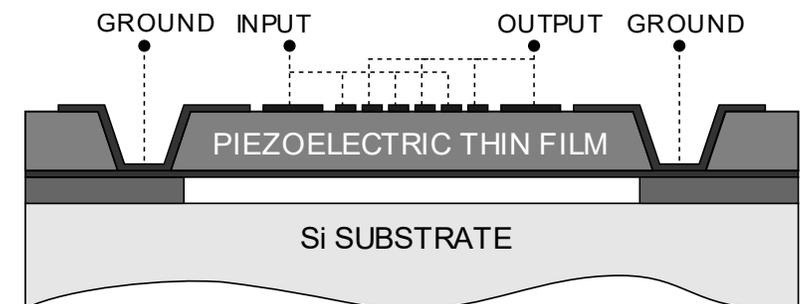


R&D example – LBAW filter

- BAW/FBAR type thin film manufacturing technology
- Interdigital electrode based horizontal acoustic coupling
- Relaxed critical dimensions and litho requirements as compared to SAW
- Single IDT filter function - no reflectors needed
- Applicable at least to up to ~ 3.5 GHz
- Small size
- Wide bandwidth (> 10 %) with proper matching

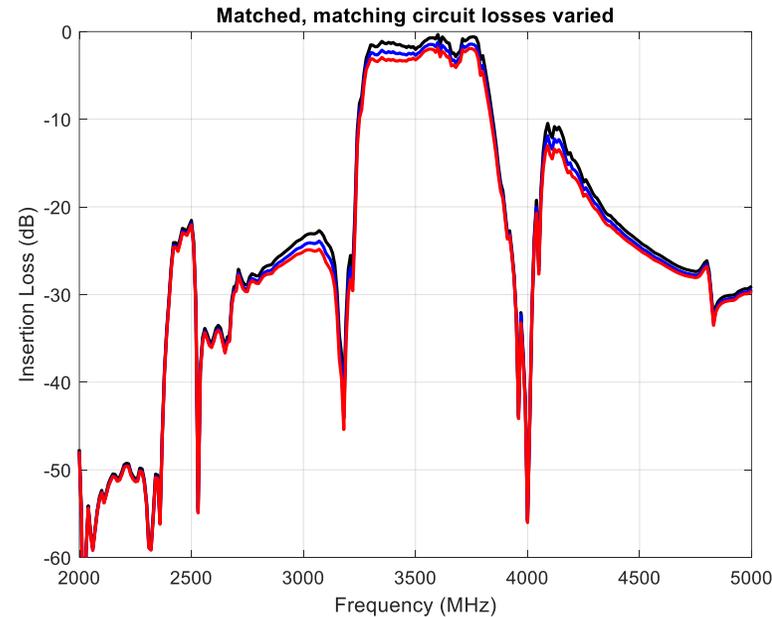
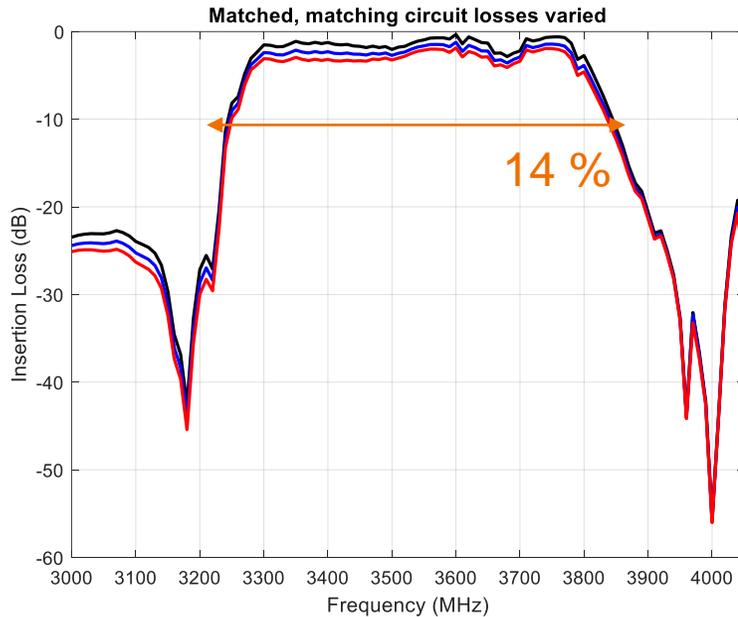


Solidly mounted LBAW



Membrane LBAW

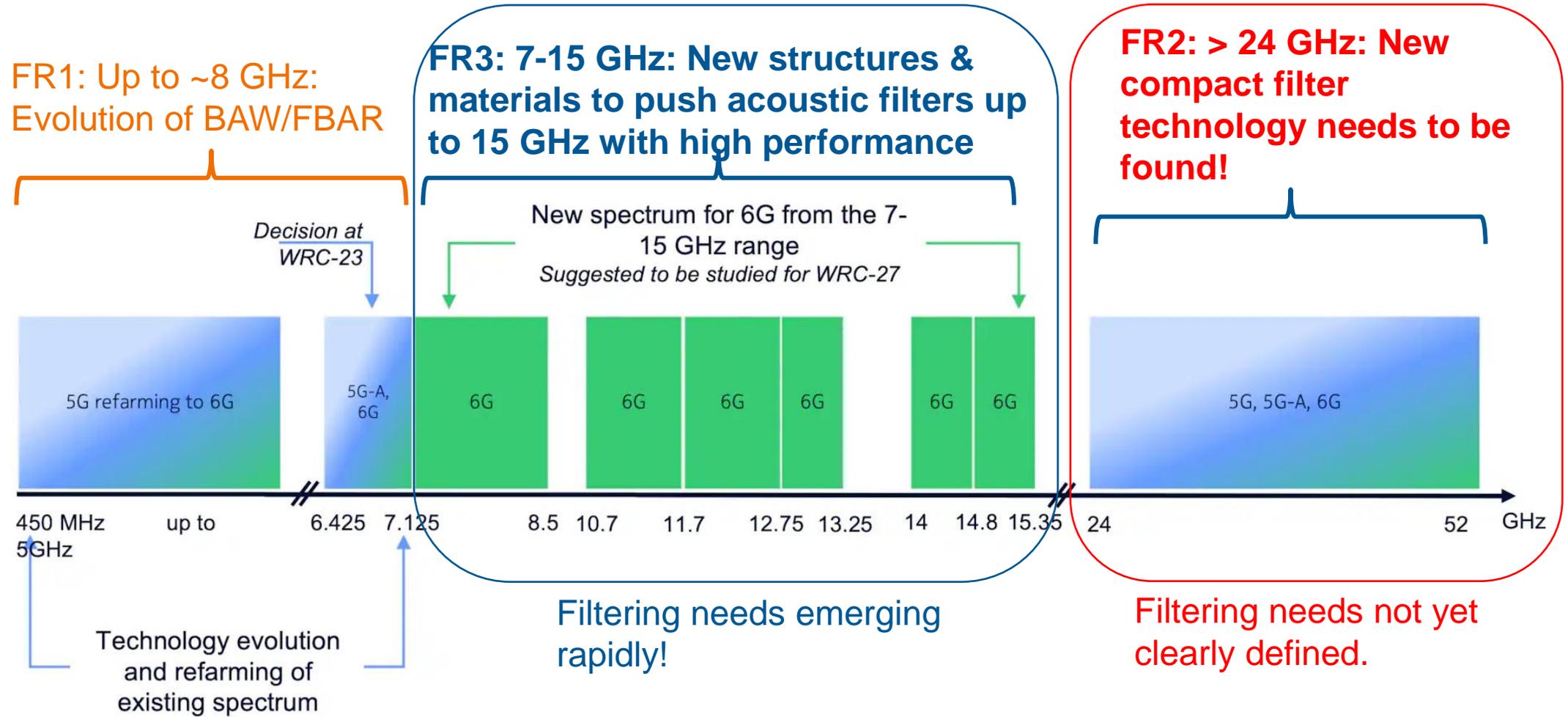
5G Band N78 design study – 500 MHz (14 %) of bandwidth at 3500 MHz



- Acoustic filter size: ~ 0.6 mm x 0.1 mm
- Smallest lithographic dimension: 0.5 μm
- Inductor matching: ~1 nH inductors
- Development and tuning possibilities:
 - Tune acoustic notches to steepen upper edge roll-off
 - Various options for matching
 - Use ScAlN instead of AlN - relaxed matching needs

Membrane type LBAW filter, plain AlN piezolayer

RF filters for the 6G front end



[From: Spectrum for 6G explained | Nokia]

VTT goals & contribution

- Find, develop and demonstrate a missing compact & mass producible filter technology addressing the FR2 range at > 24 GHz (cm-waves)
 - Filter technology allowing miniaturization, required tolerances, and cost- efficient mass production
 - Use existing technologies as steppingstones, combine, introduce new elements
- Pursue novel acoustic BAW filter technology to bring frequencies up to covering the FR3 range at 7-15 GHz maintaining high Q-value
 - Advanced ultra-thin multilayers and material combinations, deposition methods
 - Novel device structures and approaches to manufacturing
 - Combine surface micromachining, layer transfer, improved crystal quality & texture of materials, novel thin film materials
 - Develop methods for thickness control with up to 10x stricter tolerances than in FR1
 - Study fundamentals of acoustic performance of materials in very thin films at > 10 GHz in theory and with experiments

VERY
LOW TRL

LOW TRL

VTT technology contribution & resources available

- Integrated passives (IPD), micromachined waveguides
- Surface MEMS, Si-MEMS processes (SOI, CSOI), access to epitaxial deposition
- New material system development and utilization
- LTCC

- BAW filters: FBAR & SMR platforms
 - Existing approaches to FR3 and concepts for evolution towards FR2
- Advanced sputtering AlN, ScAlN, electrode systems, new material system development
- ALD, atomic layer etching, ion beam trimming

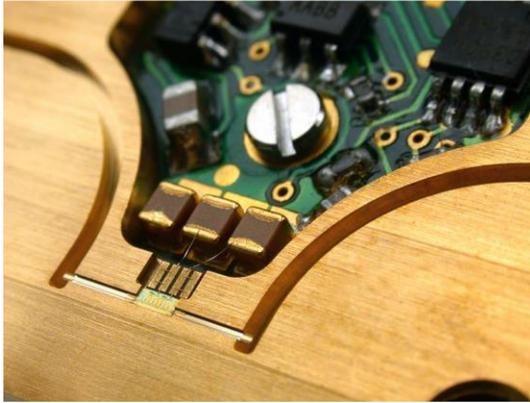
Consortium & project partners sought

- Complementary hardware/component developers
- New material and deposition beyond sputtering, e.g. epitaxial/single crystal etc., materials science and characterization
- Heterogenous integration, packaging technology
- Radio hardware developer on (front end & system level)
- Active component developers (PA, LNA)
- Application hardware developers

A large, repeating 3D geometric pattern occupies the left side of the slide. It features a grid of interlocking cubes or hexagonal shapes, each with a different color: orange, blue, black, and light grey. The perspective is from an angle, giving the pattern a three-dimensional appearance.

Micromachined 3D integration of RF devices for THz frequency range

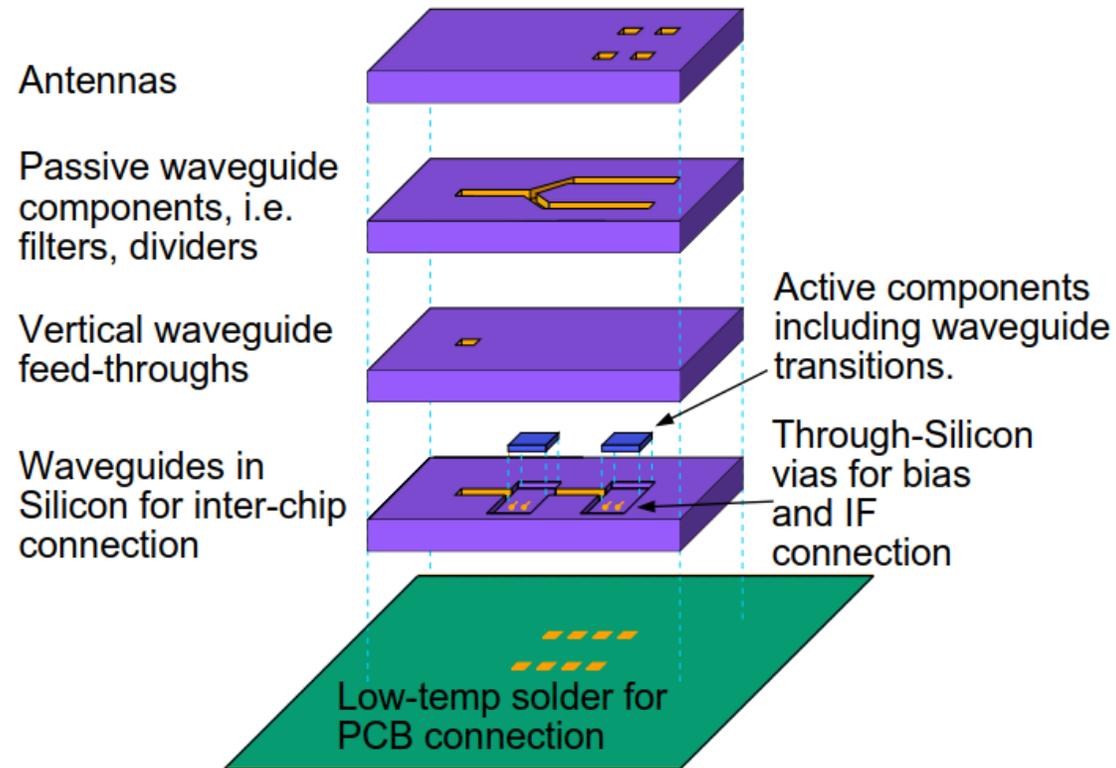
Heterogenous integration and packaging - How to build low cost and mass- producible sub- millimeter wave or THz systems?



A. Tessman and el, 2006

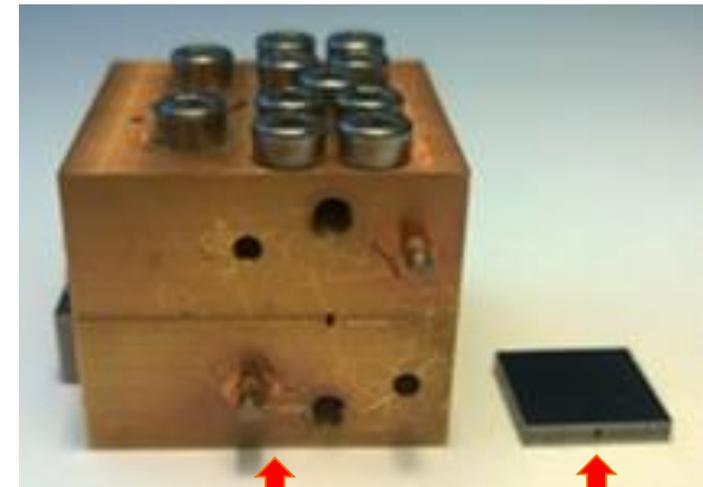
- Good progress have been done with mass-producible active components on MMIC
- Integration of MMICs to a system is a challenge
 - ✓ Planar integration methods, such as PCB, LTCC, IPD, typically fail at around 100 GHz.
- State-of-the-art at THz range integration is split-block integration
 - ✓ Expensive (fabrication of split-block systems with accuracy (3-5 μm) requires high-precision micromachining)
 - ✓ Leads to big systems
- **Need for integration method that enables optimal combination of small MMICs and high-quality passives and antennas.**

Our vision



To use micromachined waveguides on Silicon to realize passive components at THz range and to connect all elements of the system: active MMICs, passive components and antennas. The system can be realized on stacked Si wafers.

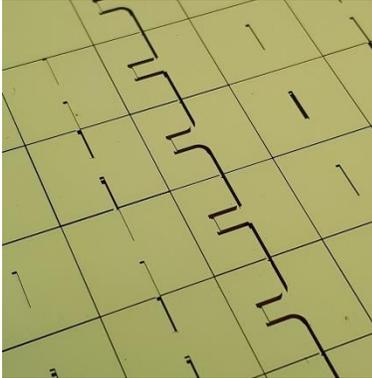
- Optimal use of MMIC area
- Low-cost integration platform with simple process
- Low temperature bonding process to reduce need for external mechanical support



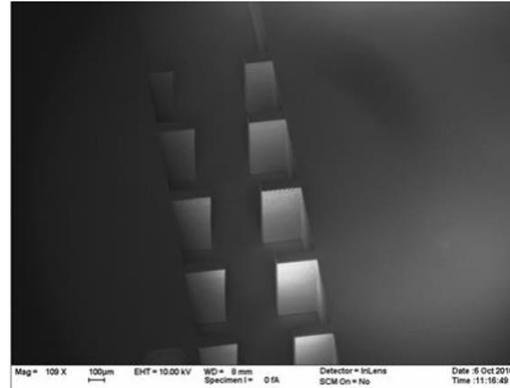
Split-block module

Micromachining module

Fabricated structures



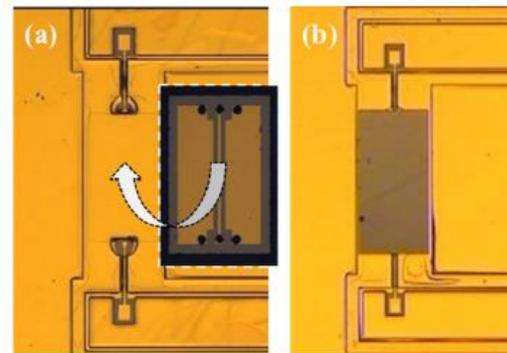
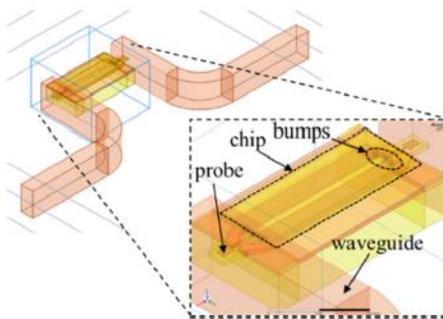
View of a wafer with WR-3 fabricated structures



Band-pass filter

- We demonstrated components and modules on WR-3 (860 μm x 430 μm ; 220-325 GHz):

- Straight and bent waveguides
- Low-pass filters
- Band-pass filters
- MMIC transition
- Vertical vias
- Module integration of MMIC
- WR-6 (110 – 170 GHz) waveguides are demonstrated also



Module integration of MMIC

Heterogeneous integration technology for future THz semiconductor components and systems

Call

- HORIZON-Chips-2024-3-RIA

Status

- At VTT wafer level silicon micromachine integration technology has been developed. The technology is ready to be used and capable of heterogeneous integration of individual MMICs in different technologies for radio systems up to 300 GHz and above
- Antennas, active and passive components in scalable small-size, light-weight, and low-cost platform

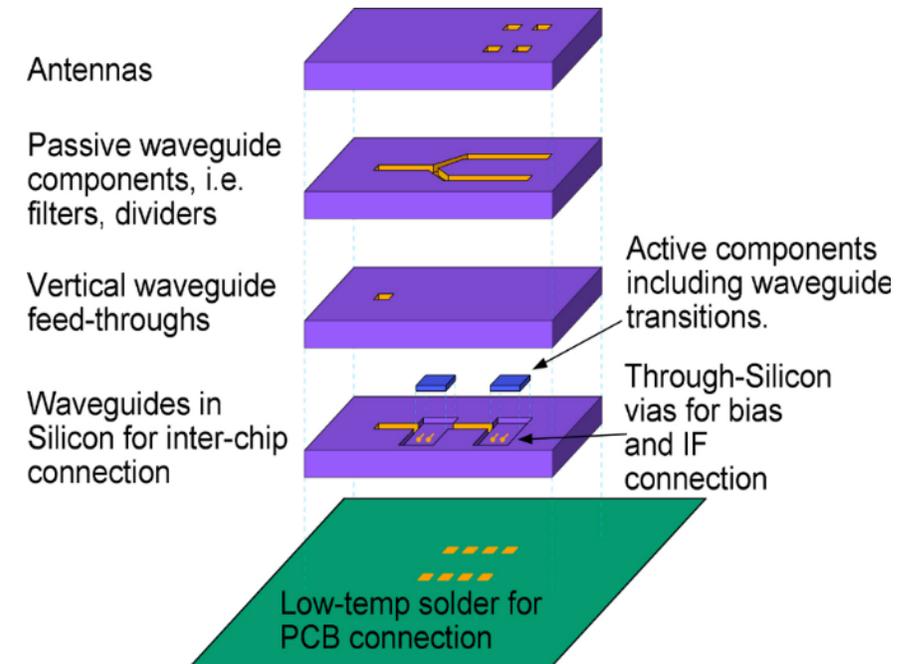
Proposal

- Push the disruptive heterogeneous packaging technology developed previously to higher TRL levels
- Utilize the developed micromachining technology into a complete THz communication and/or sensor demonstrator (RADCOM)

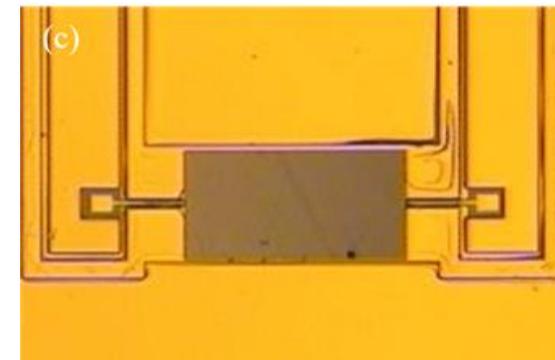
Partners for joint project

- competences in III-V and/or silicon MMIC technologies
- competences in mmW and THz communication and sensor technologies

VTT's 3D modular silicon wafer level integration technology



Flip-chip assembled IC with air filled waveguides*



* V. Ermolov et al., *IEEE MWTL*, Feb. 2024

A large, repeating geometric pattern of interlocking hexagons in orange, blue, black, and light grey covers the left half of the slide. The pattern is composed of three interlocking shapes: a white hexagon, a blue hexagon, and a black hexagon, with orange hexagons filling the remaining spaces.

Advanced quantum sensors and electronics

Advanced Functionalities

SQUIDs

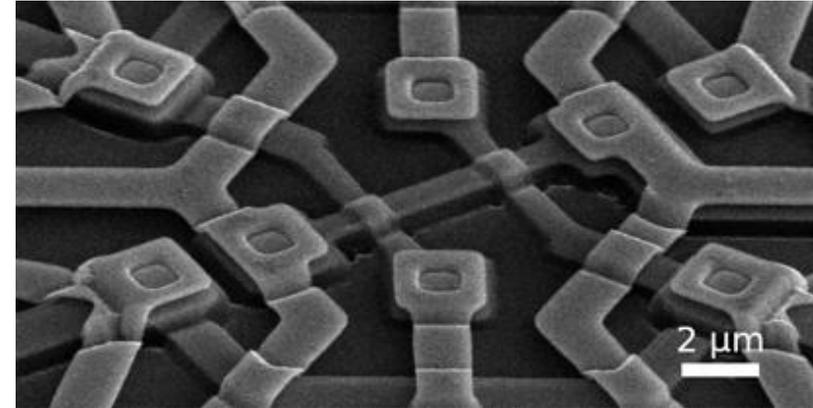
- The most sensitive magnetic field sensors available based on superconductive loops containing Josephson junctions.
- Application areas: Magnetometry for medical applications, mineral search, other weak fields, as current amplifiers for readout of other superconducting sensors.

Single-photon detectors

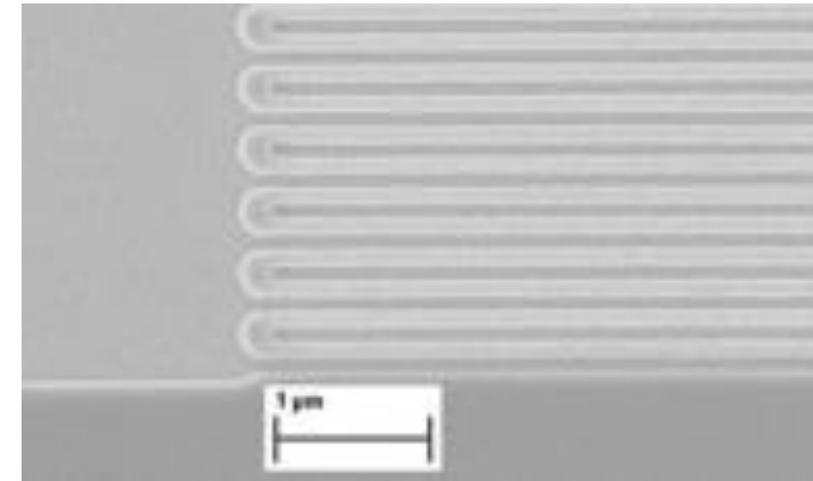
- For optical detection of qubit data that comes as single photons (in silicon photonic quantum computers).
- Development of superconducting nanowire single photon detectors (SNS-PDs) and transition edge sensors (TES)

Josephson travelling-wave parametric amplifiers

- super-conducting quantum processor readout for wide-band 4 to 8 GHz
- for quantum sensing and spin-qubit readout



SQUIDs for magnetic field sensing



Microscope picture of a SNSPD fabricated at VTT



THANK YOU



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