Advancements in Neuromorphic Computing Using Silicon Nitride Memristors for IoT and Security

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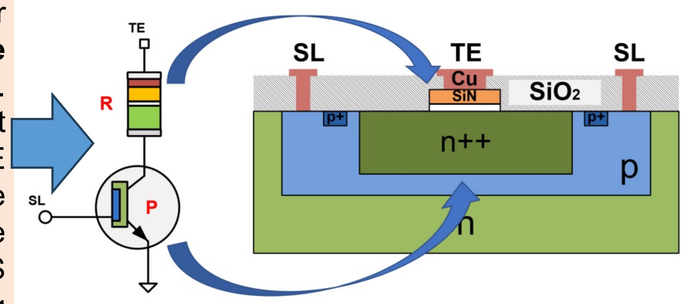
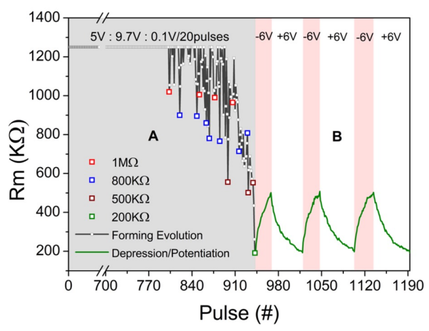
A new 1Ph1R image sensor with *in-memory* computing properties based on silicon nitride devices

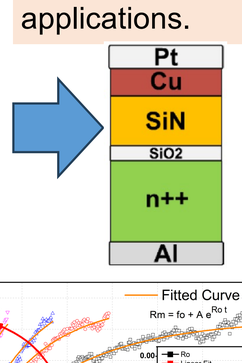
Silicon nitride, valued for its insulating properties, strength, and chemical resistance, serves as a key material in the IC industry. The silicon nitride **memristor**, composed of five materials, is fabricated through a compatible CMOS process. Its characteristics include analog resistance tuning and controlled switching behaviors. Faster pulsing systems allow **precise control of trap distribution**, leading to filamentary states for potentiation and depression. Exponential models describe tuning behaviors related to voltage amplitudes.

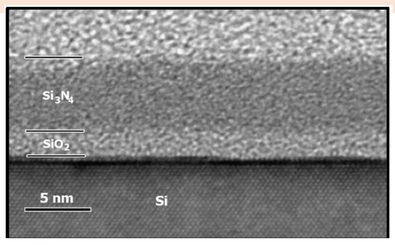
The **1P1R circuitry** integrates a memristor with a bjt-phototransistor, enabling **resistance** adjustments **proportional to light** intensity. The process involves resetting, light exposure, and reading phases. SPICE simulations illustrate discrete resistance states within the tunable range. The integration of memristors into CMOS processes simplifies circuit design, offering versatility and controllability in various applications.

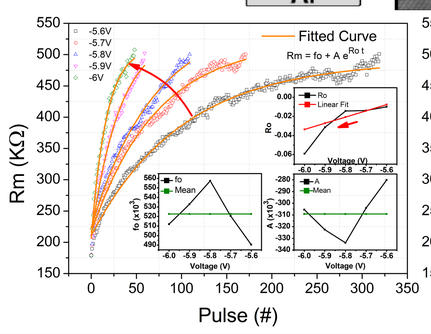


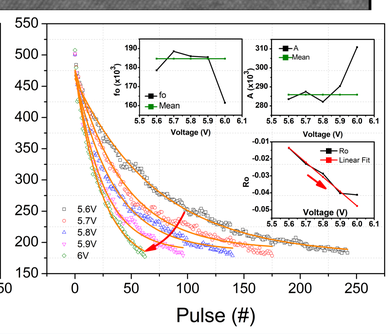
The 1P1R concept extends to a **crossbar array** for image sensing. Memristors adjust resistances based on light absorption, functioning as pixels. **Filtering masks** enable simultaneous reading and current accumulation of neighboring pixels, facilitating image processing. SPICE simulations demonstrate **image capture, filtering,** and **edge detection** capabilities.

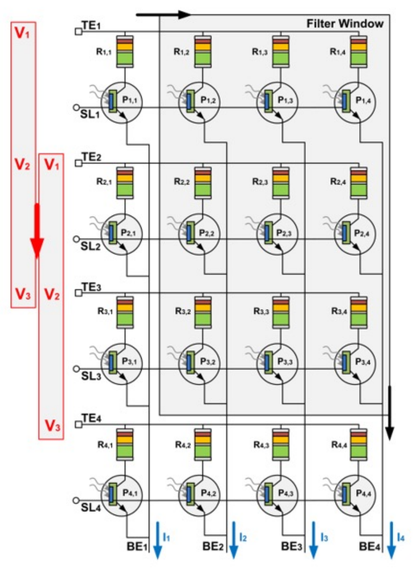


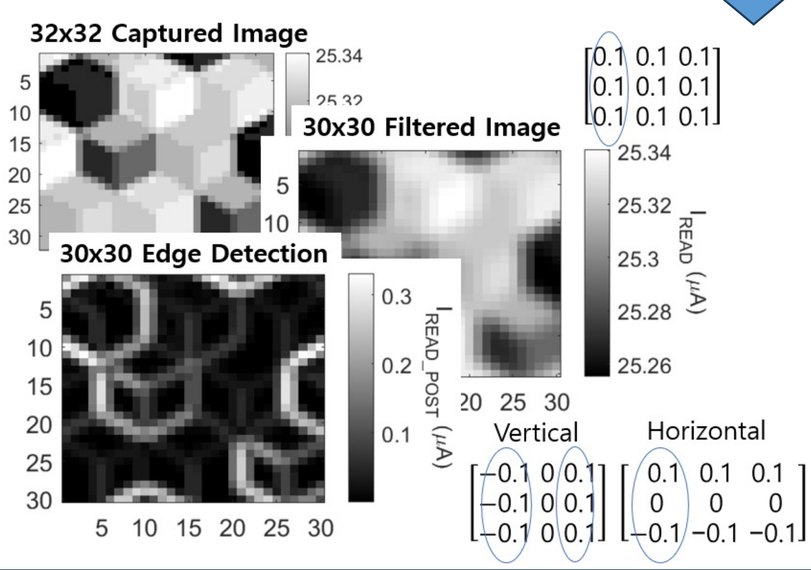










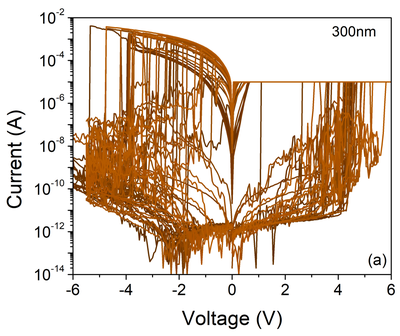


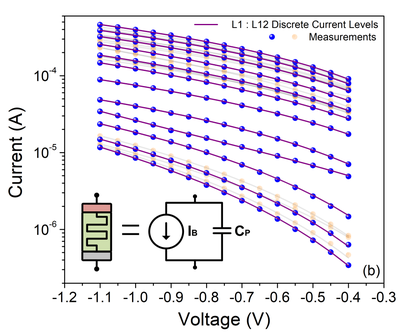
Novel crossbar array of silicon nitride resistive memories on SOI enables memristor rationed logic

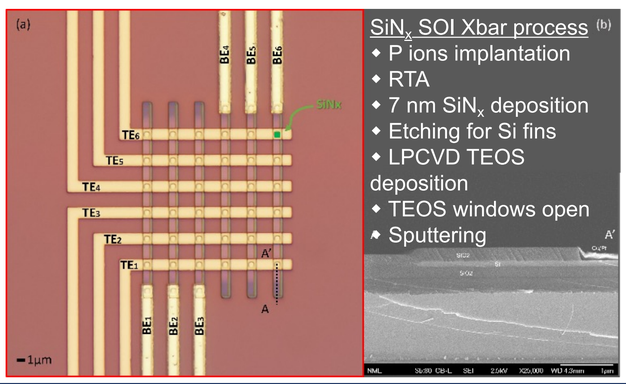
- **In this work, the fabrication of Xbar arrays of SiNx resistive memories on SOI substrate and their utilization to realize MRL circuits are presented.**
- **Typical electrical characterization of the memristors revealed their ability of multi-state operation by the presence of 12 well separated resistance levels.**
- **Through a dedicated fitting model, a reconfigurable logic based on MRL scheme is designed/evaluated and a Xbar integration methodology was proposed.**
- **Several circuitry aspects were simulated in SPICE with a SiNx SOI Xbar array calibrated model and power optimization prospects were discussed.**

◆ The RS mechanism is attributed to the presence of **native traps** created by the **nitrogen deficiency** and their subsequent density enhancement under the applied electric field.

◆ Significant **current fluctuations** are observed **due to** the unhindered **electron exchange** between the N^{++} Si (BE) and the SiN_x boarder traps.







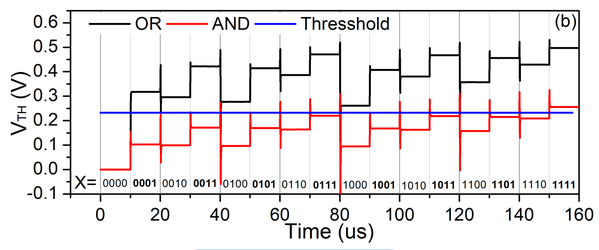
◆ **Parallel connected** SiN_x memristors at a common node V_{th} with a resistor R_{th} are a reconfigurable structure as it is possible to **change** the **voltage** of common node $\mathbf{V_{th}}$ by **varying** the conductance state of each memristor.

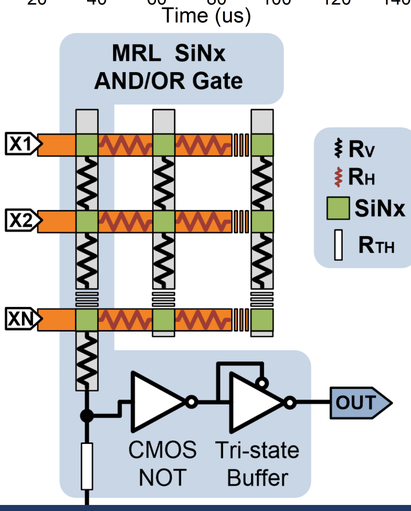
◆ **Logic 1** (True) is represented by 1V while **Logic 0** (False) by Non-Contact (NC).

◆ Reduced complexity with **simplified design** ready for larger scale integrations using a **unique** threshold $\mathbf{V_{th}}$ and **unique** node resistance $\mathbf{R_{th}}$.

◆ **Intermediate resistances** as well as the increasing **number of inputs** can affect the performance of the proposed MRL.

◆ **Larger MRL gates** can be achieved by combining more smaller crossbars **using the segmented** architecture of crossbars.





● **True random number generators** (TRNGs) utilize physical randomness from sources like **flicker noise** or **random telegraph noise** for cryptographic purposes.

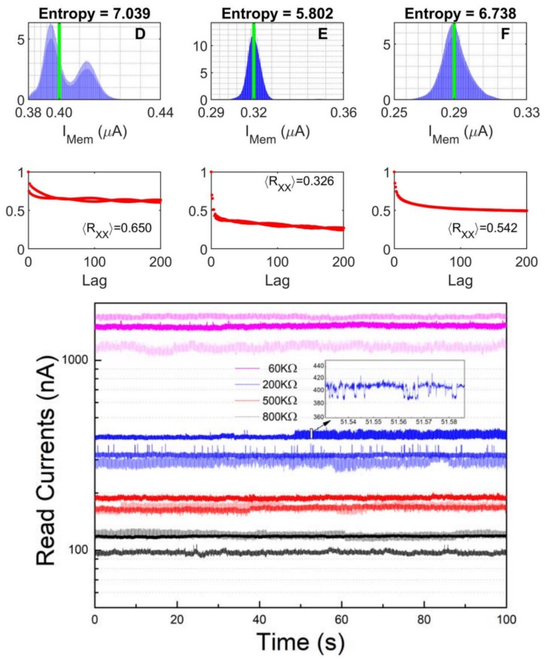
● TRNG systems face challenges including **high power consumption** and design **complexity**, limiting their use in IoT applications.

● Proposed solutions like **memristive TRNG** aim to address these issues by offering **modularity to the entropy source device**, enhancing system flexibility and tweakability.

◆ The study explores **twelve states** achieved through a tuning algorithm, showcasing dominant resistance levels in silicon nitride devices.

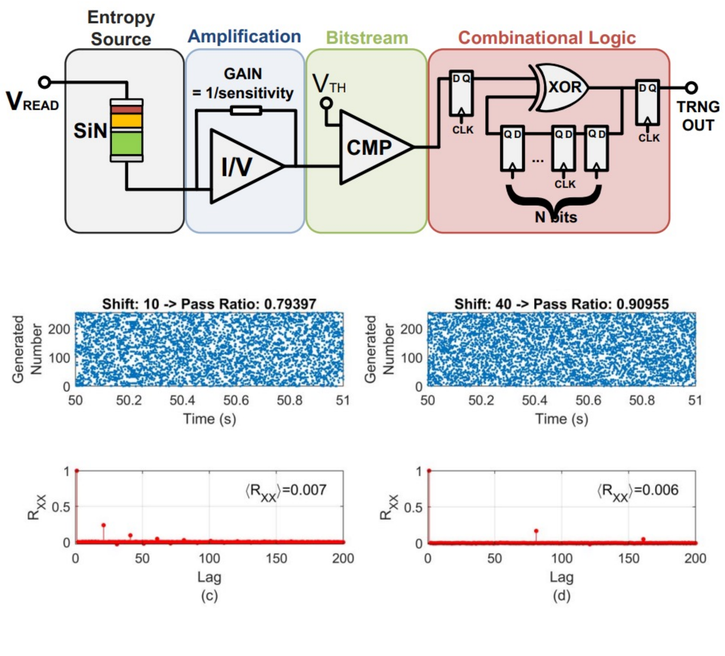
◆ Noise analysis reveals **flicker** ($1/f$) and **RTN noise** ($1/f^2$) due to trap charging.

◆ Entropy sources' **randomness** and periodicities are examined through **histograms** and **auto-correlation** diagrams.



◆ The Memristive TRNG circuit employs SiNx memristors to generate current noise signals. A **comparator** generates a bitstream based on a threshold. Postprocessing involves an **XOR shift logic** for randomness enhancement.

◆ **Multiple sources** can create multiple or combined bitstreams using **crossbar arrays**.



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