SAMSUNG

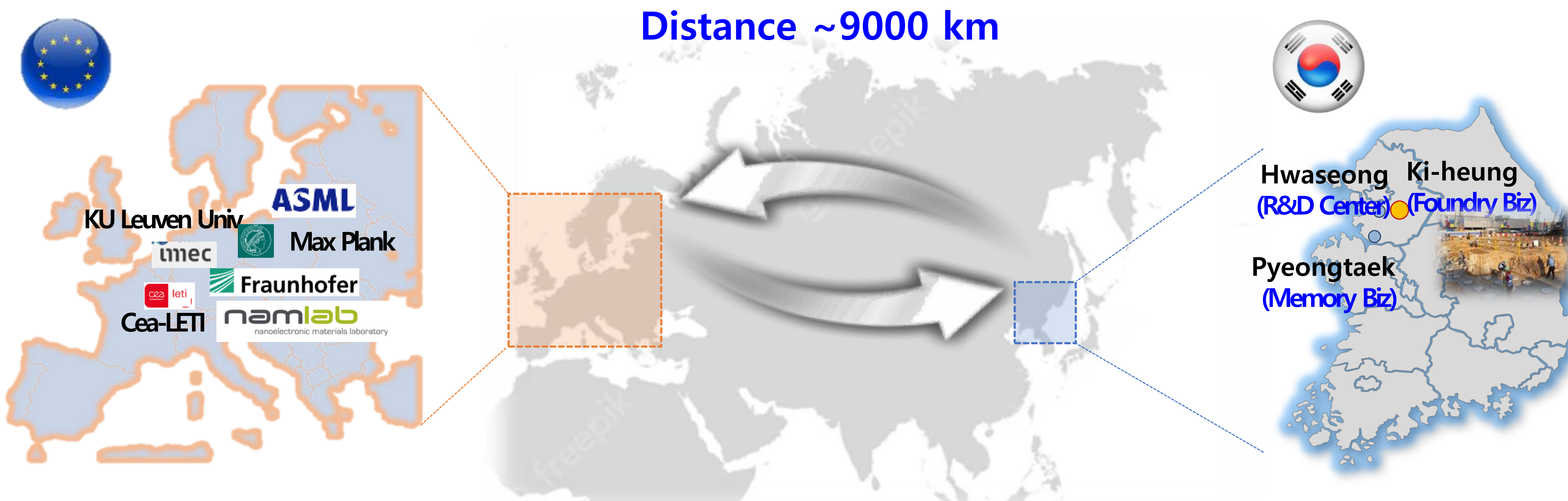
Innovative materials and devices for future logic and memory technologies

Sujin Ahn

EVP, Advanced Technology Development Office,
Samsung Electronics

Collaboration Journey with EU over 20 years

History of Overcoming Technical Challenges in Device Scaling



1. Memory Tech.

- imec - Advanced Patterning
- MPI - Disruptive Device / Material for VNAND
- namlab - DRAM Cap Boosting

2. Logic Tech.

- imec - CMOS Device/Process/Mat.
- cea leti - Monolithic 3D, SOI (Awareness)
- Fraunhofer - FeFET (Awareness)

3. Equipment

Samsung

IMEC

ASML

- High NA EUV & Patterning

4. Human Intercourse

- KU Leuven Univ. - Samsung

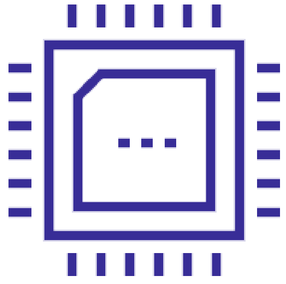
Academic Training

SAMSUNG

01 **New Eras Driven by Semiconductors**

02 **Upcoming Challenges and Innovations**

03 **Conclusion**



New Eras Driven by Semiconductors

Paradigm Shift in Computing over the Past 80 Years

Every 15 Years, Introducing New Devices and Accelerates Computing Speed x1000 times Faster

Calculations per Second per $1,000

10^{40}
10^{30}
10^{20}
10^{10}
10^{0}
10^{-10}

Mainframe Era

Mini–Computer Era

Personal Computer Era

Cell Phone/Sever Era

Hyper-scale Connectivity & AI Era

Vacuum Tube

Micro Processor

Mobile AP

Memory

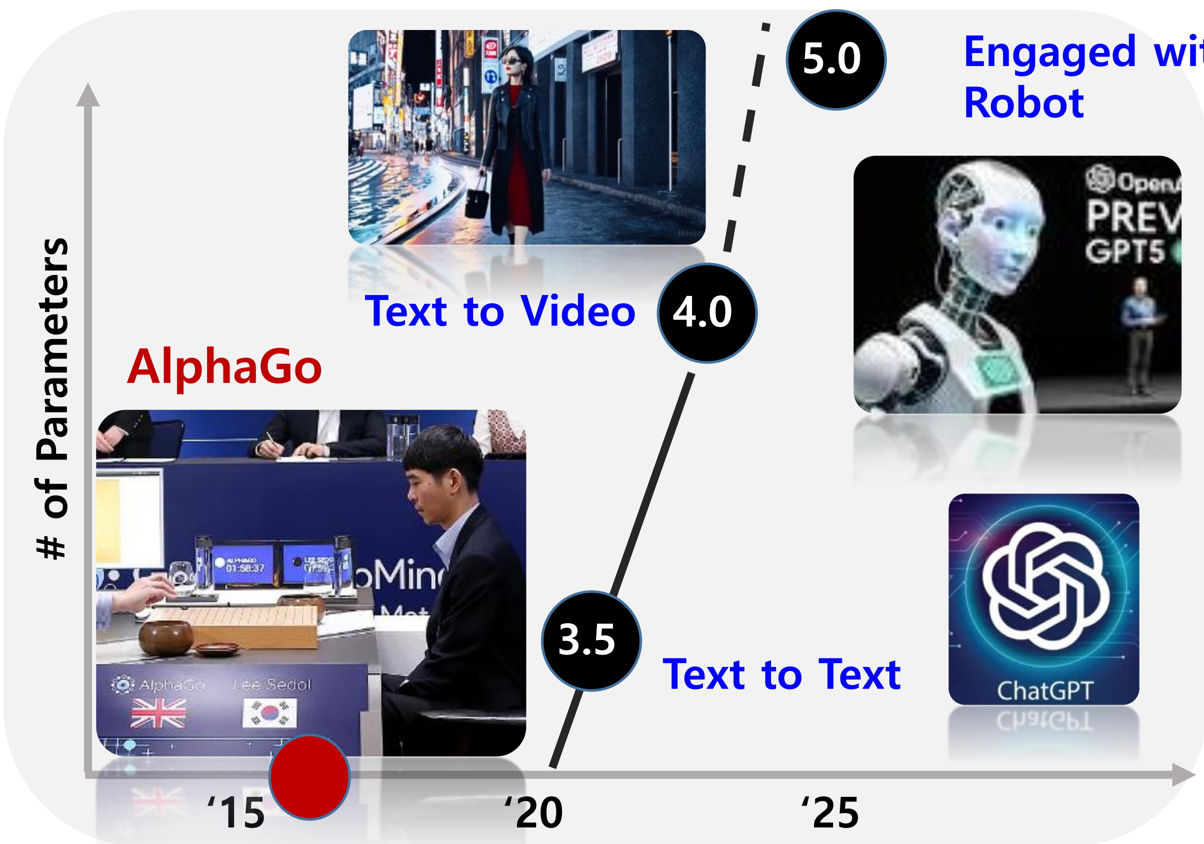
'40 '60 '80 2000 '20 '40 '60

Source: www.thekurzweillibrary.com Ruben Laukkonen (2018)

The Future Transformed by Generative AI

The Expansion of Large-scale LLM models Drives the Steep Growth in HPC Servers with Advanced Logic, Memory, even Packaging Technology

Development of AI in our Lives



2.5D/3D Advanced Package Platforms

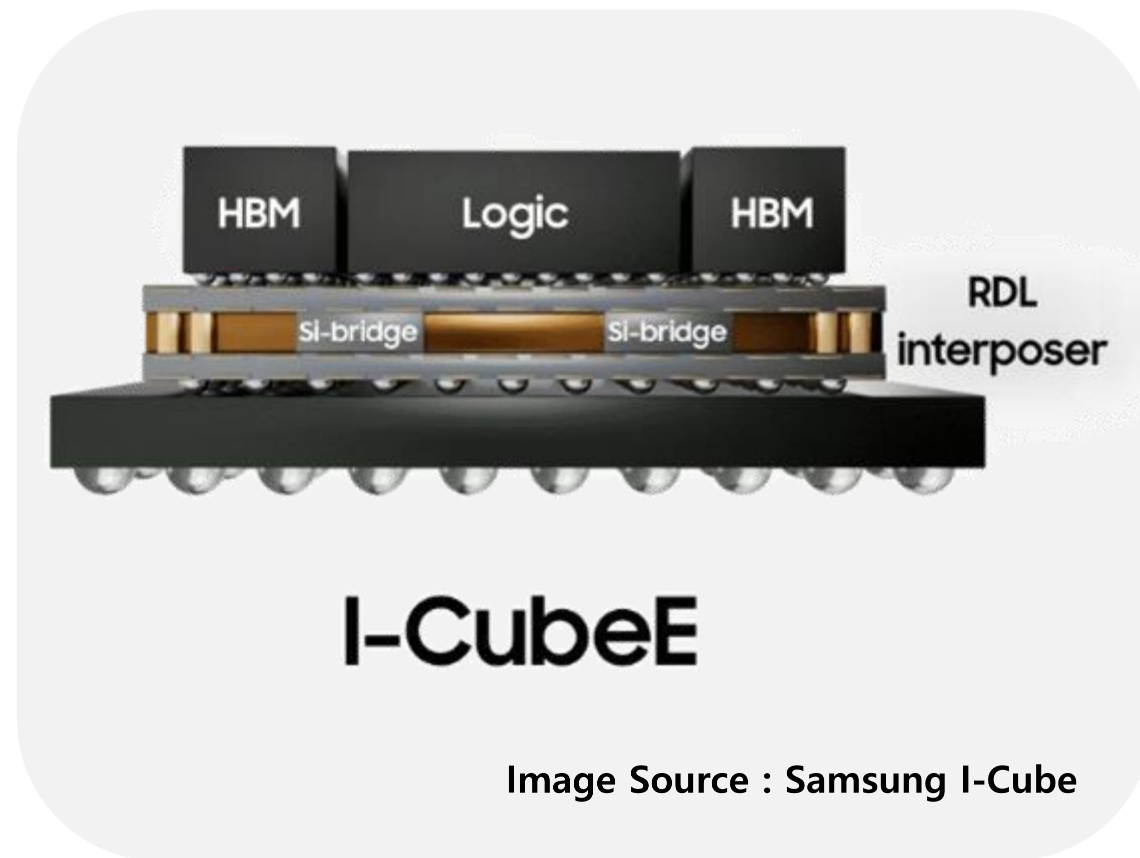
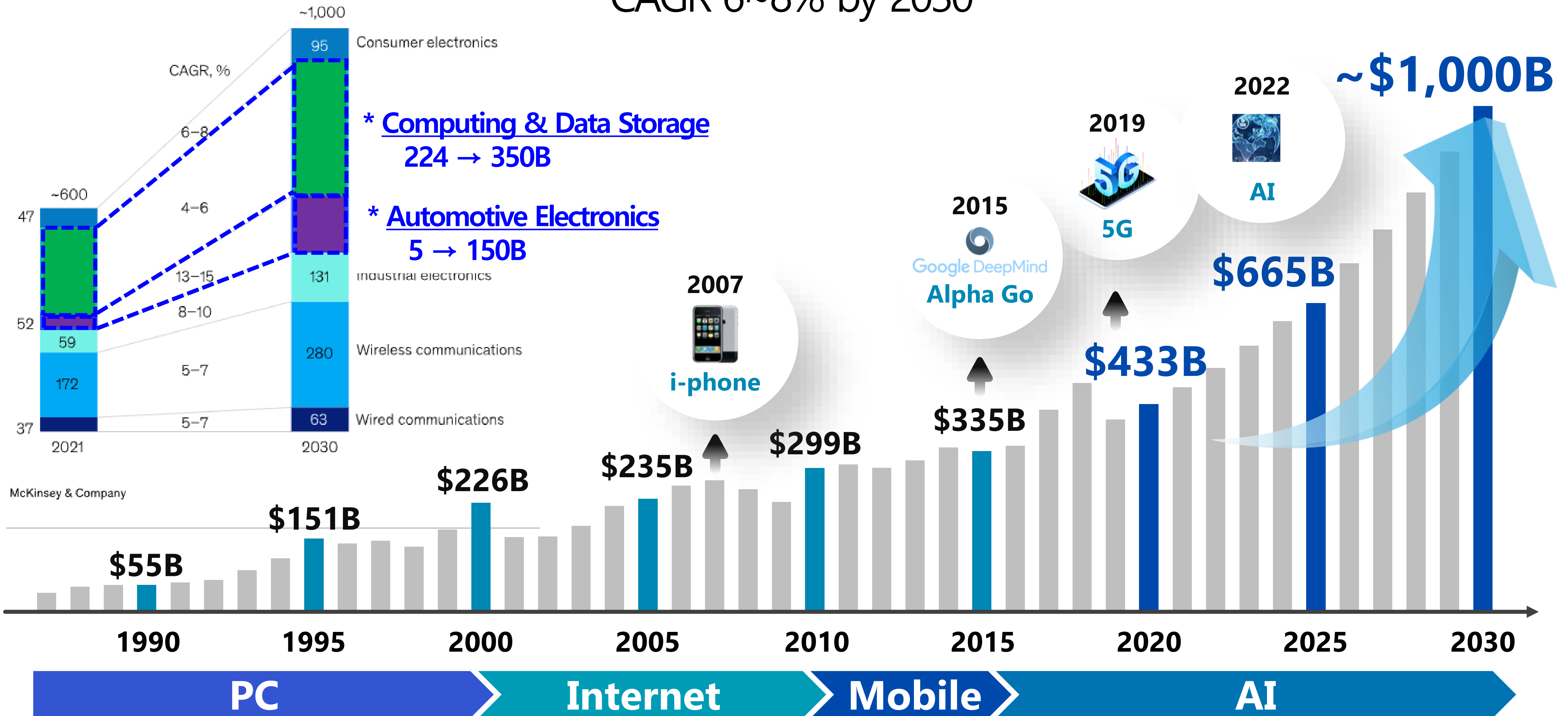


Image Source : Samsung I-Cube

SAMSUNG

Semiconductor Market Growth

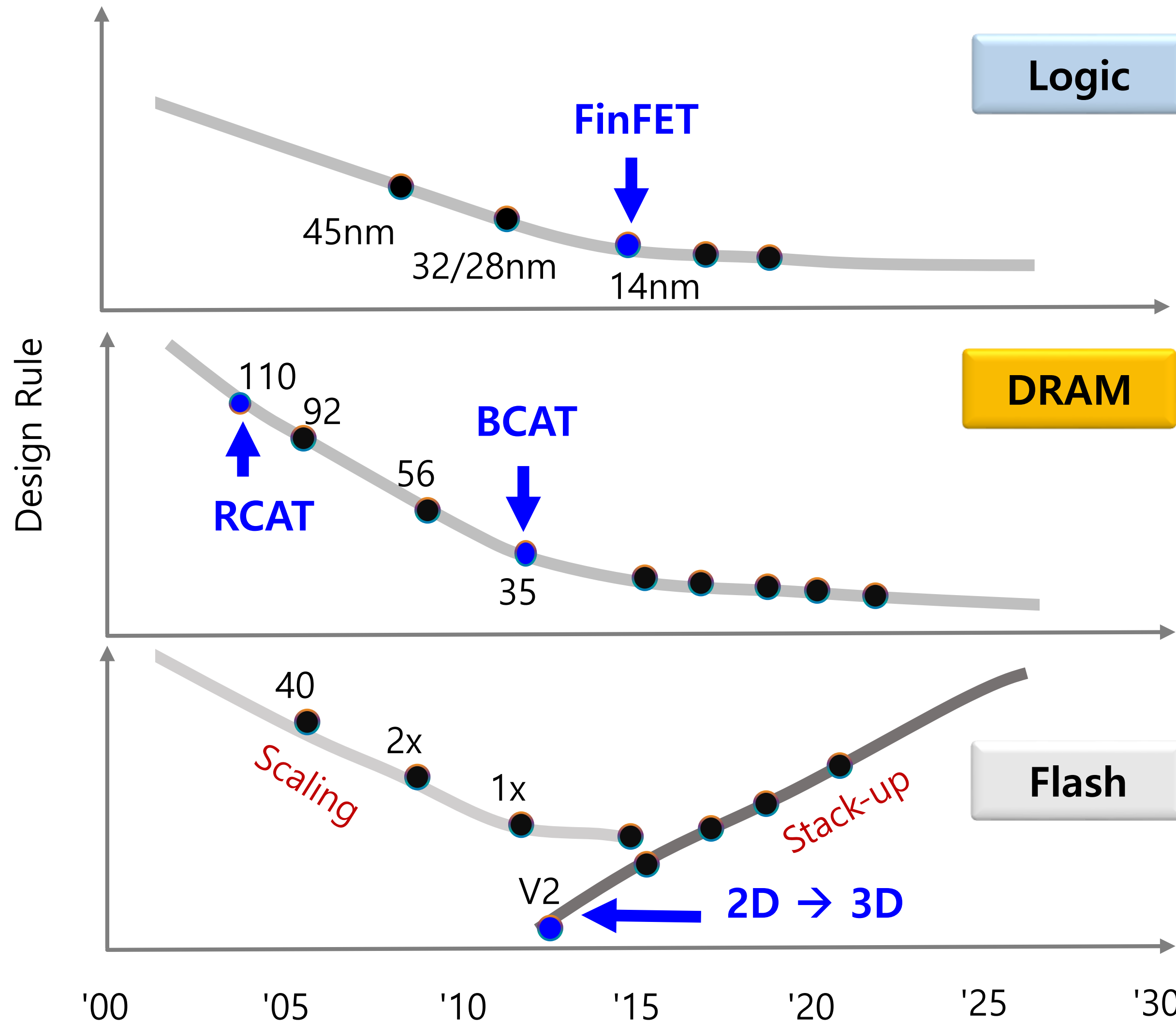


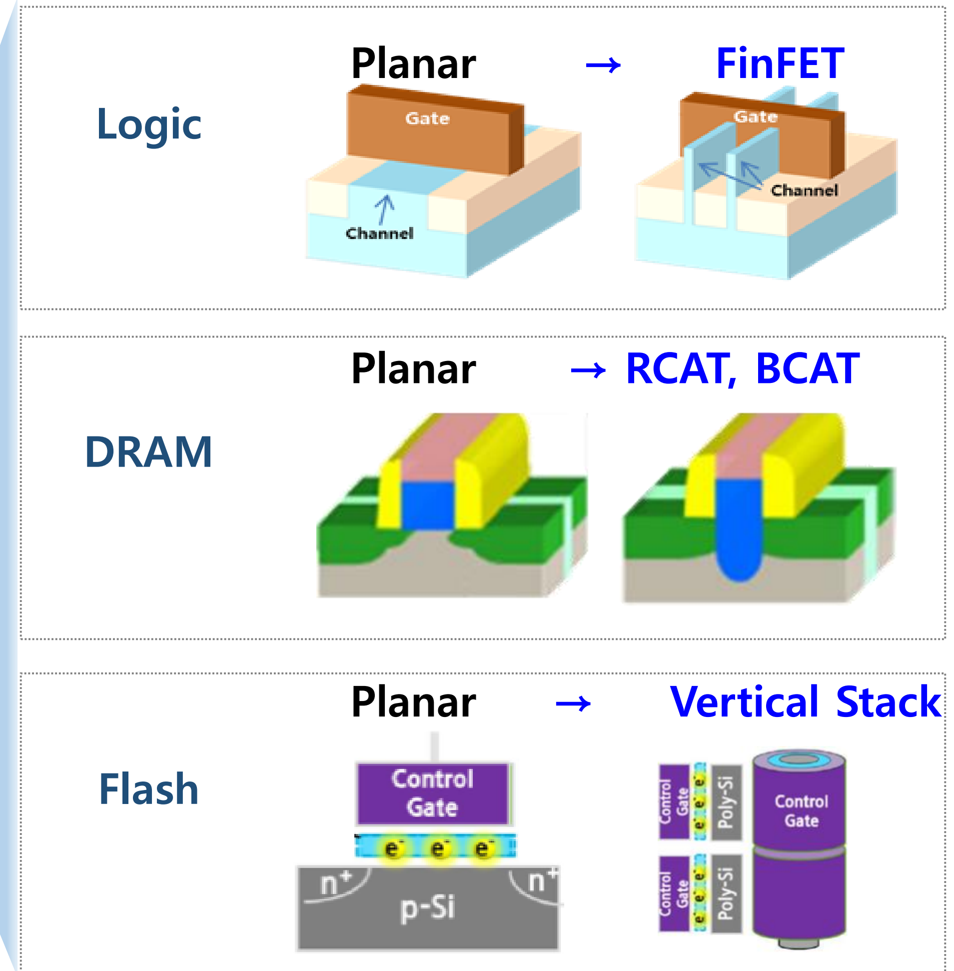
SAMSUNG

※ Source : Gartner/SEMII

Moore's Law Extended by Structure Innovations

Logic, DRAM, and Flash Transistors has changed from Planar to 3D Structures

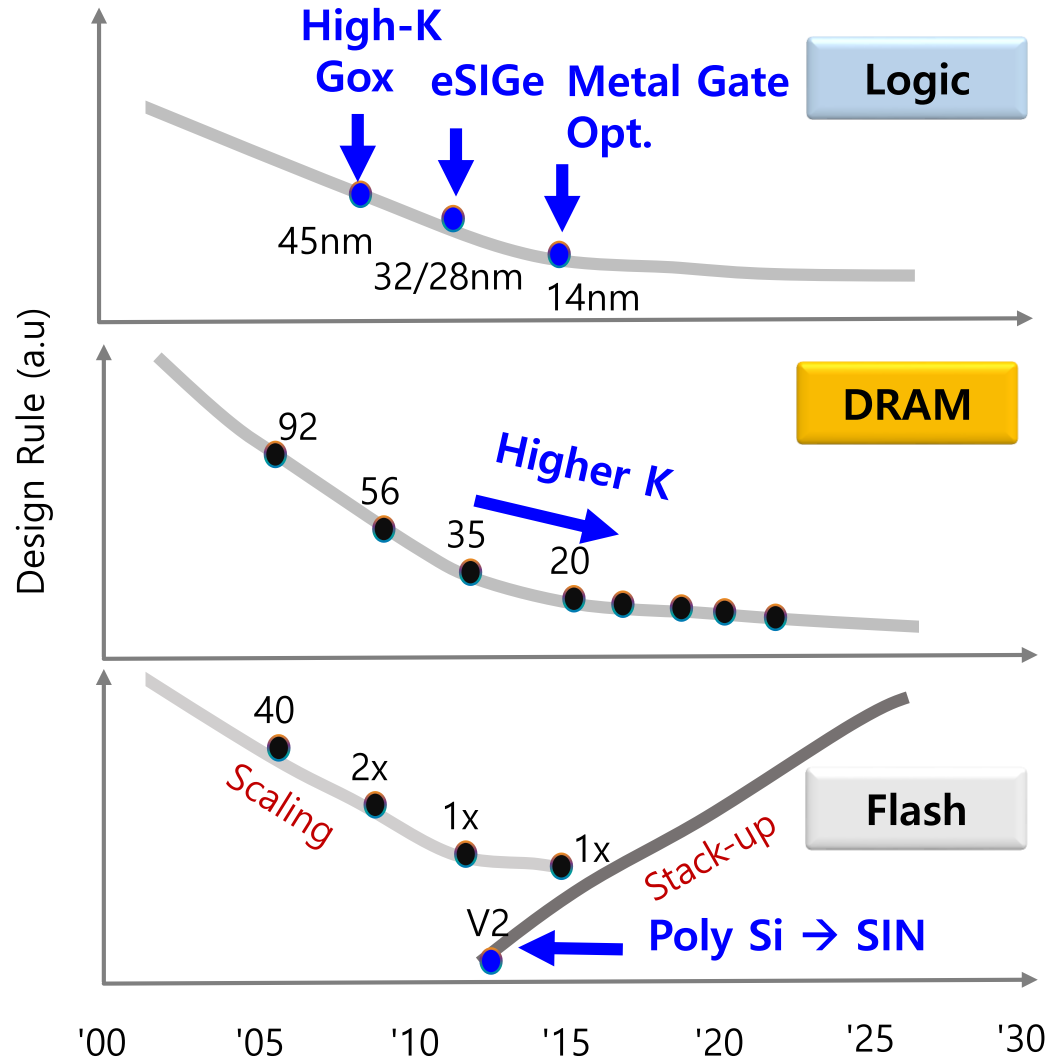




SAMSUNG

Moore's Law Extended by Material Innovations

High-K Dielectrics, SiGe Epi, Metal Gates, and New Gate Stack Integration



Logic Gate

High-K → eSiGe → Metal Gate

SiO_2 → HfO_2

TiAl, TiAlC, TiN, TiAlN

DRAM Capacitor

Flash Gate

Floating Poly → CTF

Floating Poly		CTF
Poly Si	Gate	TIN, W
ONO (Low-k)	Blocking	Al2O3 (High-k)
Poly Si	Storage	SIN
SiO2	Tunnel ox.	TBE
Crystalline Si	Channel	Poly Si

SAMSUNG

SAMSUNG

Upcoming Challenges and Innovations

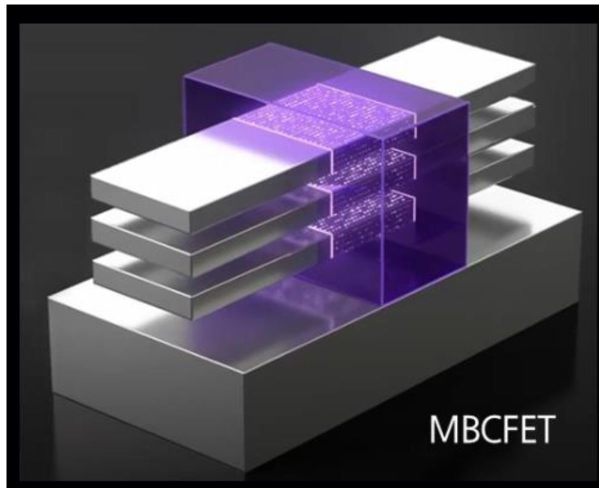
Prospects for Logic Transistor Beyond FinFET

Gate All Around Transistor followed by 3D Stack FET(CFET) and Others

3nm

World 1st 3nm GAA Transistor Samsung MBCFET ™

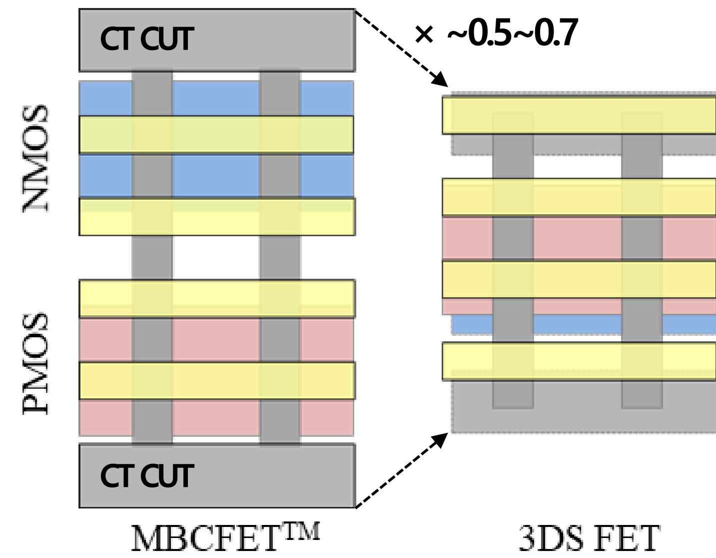
16% **Area Reduction**
45% **Power Saving,**
23% **Performance Improvement**
than 5nm FinFET



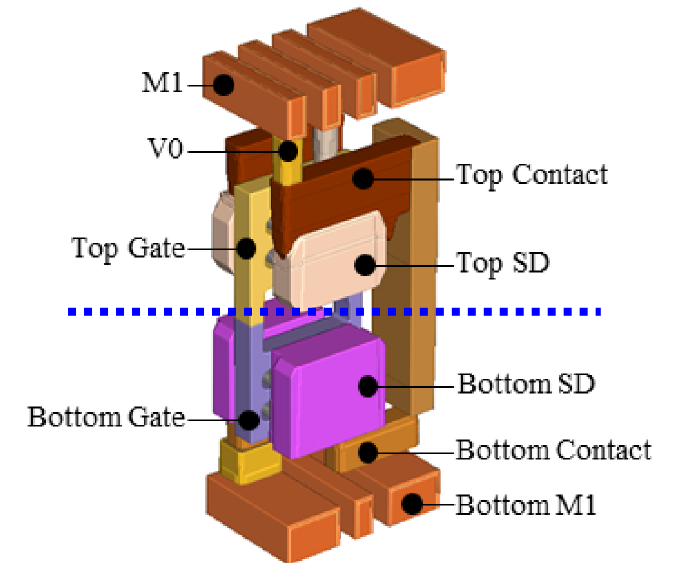
3D Stack FET(CFET) and Others

: NMOS and PMOS are Stacked Vertically
A Significant Area Reduction by up to half

[Layout Comparison]



[3D schematic]

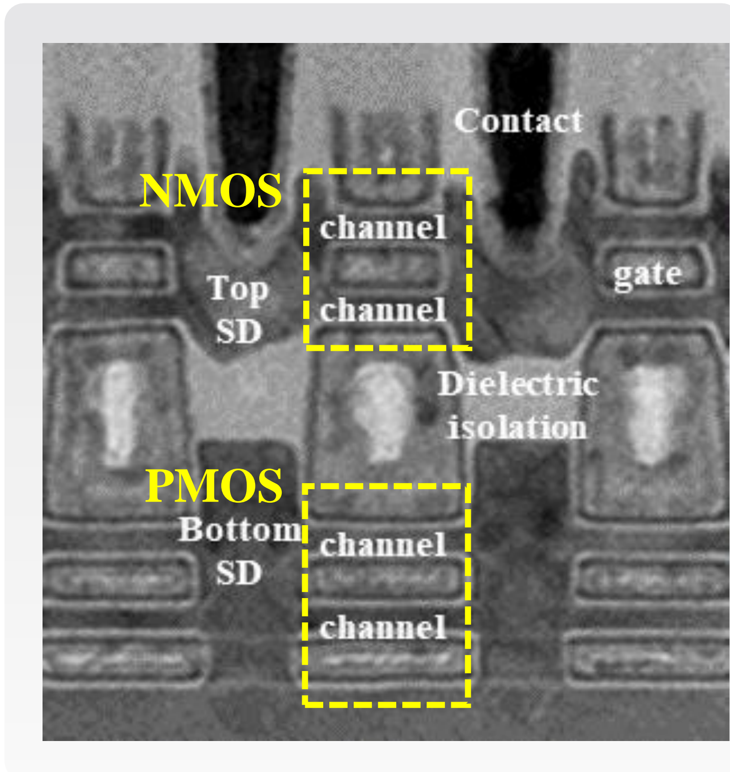


SAMSUNG

3D Stack FET in GAA Transistor Platform

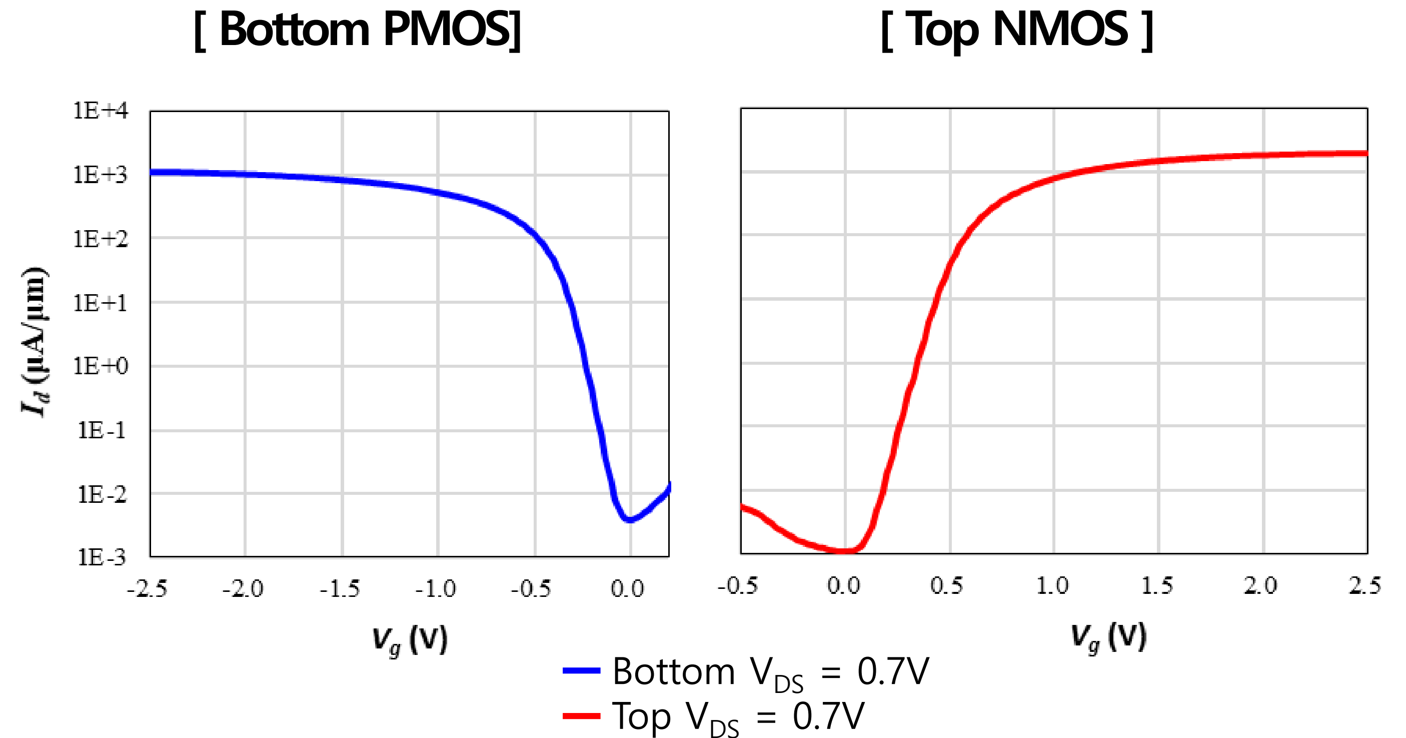
1st Successful Demonstration of Fabrication and Electrical Properties of Transistors

Vertical SEM View



'IEDM 23, JH Park, Samsung Electronics

Electrical Characterization

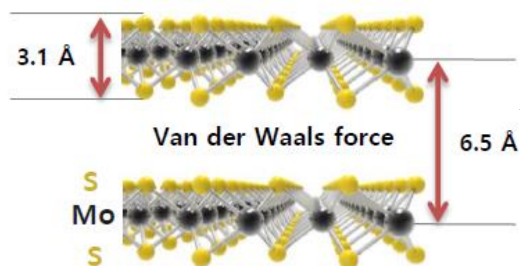


Beyond Si Channel Materials

Thin 2D Materials such as MoS2, WSe2 needs Entire Gate Stack Process Renovation

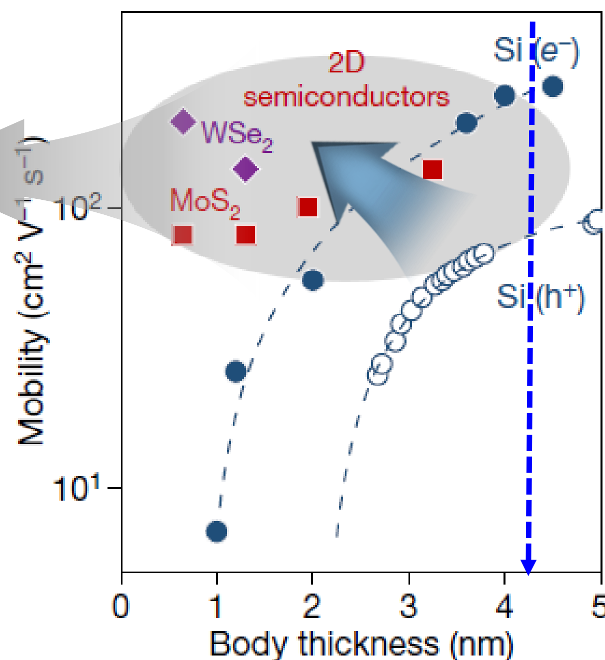
High Mobility Channel Materials

Higher Mobility 2D material > Si (@ same THK)



Y. Liu *et al.*, Nature comm., 591, 43 (2021)

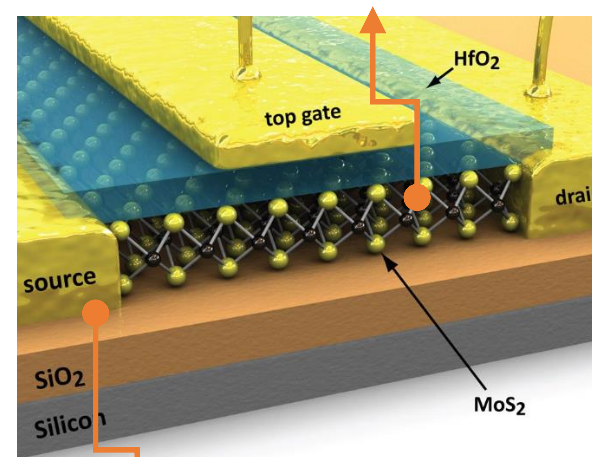
3nm GAA Transistor



Process Integration Challenges

Growth of Channel Material

- Large-area growth with low defect density
- Low-temp synthesis for BEOL applications



Gate Oxide Formation

- Weak adhesion of insulators

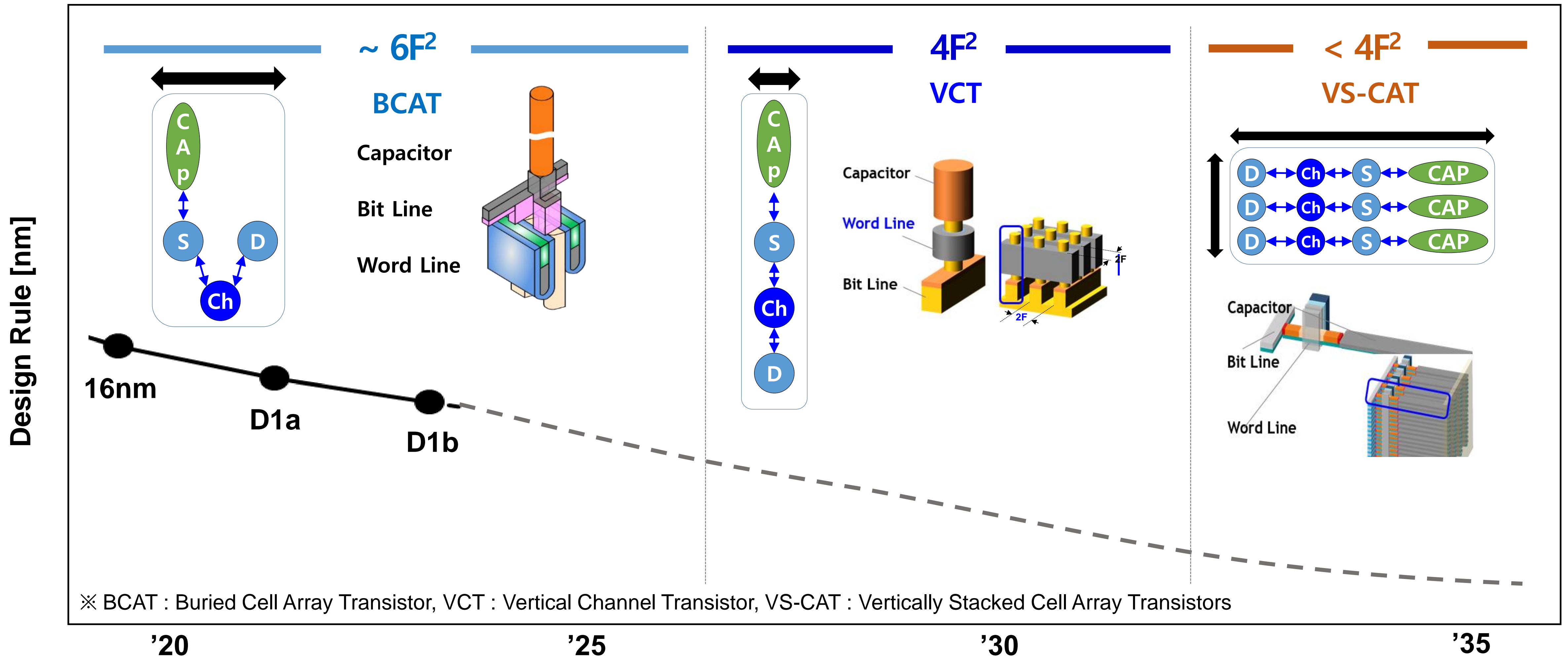
Source-Drain Contacts

- P-type doping and contacts

* Image from EPFL Laboratory of Nanoscale Electronics and Structures (LANES)

Prospects for DRAM Cell Beyond 10nm

Area Scaling Continues via Vertical Channel Transistor or Vertically Stacked Cell Array

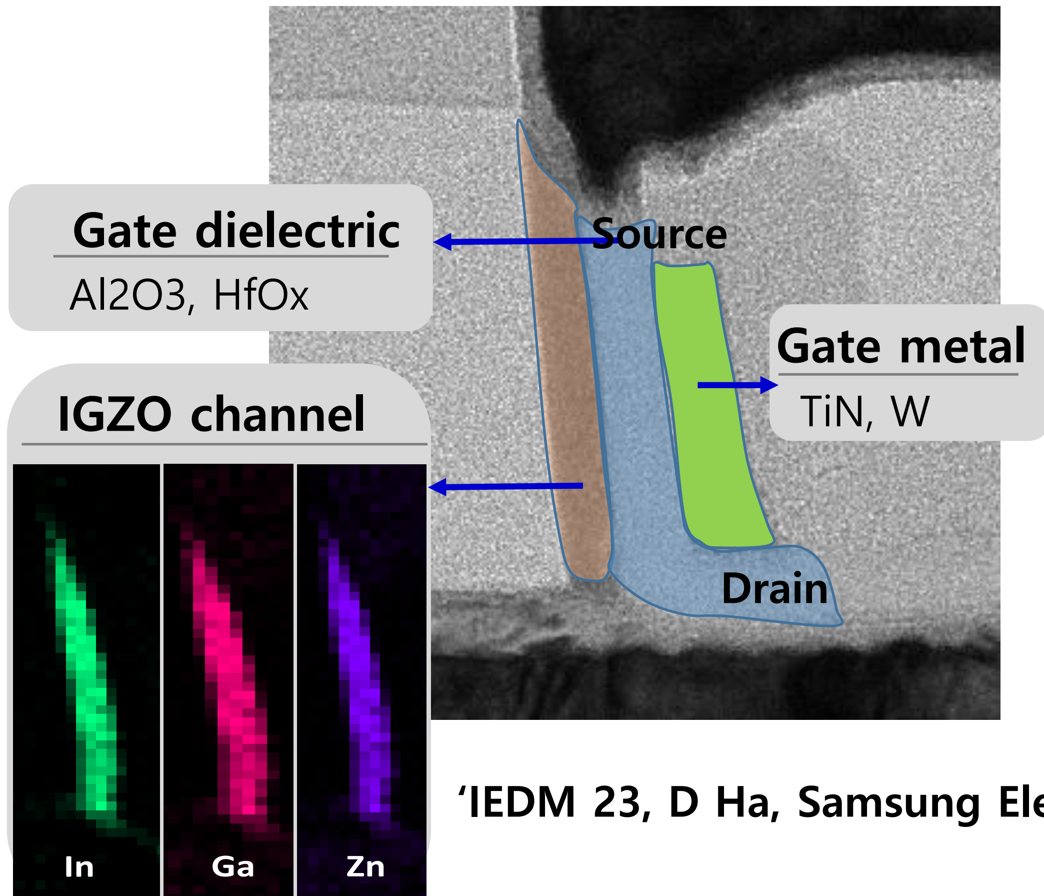


SAMSUNG

Vertical Channel Transistor

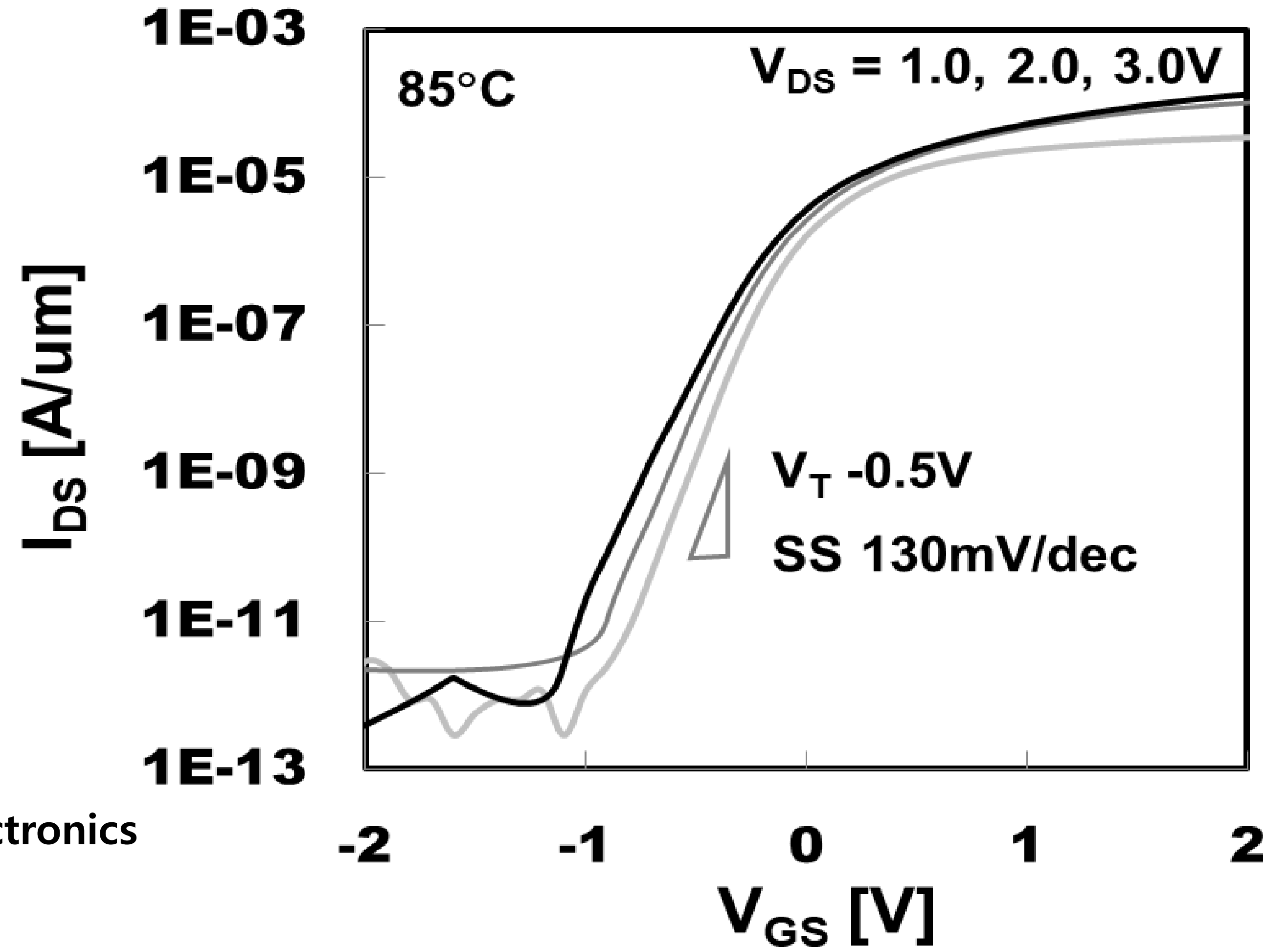
Successful Demonstration with Non-Silicon Channel(IGZO) Transistor

Vertical SEM View



'IEDM 23, D Ha, Samsung Electronics

Electrical Characterization



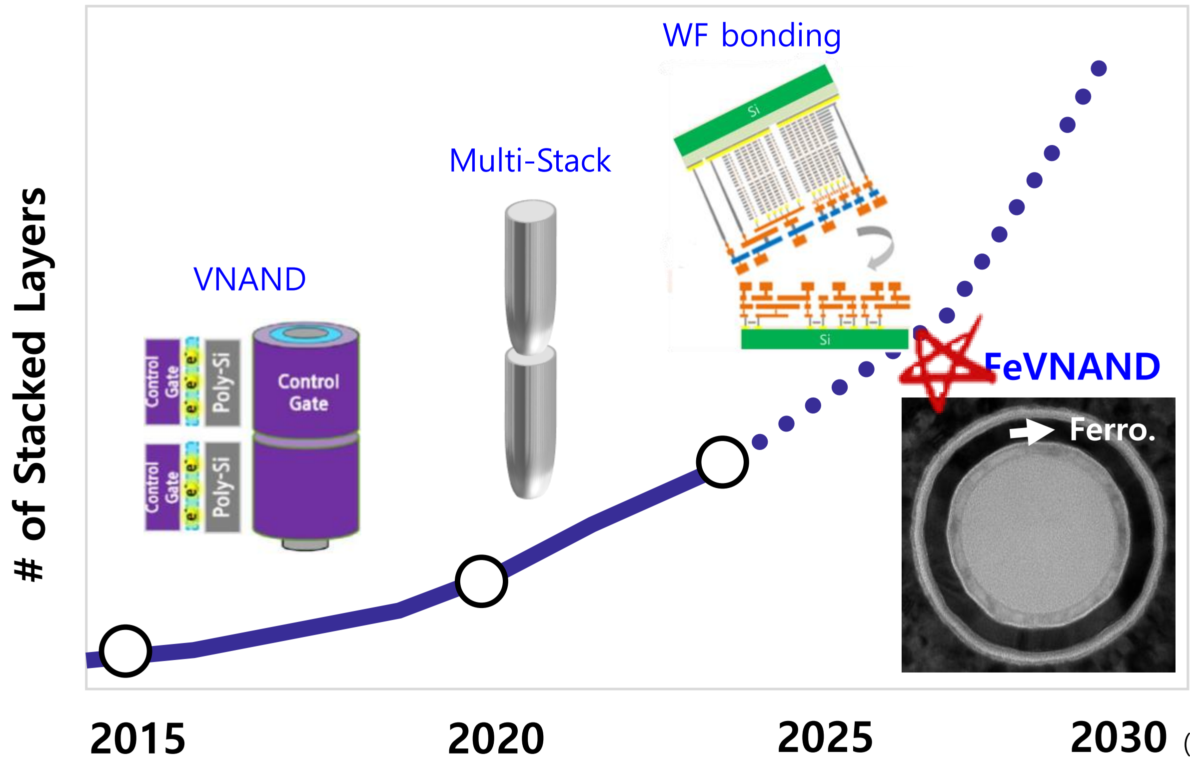
SAMSUNG

Prospects for Non-Volatile Memories

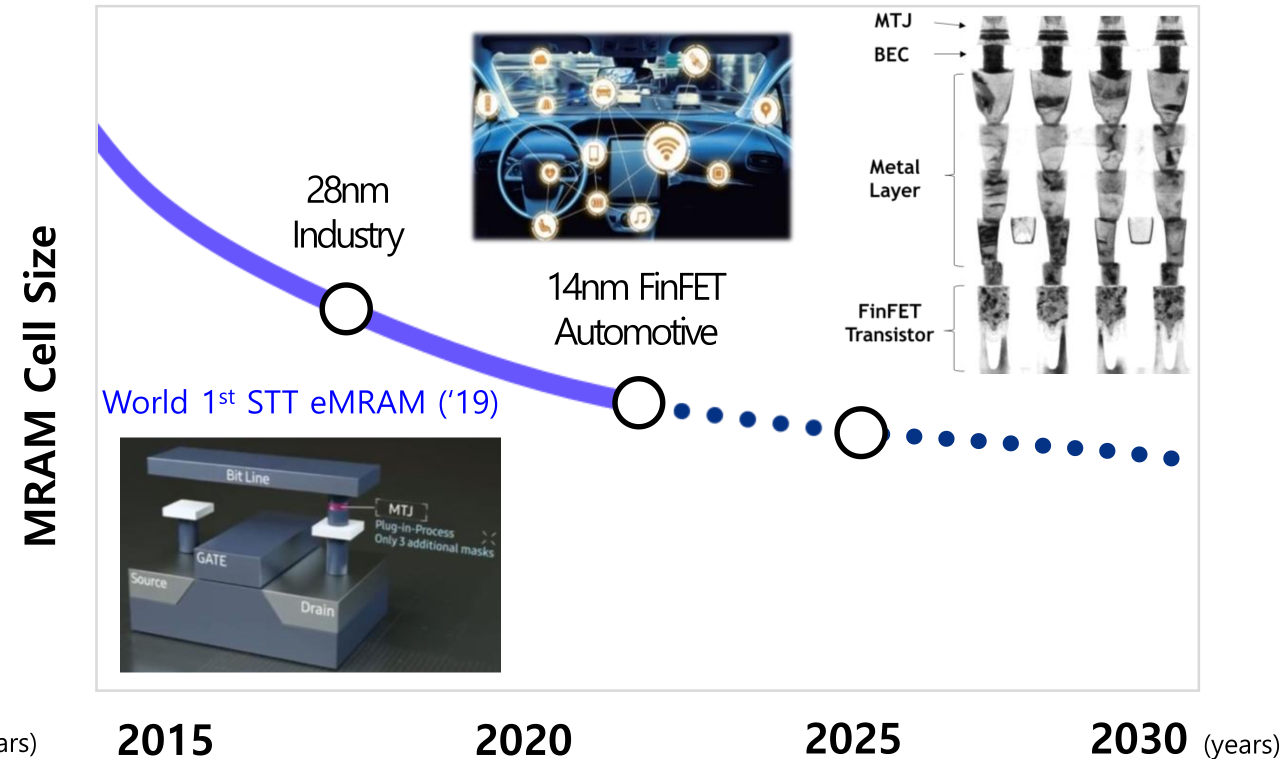
VNAND Continues to Stack Up with Cell-Peri Bonding and New Storage Media Adoption

Embedded MRAM Continues to Shrink with MTJ Stack and Process Innovations

VNAND Flash



Embedded MRAM



SAMSUNG

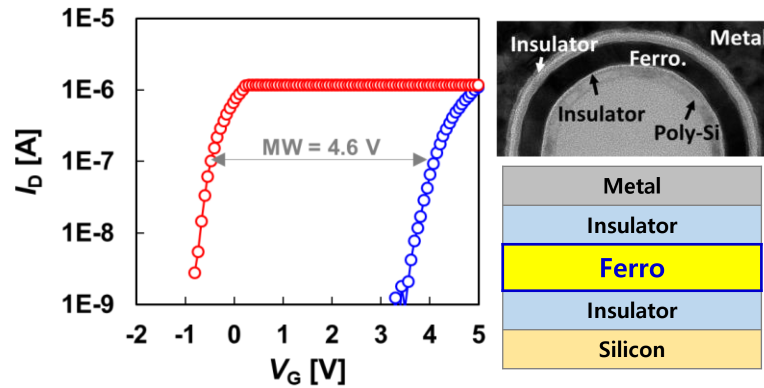
Emerging Technologies for Non-Volatile Memories

Research and Developments Activities With Various Materials and Process Innovations

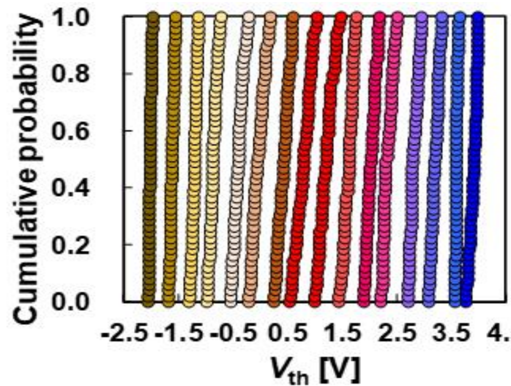
Fe-VNAND

* Ferroelectric VNAND

Memory Window



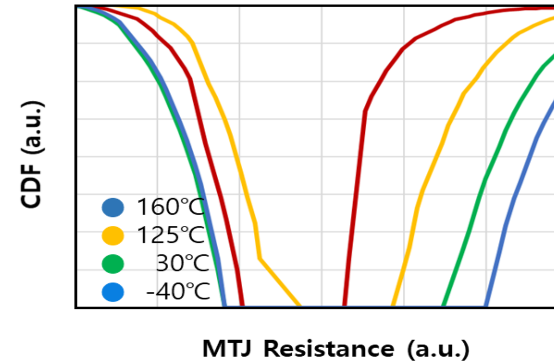
QLC Feasibility



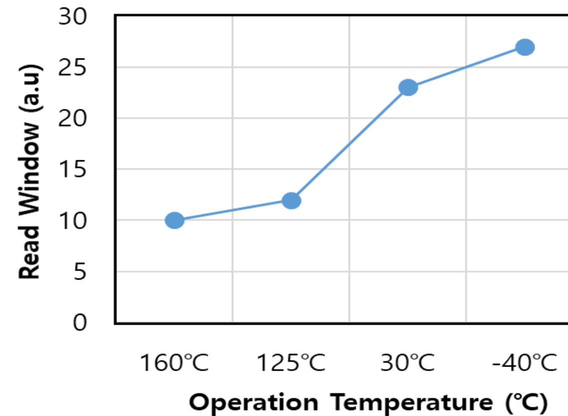
IEDM 23, S Lim, Samsung Electronics

Embedded MRAM

CDF



Read Window

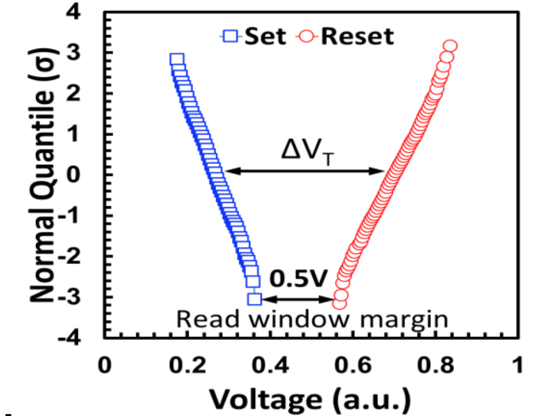


VLSI 23, S Ko, Samsung Electronics

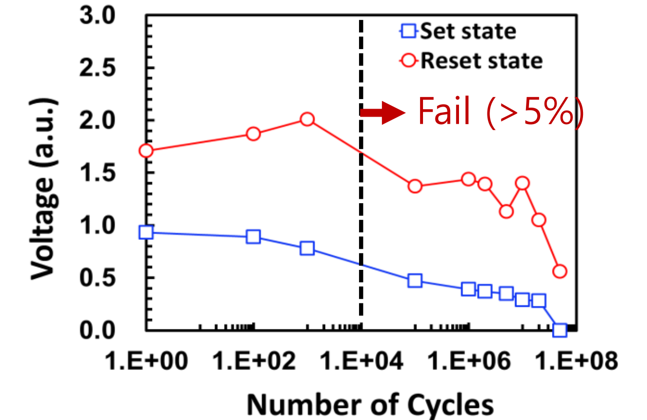
SOM

*Selector-Only-Memory

Read Window



Endurance



IEDM 23, I Park, Samsung Electronics

SAMSUNG

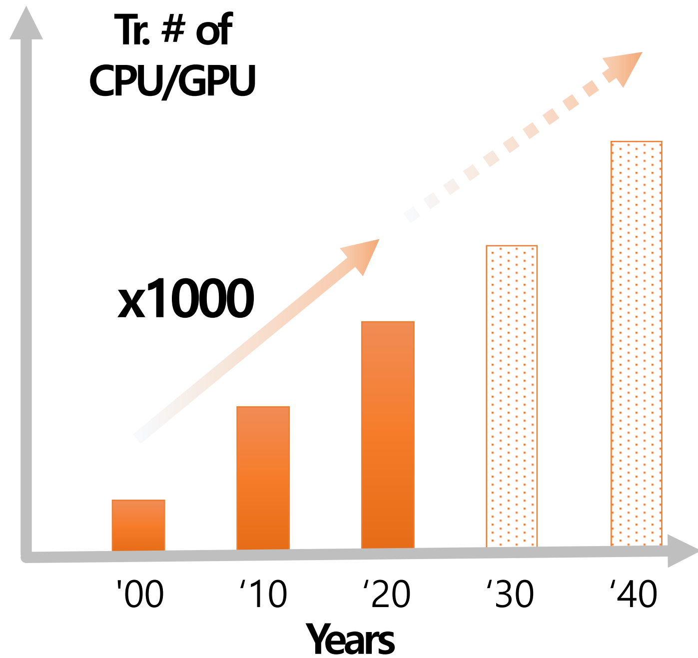
Conclusion

SAMSUNG

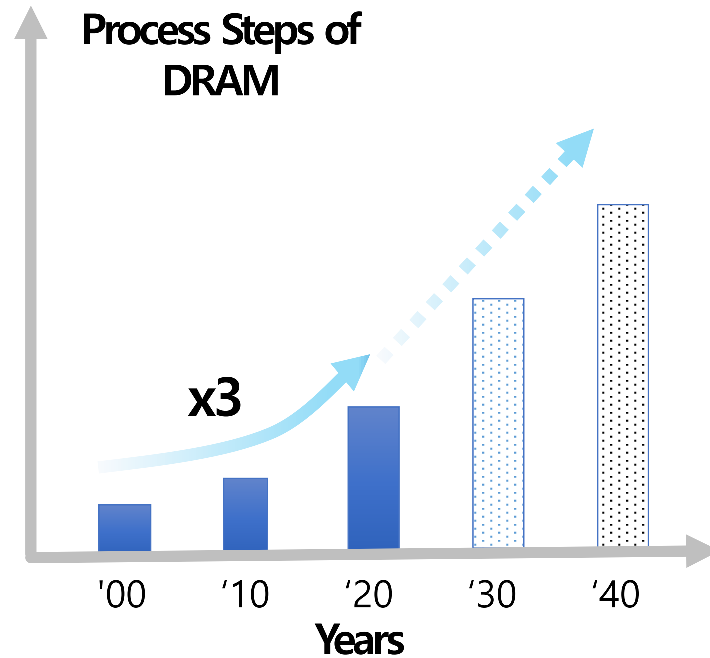
Another Challenges faced by Semiconductor Industry

More Complex, More Difficult, More Expensive

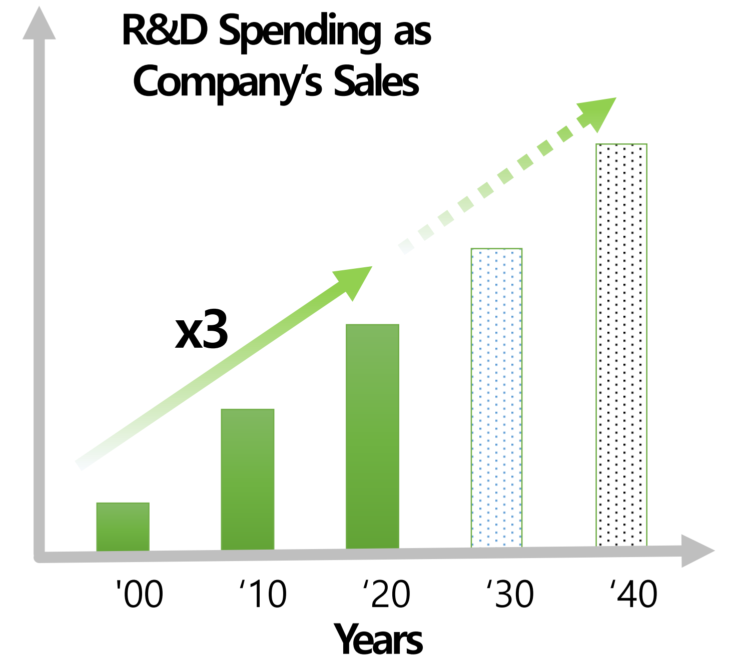
Design Complexity



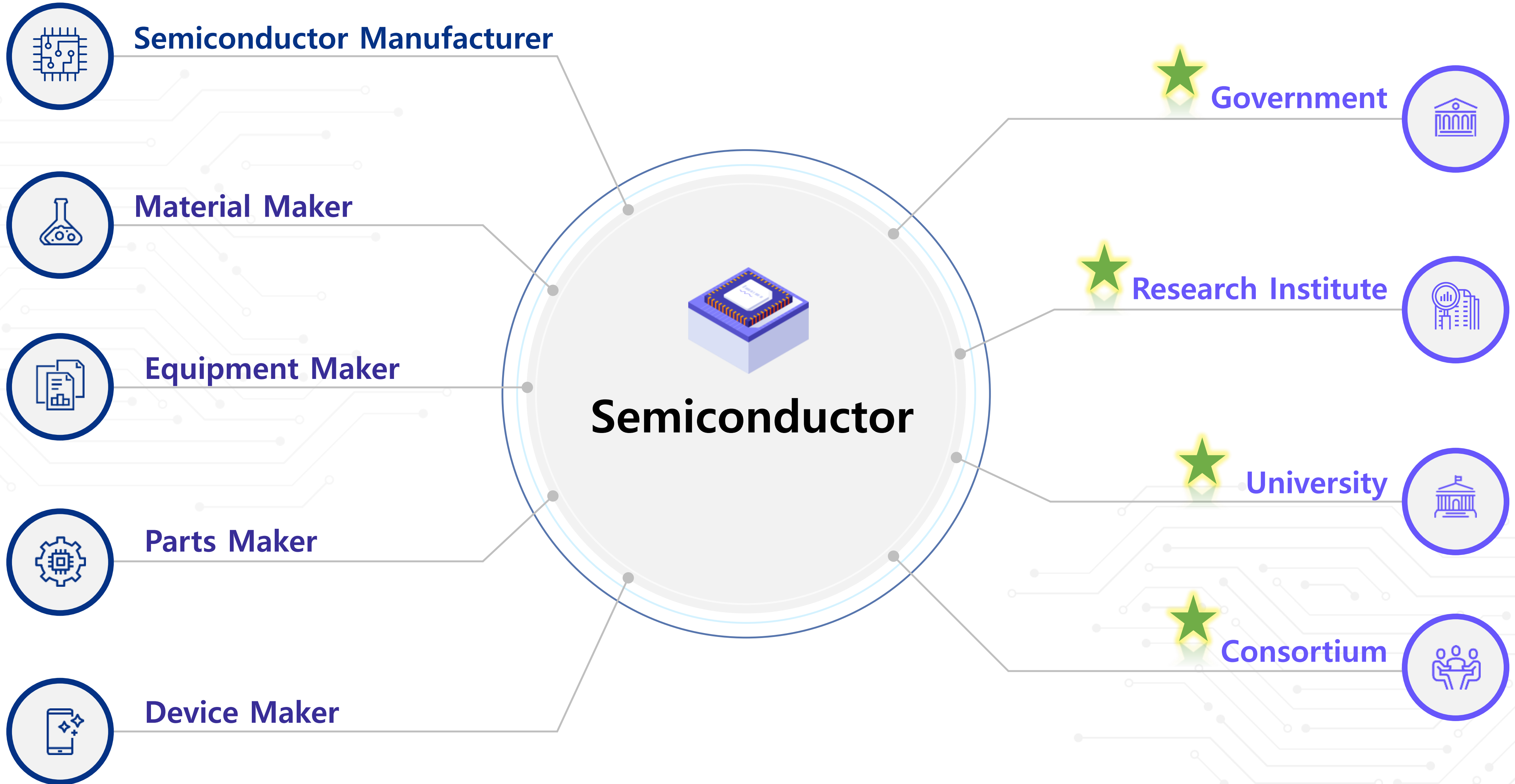
Process Difficulty



R&D Expenditure



Co-operative Global ECO system



SAMSUNG

Thank You