EU - SOUTH KOREA – Joint Researchers Forum on Semiconductors

Advanced compute scaling: a new era of exciting innovations with nanosheet-based devices and increased interdisciplinary synergies

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imec

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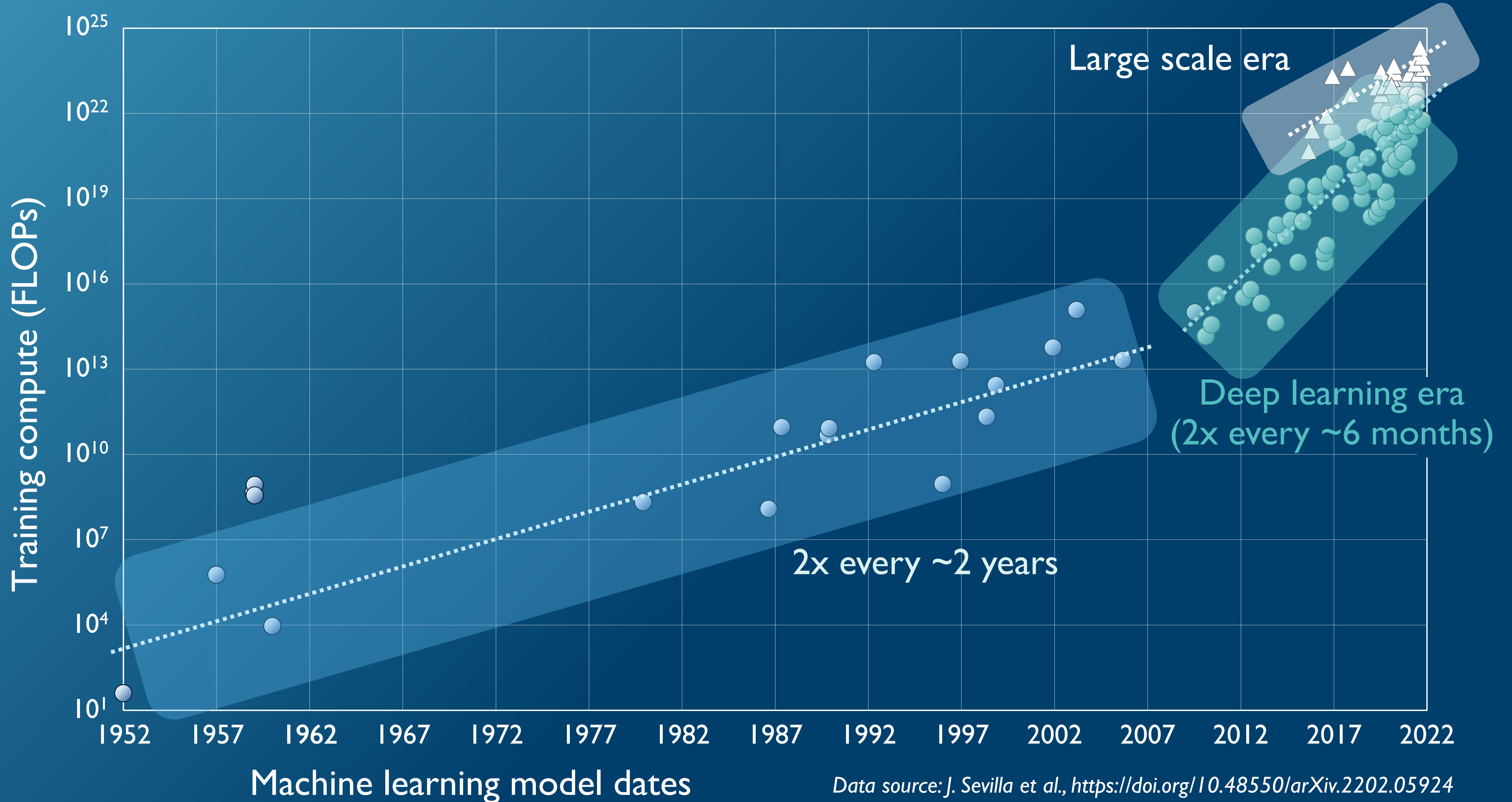
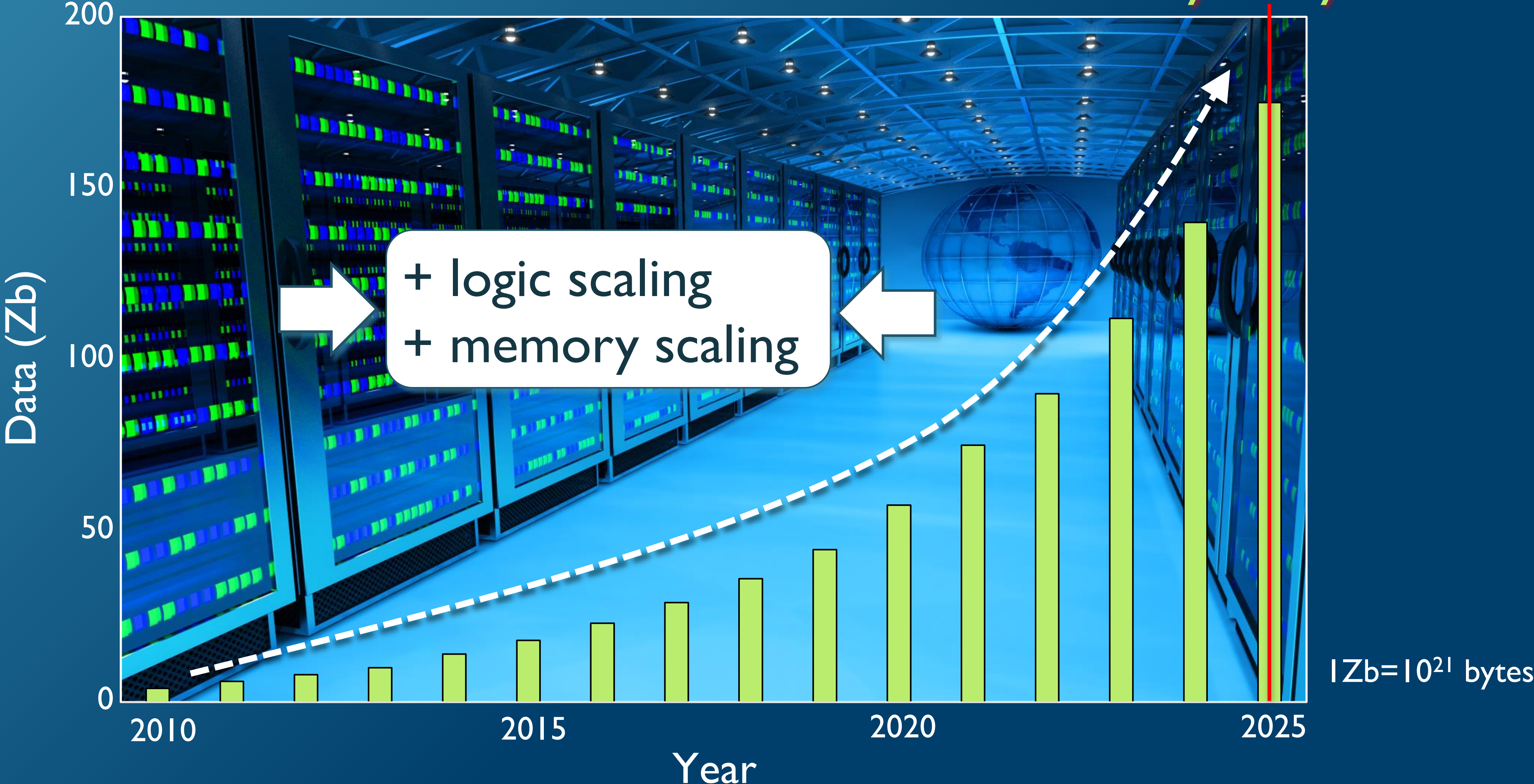
Outline

- ❑ Introduction
- ❑ Potential logic scaling roadmap
- ❑ Evolution of transistor device architecture:
  - ➢ entering the nanosheet-based FETs device era
- ❑ Introduction of scaling structural boosters like backside power delivery
  - ➢ paving the way towards a truly functional backside
- ❑ New STCO opportunities with the move CMOS → CMOS 2.0
- ❑ Some key takeaways

Compute needs continue to grow at an ultra-fast speed



Global data growth ⇒ requiring more and more density

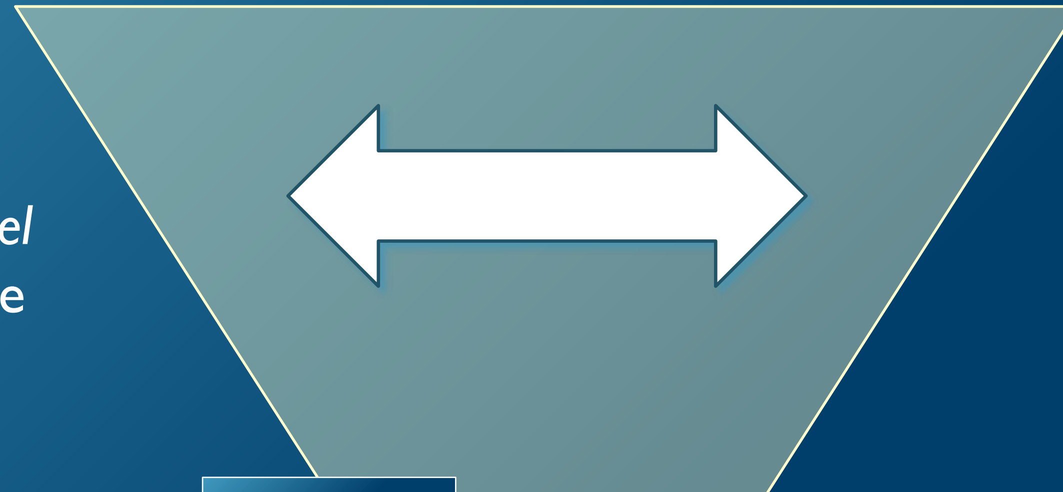


Source: *Data Age 2025, IDC Global DataSphere, May 2020*

Compute systems: evolution towards smart disintegration

TECHNOLOGY

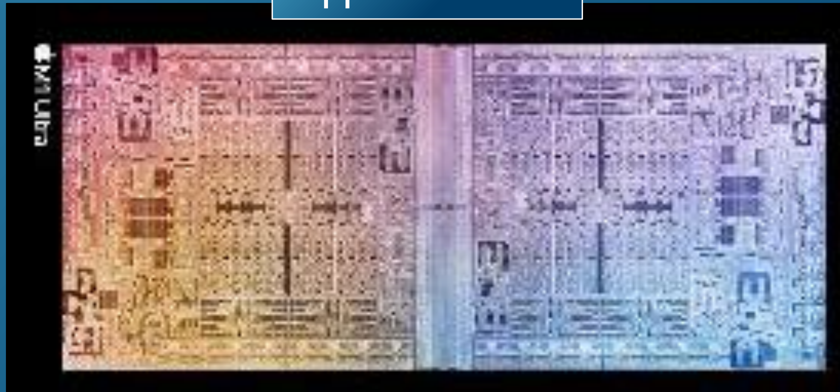
Advanced interconnect solutions offering *SoC-level* connectivity performance



APPLICATION

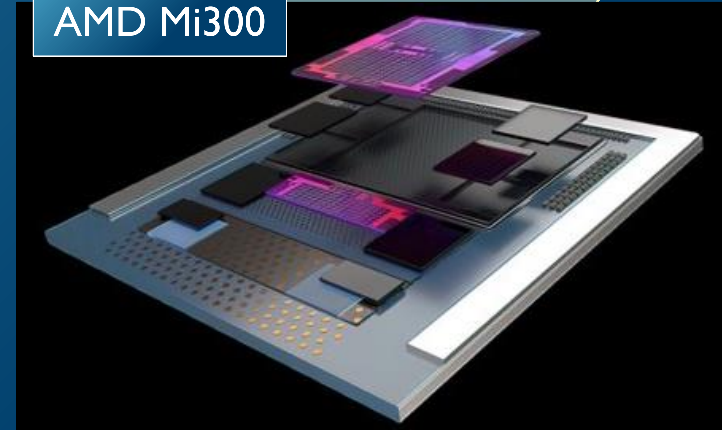
Diversity of applications requiring ever increasing compute and memory resources

Apple M1 Ultra



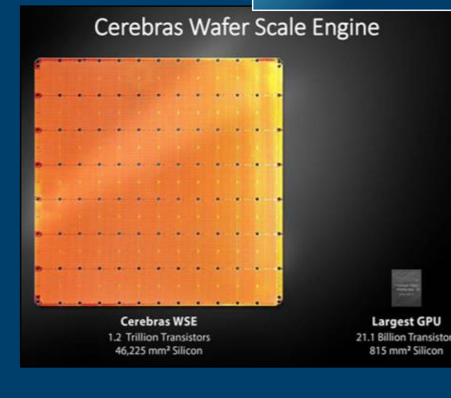
HP Mobile

AMD Mi300



HPC

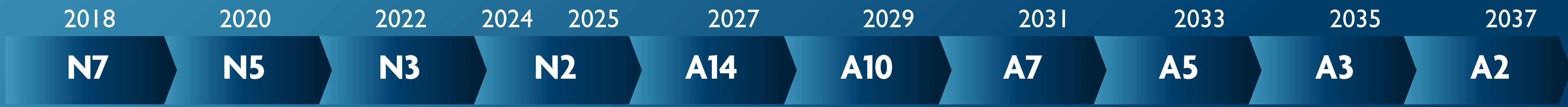
Cerebras



Nvidia H100

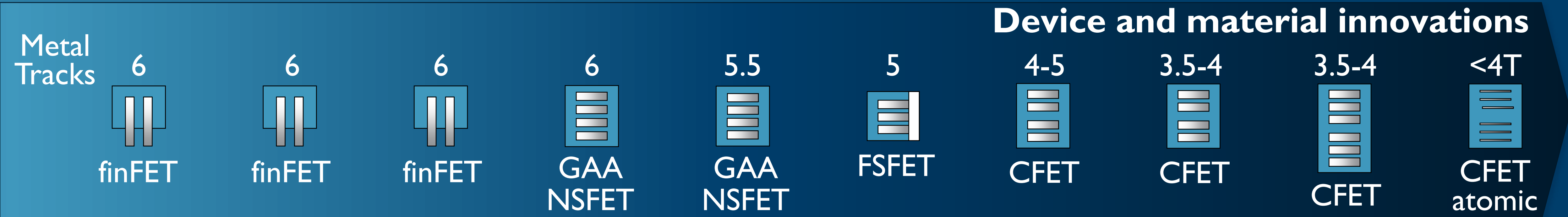
AI/GPU

Potential logic scaling roadmap extension



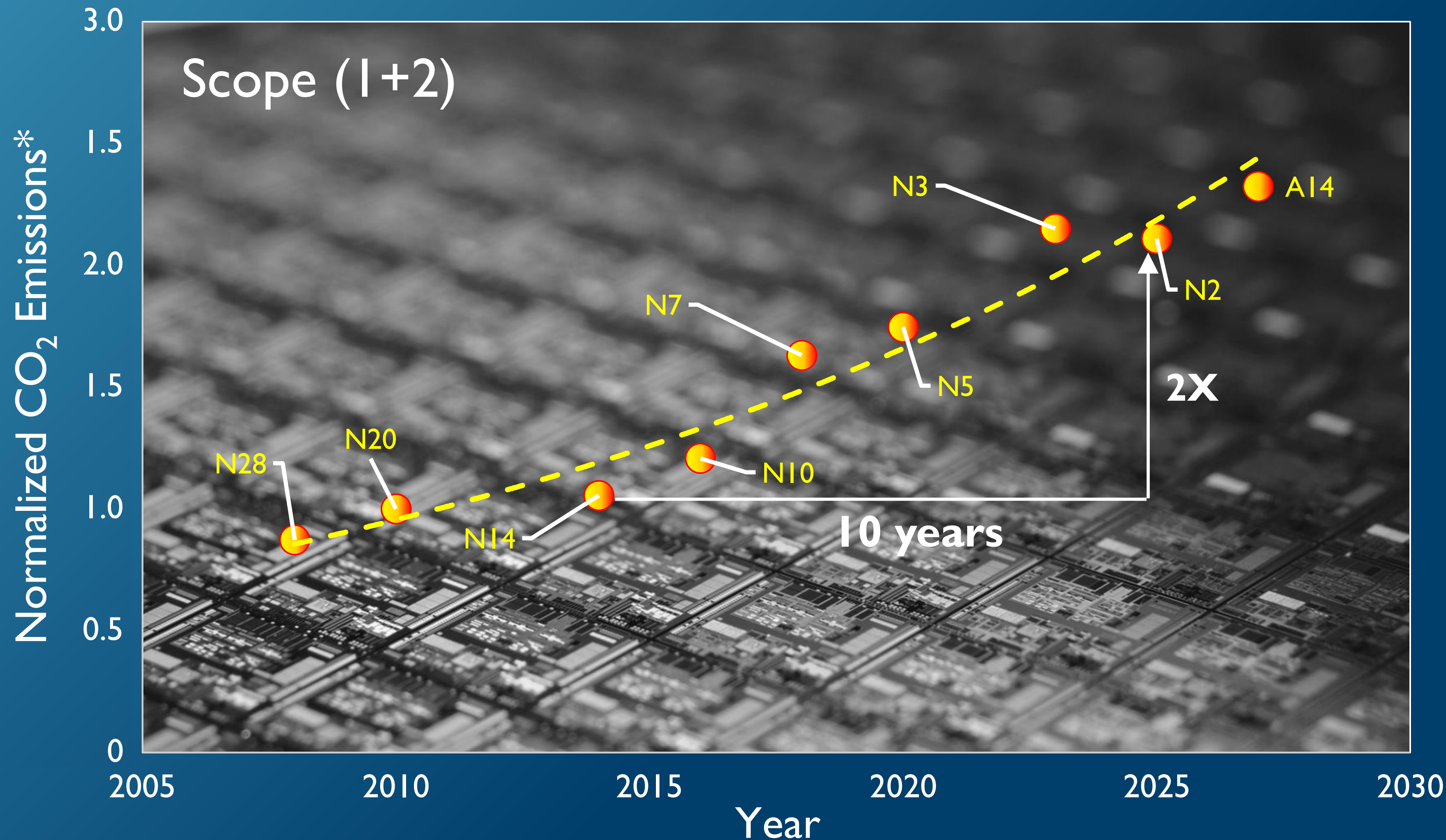
Metal Pitch (nm) 40 28 23-26 22 21 18 16-18 14-18 12-16 12-16

Continued dimensional scaling



imec

CO_2 emissions in recent logic nodes have been increasing ⇒ adding environmental impact as a technology FOM: PPAC-E

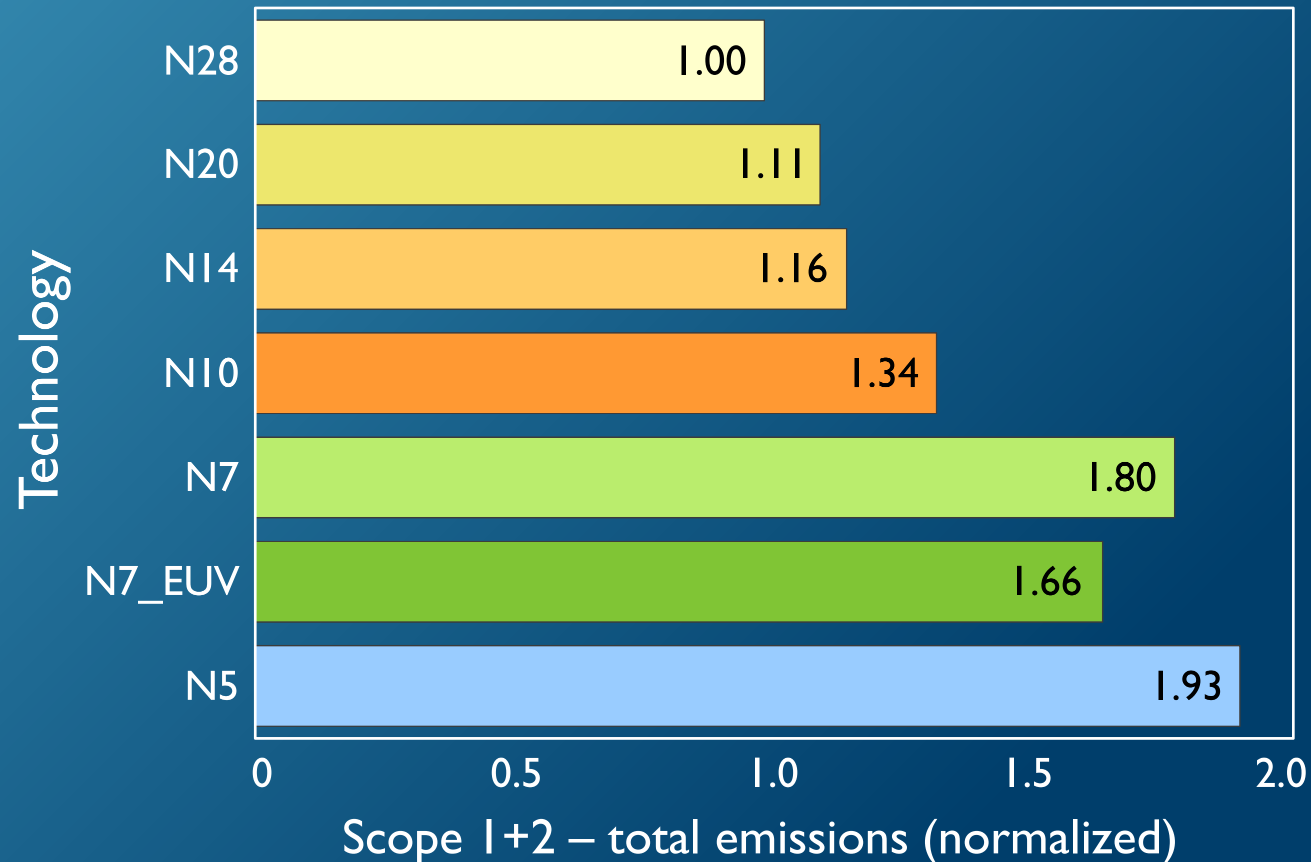


*imec.netzero: emissions estimate of imec process nodes representative of foundry nodes

0.49kgCO_2eq/kWh assumption for electricity

Photo by Laura Ockel on Unsplash

Public version of imec.***netzero*** released on June 30th 2023

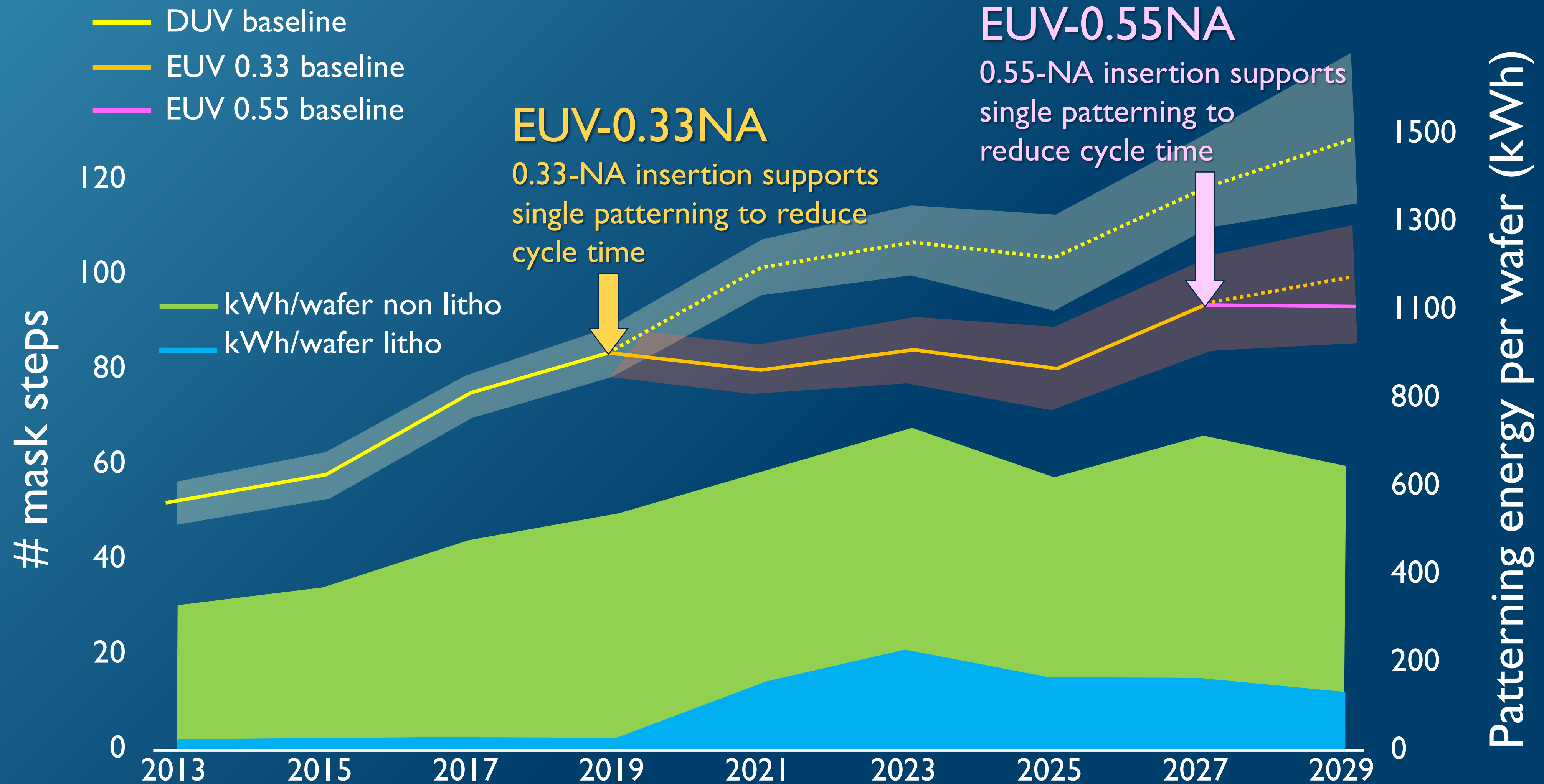


- imec.**netzero** is a Web App by imec's SSTS* program – it quantifies the environmental impact of manufacturing IC chips in a HVM fab
  - with this tool, imec aims to help identify and classify high-impact environmental challenges in the industry

- go to https://netzero.imec-int.com and sign-up for imec.**netzero**

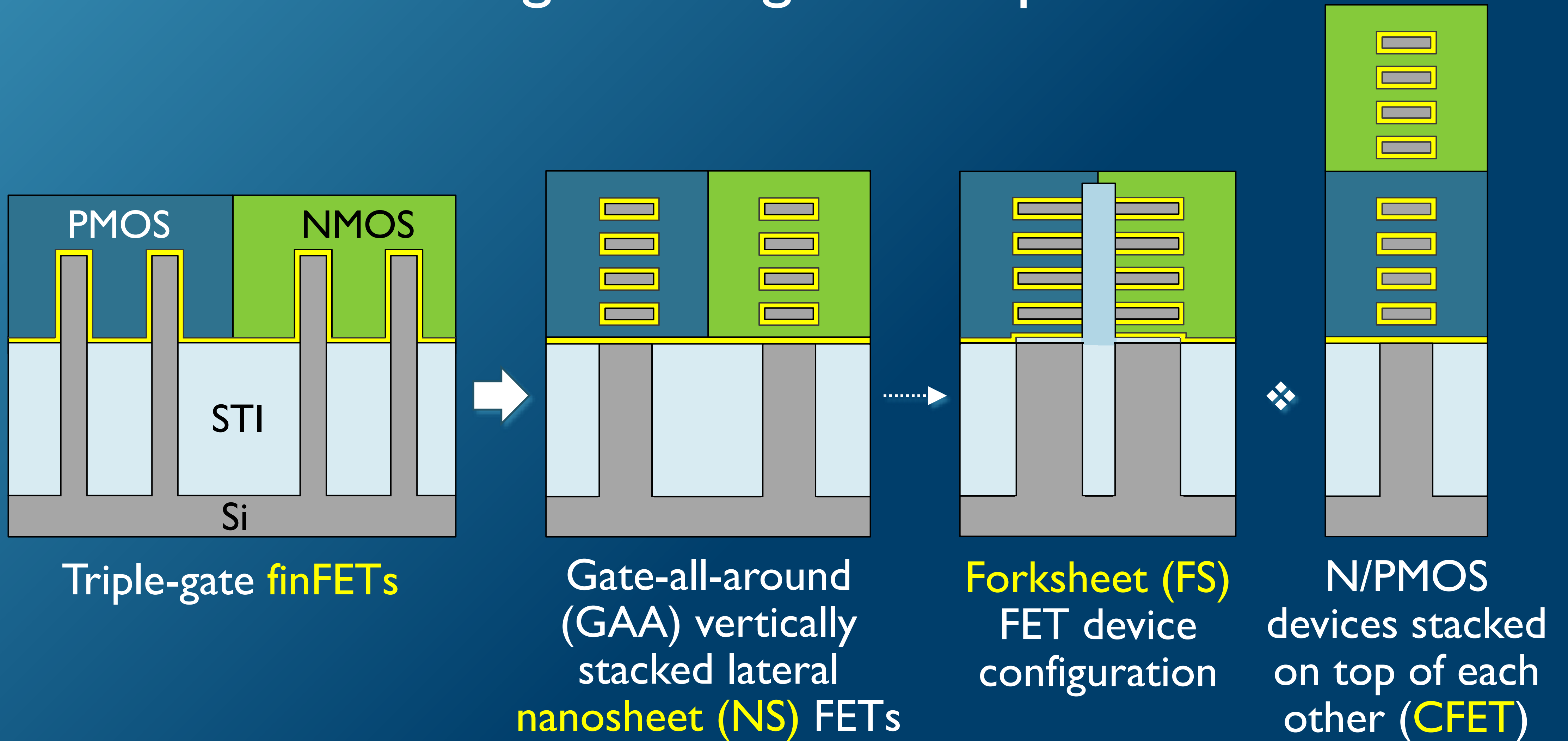
* Sustainable Semiconductor Technologies & Systems

EUV/High-NA EUV lithography key for enabling cost-effective scaling and lower energy consumption



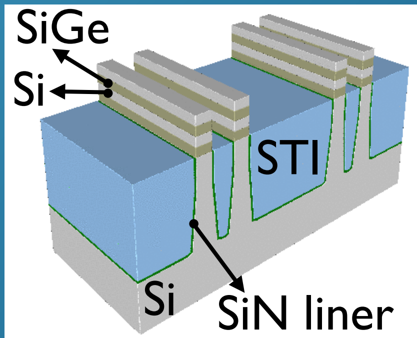
M. van den Brink, ASML @ plenary talk at VLSI Symposium 2022

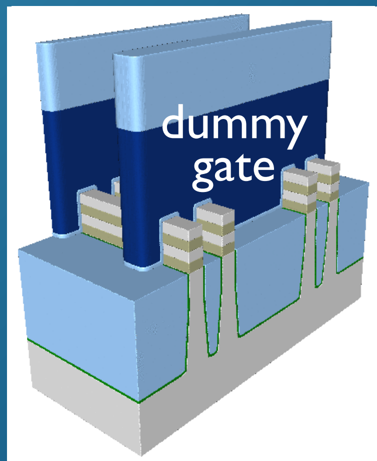
A possible transistor's evolution path to help support the logic scaling roadmap



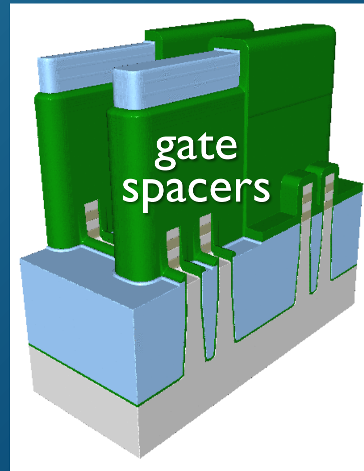
Some key fabrication steps to build GAA nanosheet FETs

fins formation with Si/SiGe multi-layers

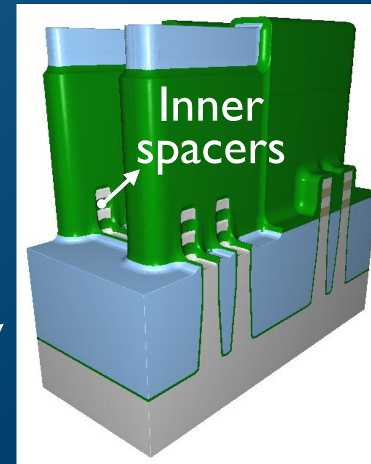




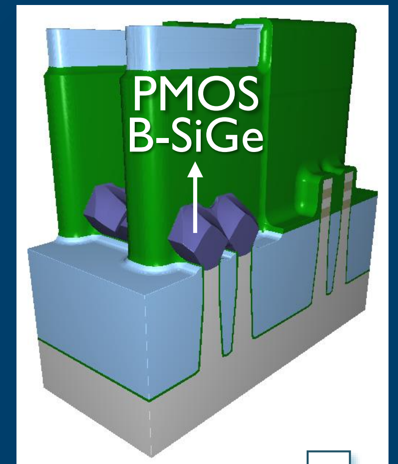
dummy gate patterning

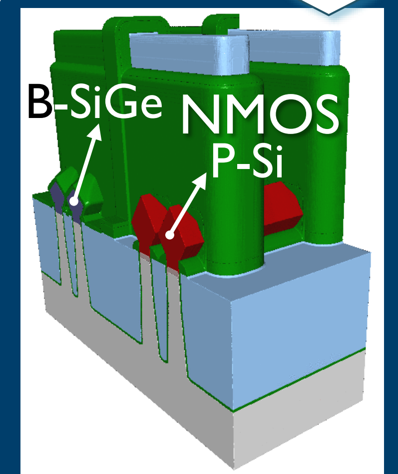


gate spacers formation

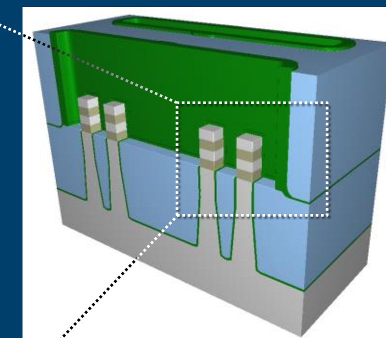


inner spacers formation

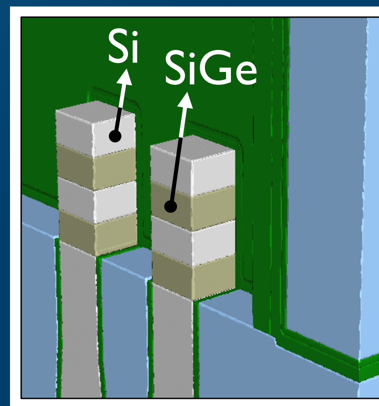


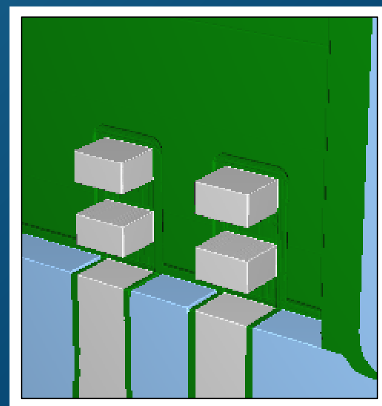


S/D epitaxial growth

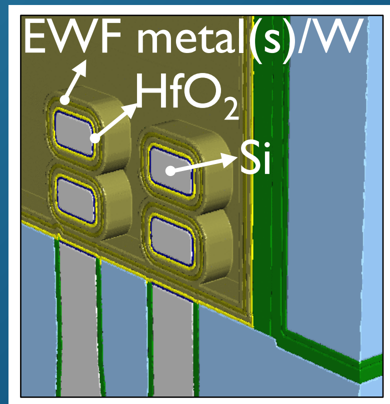


dummy gate removal



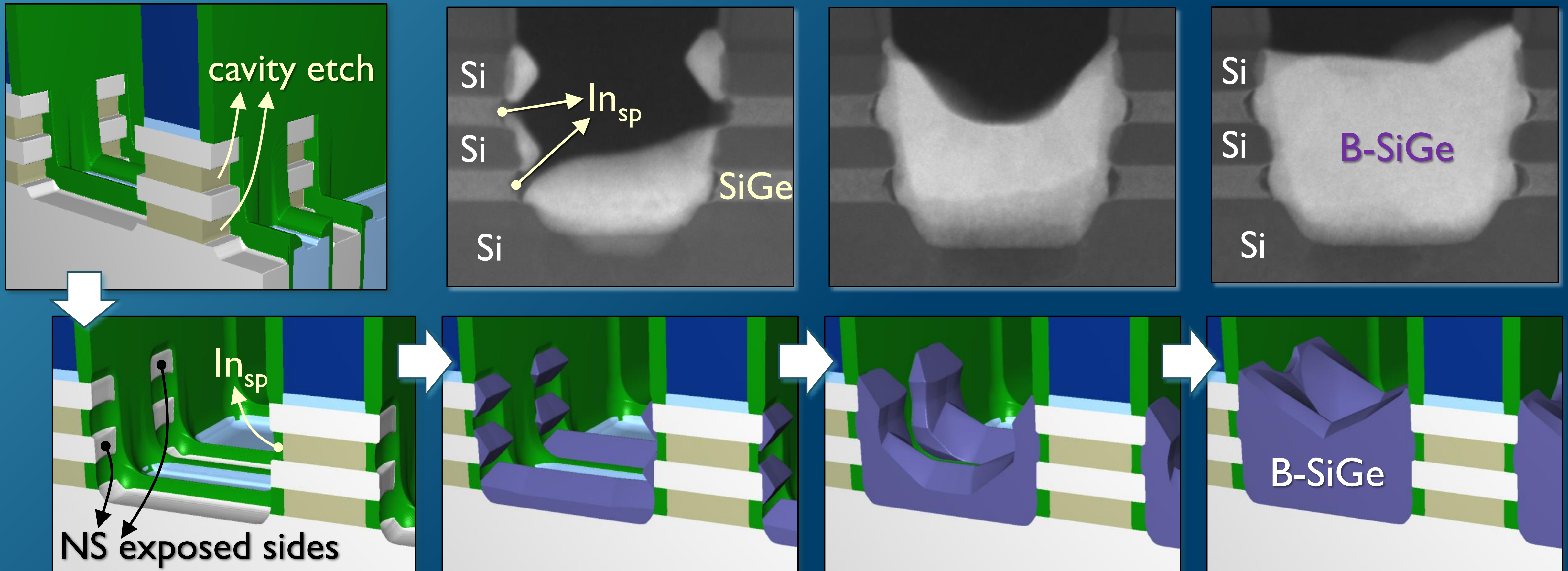


NS release



gate stack deposition

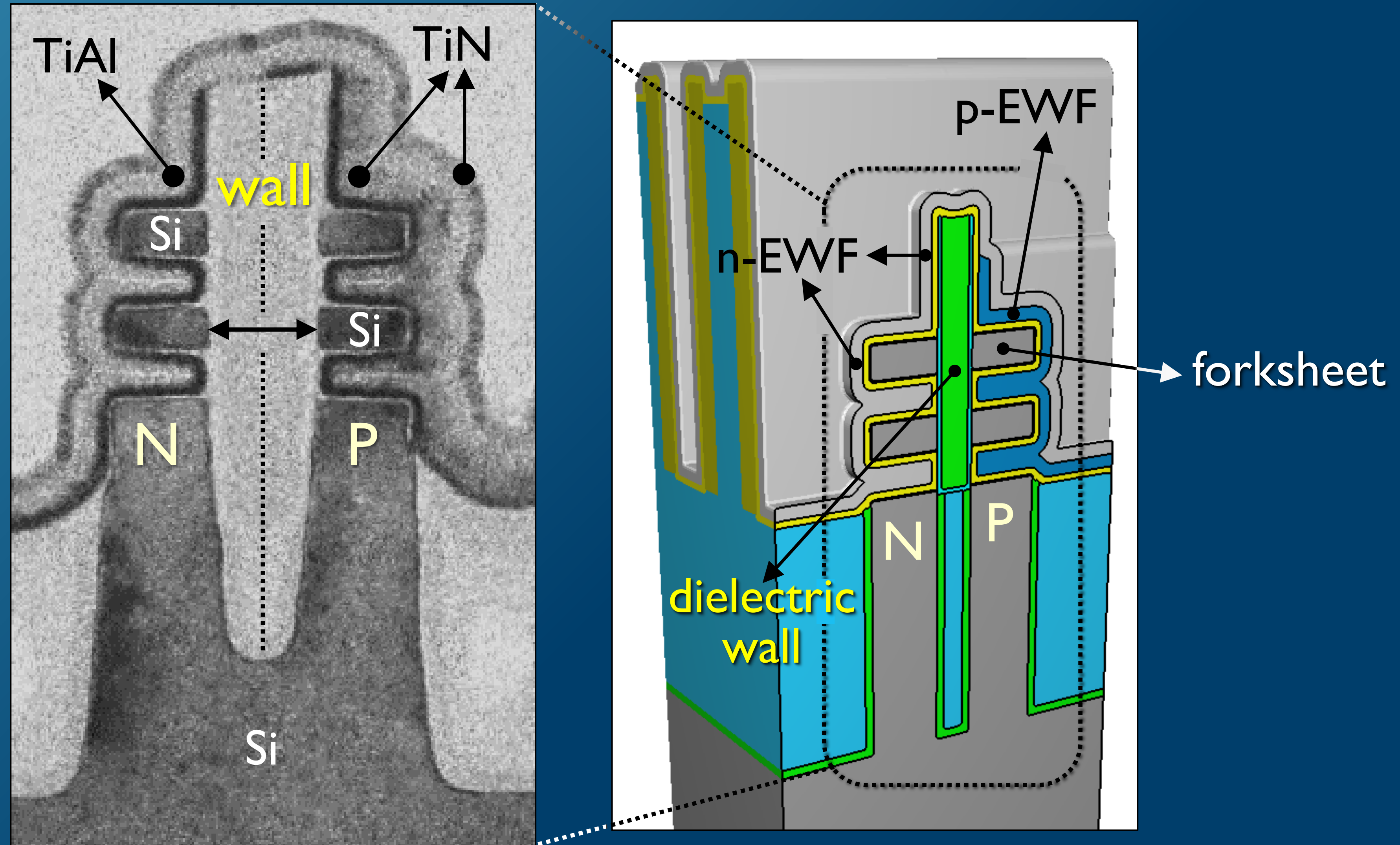
Inner spacers & S/D epitaxial growth co-integration: a key block in the flow to build nanosheet FETs



- Different S/D epitaxial growth regimes in NSFETs with inner spacers *vs.* finFETs

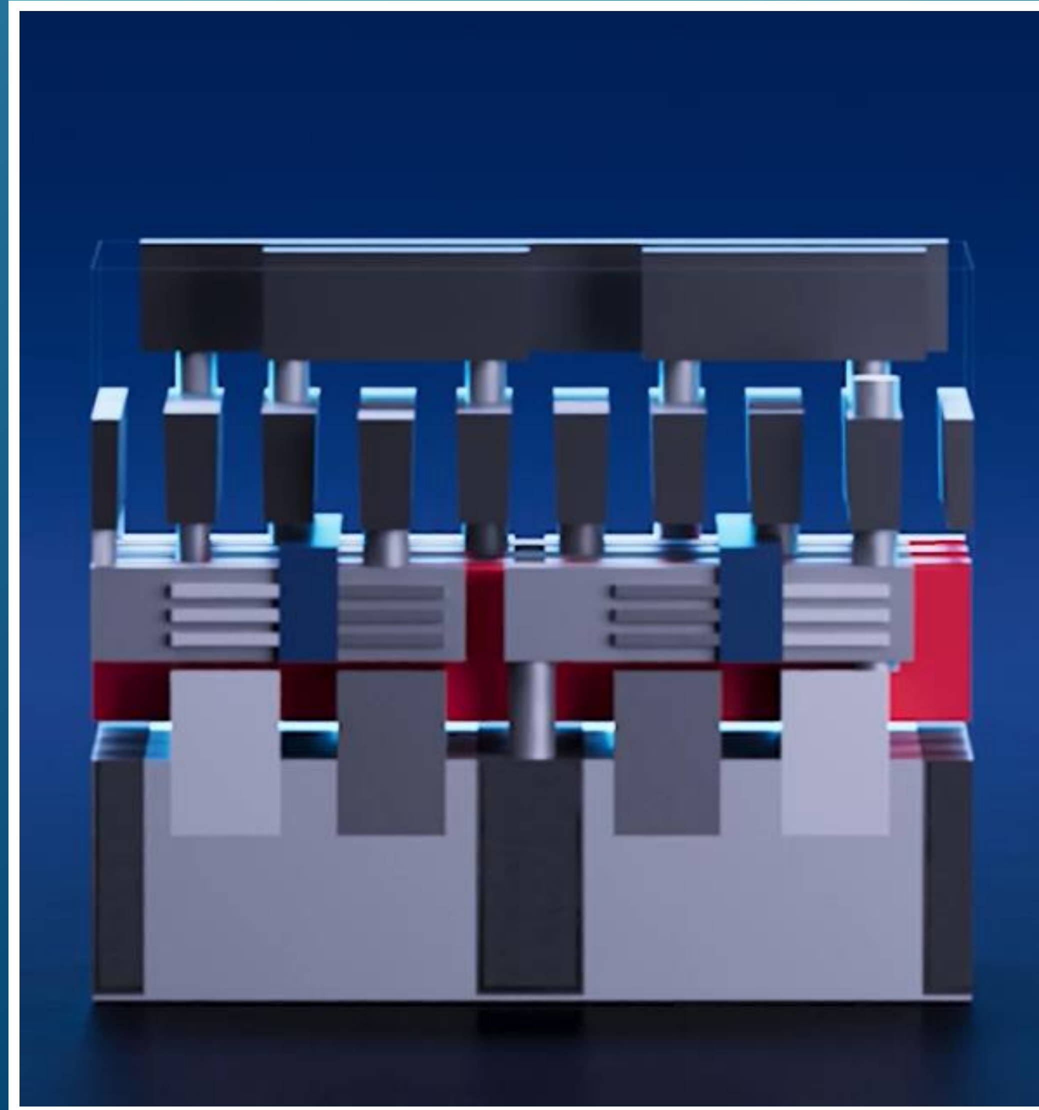
A.Veloso *et al.*, ICICDT 2022

Possible extension of nanosheet FETs into forksheet FETs



H. Mertens *et al.*, VLSI 2021

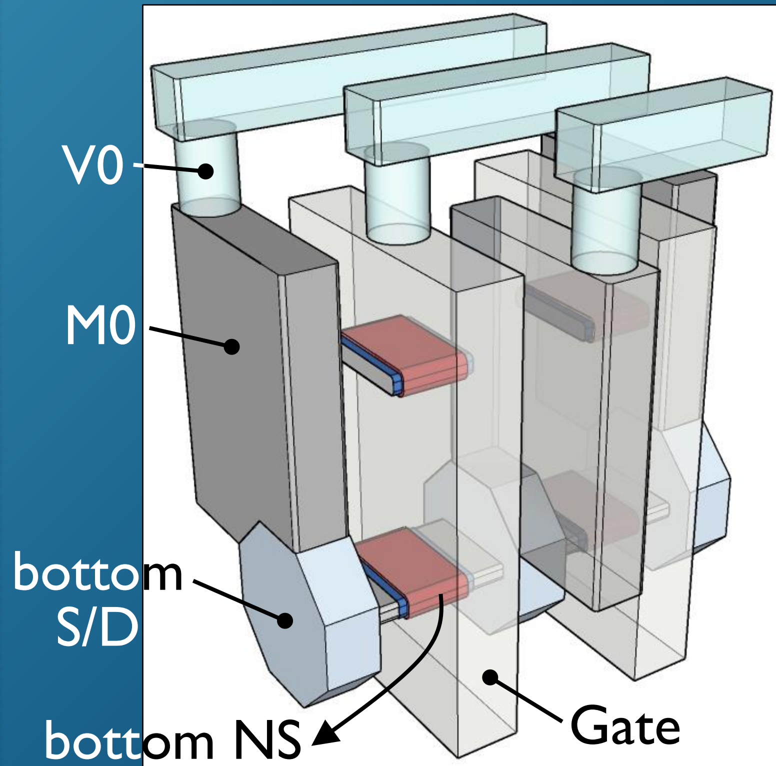
Nanosheet-based FETs' ultimate scaling limit: the CFET



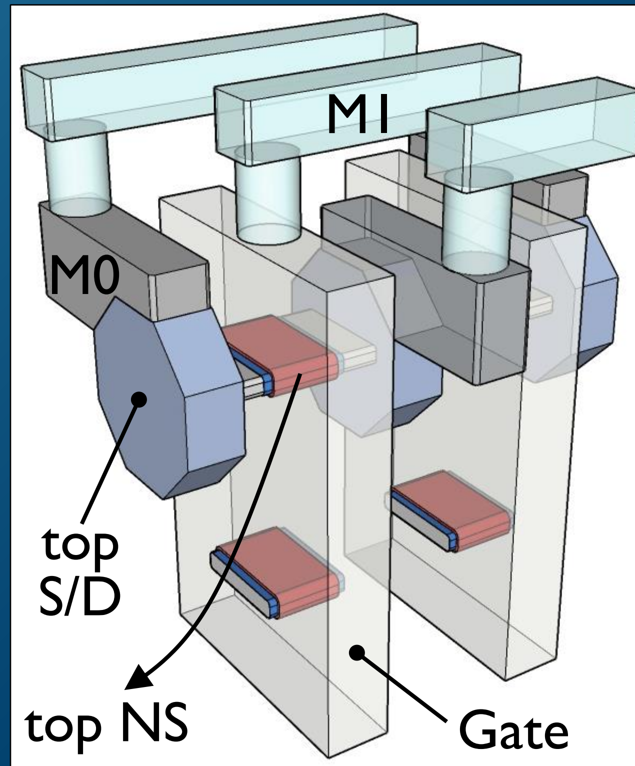
CFET: Complementary FET

Early device demonstration for enabling CFET architecture

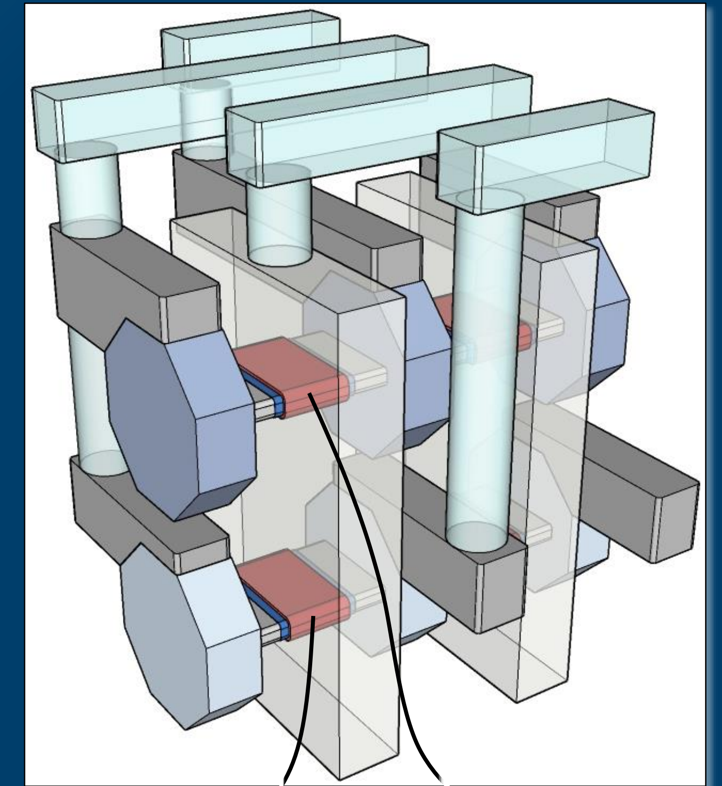
assessing only the CFET's bottom device



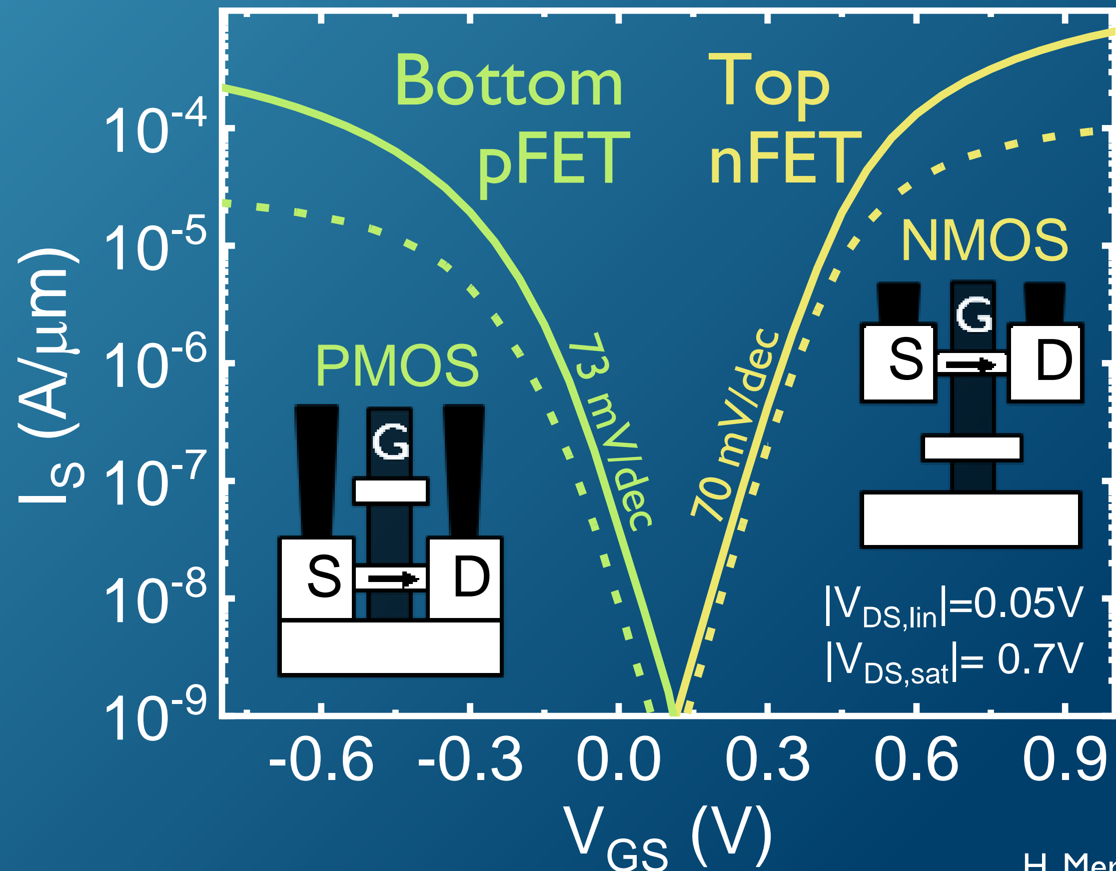
assessing only the CFET's top device

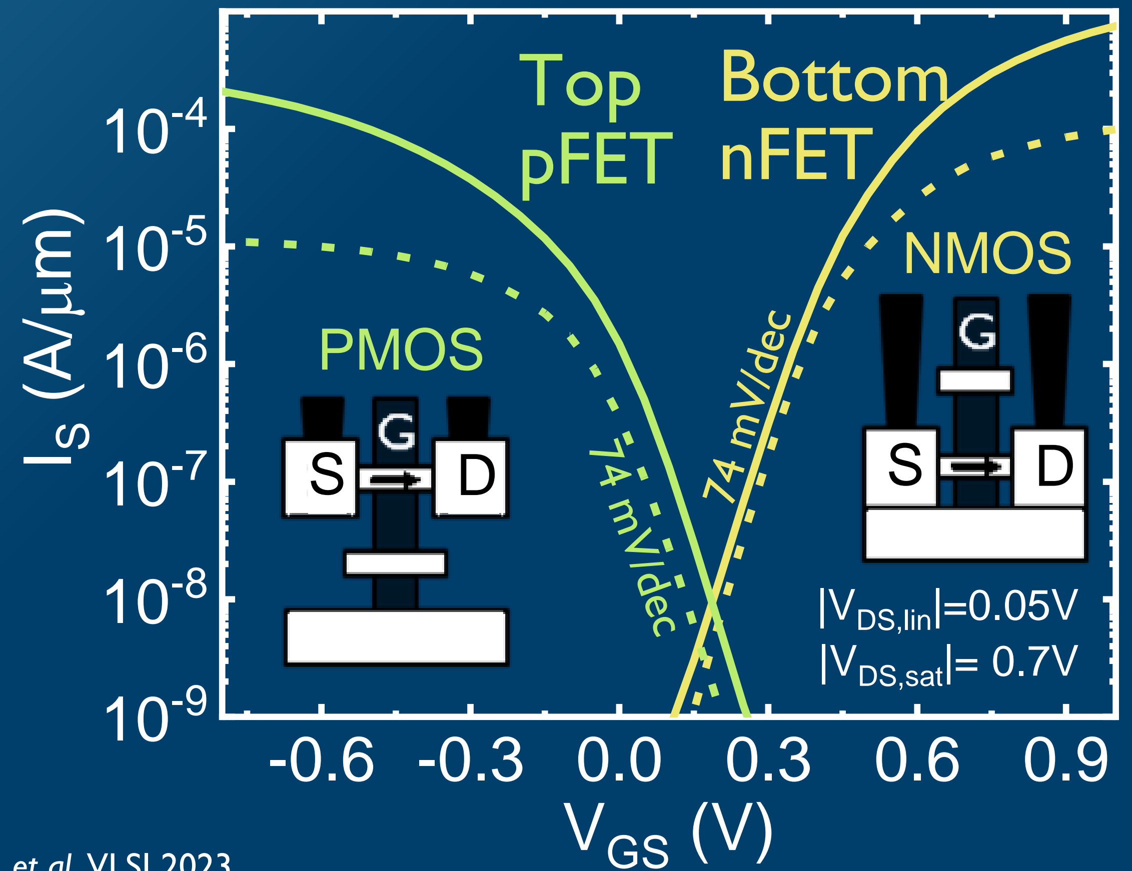


CFET architecture
(with 1NS per device)



Early device demonstration for enabling CFET architecture at scaled dimensions (CPP=48nm)

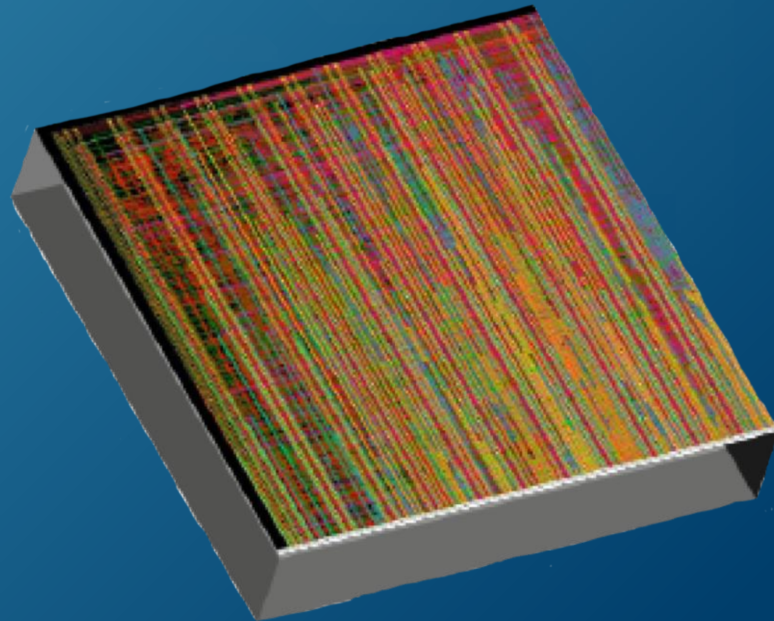


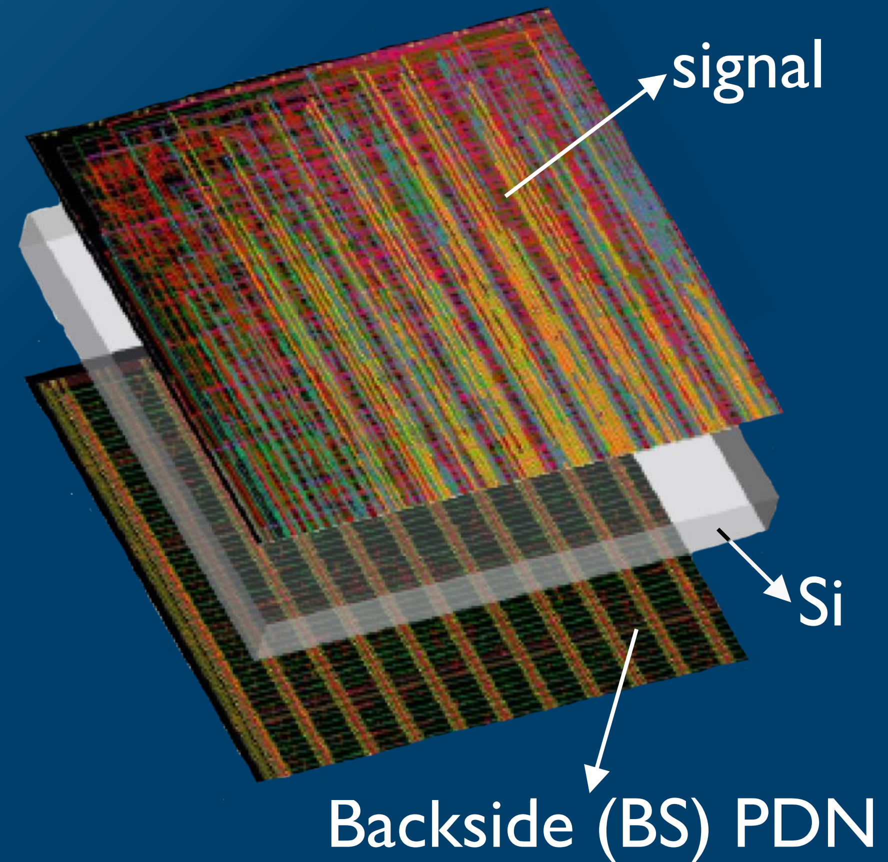


H. Mertens *et al.*, VLSI 2023

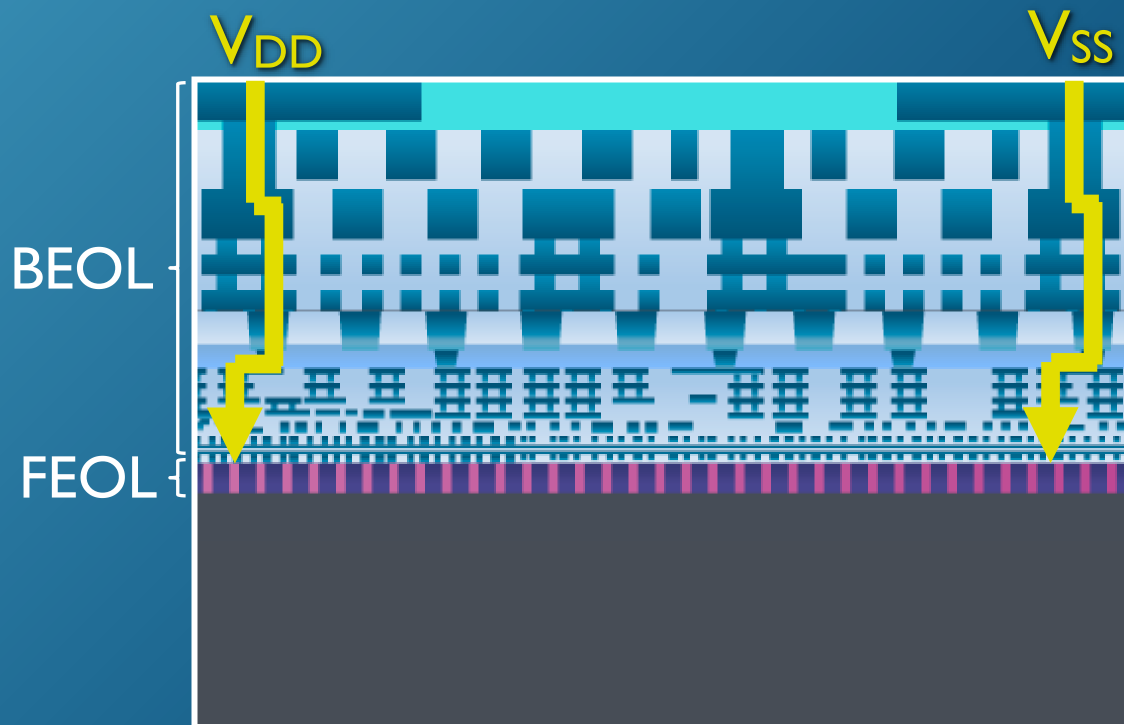
Backside Power Delivery Network (BSPDN): a game changer for on-chip power distribution

Frontside (FS)
power delivery network (PDN)
& signal



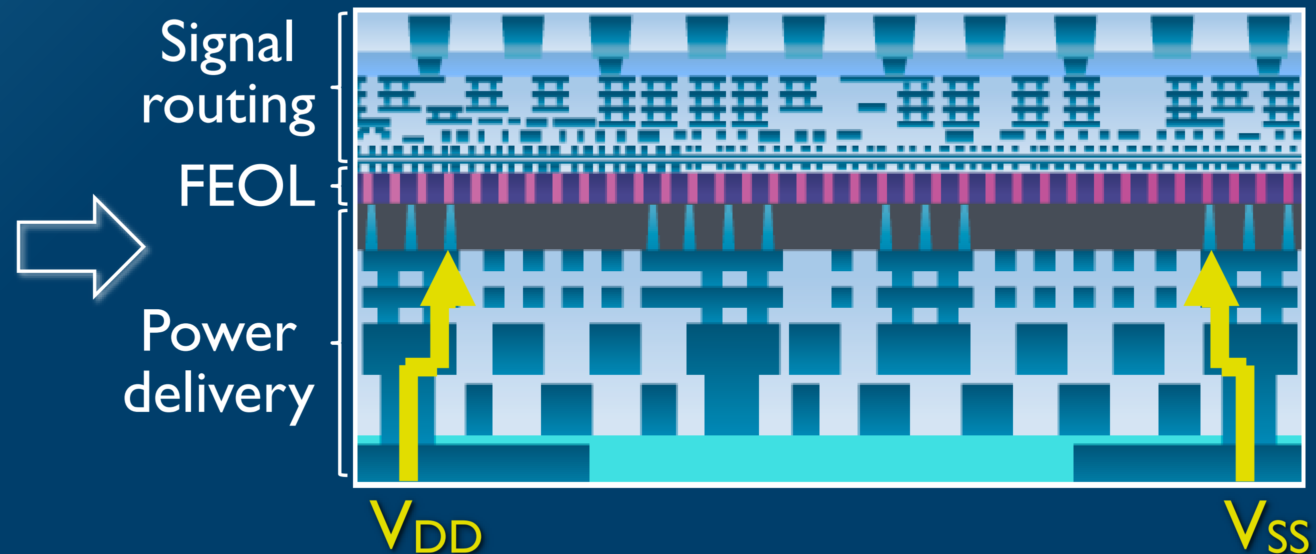


Moving from standard power distribution defined on the wafer's frontside towards BSPDN



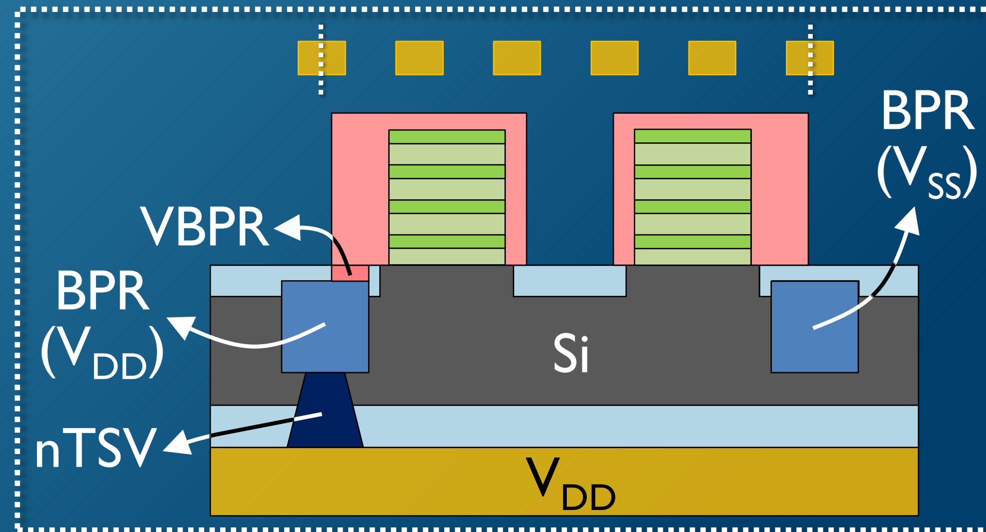
- Moving the power delivery network (PDN) to the wafer's backside (BS):

  helps to alleviate routing congestion in BEOL, allowing for a separate (and with more room) optimization of signal & power wiring

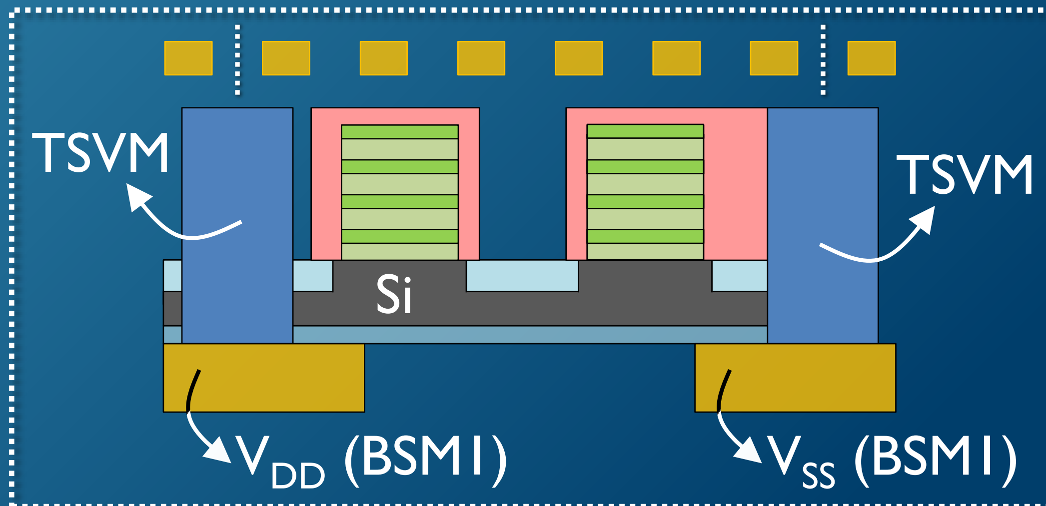


Several BSPDN implementation options possible

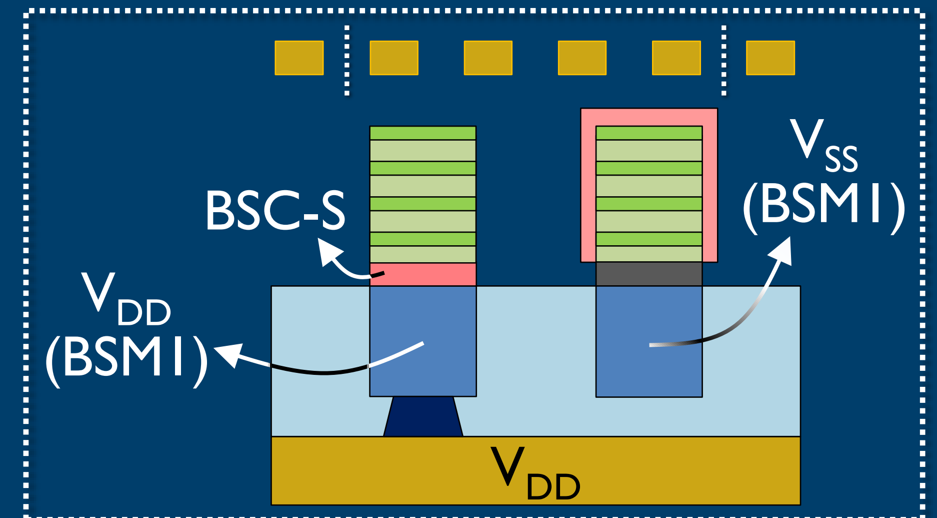
Buried Power Rail (BPR)



TSV Middle (TSVM)

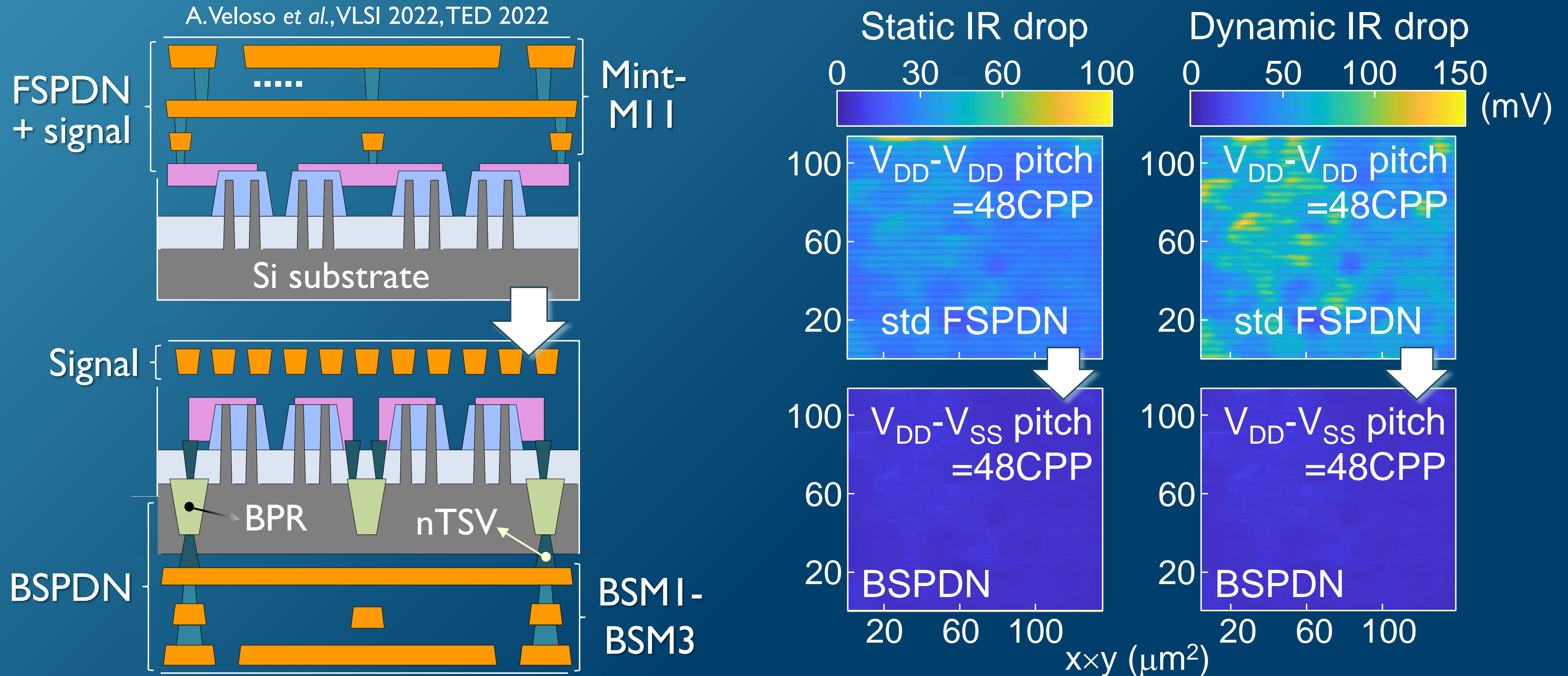


Backside Contact on Source (BSC-S)



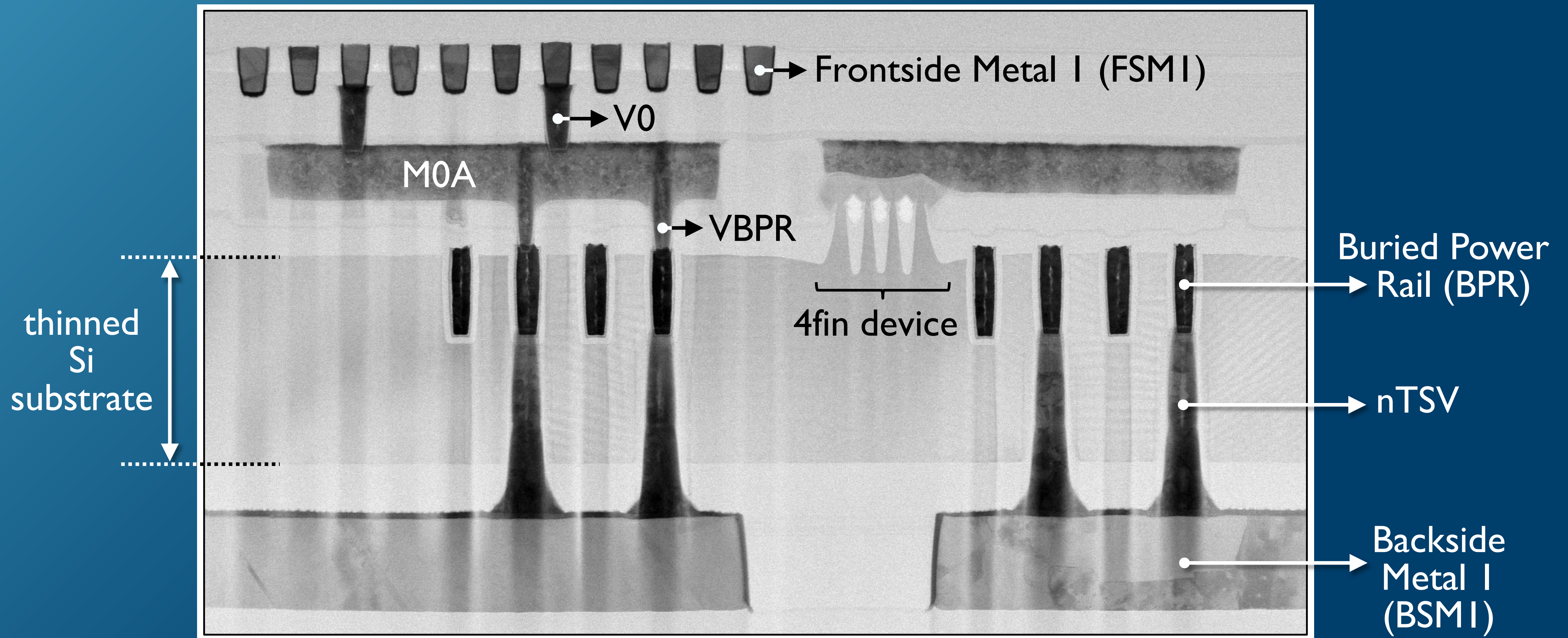
G. Hiblot *et al.*, Short Course IEDM 2022

BSPDN beneficial for enabling lower IR drop values



- On-chip IR drop heat maps simulated for a low power 64-bit CPU (A14 HD design rules, V_{DD}=0.7V) show BSPDN is clearly advantageous *vs.* standard FSPDN, enabling tighter distributions and smaller IR drop values, for both dynamic and static modes

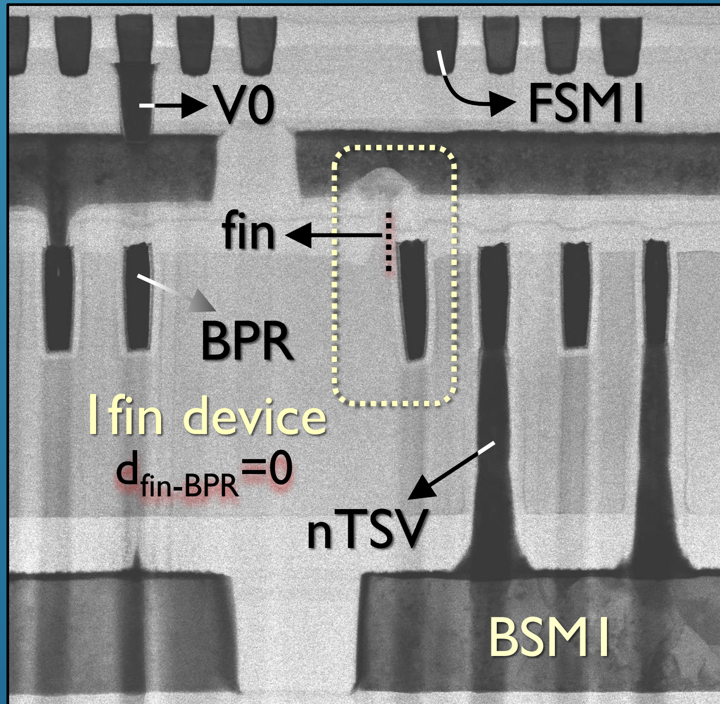
Device demonstration with front & backside connectivity



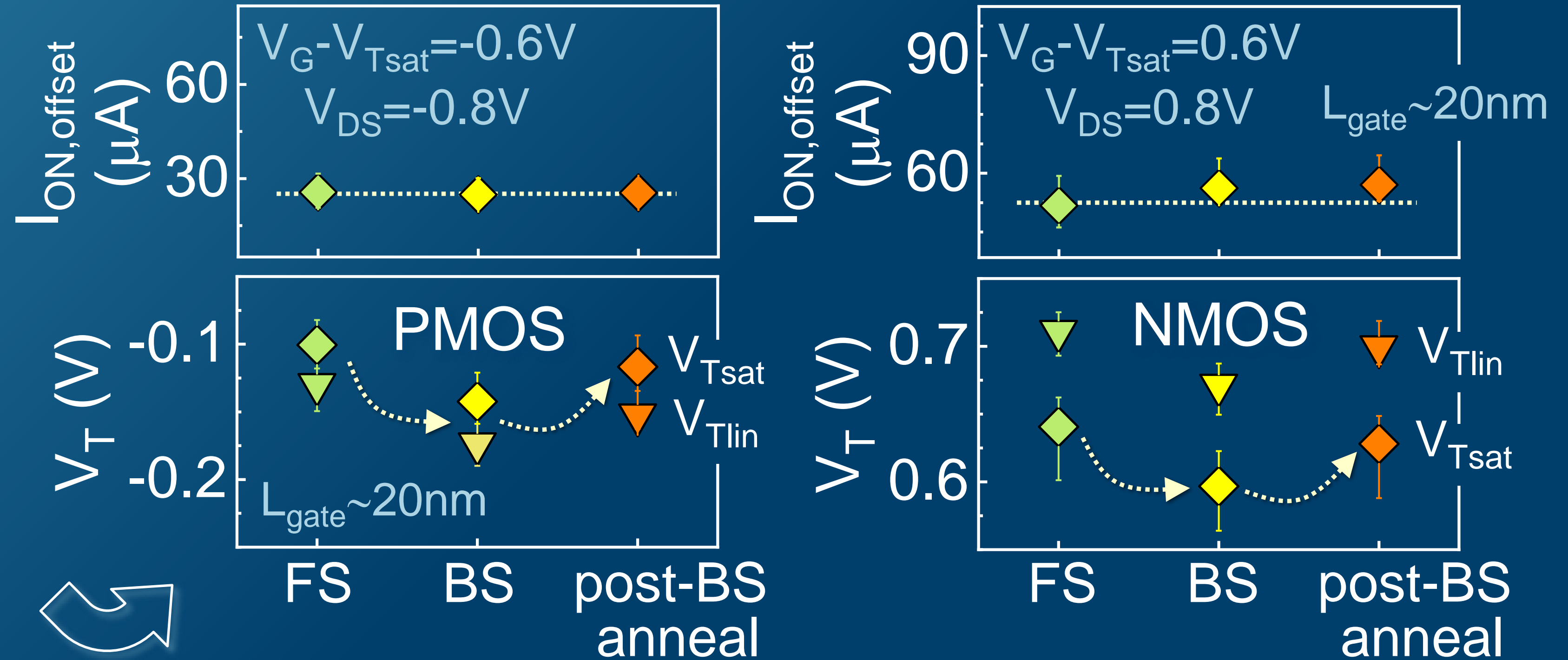
A.Veloso *et al.*, VLSI 2022

Healthy devices built with connections from both wafer sides

A.Veloso *et al.*, VLSI and IEDM 2022

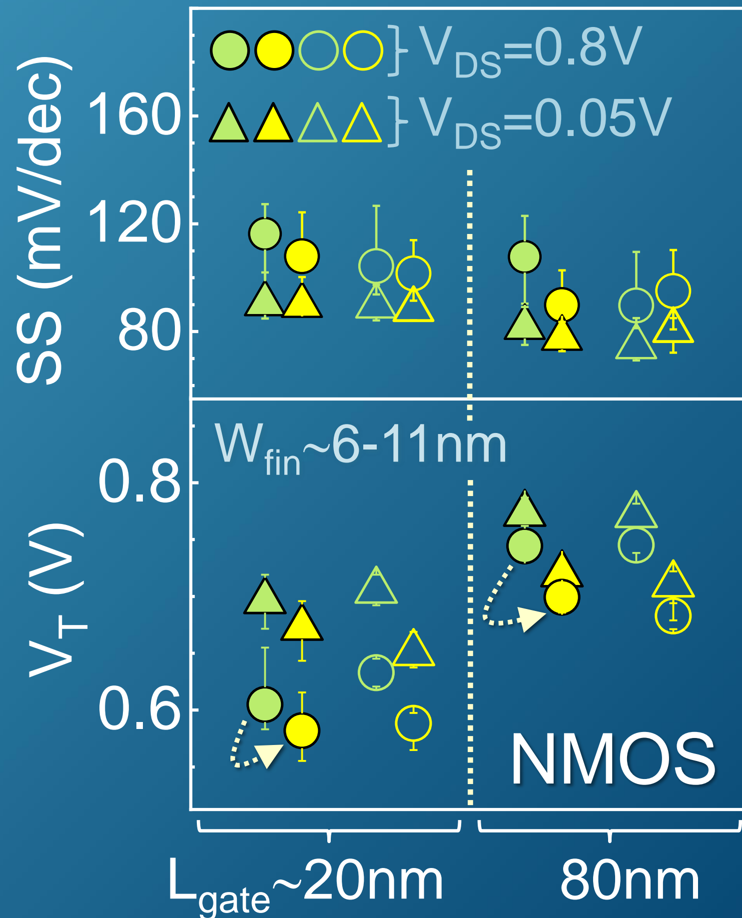


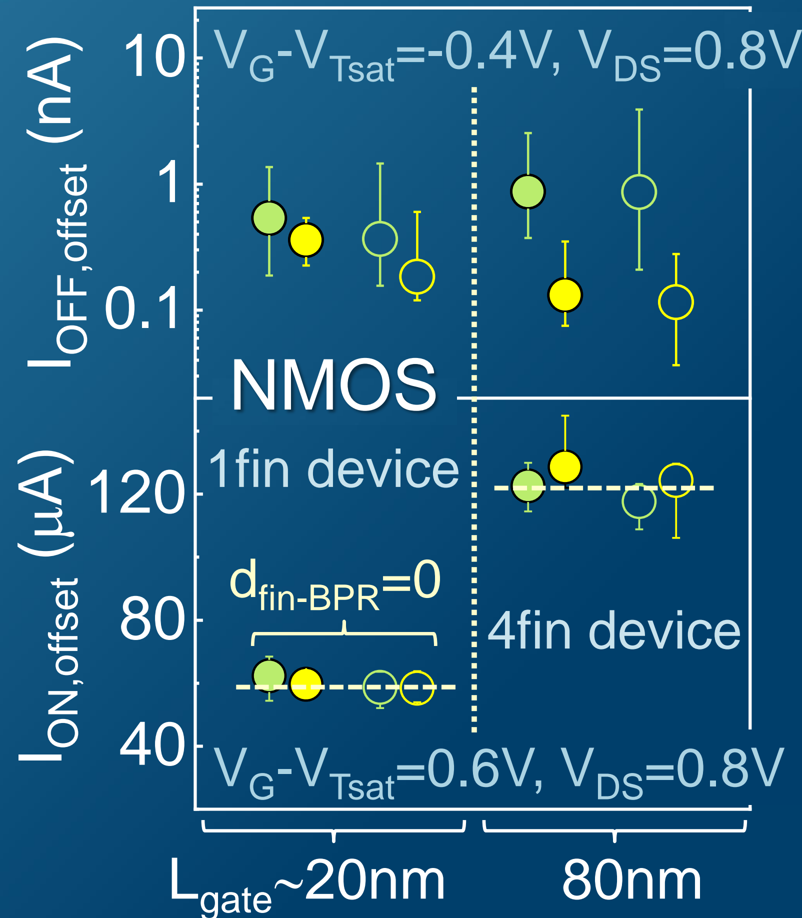
In-line measurements after the various stages of fabrication:

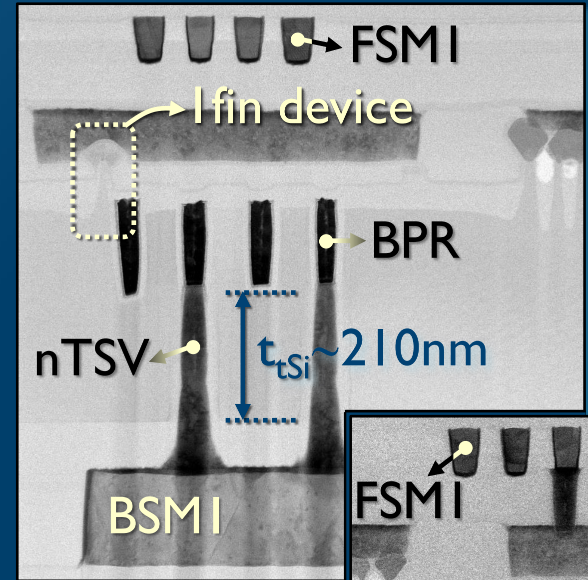


- Healthy device characteristics confirmed at EOP for scaled finFETs connected from both wafer sides, with final post-BS anneal(s) able to compensate for BS processing-induced de-passivation effects (& enable improved device characteristics)

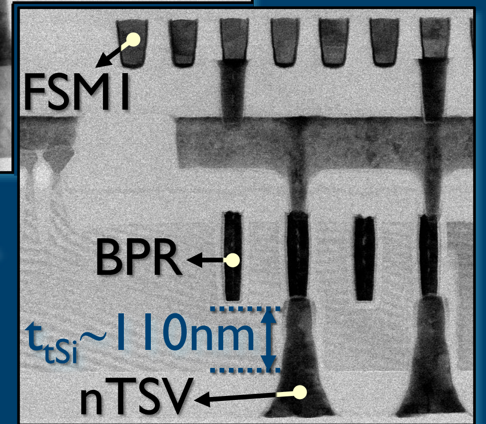
FS → BS processing: no device impact from ≠ thinned Si subs.







t_{tSi} ↓

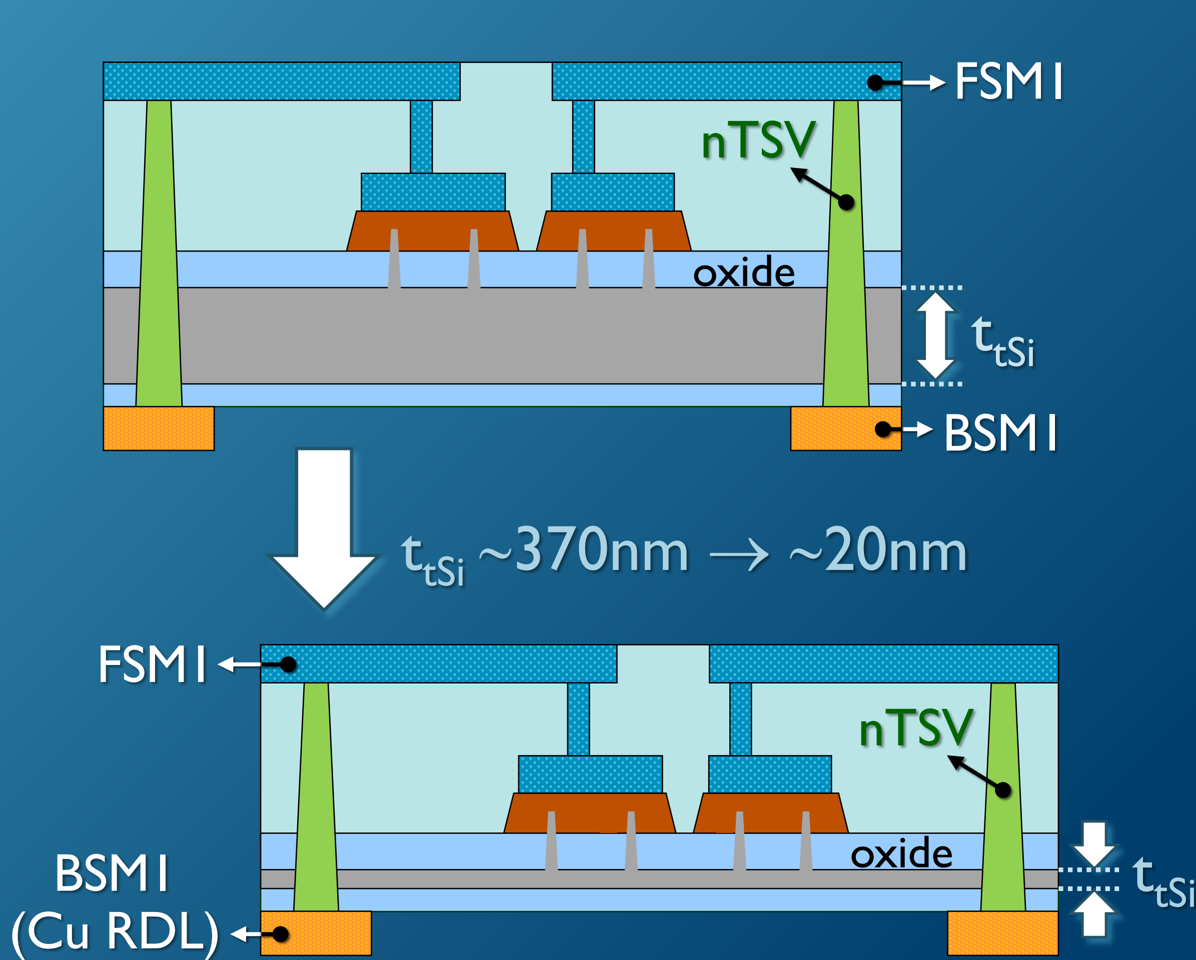


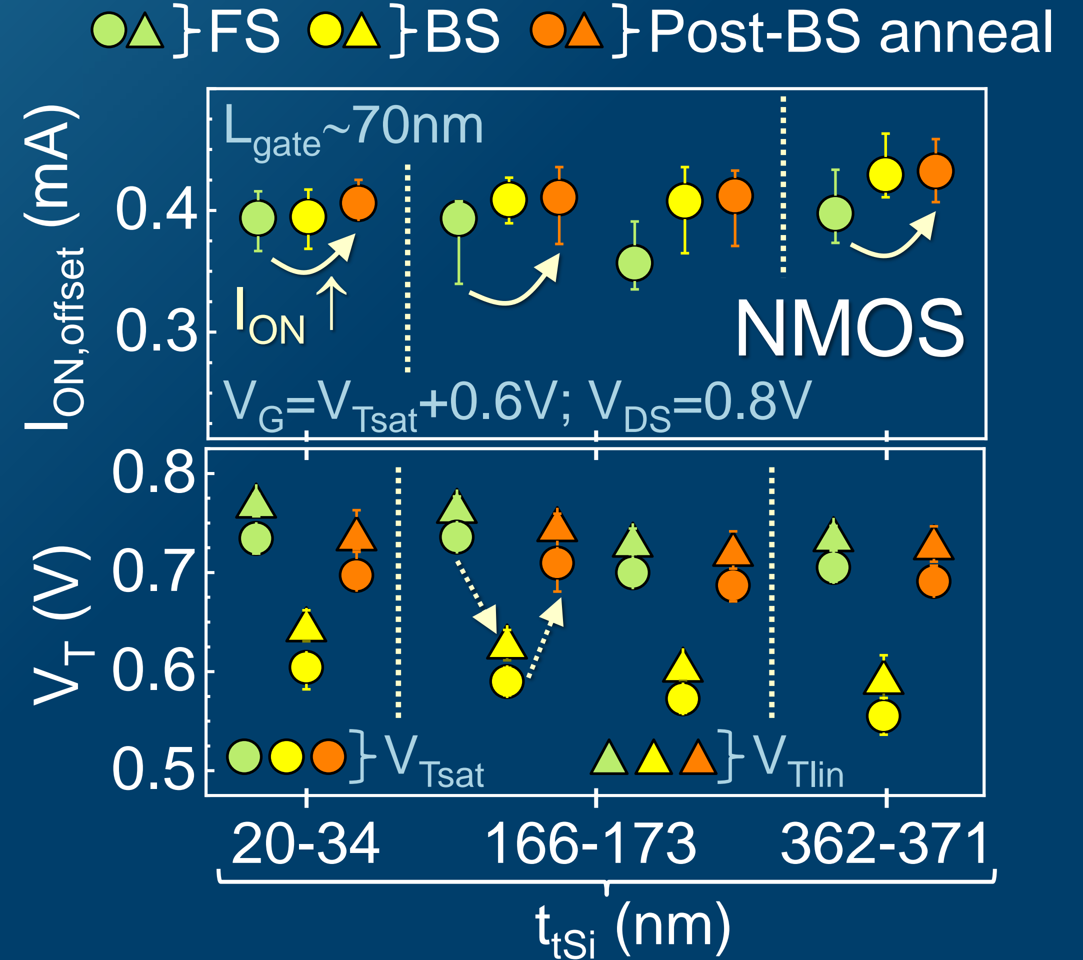
A. Veloso *et al.*, IEDM 2022

FS{●▲○△ BS{●▲○△ ●▲●▲ — thinner t_{tSi} → ○△○△

- Similar FS → BS behavior for N/PMOS built on wafers with ≠ thinned Si thicknesses

No device impact for extreme thinned silicon substrates

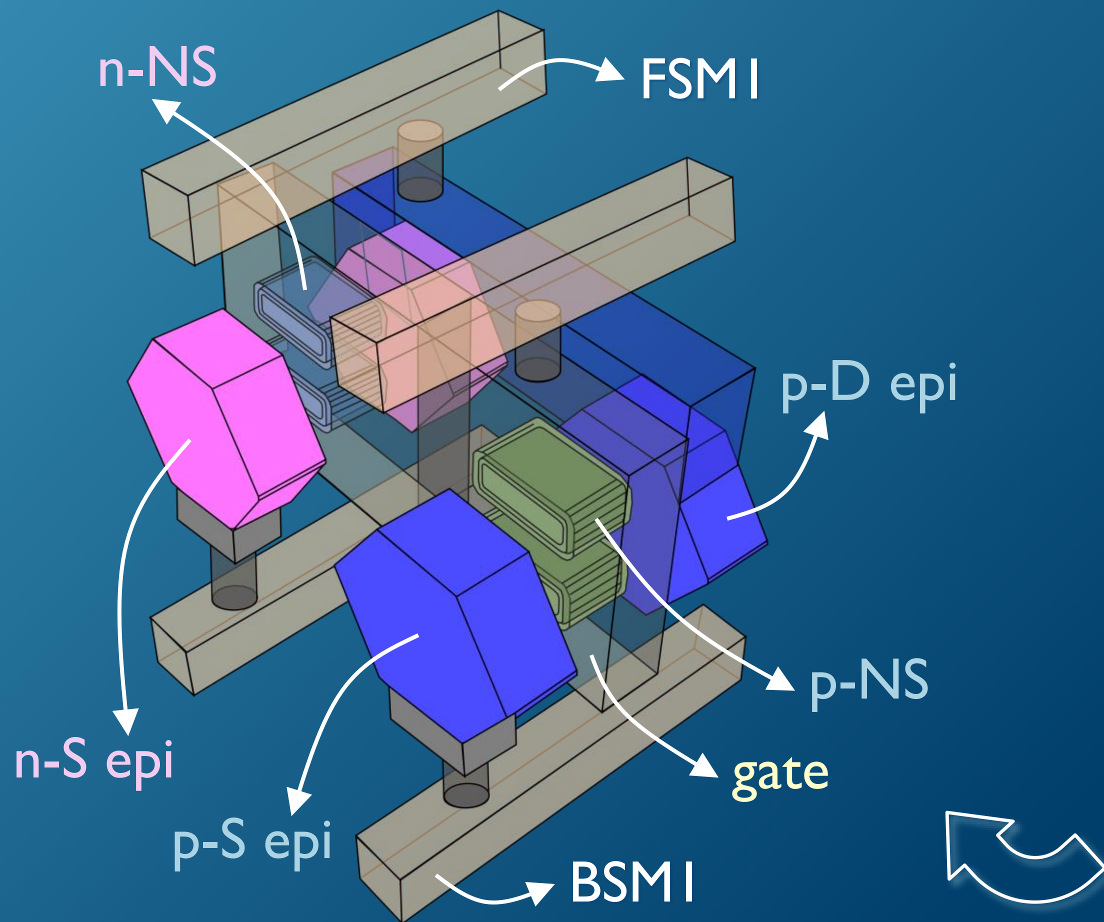


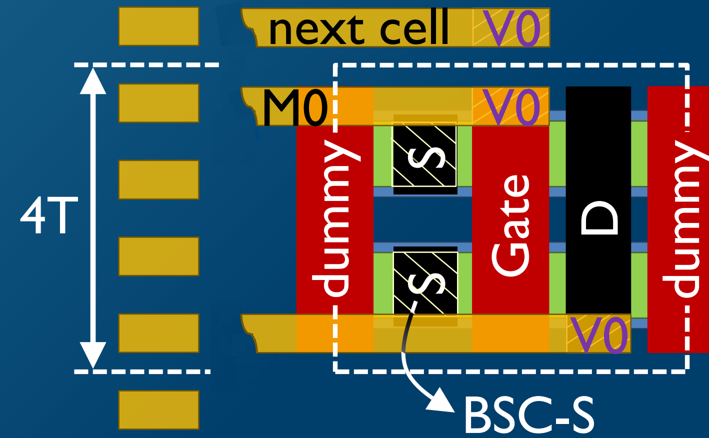


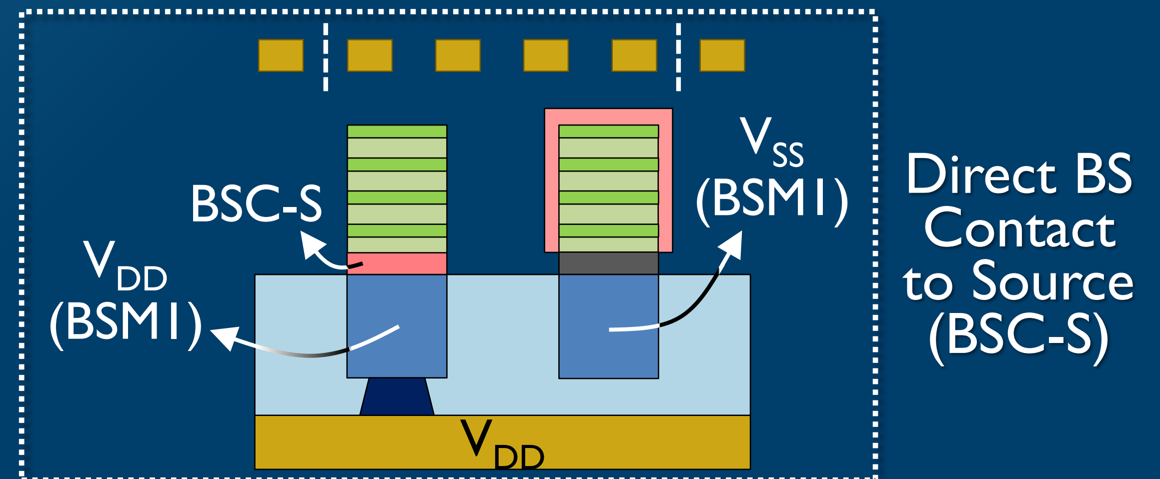
A.Veloso *et al.*, VLSI 2021

- Similar FS → BS behavior obtained for N/PMOS for extreme thinned Si substrates

BSPDN & cell's scalability: higher potential of BSC-S scheme





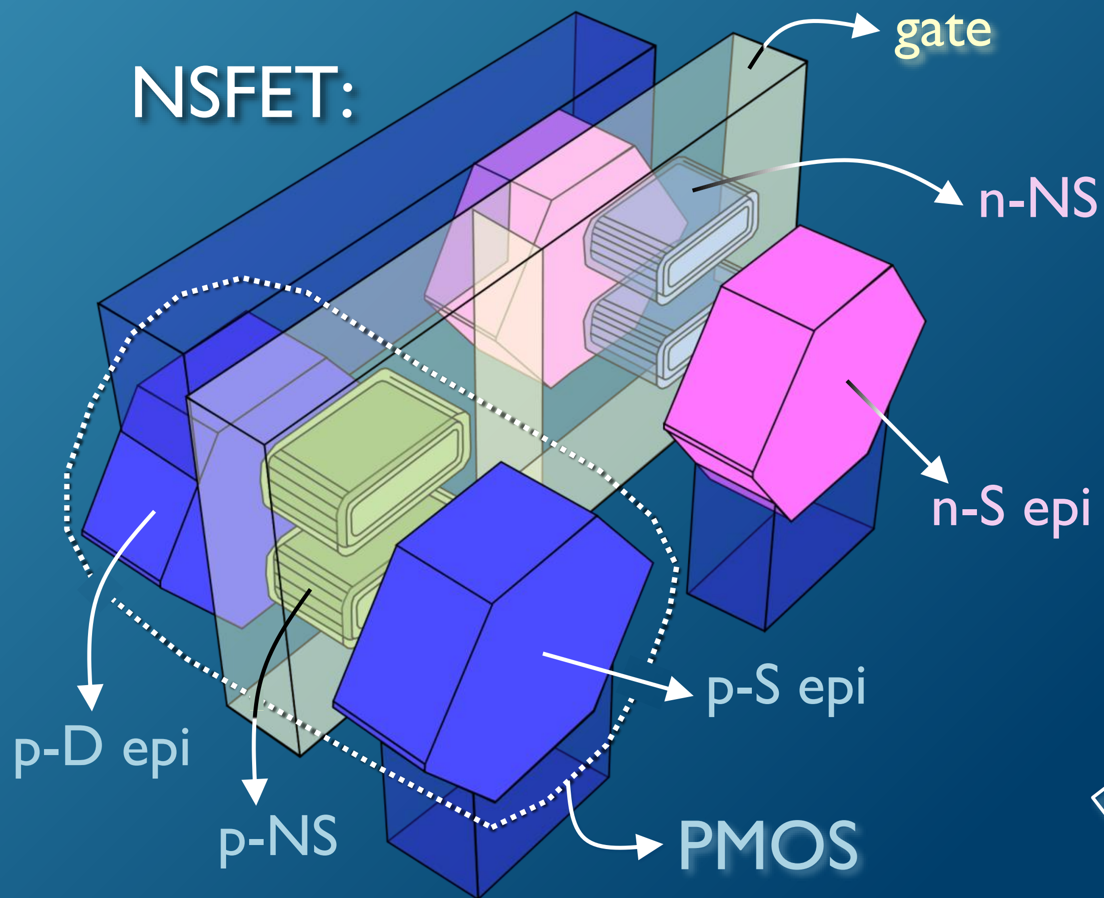


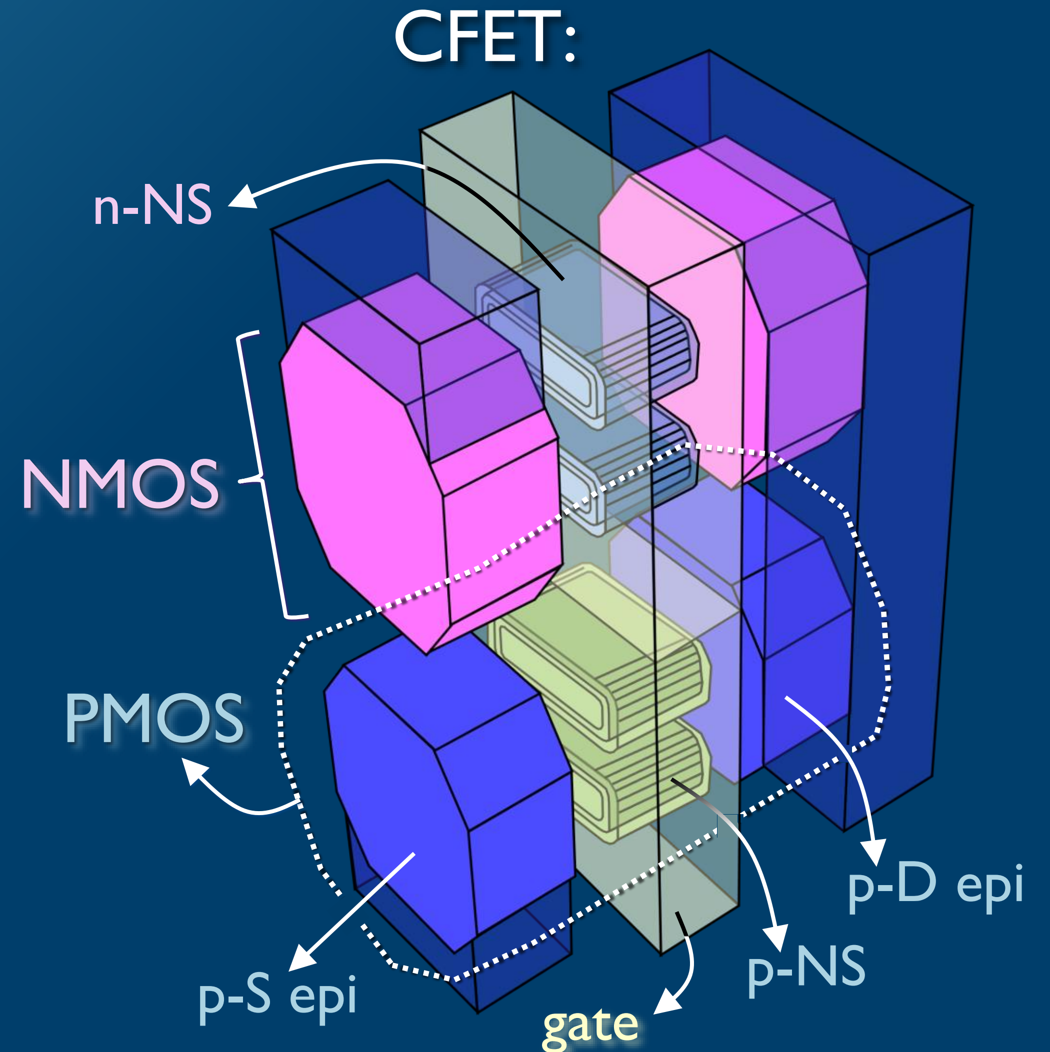
Direct BS Contact to Source (BSC-S)

- ❑ With various types of device connectivity options possible
  - ➢ BSC-S scheme enables further cell's scalability/cell's height shrinkage

A. Veloso *et al.*, IEDM 2023

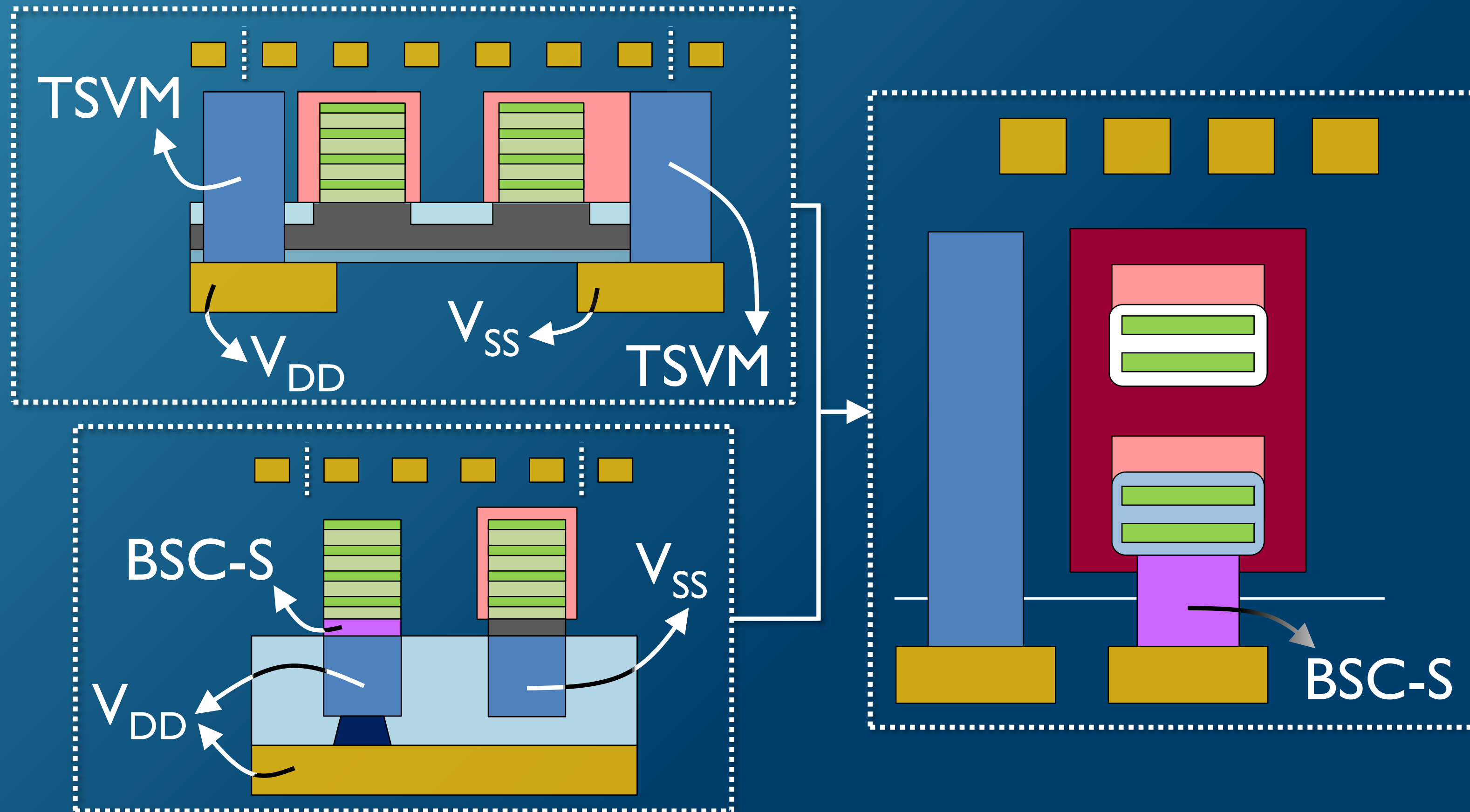
Towards the ultimate scaling limit of NSFETs: the CFET





A. Veloso *et al.*, IEDM 2023

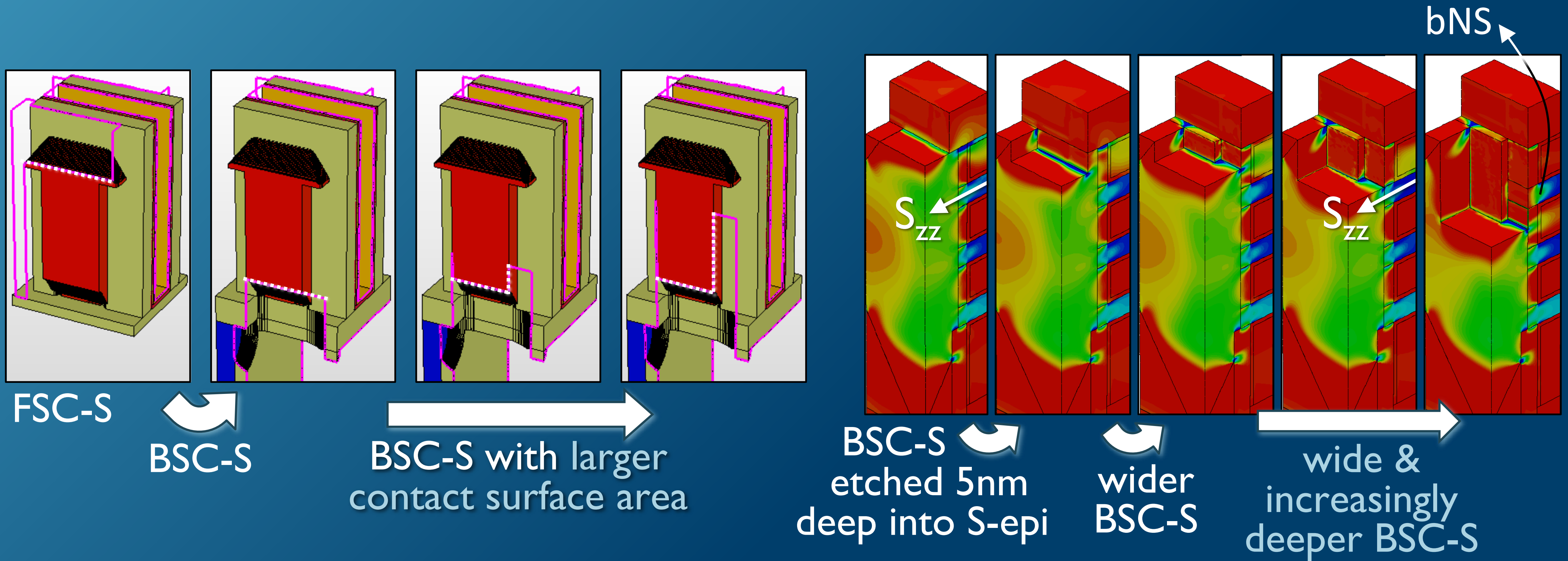
BSPDN for 3D stacked CMOS such as CFET



- BSPDN for CFET is envisioned to be a combination of several of the integration options first considered in the context of NSFETs

A.Veloso *et al.*, IEDM 2023

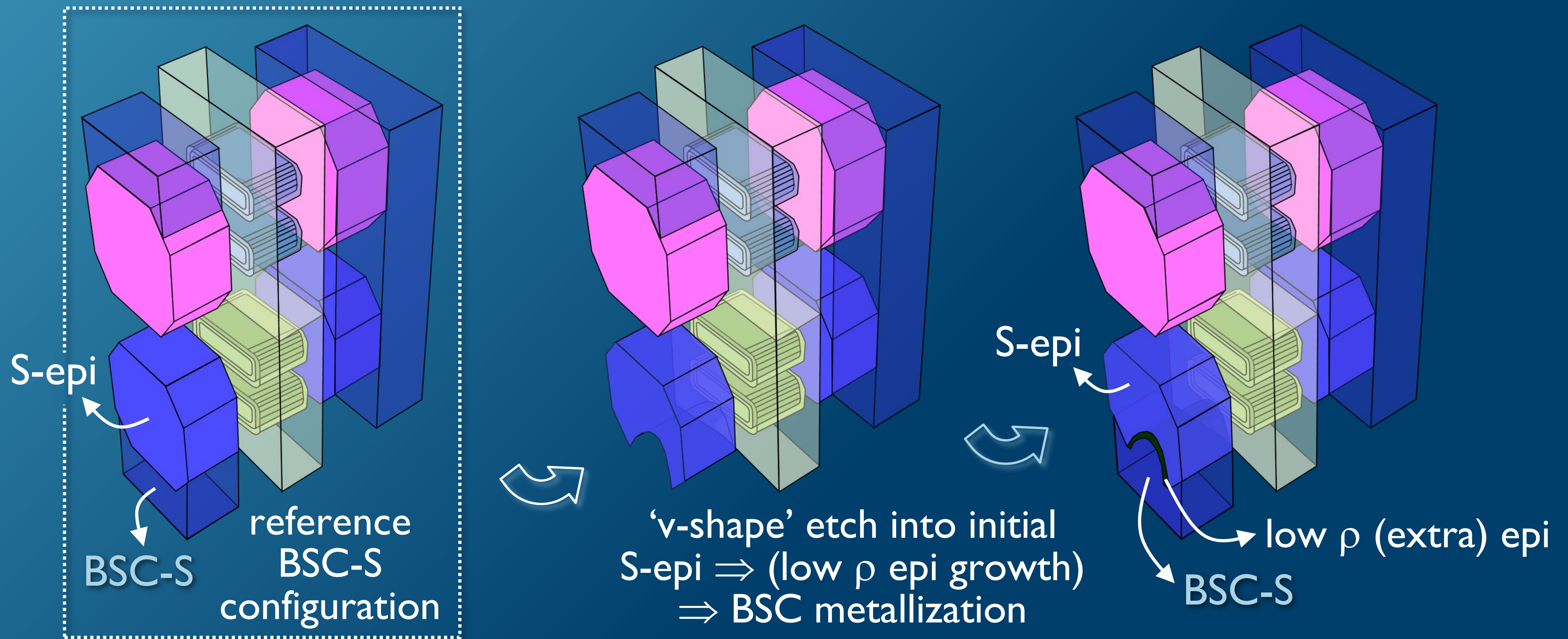
Devices with BSC-S: contact resistance & stress evaluation



- ➢ Larger contact surface area (from BSC etch optimized for a more wrapped-around type of BSC) also expected to be beneficial for BSC-S's contact resistance (R_{cont})
- ➢ Partially consuming some source-epi during the BSC-S opening step does not seem to detrimentally impact the bNS's channel strain

A. Veloso *et al.*, IEDM 2022 and IWJT 2023

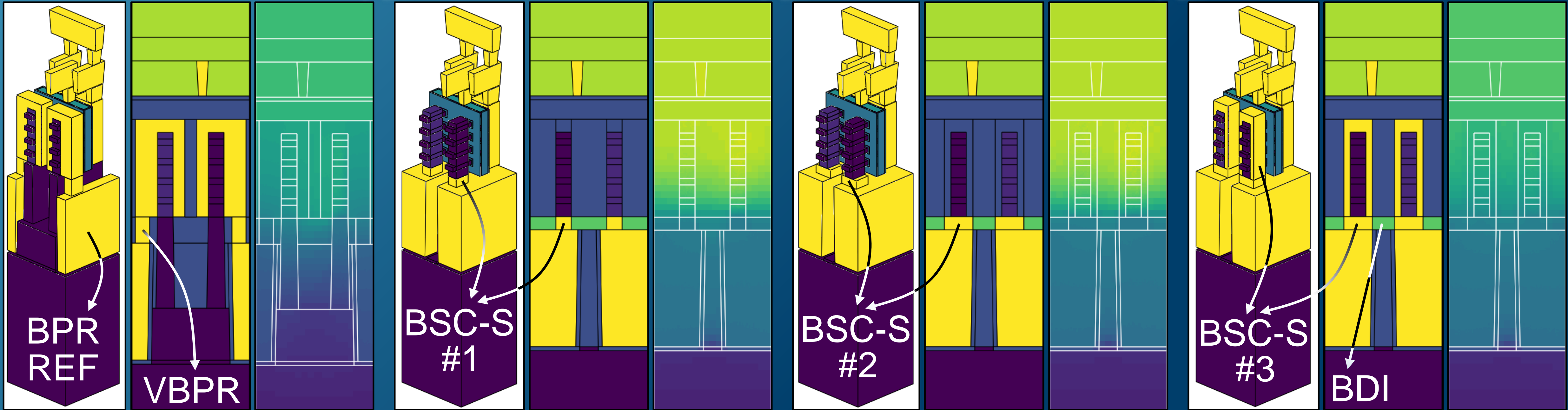
Several options available for R_{cont} optimization of BSC-S



- ❑ There are several interesting options for enlarging the contact surface area for BSC-S (e.g., 'v-shape' etch into S-epi during BSC-S open area), hence also for reducing its R_{cont}

A.Veloso *et al.*, IEDM 2023

Self-heating for various BSC-S configurations *vs.* BPR reference



A.Veloso *et al.*, IEDM 2023

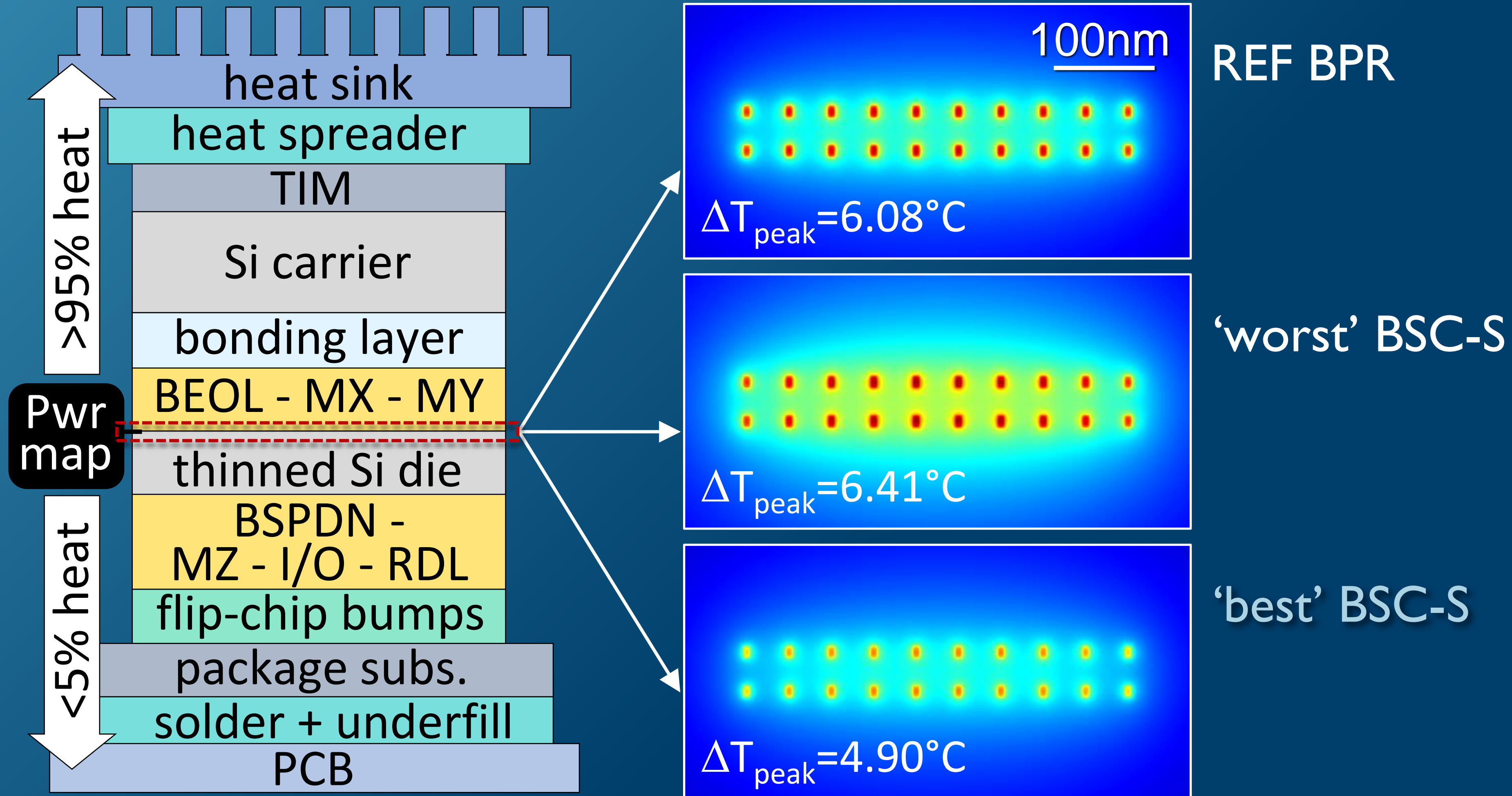
0 1 2 3 4 5 °C at 1 μW/transistor

A14 HD design rules
(CPP=42nm, L_{gate}=14nm, M1 pitch=18nm)

thermal cross-section maps provided via a vertical cut through the source terminal
(comparison for NSFETs with various BSC-S configurations *vs.* REF BPR case)

- ❑ Self-heating (relative to the cell's bottom) assessment of various NSFET configurations highlights the delicate interplay between cell's geometry & materials' thermal properties

Mitigating hotspots with use of optimized BSC-S configuration

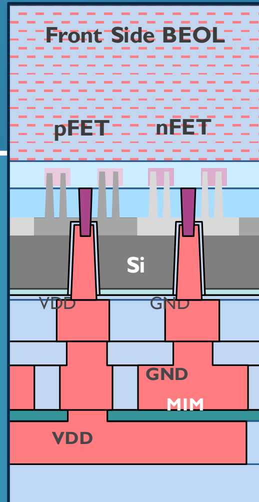


- An optimized BSC-S configuration can help alleviate hotspots that arise locally, relative to the chip background, in circuit regions with much higher activity factors (e.g., buffer cells in images for a SoC with A14 HD NSFETs)

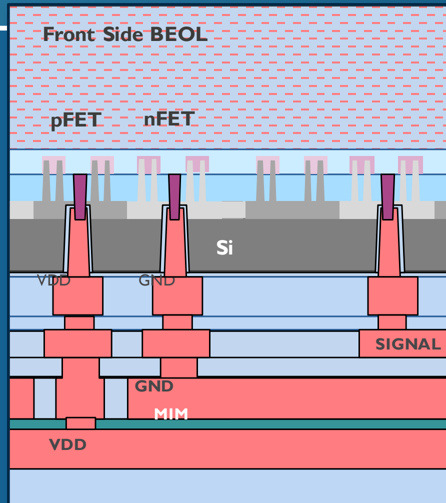
A. Veloso *et al.*, IEDM 2023

BSPDN paving the way to a truly functional backside

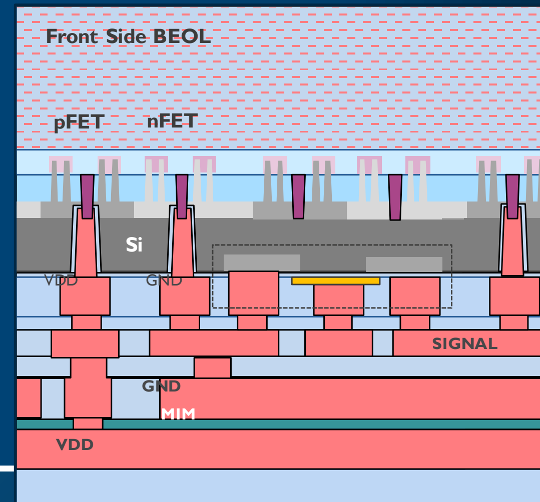
Backside Power Delivery



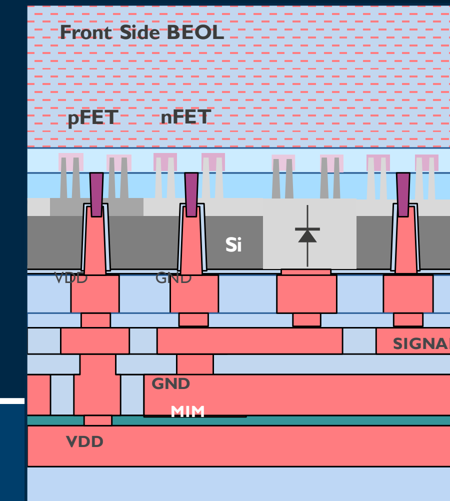
Backside Global Interconnect



Backside Devices



Device Backside Extension

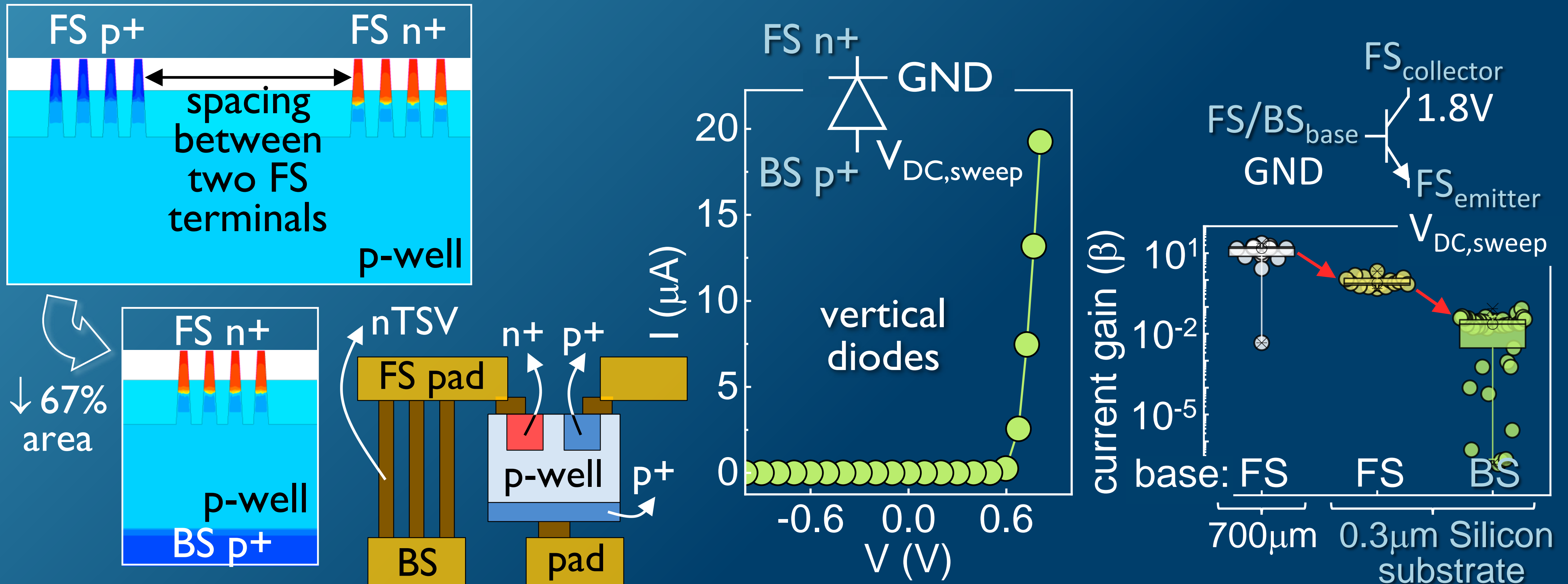


Functional backside roadmap

➢ Enhancing system performance by adding devices/migrating system functions to the wafer's backside

J. Ryckaert, ITF Japan 2022; A.Veloso *et al.*, IEDM 2023

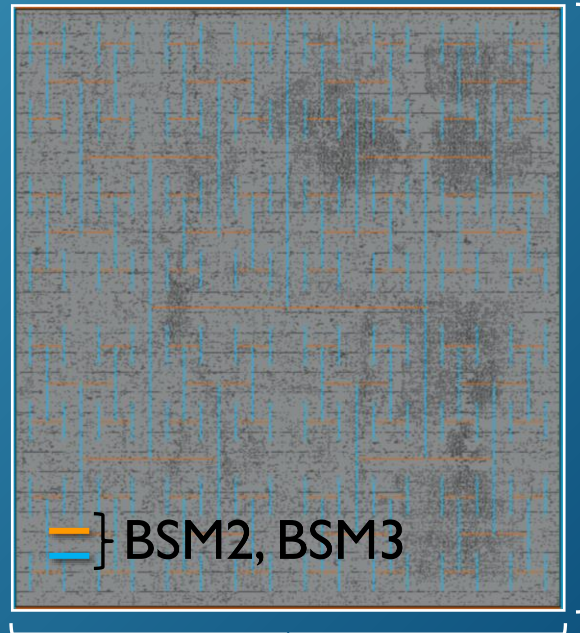
More compact vertical ESD diodes with BS contacts



- More compact ESD vertical diodes with BS contacts
  - improved latch-up immunity thanks to lower parasitic bipolar current gain (β) values *vs.* FS only versions

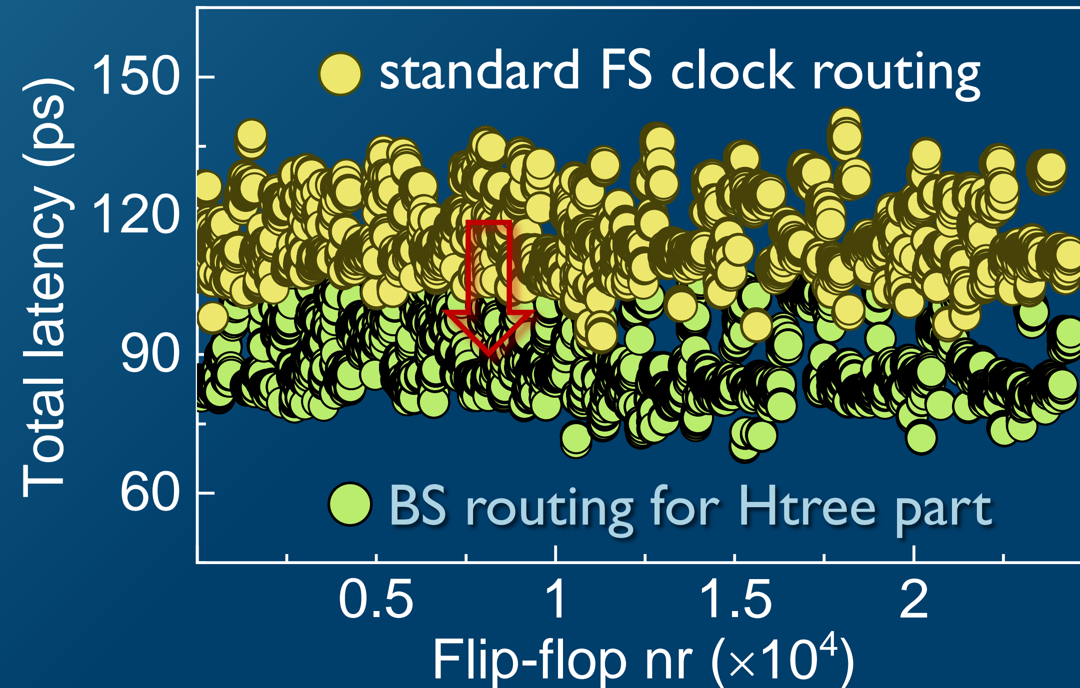
K. Serbulova *et al.*, VLSI 2022

Clear benefits also obtained by moving clock signal to the BS



Global routing with a 16×16-grid distributed clock's layout design

Exploration of introducing BS routing for the clock's Htree portion of a HP CPU at A14 design rules:

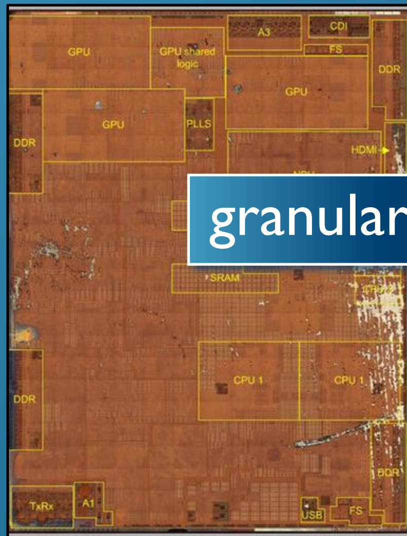


- ❑ Lower clock latency when clock implemented with (partial – Htree portion) BS routing
  - ➢ moving larger amounts of clock signal to the BS expected to lead to further latency reduction, needing careful optimization for optimum BS (power and signal) routing

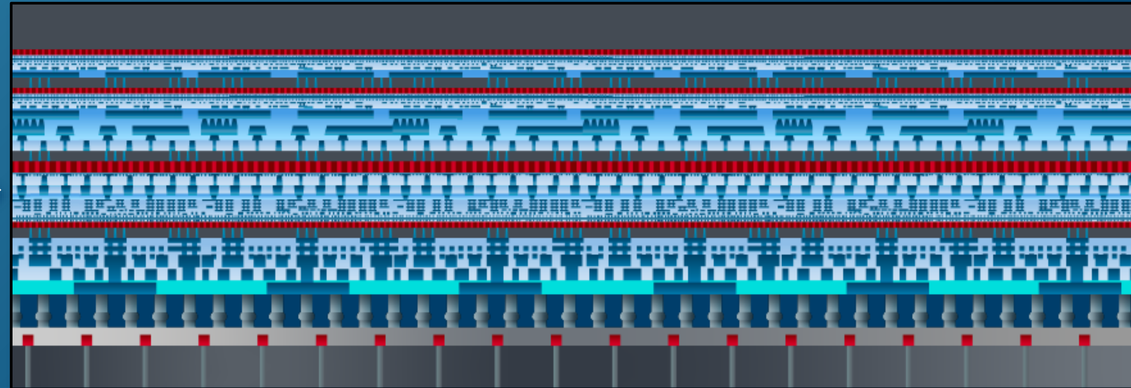
A. Veloso *et al.*, IEDM 2023

New STCO opportunities with BS technology: moving towards a heterogeneous CMOS platform

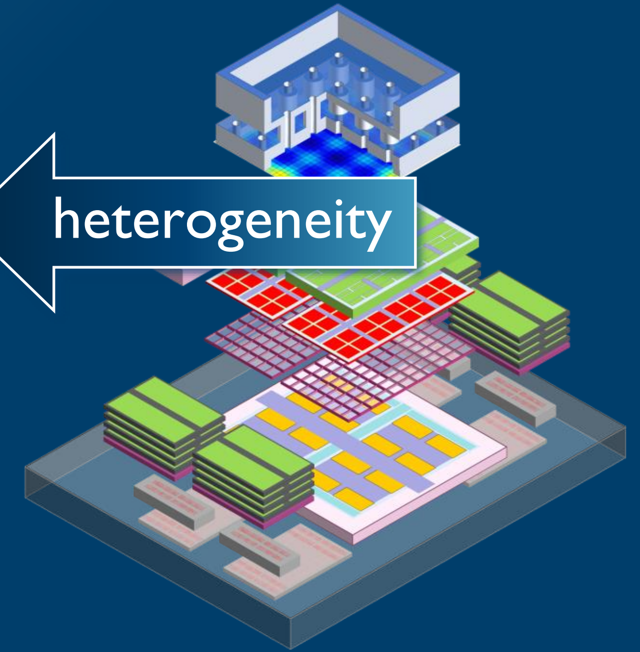
J. Ryckaert, ITF Japan 2022; A. Veloso *et al.*, IEDM 2023



granularity



heterogeneity



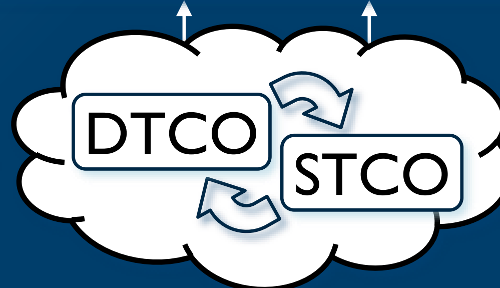
CMOS 2.0 = same 'look & feel' as a classical CMOS platform but offering versatility for system optimization

versatile SoC technology platforms

3D-SoC
Seq-3D
BS

technologies

hybridization



new materials
new processes
new devices

Some key takeaways

- ❑ Logic standard cell scaling remains at the core of the compute roadmap supported by:
  - ✓ continued dimensional scaling
  - ✓ introduction of new device architectures and materials
    - ➢ entering the nanosheet-based FETs era (single-level → 3D stacked)
  - ✓ adoption of backside power delivery and the use of both wafer sides
    - ➢ paving the way towards a truly functional backside roadmap
    - ➢ envisioning the move from CMOS to CMOS 2.0
- ❖ Power-Performance-Area-Cost (PPAC) → PPAC-Environmental impact (PPAC-E)

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imec

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