ESSCIRC/ESSDERC 2023

SiNANO-ICOS Workshop

"European Strengths and Gaps in Emerging Semiconductor Technologies"

Smart Energy: review of the main EU and international activities and technologies

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Definition

- Smart energy is a collective term for so-called intelligent technologies from the areas of energy conversion ("energy generation"), energy storage, energy transmission and consumption control. These areas cover the entire value chain of the energy industry.

- Various "smart" terms have been coined for this, such as smart grid (smart electricity network), smart metering (smart meter), smart home (smart living) and smart city, which are part of the smart energy concept or cover partial packages of it.

- The increasingly decentralised energy supply with local energy converters such as wind, solar, hydro and biogas power plants is an essential factor of Smart Energy.

Scope

- In the Smart Energy session of this workshop, we will provide an overview of the main EU and international activities in leading countries in the field of **semiconductors** used for future technologies in this specific area.

- Various **devices** for industrial and automotive applications are already on the market. However, cost pressures and technological innovation are driving device performance to the next level.

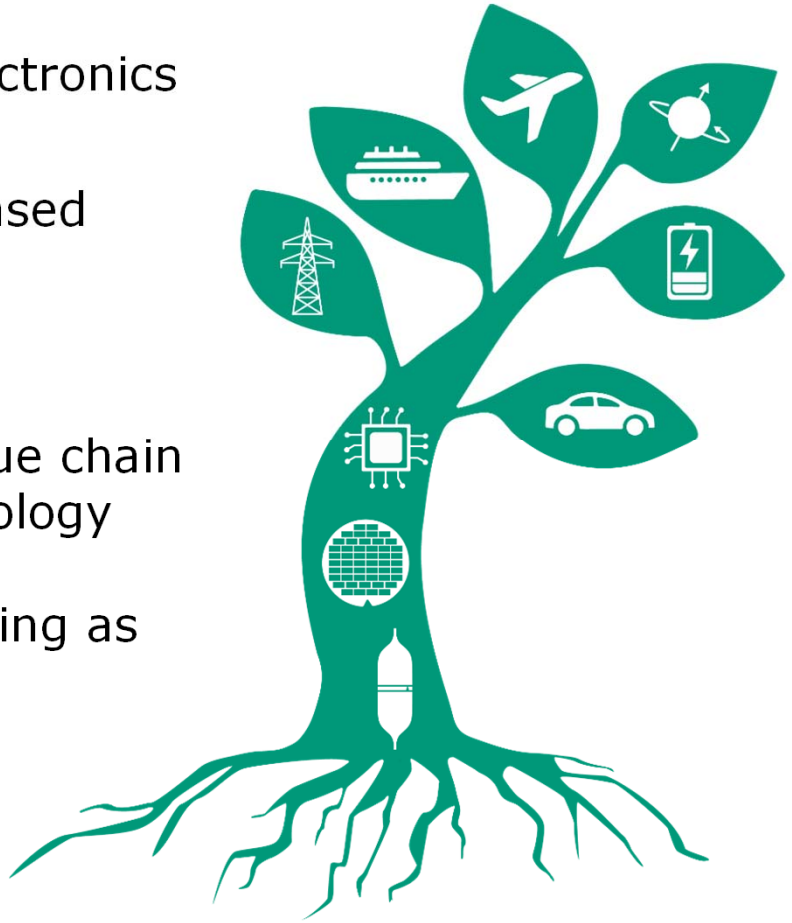
- We will highlight the research needs and gaps identified to make further progress in the field of smart energy.


KÄLTESPEI
Anwendungszentrum
DC-Netztechnologien
Mittelspannung
Brennstoffzelle
Blockheizkraft
Großkältespeicher
Chem. Wasserstoffspeicher

The Power Electronics Institute

From Semiconductor Technology to Power Electronics

- As renowned experts for wide-bandgap-based power electronics in Europe, we ensure sustainable mobility and energy supply
- The IISB activities cover the complete value chain for Si and SiC based semiconductor technology and electronic systems. Our range of R&D services extends from concept to prototyping as well as analysis and test, up to module construction and setup of complete power electronic systems.



Outline

- Sustainability through energy efficient DC grids
- Evolution of SiC Power MOS technology
- Possible goals for further tool optimization
- Opportunities and Conclusion
- Market Outlook Power
- Talents
- Summary / Gaps

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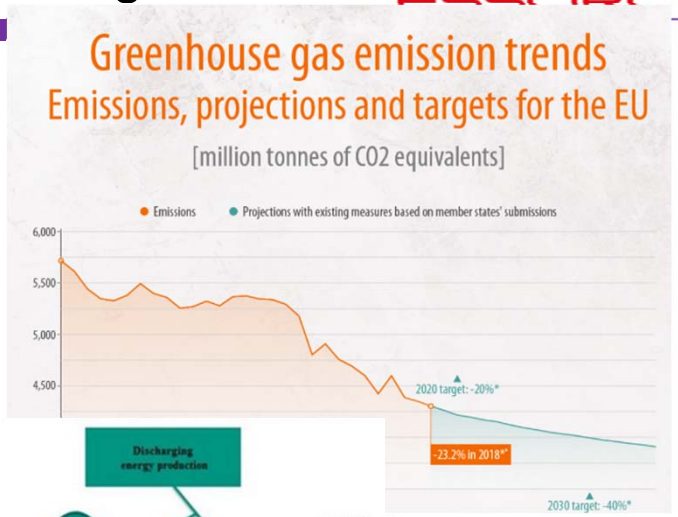
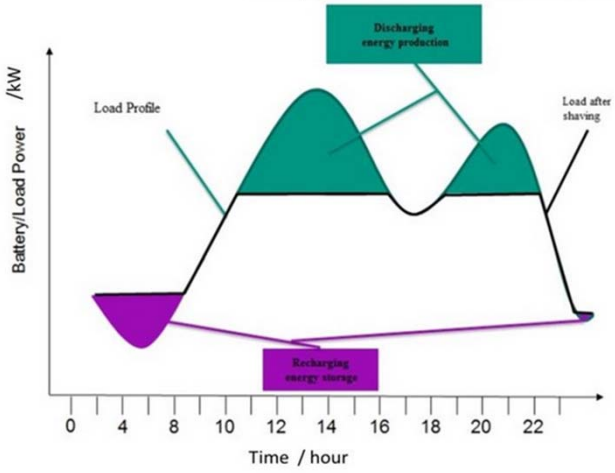
Sustainability through energy efficient DC grids

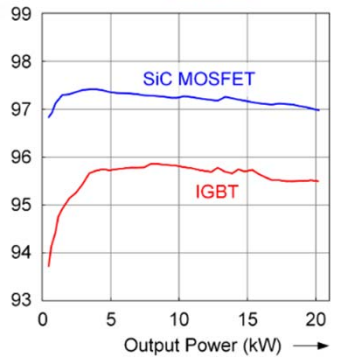
- Energy efficiency contributes to EU's CO_2 goals
  - Ecological and economical implications
    - Laws and regulations (compare Monitors)
    - Prestige and responsibility for companies

- SiC (WBG) converters offer excellent partial load properties
  - Up to 10% more efficiency compared to silicon topologies
  - Every time energy is transferred
    - Generation
    - Storage (Recuperation)
    - Consumption
  - Applicable to any source of electrical energy consumption (broad range)





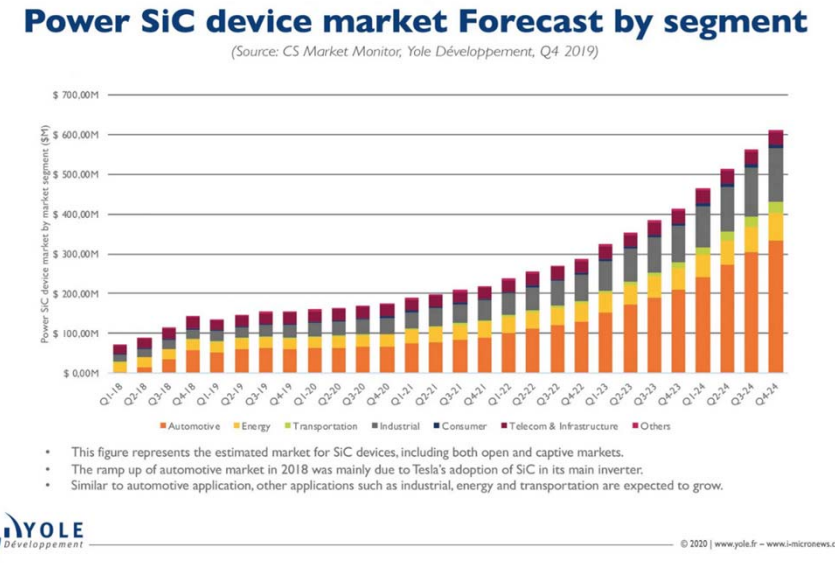
Boyouk N. et al., ISGT-Europe 2018, Sarajevo

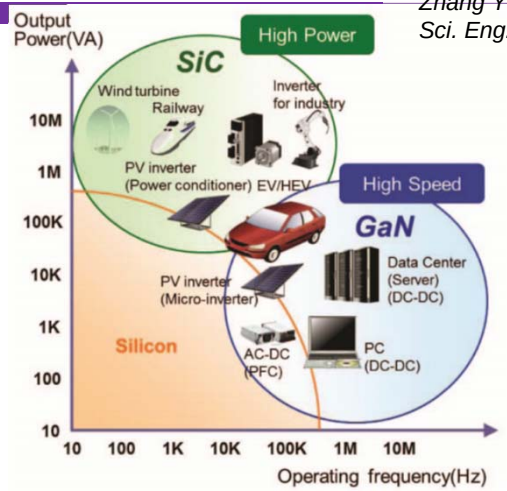


M. Nitzsche et al., PCIM 2019, Nuremberg

Sustainability through energy efficient DC grids

- Motivation, competition and market situation for SiC devices
  - Competition zone Si/SiC/GaN
    - SiC excels at 600V and above
    - High reliability demonstrated
    - Reduction of fabrication cost



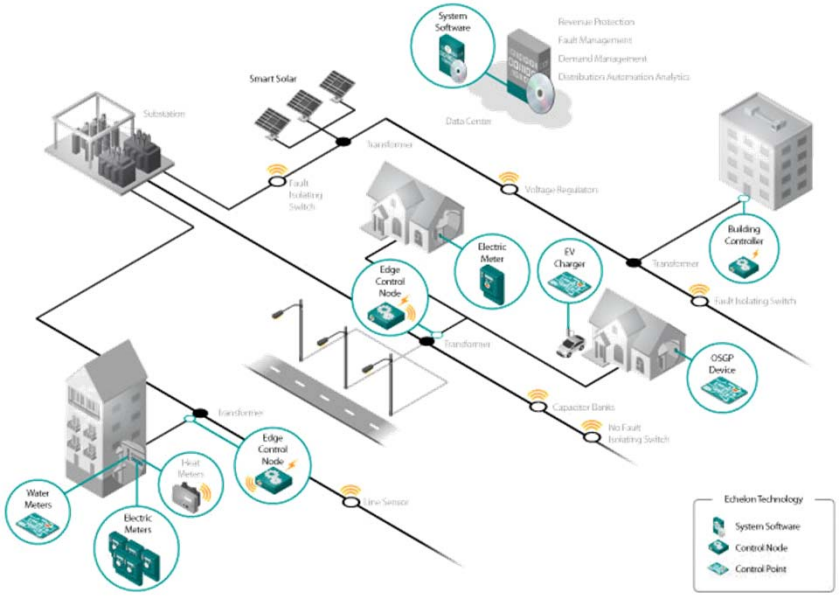


*Zhang Y., Mater. Sci. Eng. **738** 012004*

- Power SiC market trends
  - Ramp-up is imminent
    - Tesla and Toyota kicked it off
    - OEMs are following now
  - Increase in Fab capacity
    - Fab extensions (150/200mm) & Pure-play foundries
    - "Crazy China"

Sustainability through energy efficient DC grids

- Reduction of transmission losses using SiC-based switch-mode power supplies
  - Automotive traction inverters and converters are paving the way…
  - Broad range of generation and consumption for DC grids
    - PV and Wind Power
    - Electrical storage
    - EV Charging infrastructure
    - Manufacturing tools / factories (regulated motors)
    - H2 generation (hydrolysis)
    - Lighting



  - Usually partial load conditions
    - Peak loads are the exception
      → Converter designed for peaks
    - Load shifting or Peak shaving?

Outline

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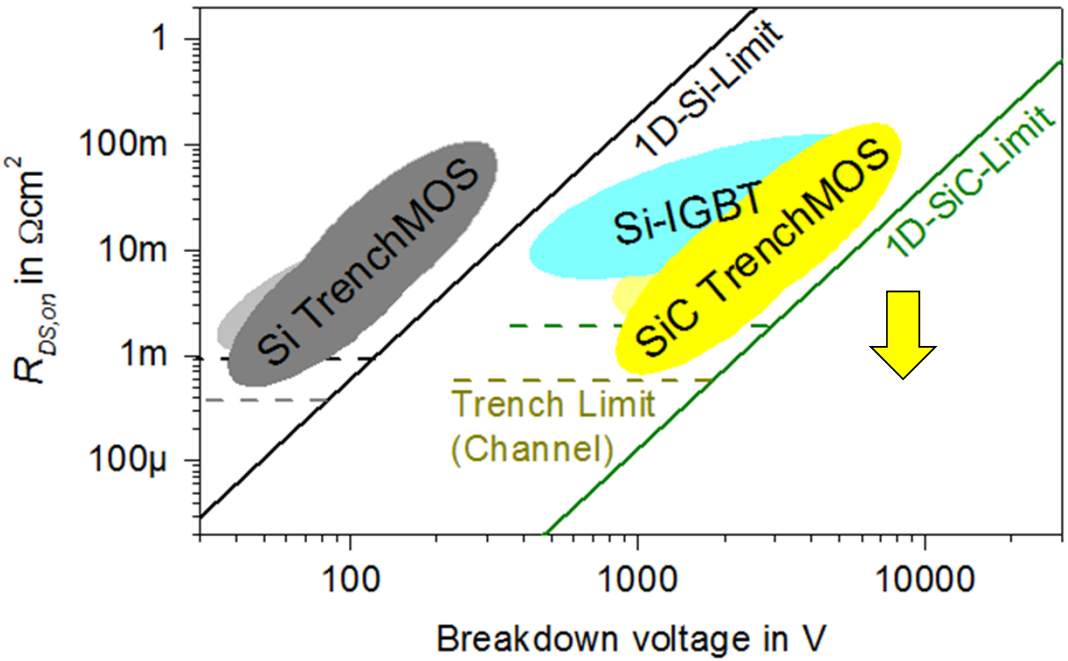
Evolution of SiC Power MOS technology

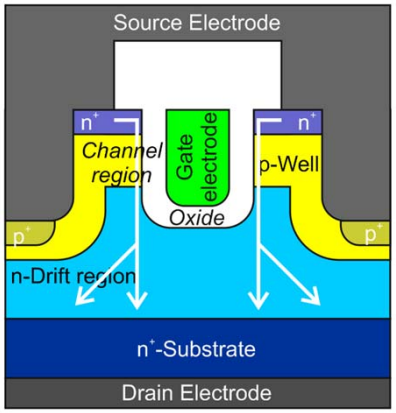
- Task 1: Reduction of On-State resistance to minimize die size/cost
  - Technology development depends on voltage rating



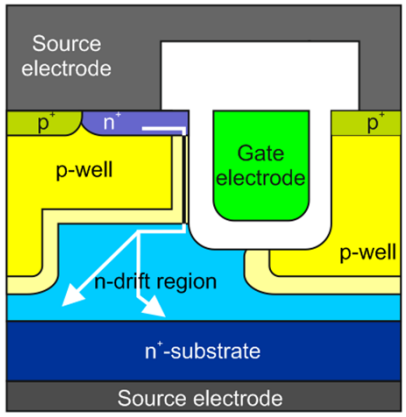
Evolution of SiC Power MOS technology

- Task 1: Reduction of On-State resistance
  - Implementation of trench gates
    - Increased channel mobility along (1 1 -2 0) orientation
    - Vertical channel → Pitch reduction compared to VDMOS
  - Shielding of trench bottom oxide vital!

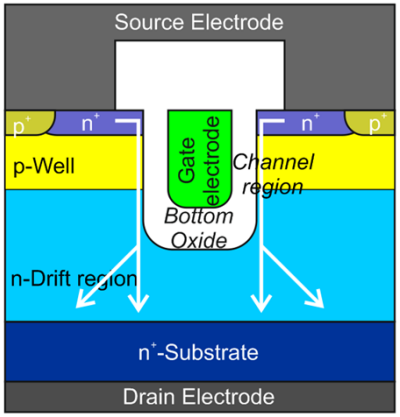
Examples of practical SiC Trench MOS concepts



Rohm / MaxPower Double Trench



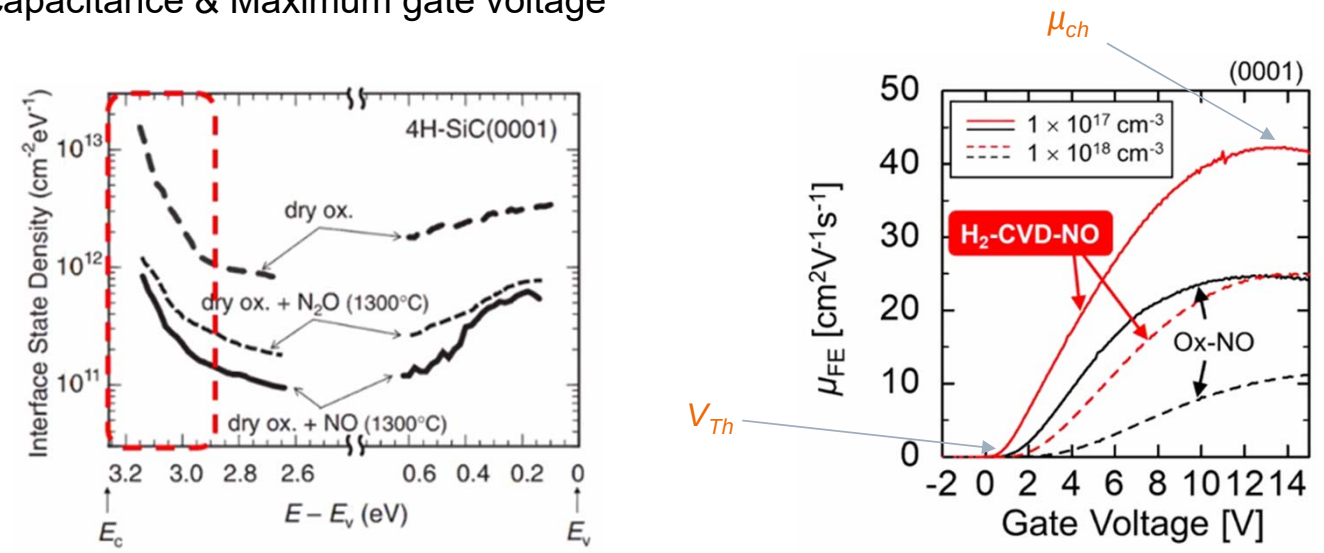
Peters et al., Power-Mag 3 (2017)



Banzhaf et al. MSF 858 (2016) 848-851

Evolution of SiC Power MOS technology

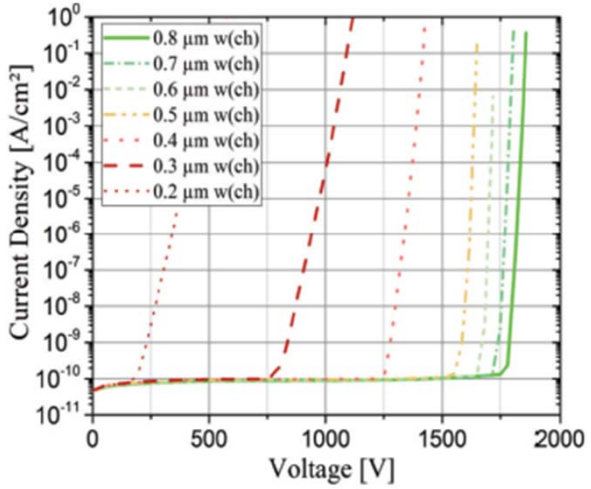
- Task 2: Design for Reliability, Manufacturability and Ruggedness
  - On-state resistance can be “traded off” to achieve application specific goals
  - Example: Gate oxide reliability
    - Choice of gate oxide affects channel resistance (thickness, mobility, V_{th} etc.)
      - Oxide capacitance & Maximum gate voltage



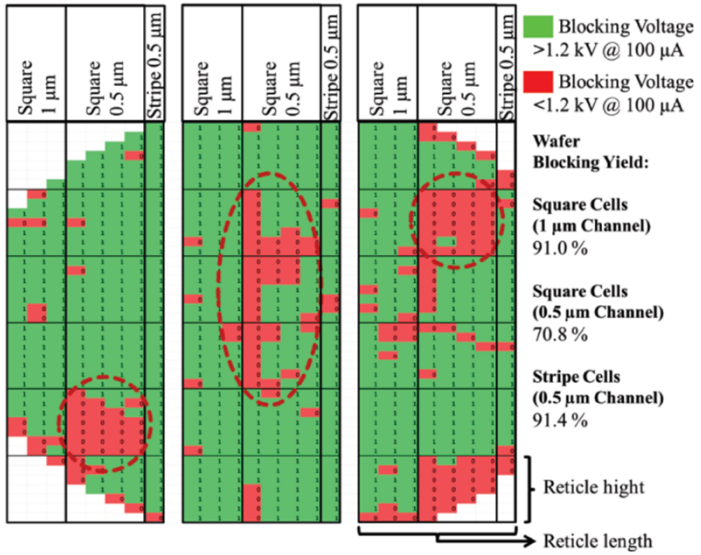
K. Tachiki et al., ECSCRM 2021

Evolution of SiC Power MOS technology

- Task 2: Design for Reliability, Manufacturability and Ruggedness
  - On-state resistance can be “traded off” to achieve application specific goals
  - Example: Integration density limited by overlay accuracy
    - Cell shrink minimizes on-state resistance → But lack of self-aligned gate process
    - Device variations and leakage currents emanate from overlay limitations
    - Self-aligned channel formation technique (additional processing effort)

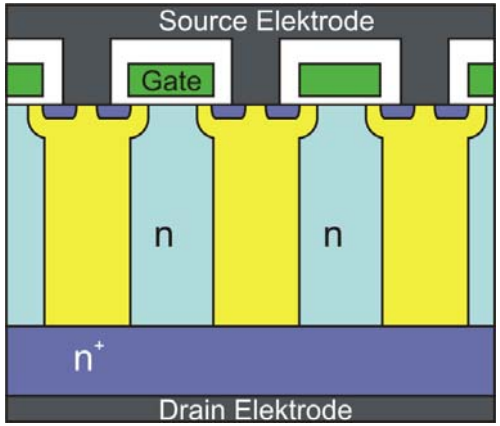


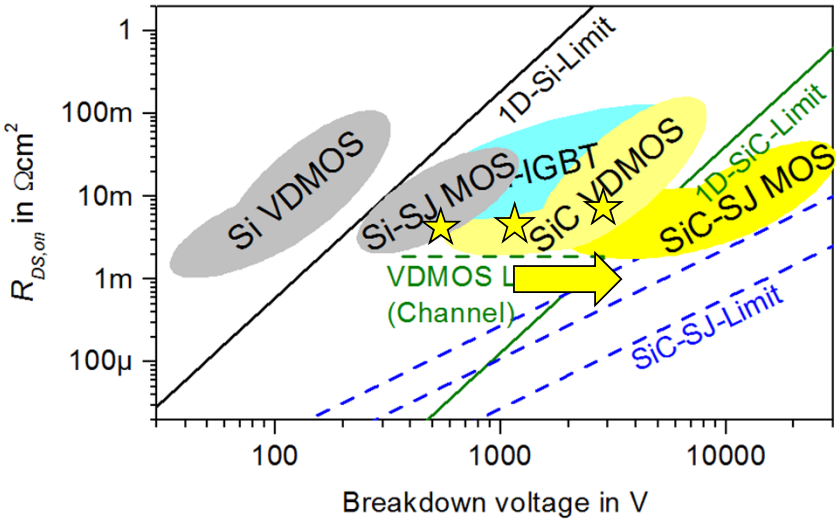
H. Schlichting et al., Mat. Sci. Forum 963 (2018) 763-767



Evolution of SiC Power MOS technology

- Challenges for further advancements
  - Unipolar high voltage devices
  - Superjunction device topology using vertical pillar structure (approx. 60µm @ 10kV)
  - Concepts (similar to Infineon / Toshiba solutions in Silicon):
    - Mid-energy ion implantation and epitaxial overgrowth (rinse & repeat)
    - High-energy ion implantation (e.g. filter implantation)
    - Deep trench etching and epitaxial refill





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Possible goals for further tool optimization

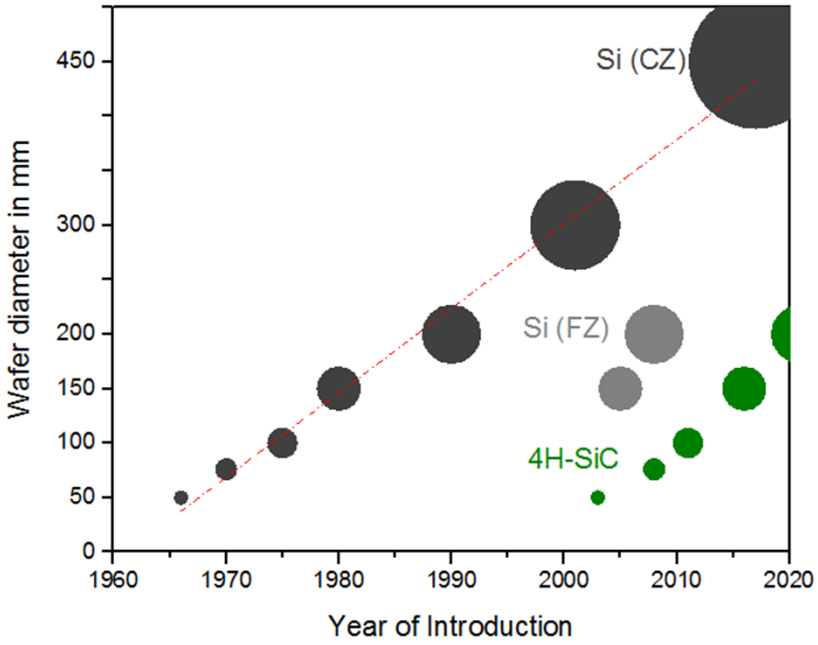
- Challenges from device processing for fabrication tools (SiC examples)
  - High temperature oxidation
    - Reliability issues for gate oxide, by defects induced by epitaxy or process.
    - Need for high reliability gate oxide → optimization of defect density
    - Investigations on long-term reliability required
    - Tool assessment and optimization for HT processing have to be established
  - Implantation and high-temperature annealing
    - Al and N as “new” dopants
    - Silicon implanters are feasible, high-temperature implantation as an addon?
    - High temperature annealing requires capping layer (typically carbon)
  - General requirements
    - Difficult handling of (200 mm) wafers due to warp/bow, need for high volume feasibility
    - Transparent wafers or “back to opaqueness” or both side-by-side?
    - Low manufacturing yield, especially for trench MOSFETs

Possible goals for further tool optimization

- Challenges from device processing for fabrication tools (SiC examples)
  - Lithography requirements are very diverse, resolution is one, but not the only factor
    - Resolution, overlay and alignment accuracy
    - High exposure field size
    - High depth-of-focus
    - High energy dose for thick photoresist
    - Wafer warpage
    - Low costs / high throughput
  - Initial wafer thickness target is 500 µm in order to reach acceptable bow/warp
    - Transition to “standard” 350 µm (for 100/150mm) or even 200 µm is anticipated
  - Backgrinding / Wafer thinning is available with laser annealing of ohmic contacts
    - Temporary wafer bonding
    - Concepts similar to silicon (90µm IGBTs) feasible, manufacturability (line yield)?

Possible goals for further tool optimization

- Challenges from device processing for fabrication tools (SiC examples)
  - 200mm wafer diameter: SiC is on the go…
    - Significant cost in SiC is wafer substrate
    - Larger wafer size enables “double cost down” (per cm^2 wafer & processing)



Main drivers:
- Cost down
- 200mm Si-Fabs available
- Application pull

Main challenges:
- High defect density
- Growing larger diameters (Restart from scratch!)
- Control of wafer bow/warp

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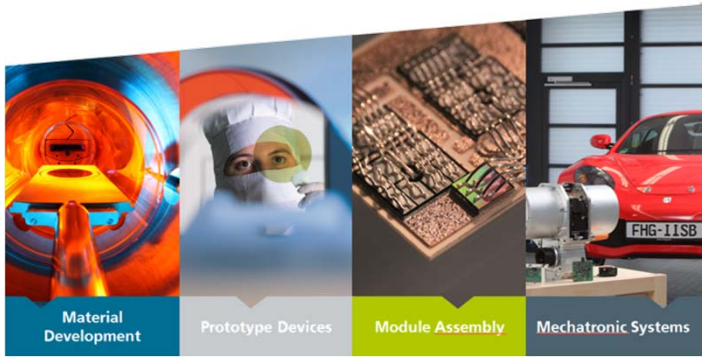
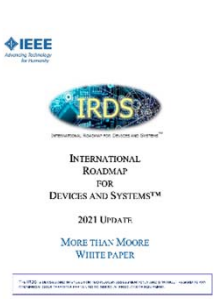
Opportunities and Conclusion

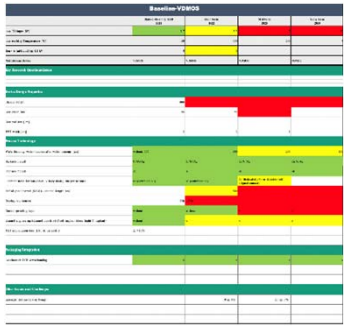
- Development of advanced WB power devices devices has started
- Strong differentiation through performance, reliability, ruggedness trade-offs
  - System performance acts as guideline!
    - *Application specific solutions*

      or

    - *Components-of-the-shelf?*
- Not all technological solutions are known
  - Roadmaps in power electronics (like ITRS/IRDS) are not publicly available, or just started to establish
  - But industry (from tools to fabs) would benefit from clear routes







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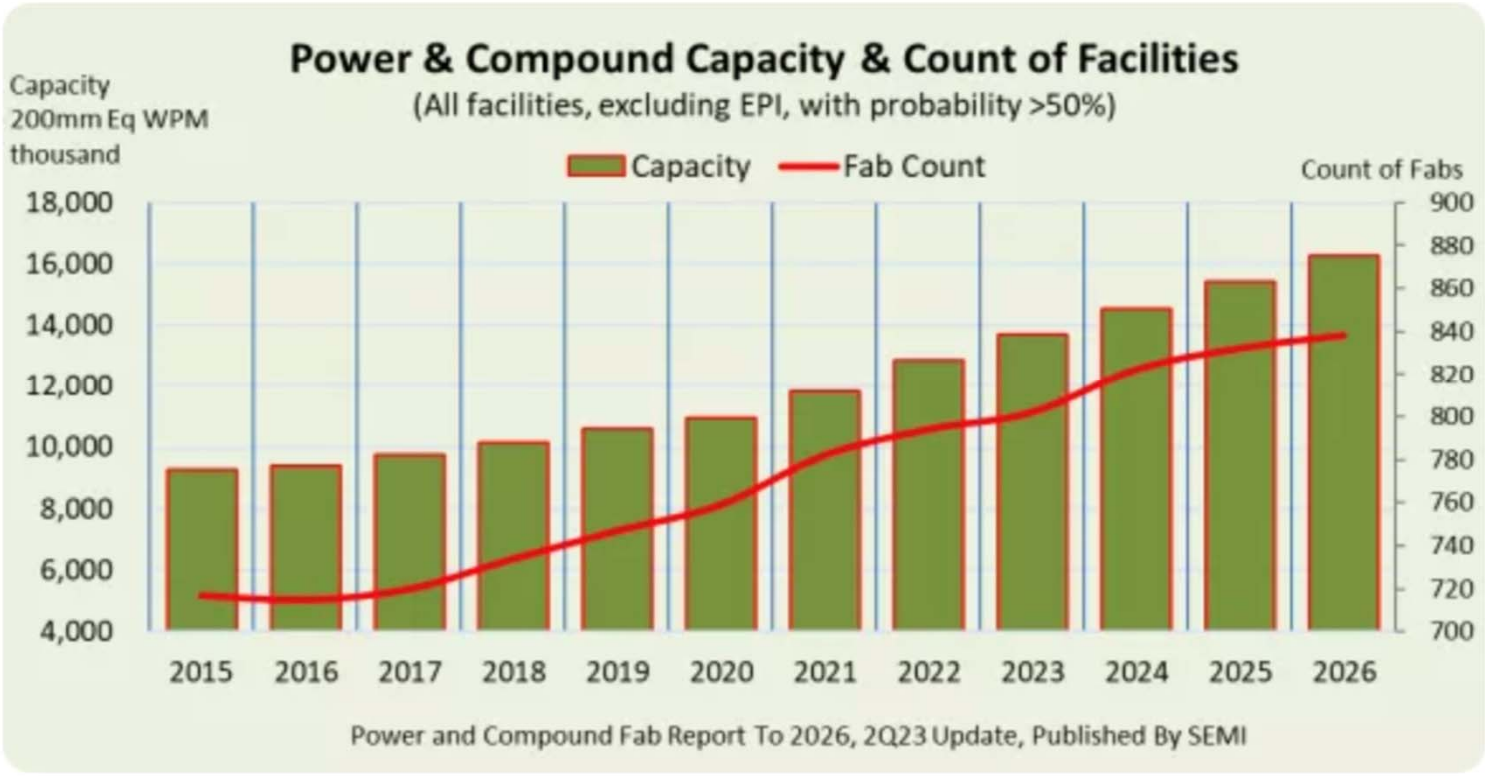
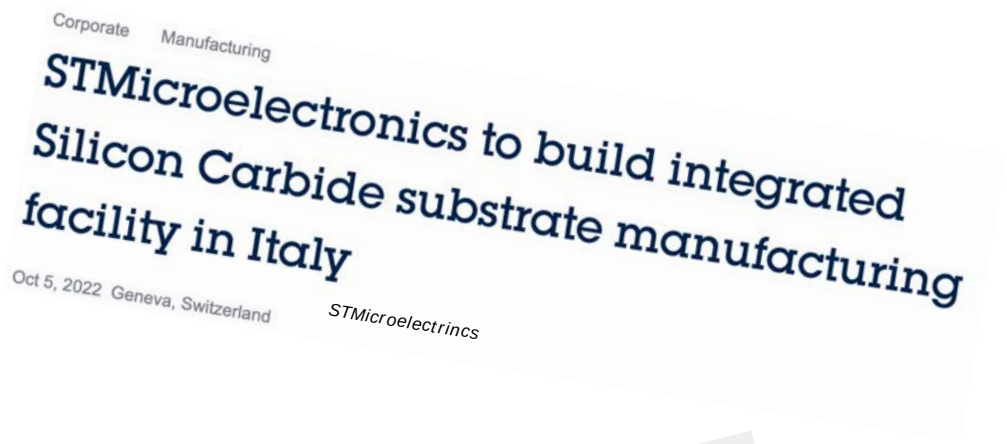
Market Outlook Power



SEMI

Announcements *(just a few examples)*


Corporate Manufacturing

STMicroelectronics to build integrated Silicon Carbide substrate manufacturing facility in Italy

Oct 5, 2022 Geneva, Switzerland

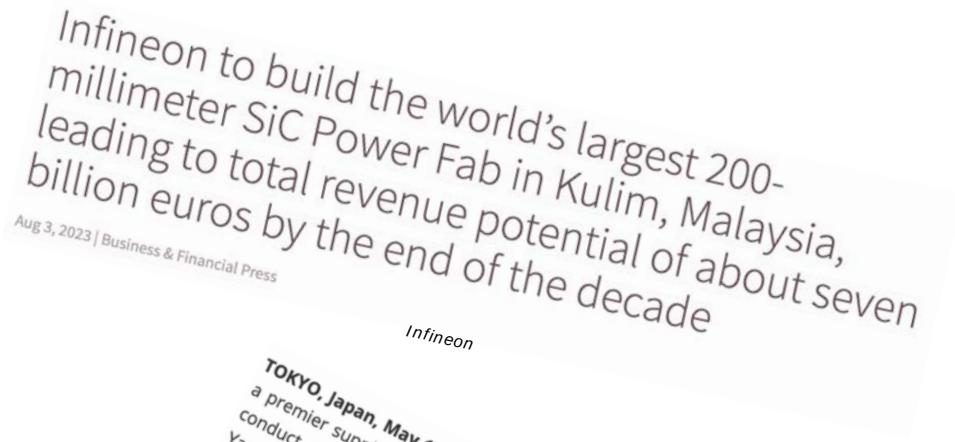
STMicroelectrincs


Corporate, Power

Wolfspeed Announces Plan to Construct World's Largest, Most Advanced Silicon Carbide Device Manufacturing Facility in Saarland, Germany

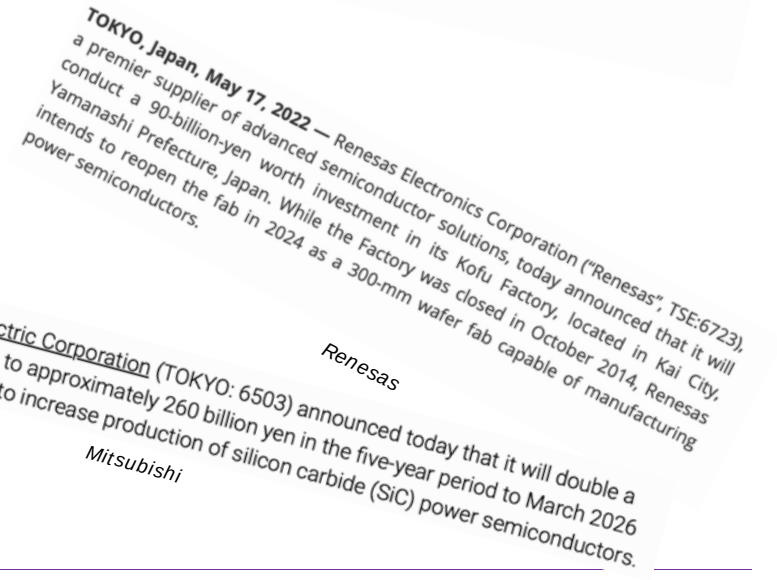
Feb 01, 2023

Wolfspeed


Infineon to build the world's largest 200-millimeter SiC Power Fab in Kulim, Malaysia, leading to total revenue potential of about seven billion euros by the end of the decade

Aug 3, 2023 | Business & Financial Press

Infineon


TOKYO, Japan, May 17, 2022 — Renesas Electronics Corporation ("Renesas", TSE:6723), a premier supplier of advanced semiconductor solutions, today announced that it will conduct a 90-billion-yen worth investment in its Kofu Factory, located in Kai City, Yamanashi Prefecture, Japan. While the Factory was closed in October 2014, Renesas intends to reopen the fab in 2024 as a 300-mm wafer fab capable of manufacturing power semiconductors.

Renesas

TOKYO, March 14, 2023 - Mitsubishi Electric Corporation (TOKYO: 6503) announced today that it will double a previously announced its investment plan to approximately 260 billion yen in the five-year period to March 2026 mainly for constructing a new wafer plant to increase production of silicon carbide (SiC) power semiconductors.

Mitsubishi

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Europe’s Semiconductor Talent Gap Widens

EETimes Europe

Adapting the bauhaus Workshop Concept (µe-Bauhaus)

- Holistic academic-technical master workshop, the “Bauhaus of Microelectronics”
- Theoretically sound and highly practice-oriented training for young master craftsmen and -women
- Committed to responsibility, ethical action and creative exchange
- In association with the Chair of Electron Devices (LEB)

Aim

- Enabling young people to create disruptive innovations
- Empowering our bauhaus community to make important contributions to our society

Headed by
Prof. Dr.-Ing. Jörg Schulze

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Summary / Gaps

- Europe is very strong in R&D
- Worldwide extension of fab capacity for power and compound
- Lack of global road mapping activities in the area of power semiconductors to drive joint development further and bring manufacturing and material costs down
- Semiconductor talent gap is problem for all areas
- Strong initiatives and collaboration in Europe required

Thank you for your attention!