FDSOI engineered substrates for advanced computing

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On Semiconductors

Outline

1- Introduction

2- FDSOI Technology

3- FDSOI Innovative substrate platforms

4- Extending FDSOI Roadmap

5- Take-Aways

Funded by the European Union

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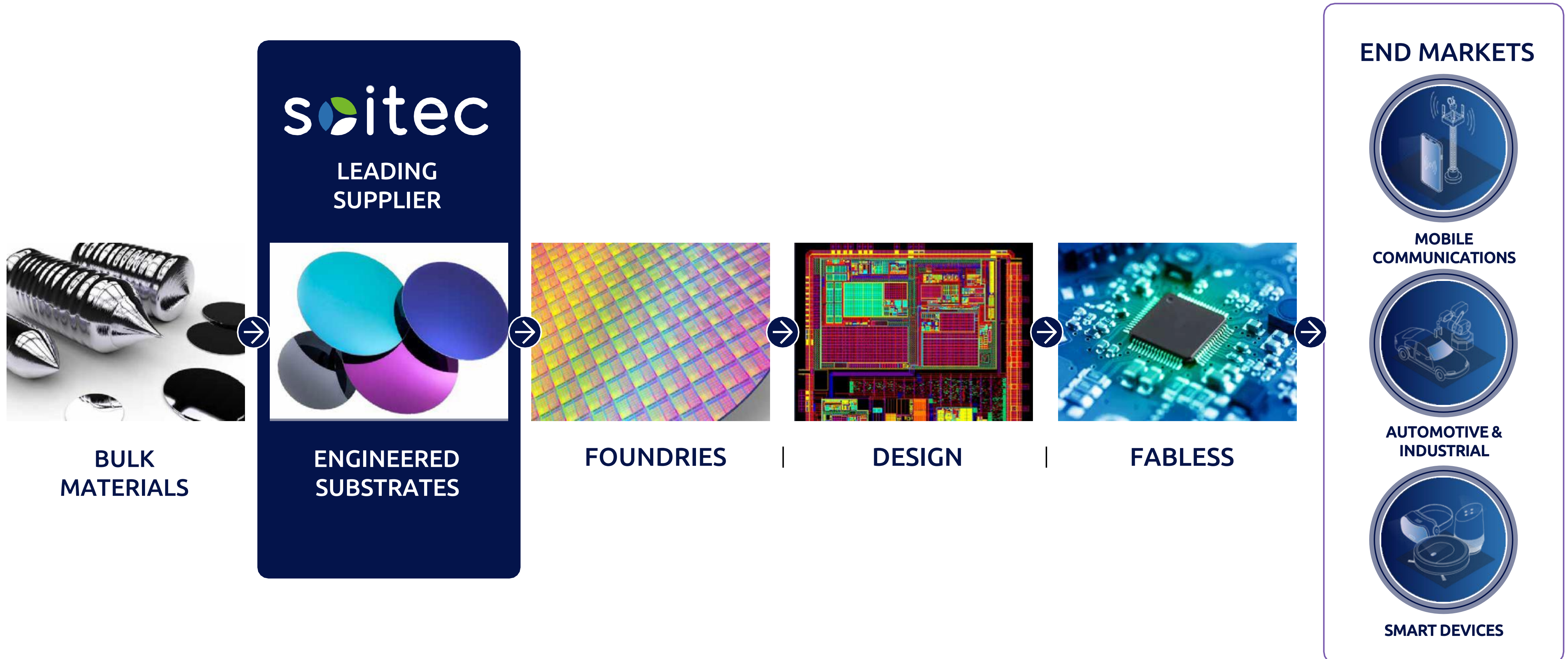
Soitec has built a unique position

In the value chain



Revolutionary Smart Cut™

A mature technology enabling powerful substrates for many applications

TECHNOLOGY

A — 1. Initial silicon — B

A — 2. Oxidation

A — 3. Implantation

4. Cleaning and bonding

B

5. Splitting

6. Annealing and CMP touch polishing

SOI wafer

7. Donor wafer becomes new wafer A

Mono-crystal Top Silicon

Active layer

Buried Oxide

Functional/insulator layer

High Resistivity Silicon

Base wafer = mechanical support
Silicon or easy to handle & active

Achieving Best-In-Class substrates

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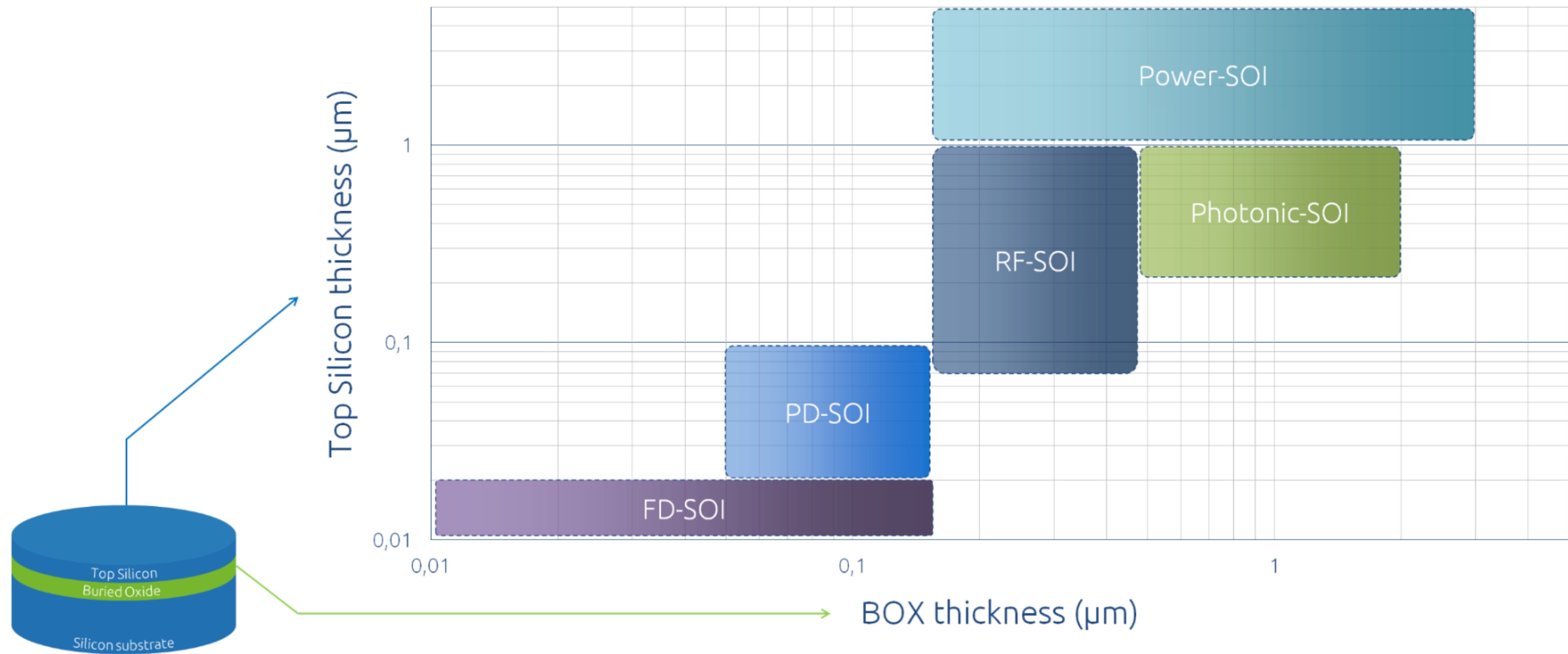
Tightly adjusted for each application



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FD-SOI technology

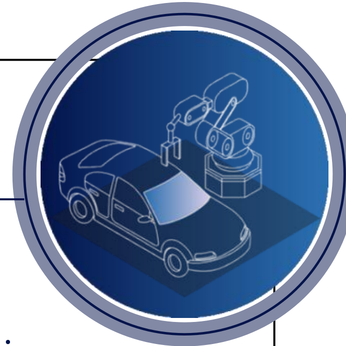
A key technology at the crossroad of 3 orthogonal markets

CONNECT

MAIN DRIVERS
- 5G mmW
- 5G sub-6 GHz
- Mobile infrastructure
- Wi-Fi 6

SOITEC PRODUCTS

Connect RF-SOI	Connect FD-SOI
Connect POI	Connect RF-GaN



AUTO

MAIN DRIVERS
- Autonomous cars
- Vehicle electrification
- Infotainment
- Industry 4.0

SOITEC PRODUCTS

Auto Power-SOI	Auto FD-SOI
Auto SmartSiC™	Auto GaN

SMART

MAIN DRIVERS
- Edge computing
- 3D sensing & Healthcare
- Smart home & Smart cities
- Data centers

SOITEC PRODUCTS

Smart FD-SOI	Smart Imager-SOI
Smart Photonics-SOI	Smart PD-SOI

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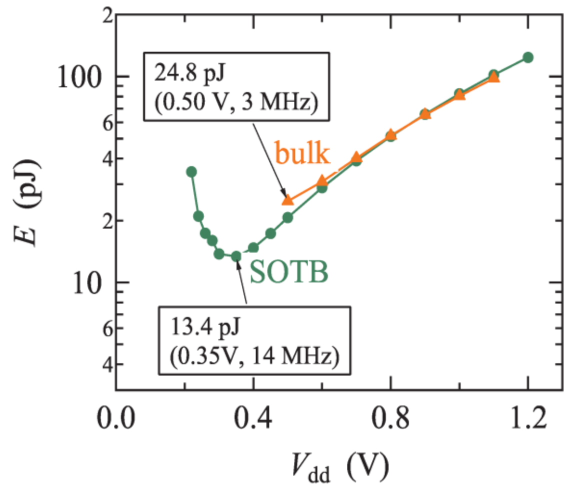
FDSOI Key features

Ultra Low Voltage

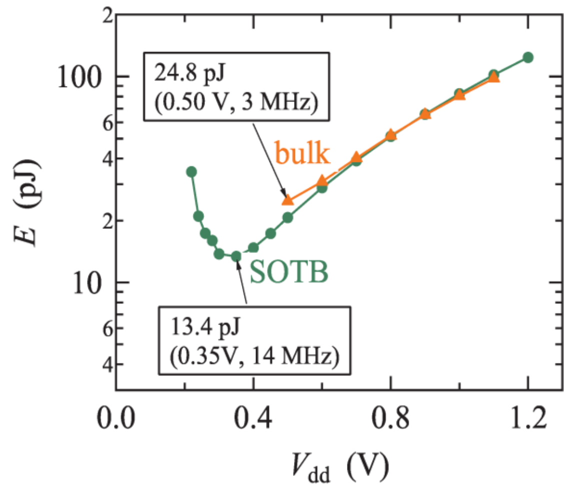


Source: Sugii ,Low Power El. Appl. 2014

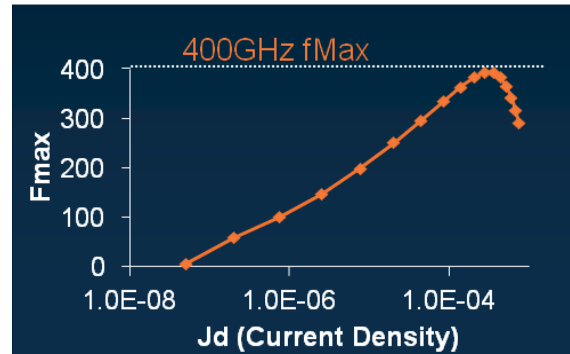
Operation at minimum energy point (<0.4V)

FDSOI Key features

Ultra Low Voltage	mmWave RF-CMOS



Source: Sugii ,Low Power El. Appl. 2014

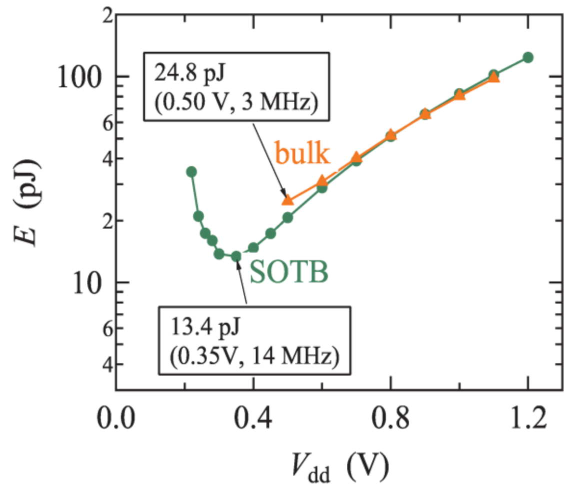


Source: GF, GTC2017

Operation at minimum energy point (<0.4V)	Best CMOS mmWave

FDSOI Key features

Ultra Low Voltage	mmWave RF-CMOS	Body Bias



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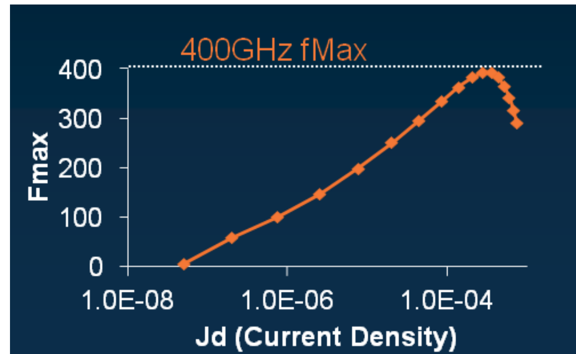
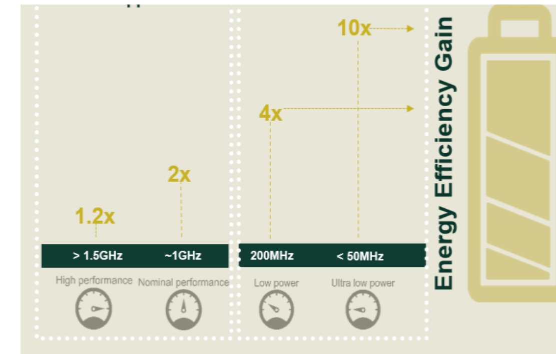


Source: GF, GTC2017



Source: P.Flatresse, ISSCC 2021

Operation at minimum energy point (<0.4V)	Best CMOS mmWave	10X energy efficiency gains

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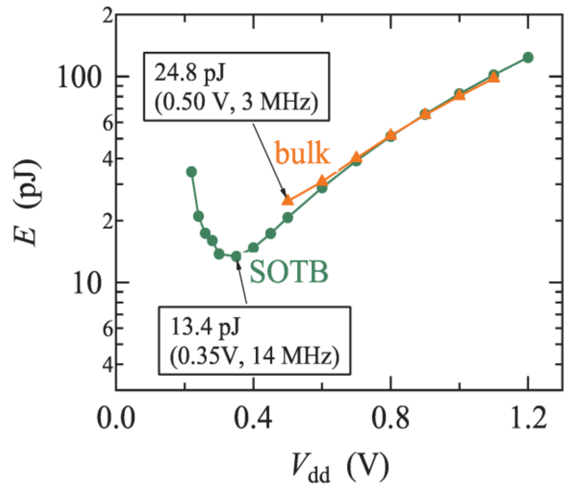
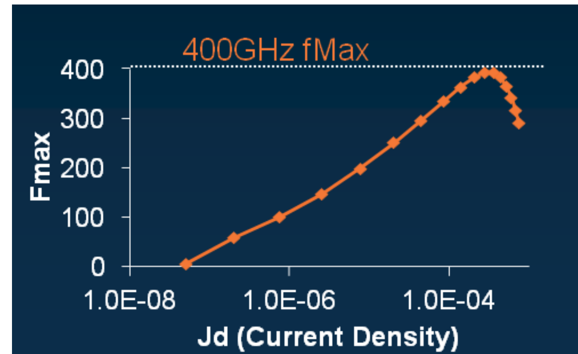
FDSOI Key features

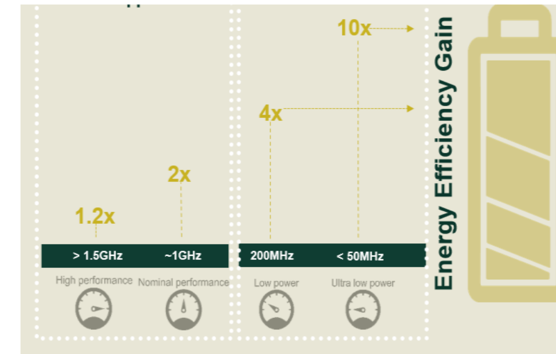
Ultra Low Voltage	mmWave RF-CMOS	Body Bias	Reliability



Source: Sugii ,Low Power El. Appl. 2014



Source: GF, GTC2017



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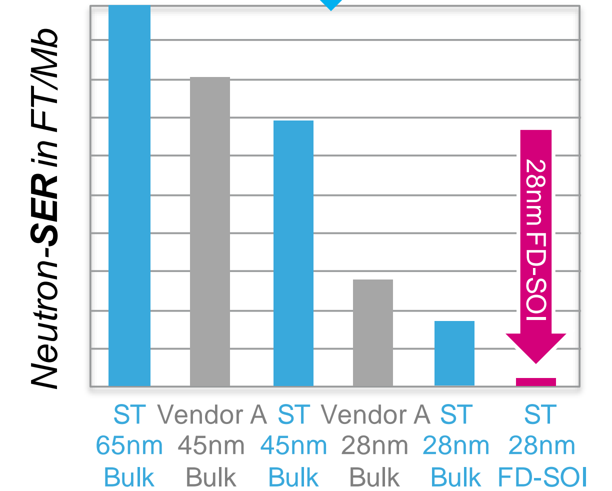

Source: ST, Shanghai FDSOI forum, 2015

Operation at minimum energy point (<0.4V)	Best CMOS mmWave	10X energy efficiency gains	20x Soft Error Rate improvement vs. bulk

A multi nodes FDSOI substrates roadmap

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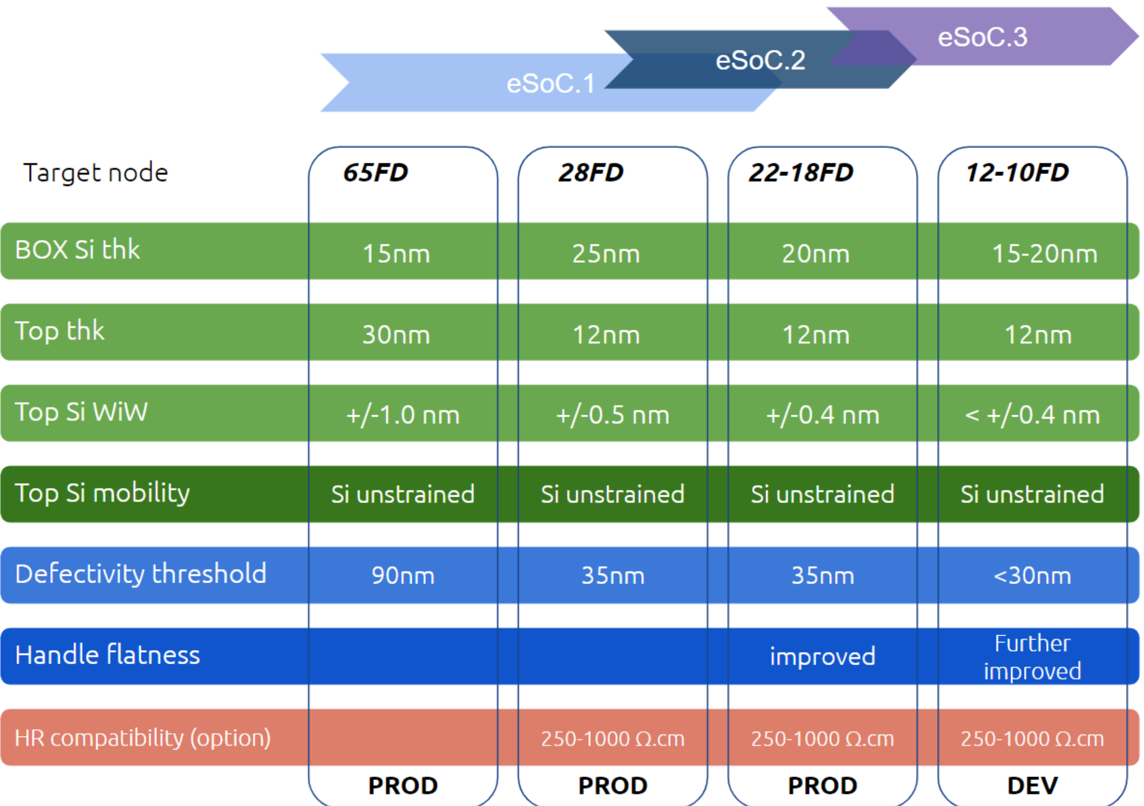
Evolutionary scaling through FDSOI roadmap

- FDSOI substrates generations named eSoC (electrical Shrink On Chip)

eSoC.1
Towards zero poxer and cost optimization
Single & Multichip gen
Low Power
Higher Fmax

eSoC.2
More Energy efficiency
Higher performance
Digital & mmW co-integration

eSoC.3
More Intelligence and Connectivity
Higher edge computing
High speed network
High speed connect



Target node	65FD	28FD	22-18FD	12-10FD
BOX Si thk	15nm	25nm	20nm	15-20nm
Top thk	30nm	12nm	12nm	12nm
Top Si WiW	+/-1.0 nm	+/-0.5 nm	+/-0.4 nm	< +/-0.4 nm
Top Si mobility	Si unstrained	Si unstrained	Si unstrained	Si unstrained
Defectivity threshold	90nm	35nm	35nm	<30nm
Handle flatness			improved	Further improved
HR compatibility (option)		250-1000 Ω.cm	250-1000 Ω.cm	250-1000 Ω.cm
	PROD	PROD	PROD	DEV

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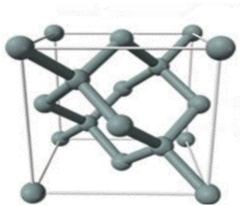
Atomic size control of SOI uniformity

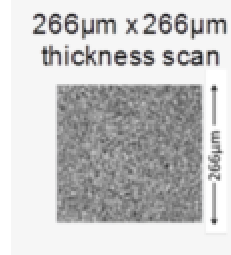
Soitec State of the art – eSoC.2 performances

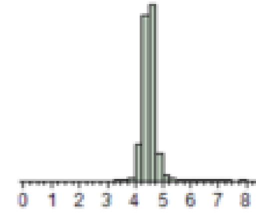
Millions wafers controlled at atomic level, all points,all wafers

± 4 Å

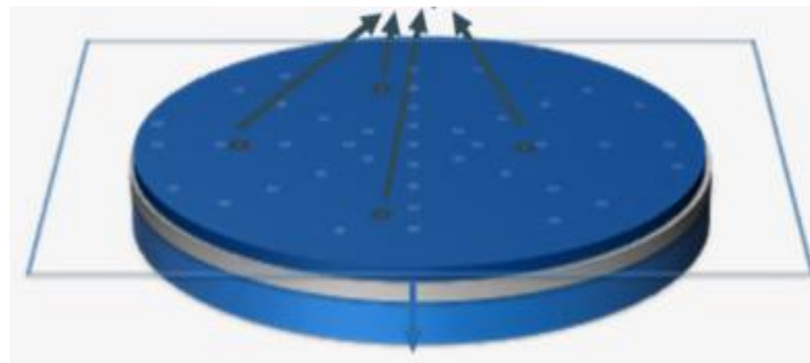


Mature process and yield in HVM

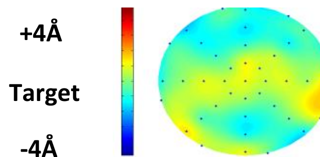


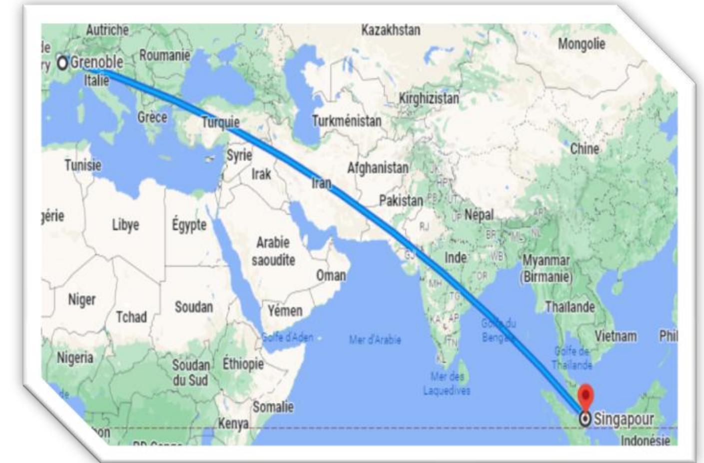


Die level thickness range



Top Silicon
Full wafer thickness deviations





Grenoble – Singapore
+/- 3cm

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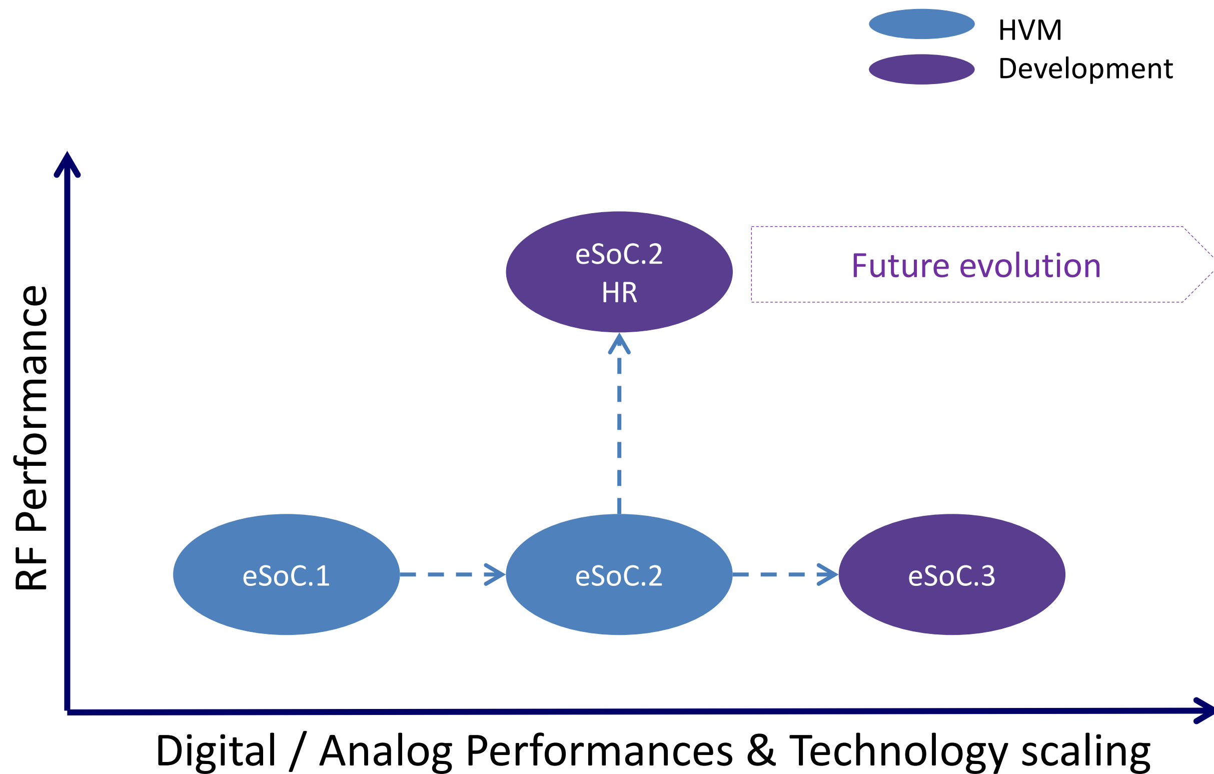
FDSOI substrates enhancement

High digital, analog & RF performances



3 market drivers for eSoC.2 HR & eSoC.3 platforms :
AI MCUs , 5G mmW & Automotive

Arbe Robotics ; 4D imaging radar
22nm FD-SOI

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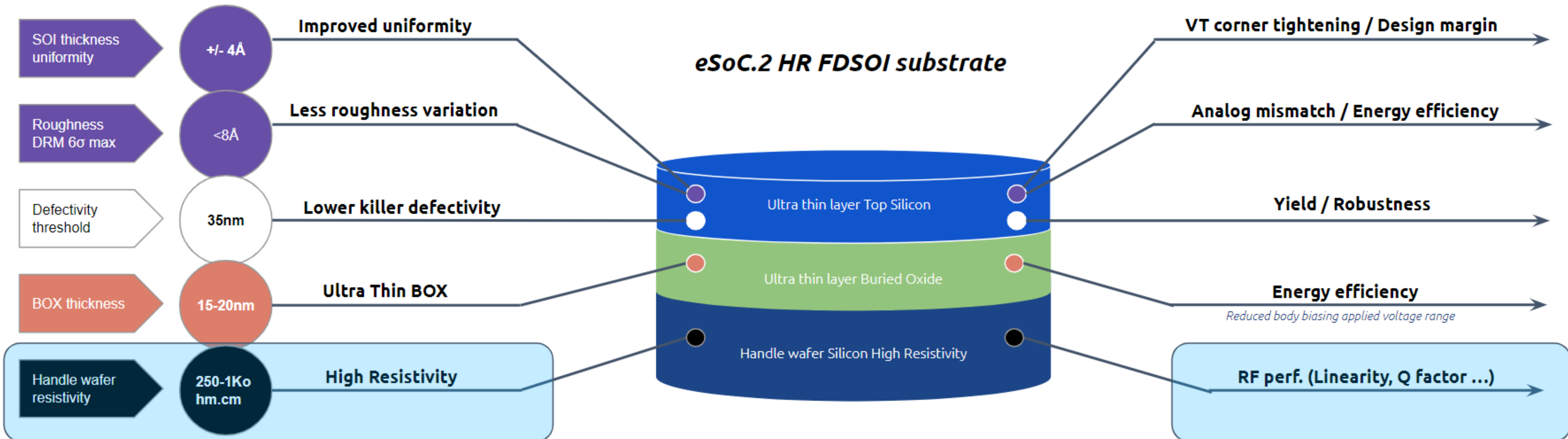
eSoC.2 HR

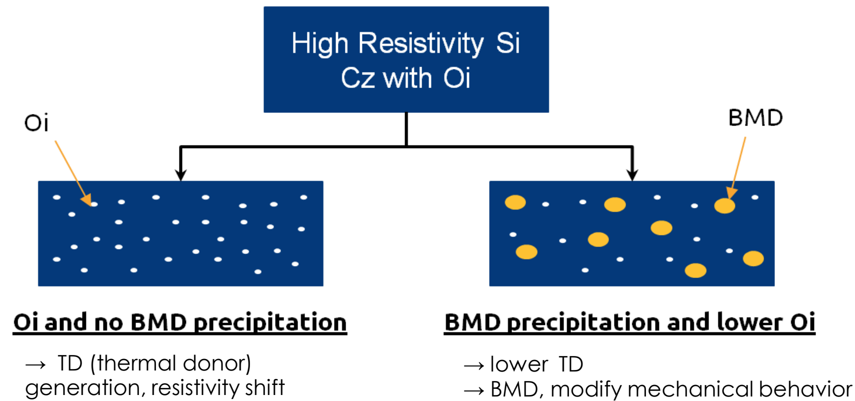
eSoC2.HR enables digital & RF co-integration performances

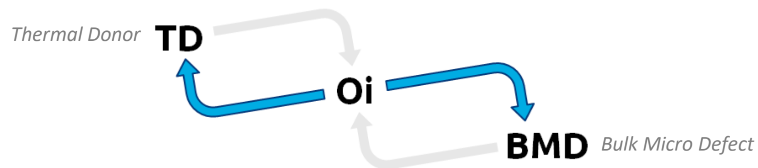


FD HR substrate technical challenges

*Interstitial Oxygen concentration

[Oi]* control is key to manage technical risks



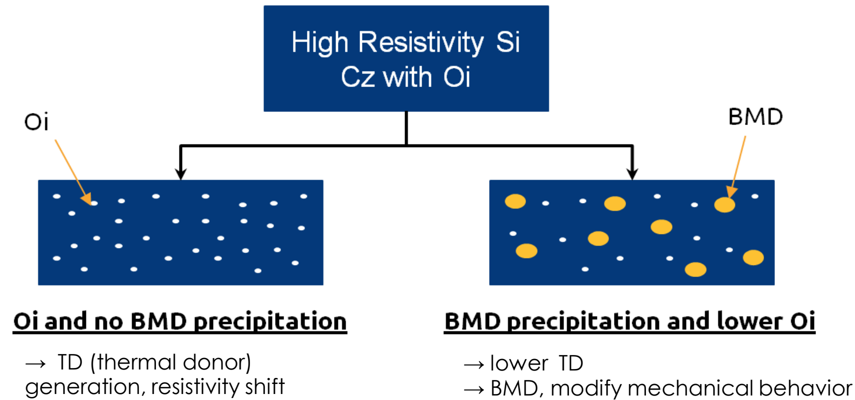


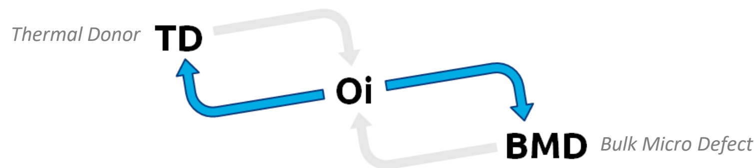
TD generation or BMD precipitation from Oi depending on thermal budgets

FD HR substrate technical challenges

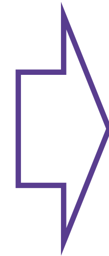
*Interstitial Oxygen concentration

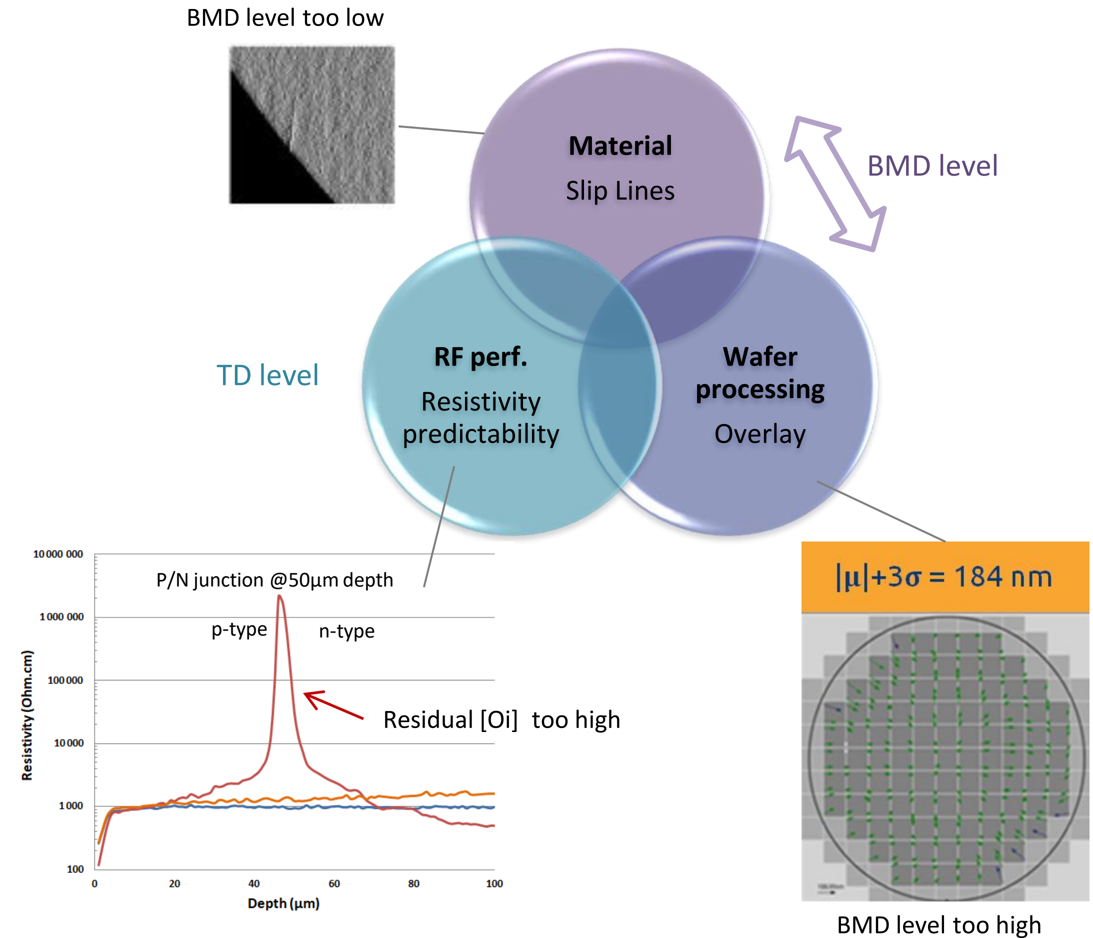
[Oi]* control is key to manage technical risks





TD generation or BMD precipitation from Oi depending on thermal budgets





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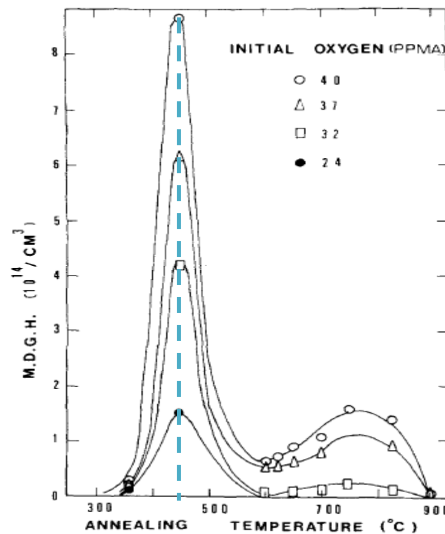
eSoC.2 HR performances

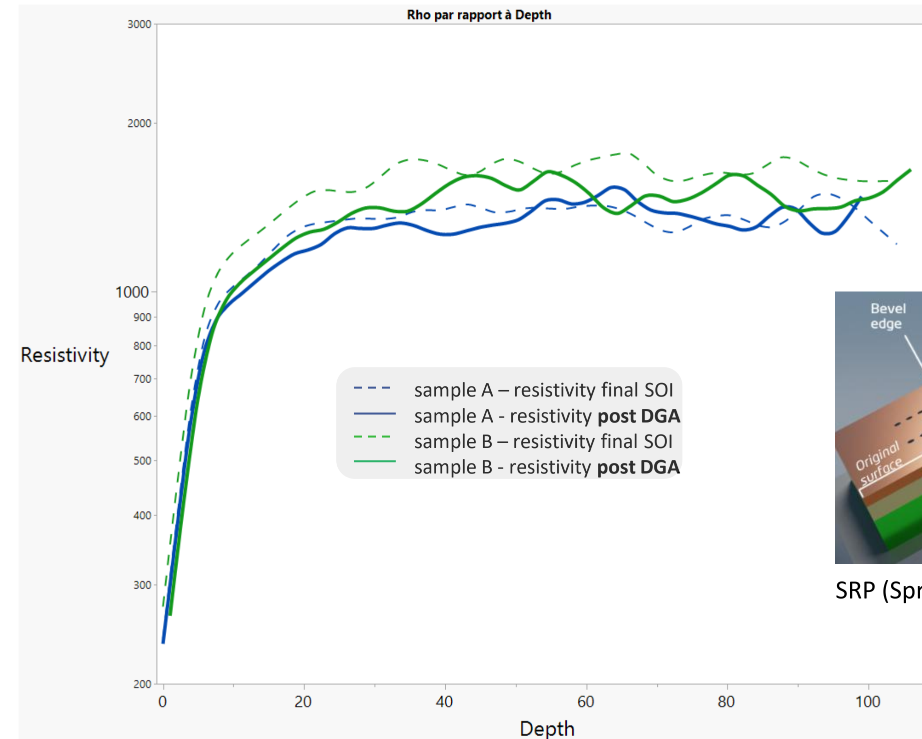
Resistivity predictability

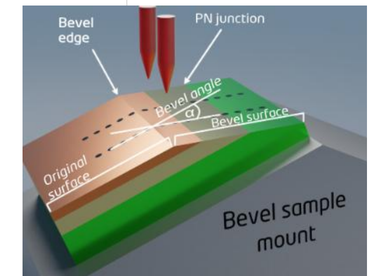
Back-end of line simulation

=> DGA (Donor Generation Anneal) on final SOI substrate between 400 & 450°C



Source : Cazcarra and Zunino, J.A.P 1980





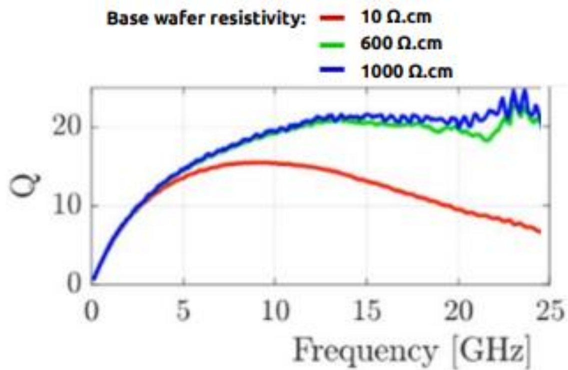
SRP (Spreading Resistivity Profile)

Resistivity stability post DGA : validates eSoC.2 HR process & material orientations

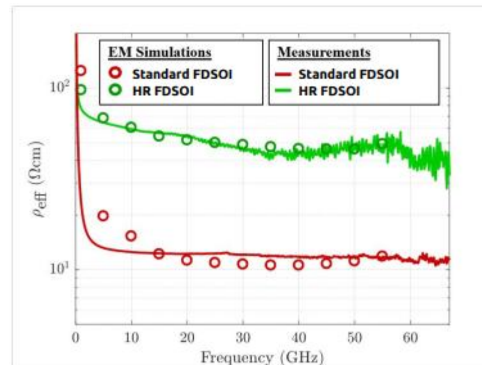
eSoC.2 HR performances

At device level

RF Performances

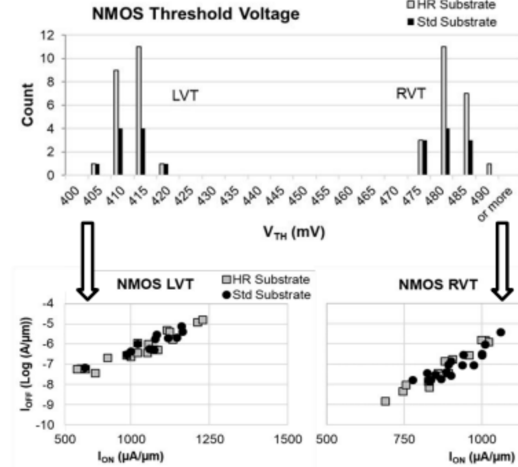


Adapted from L. Nyssens et al. MIKON 2022



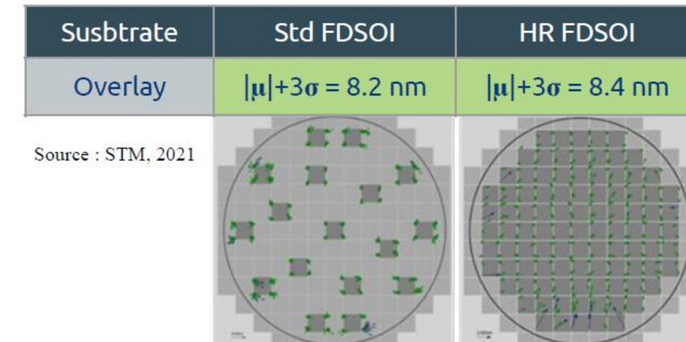
L. Nyssens et al. EUROSOI 2022

Logic performances



Adapted from I. Bertrand et al. ECS 2022

Wafer processing



Susbtrate	Std FDSOI	HR FDSOI
Overlay	$\lvert\mu\rvert+3\sigma$ = 8.2 nm	$\lvert\mu\rvert+3\sigma$ = 8.4 nm

Source : STM, 2021

Adapted from I. Bertrand et al. ECS 2022

50% inductor Q-factor improvement and increased effective resistivity

Moving to HR base impacts neither wafer processing nor logic devices performance

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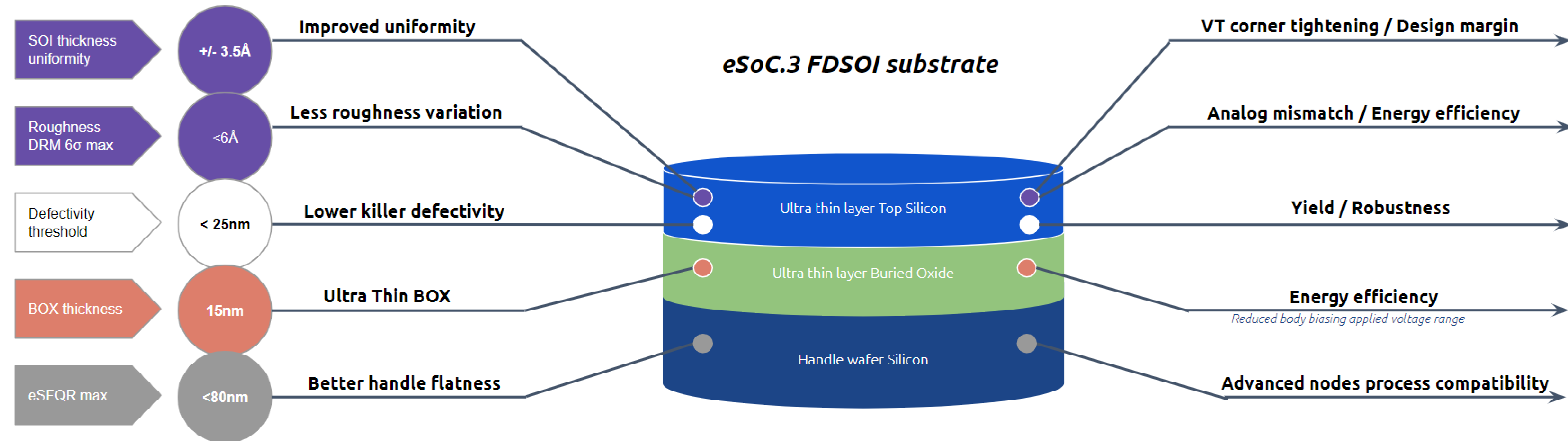
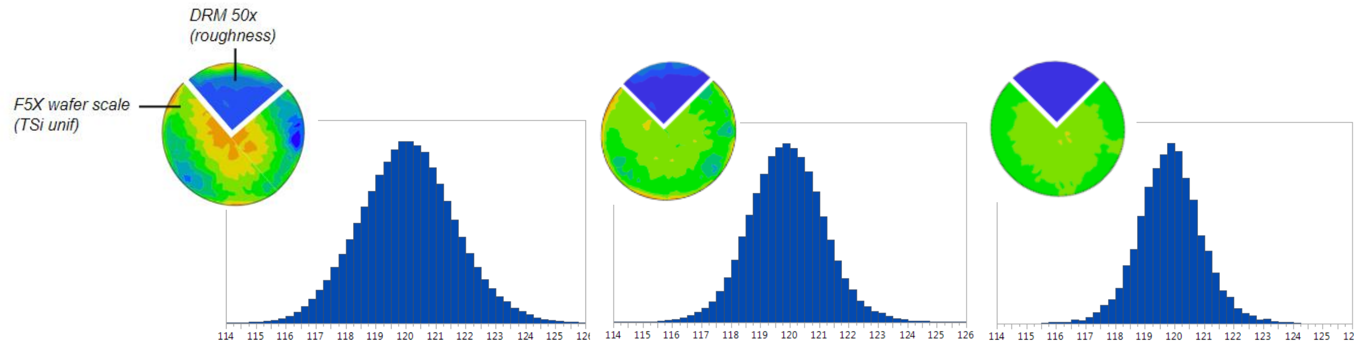
eSoC.3 new platform

Innovative substrate pushing device gains / performances

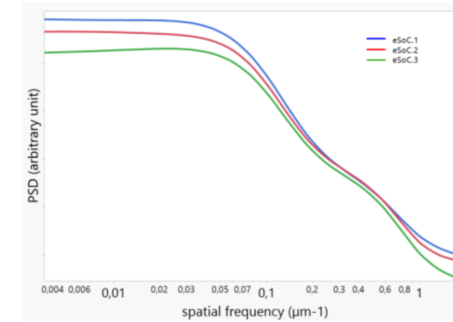


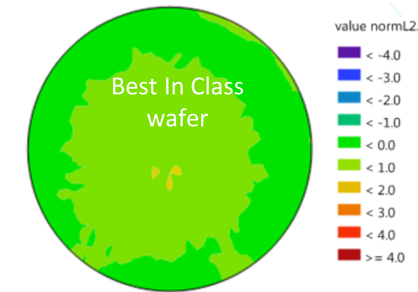
eSoC.3 perfomances

Ultimate thickness control at each spatial frequency



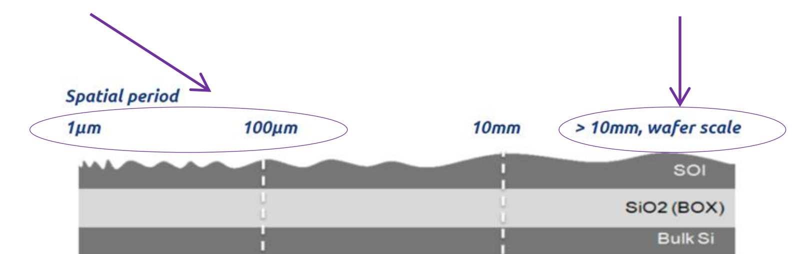
eSoC.1	eSoC.2	eSoC.3
Global Tsi uniformity (41 points per wafer measuring min / max)		
+/-5Å	+/-4Å	+/-3.5Å
Roughness DRM 6σ		
<10Å	<8Å	<6Å



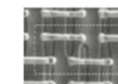


From Local …

to Global thickness control

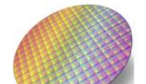


Transistor


Elementary circuits

Integrated sub-circuit

Die


Wafer

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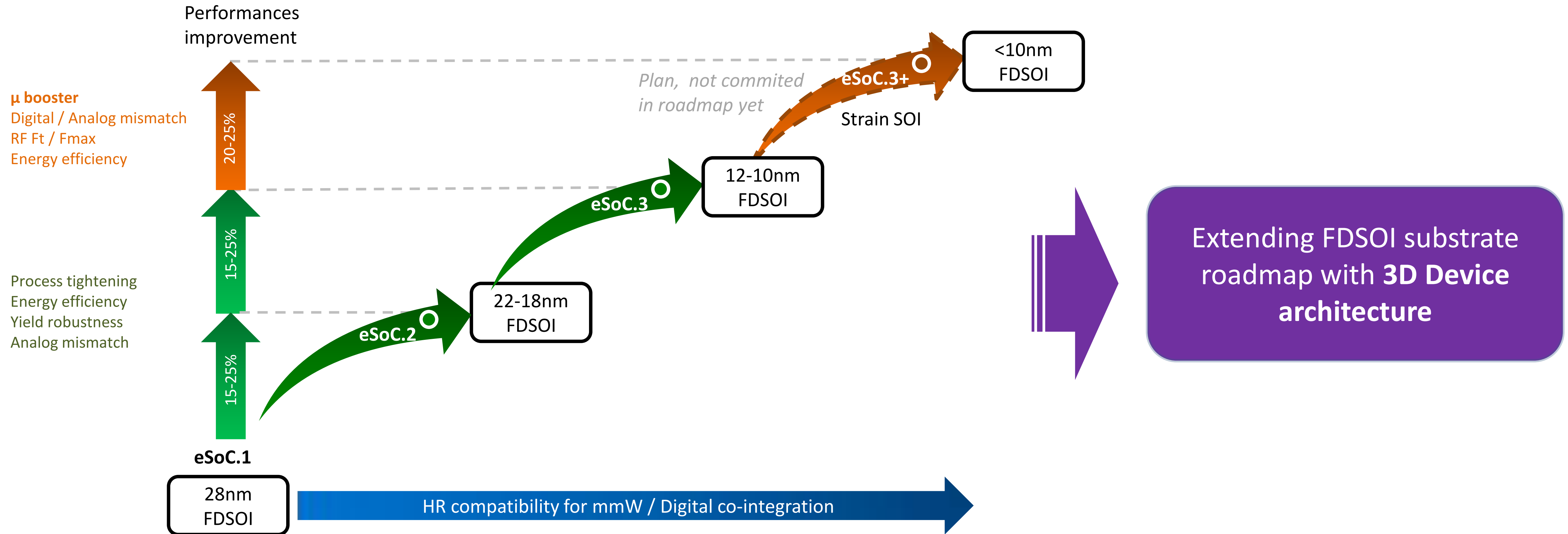
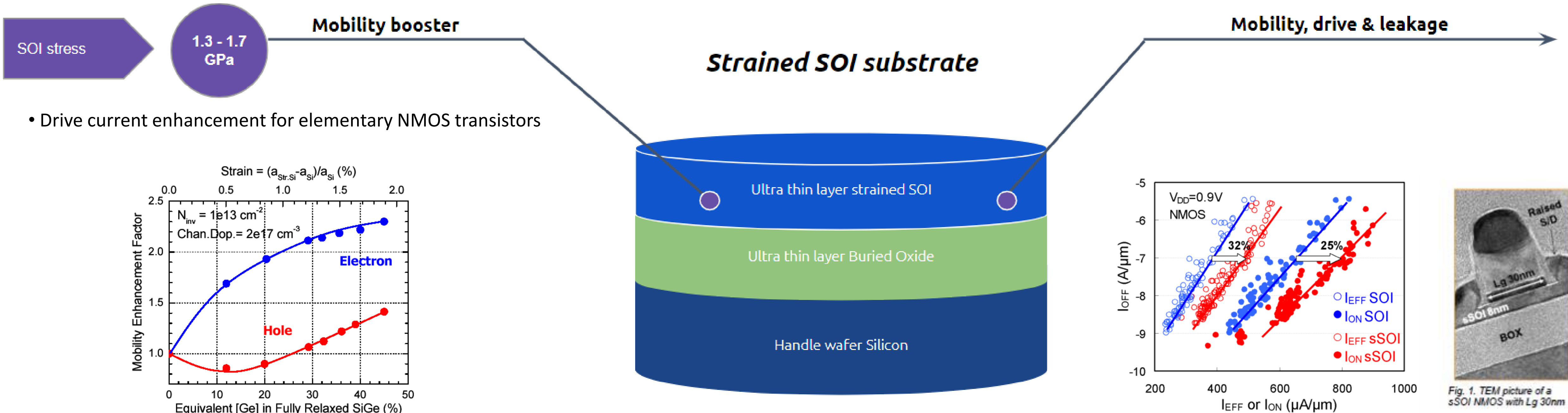
Extending FDSOI roadmap

Going beyond 10nm ?



eSoC.3+ Strained SOI

Innovative substrate pushing device gains / performances



- Drive current enhancement for elementary NMOS transistors

Fig. 4. Mobility enhancement vs. strain and [Ge] in strained Si/relaxed SiGe MOSFETs at 1e13 cm-2 carrier concentration.

Fig. 1. TEM picture of a sSOI NMOS with Lg 30nm

O. Faynot et al., IEDM'10

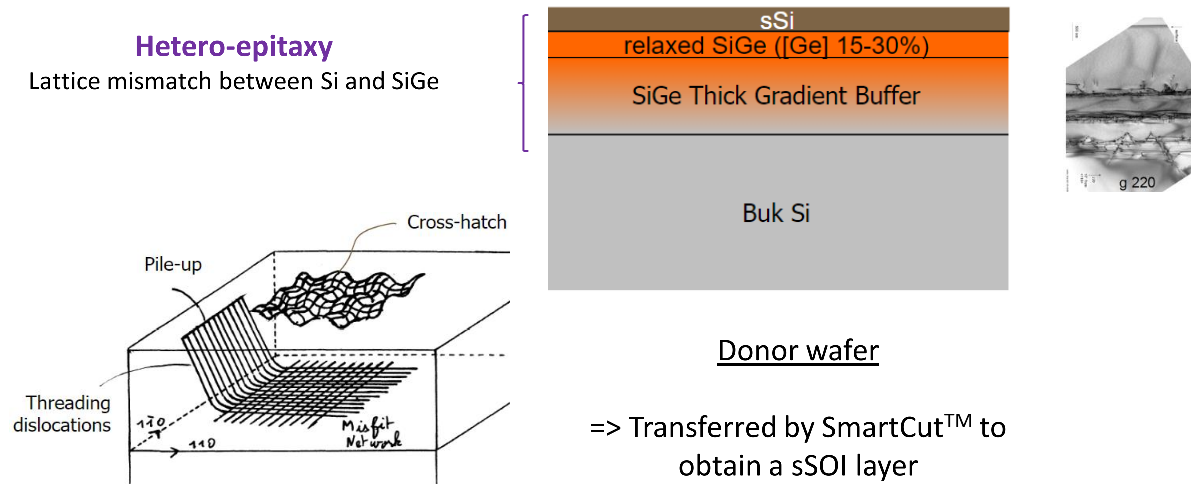
- Strain relaxation for PMOS co-integration

eSoC.3+ Strained SOI

Technical challenges , perspectives

Cristalline quality considering defectivity (Threading Dislocations Density, Voids)

Hetero-epitaxy
Lattice mismatch between Si and SiGe



Donor wafer

=> Transferred by SmartCut^{TM} to obtain a sSOI layer

Funded by the European Union

eSoC.3+ Strained SOI

Technical challenges , perspectives

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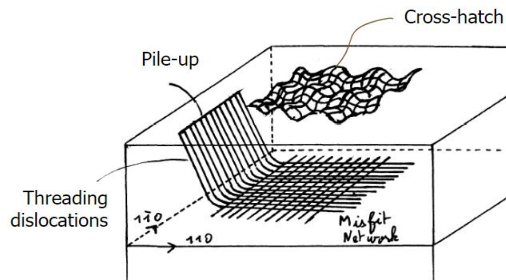
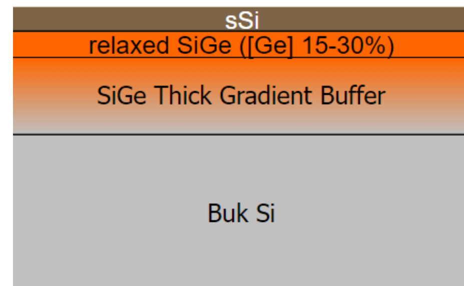
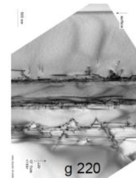
Lattice mismatch between Si and SiGe







Donor wafer

=> Transferred by SmartCut™ to obtain a sSOI layer

sSOI collaborative program perspectives

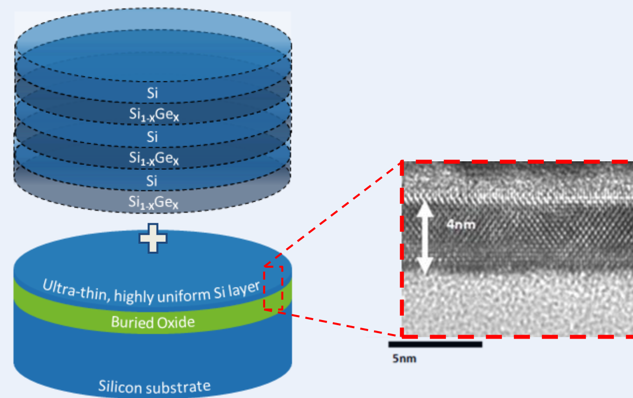
Long term for FDSOI Ecosystem expansion & solidification leading to sovereignty in Europe

Extending FDSOI roadmap

Gate-All-Around & CFET

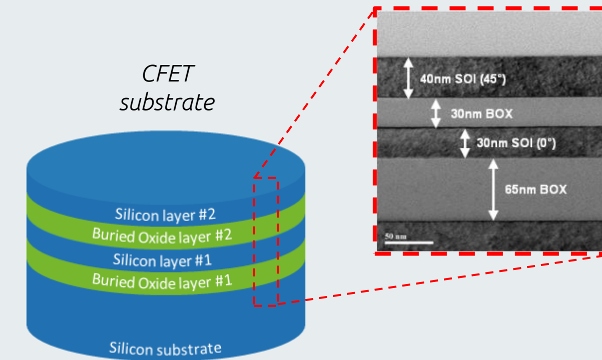
For GAA devices

- *Ultra-thin FD-SOI substrates, allowing uniform Si/SiGe superlattice growth*
- *Buried oxide cancels leakage current and brings lower capacitance with respect to bulk*



For CFET devices

- *Multi-layered FD-SOI substrate featuring Hybrid Orientation Technology, maximizing mobility*
- *Channels isolated from each other, enabling material co-integration*
- *Buried oxide to better control elevation during processing*



Extending FDSOI roadmap

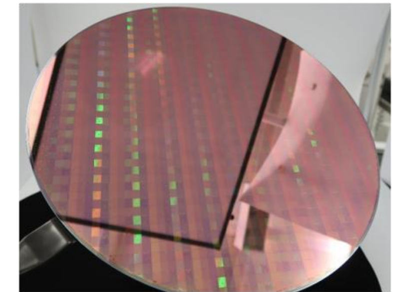
Ultimate 3D integration and co-integration

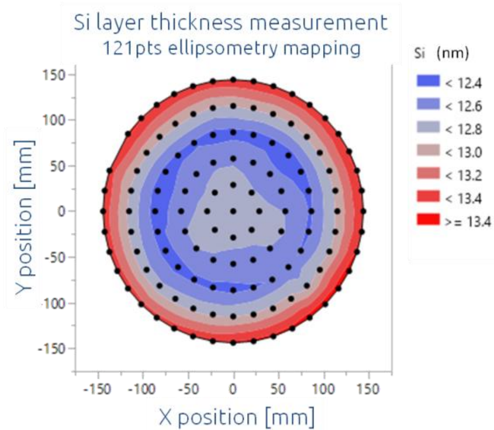
FD-like, ultra-thin layer transfer on processed wafers for:

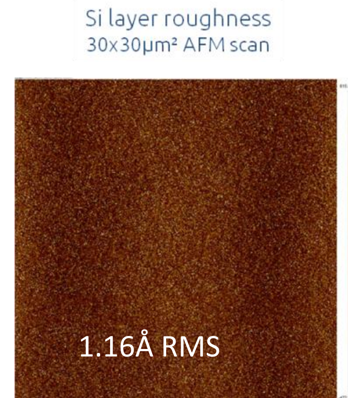
- **CFET-like scaling approach**

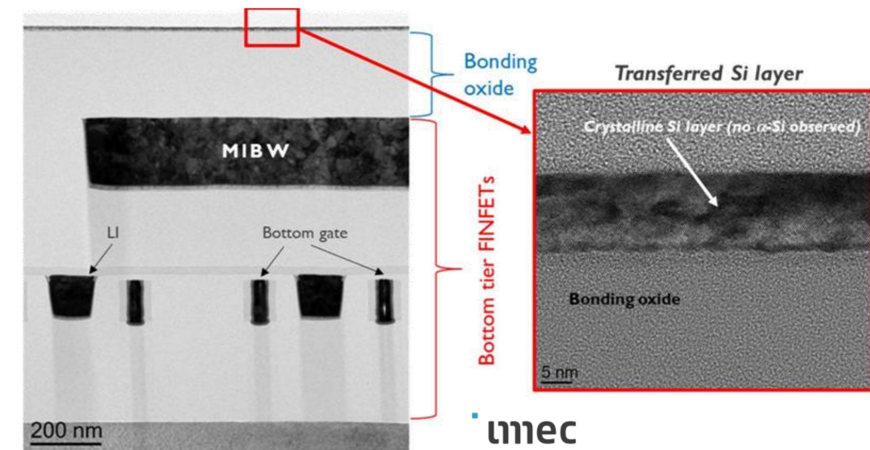
&

- **Heterogeneous integration**









ICOS International Cooperation On Semiconductors

Outline

1- Introduction

2- FDSOI Technology

3- FDSOI Innovative substrate platforms

4- Extending FDSOI Roadmap

5- Take-Aways

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Take-Aways

- FD-SOI is progressing rapidly across all the three orthogonal markets, especially in 5G mmWave, AIoT & Edge computing

- FD-SOI Innovative substrate roadmap is in phase with advanced CMOS evolutionary scaling

- eSoC.2 HR & eSoC.3 FD-SOI platforms open huge opportunities for digital, analog & RF performances

- Extending FD-SOI roadmap can scale beyond 10nm through sSOI & 3D Integration opportunities

- Time is of the essence: Engineered substrates are at the beginning of the value chain and require collaboration, investment and strong motivation to happen

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WORKSHOP - Sustainable Electronics & International Cooperation On Semiconductors

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