The EU Test and Experimentation Facility for Hardware Edge AI: PREVAIL

a platform for development of new solutions

Carlo Reita

CEA-LETI, Director of Strategic Partnerships and planning

Digital Europe Programme – Testing and Experimentation Facilities

AI at the edge

Testing and Experimentation Facilities for Edge AI Components and Systems

Marco Ceccarelli

Competitive Electronics Industry
DG Cnect

Edge AI for EU competitiveness

- Europe does not have a strong position in **computing hardware**
  - No dominant player: Intel, Samsung, Nvidia, Apple, Qualcomm…
  - GAFAM+BATX Platforms with vertical integration (internal HW devt)
  - No foundries to compete in "More Moore" (miniaturisation)
- EU landscape is rather scattered, many innovative SMEs

- EU has R&D **strengths** in alternative computing models ("More than Moore", Beyond CMOS and beyond Von Neumann)
  - But incumbents may decide any time to accelerate in new computing technologies

    => ***EU must act fast !***
- The only way to maintain competitiveness is to **join forces…**
- Europe needs a **TEF platform for Edge AI** to:
  - **Exploit synergies** across Europe from its centres of excellence
  - Create critical mass for **economy of scale**
  - Provide fast-track prototyping and first silicon in new computing technologies for EU companies, large and small, in different sectors

Testing & Experimentation Facilities for **Edge AI** HW

EU has strengths in:

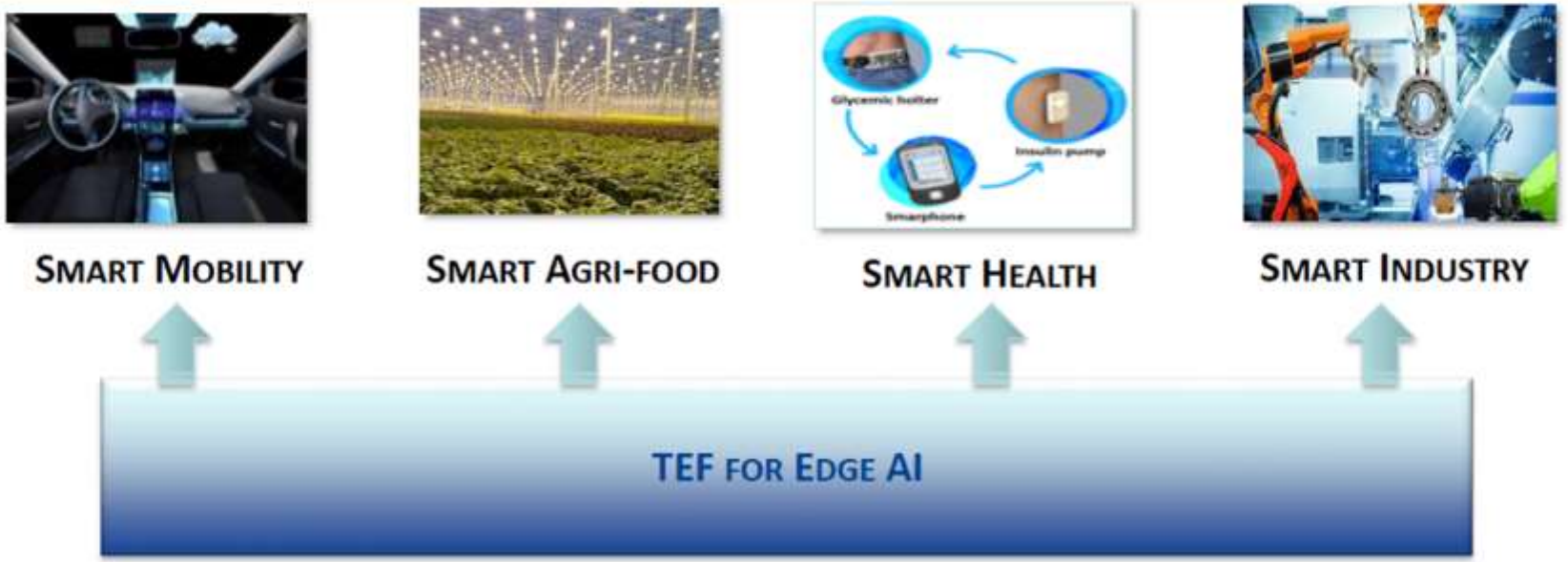
- embedded systems, sensing and low power computing
- R&D in neuromorphic computing, HW neural networks with ultra-low power consumption

TEF Objectives:

- **European platform** enabling companies of any size to test and experiment innovative edge AI components based on advanced **low-power computing technologies**
- support for **prototyping and validation** of novel edge AI technologies for end-user applications

European Commission

Edge AI TEF – Strategic sectors



TECHNOLOGY JUSTIFYING LARGE SCALE TESTING AND EXPERIMENTATION FACILITIES (TEF)

➔ **EDGE AI: Deployment of low-power advanced AI Chips** - Applying the most advanced computing technologies for edge components, from Deep Neural Networks to Neuromorphic computing (100 to 1000 times more energy efficient)

- **Major initiative**: infrastructure facilities to design, test, experiment and validate for industrial use.
- Joint Member States / European Commission effort

Edge AI TEF call

Budget

78M€ from EU (50%, the rest from MS)

TEF project = distributed infrastructure

- Funding: large part for **procurement** of the equipment, the rest for the infrastructure set-up and operation
- Consortium should bring together **top EU competences** and offe nd-users:
  - Technology Services and Demonstrators
  - Prototype and Pilot Production, Technology Transfer
  - Support to SMEs through DIH
- Open and fair access for end-user companies

European Commission

The EU call (Q4-2021)

Testing and Experimentation Facility for Edge AI

- The first phase of the project will focus on the procurement, installation and preparation of the infrastructure, developing the necessary interfaces and testing of existing solutions, and the development of frameworks for hardware/software co-design and prototyping. In the following phases, the project will develop innovative prototypes employing the most advanced architectures and technologies beyond the state-of-the-art, incorporating energy efficiency, operational trust and security, which will be tested and validated in the respective field of application, before transfer for industrialization and production by IDMs or foundries. Personnel costs incurred by beneficiaries to carry out the above activities next to procurement, will be considered eligible.

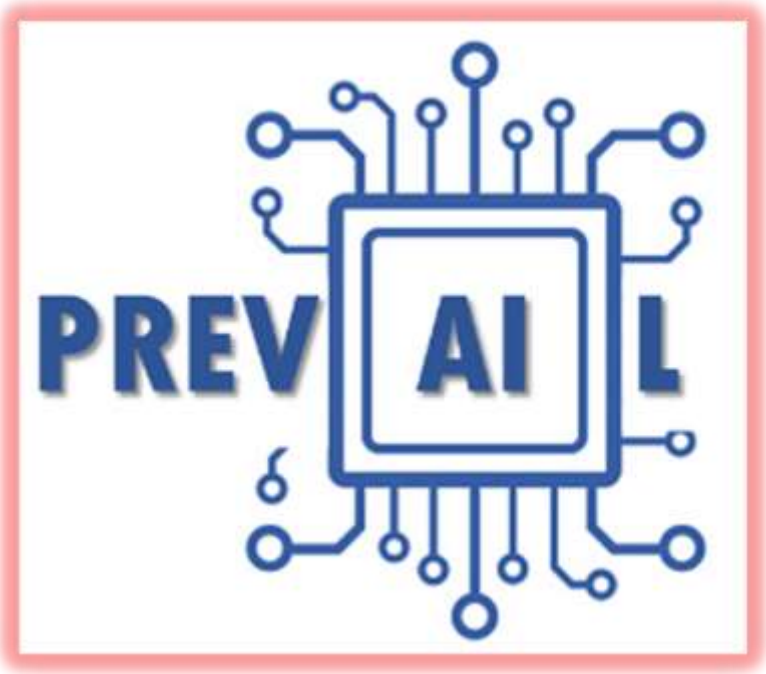
Outcomes and deliverables

- Procurement and preparation of the infrastructure
- Equipment installation, design tool finalisation, definition of device functionalities with users, distribution
- Production of System Exploration Platform software for emulation of hardware
- Progress of key building blocks (such as sensing, in-memory computing, 3D architectures) to higher TRLs and validation of their design kits
- Integration of building blocks into solutions, implementing rules and procedures for testing and transfer to industry

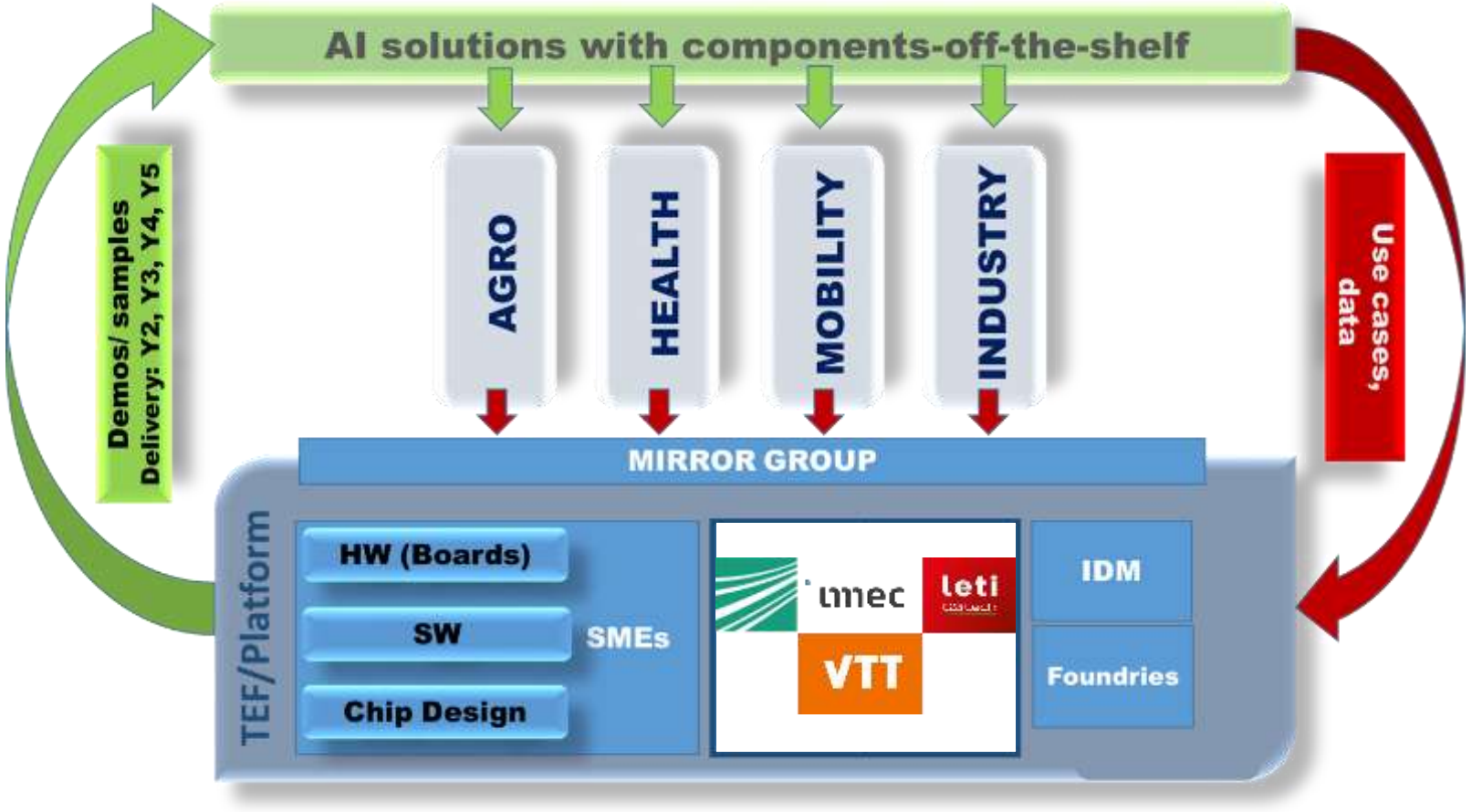
Test and Experimentation Facility for Edge AI Components and Systems (TEF HW AI)

Project PREVAIL

(Partnership for Realization and Validation of AI hardware Leadership)

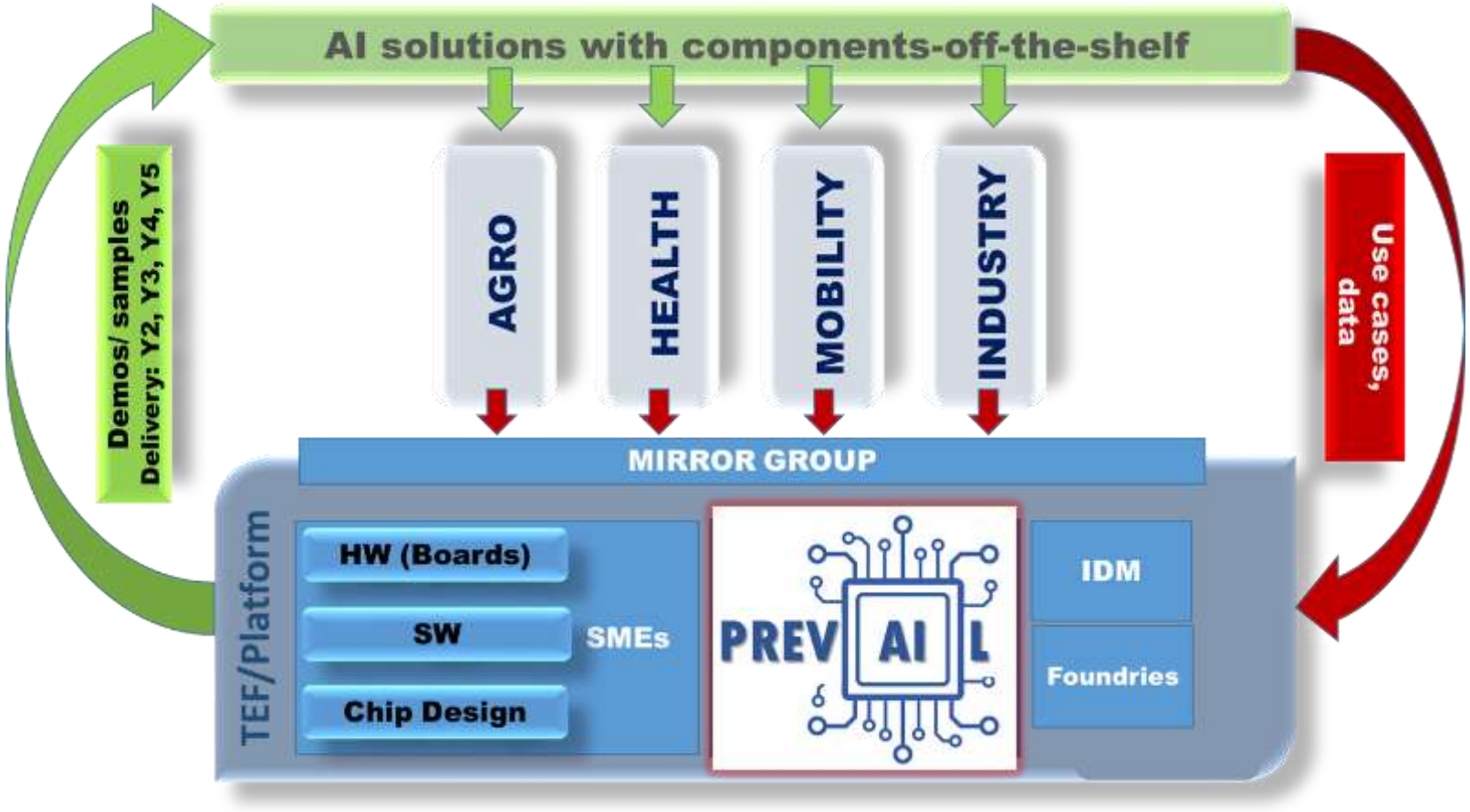


The Vision
open access pilot line for Edge Ai chip prototyping



Establish and start operating the core of **a networked, multi-hub platform providing prototype chip fabrication capability,** in advanced technology, to EU stakeholders for Artificial Intelligence (AI) applications

The Vision
open access pilot line for Edge Ai chip prototyping



The partners in the platform provide a set of 300 mm technologies, open to any user, in order to fabricate prototype Edge AI chips (a few units) required by the user for non commercial purposes.

Proposals are examined by the partners to verify feasibility, cost and delay.

Proposals can come via DIH, KDT projects, directly.

IP necessary for the execution and originating from the user remains his property and partners have access only for execution. The IP originating from the partners remains their property and, if necessary for exploitation, non-exclusive licenses will be provided. IP generated during the execution is property of the inventor.

The user receives the prototypes and test them in its field of application.

ID of the project

Project number:	101083307
Project name:	Partnership for Realization and Validation of AI hardware Leadership
Project acronym:	PREVAIL
Call:	DIGITAL-2021-CLOUD-AI-01
Topic:	DIGITAL-2021-CLOUD-AI-01-TEF-EDGE
Type of action:	DIGITAL-GP
Service:	CNECT/A/03
Project starting date:	fixed date: 1 December 2022
Project duration:	42 months

- Budget: 156 M€ (50% funded by EC, 50% by State Members)
- ~86% (~134M€) of the budget dedicated to CAPEX
- ~6% (8.6 M€ & 342 pm) of the budget dedicated to Demonstrators Fabrication

Main Tasks of Prevail : create and open access European TEF HW AI infrastructure

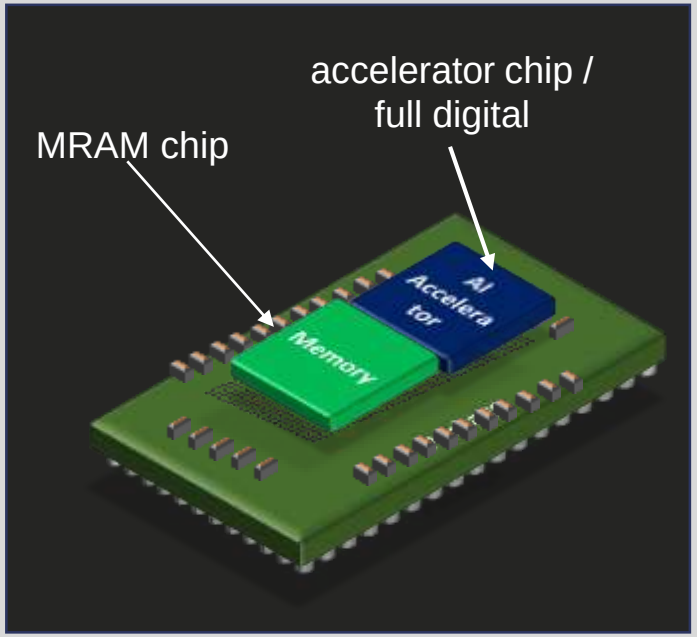
- Tools procurement
- Tools installation, preparation and validation
- Benchmark the improvement of the technologies of choice to insure a TRL suitable to address the specifications required by edge AI chips
- Fabrication of a set of pipe-cleaner demonstration vehicles, focusing on the above-mentioned technologies, to make sure of efficiency of the platform
- **Open the “PREVAIL” Pilot Line to external users**

Expected outcomes

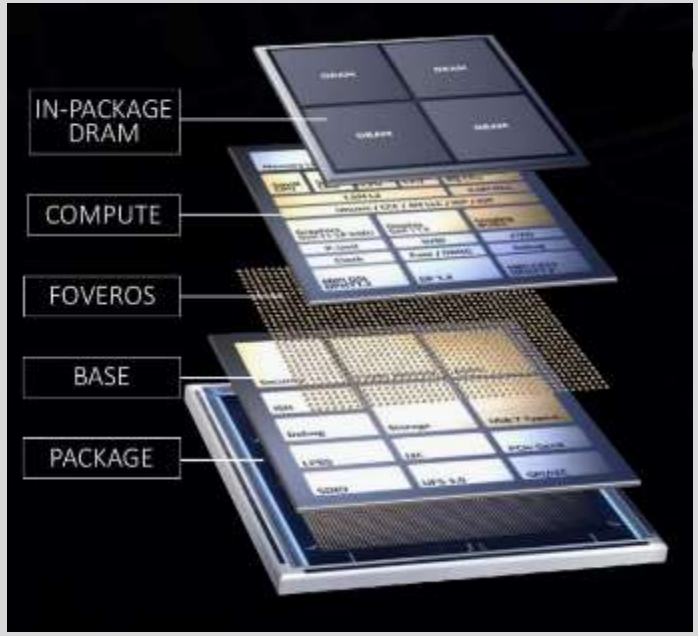
- Setup a distributed Open-Access Pilot Line for the fast prototyping of innovative chips for Edge AI applications
- Infrastructures – New dedicated equipment, mature design tools, effective fabrication and test modules
- Maturation in Key Building Block allowing new device architectures (SENSING, IN-MEMORY COMPUTING, 3D ARCHITECTURES, …)
- Single entry point for Users with a pre-defined framework for Legal, Commercial and IP
  - Building a strong cooperation environment among the consortium partners
  - Demonstrate that the collaboration between the RTOs can bring added value
- **Make PREVAIL (and PREVAIL Partners !) key players of the future Chips Act Initiative**

Prevail:Our Offer

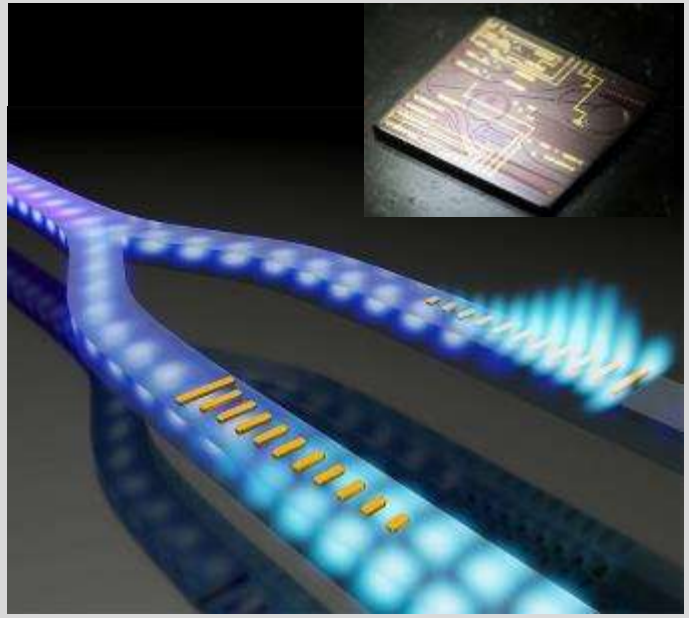
Non Volatile Memories



3D Architectures



Photonics & RF

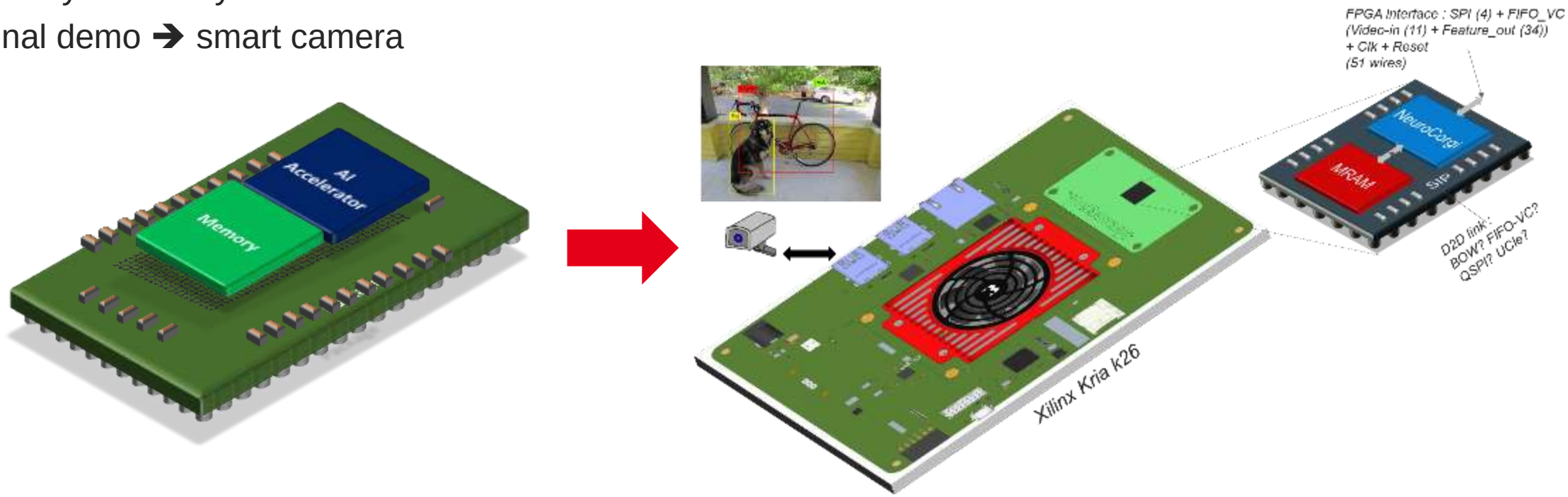


Technology contributors

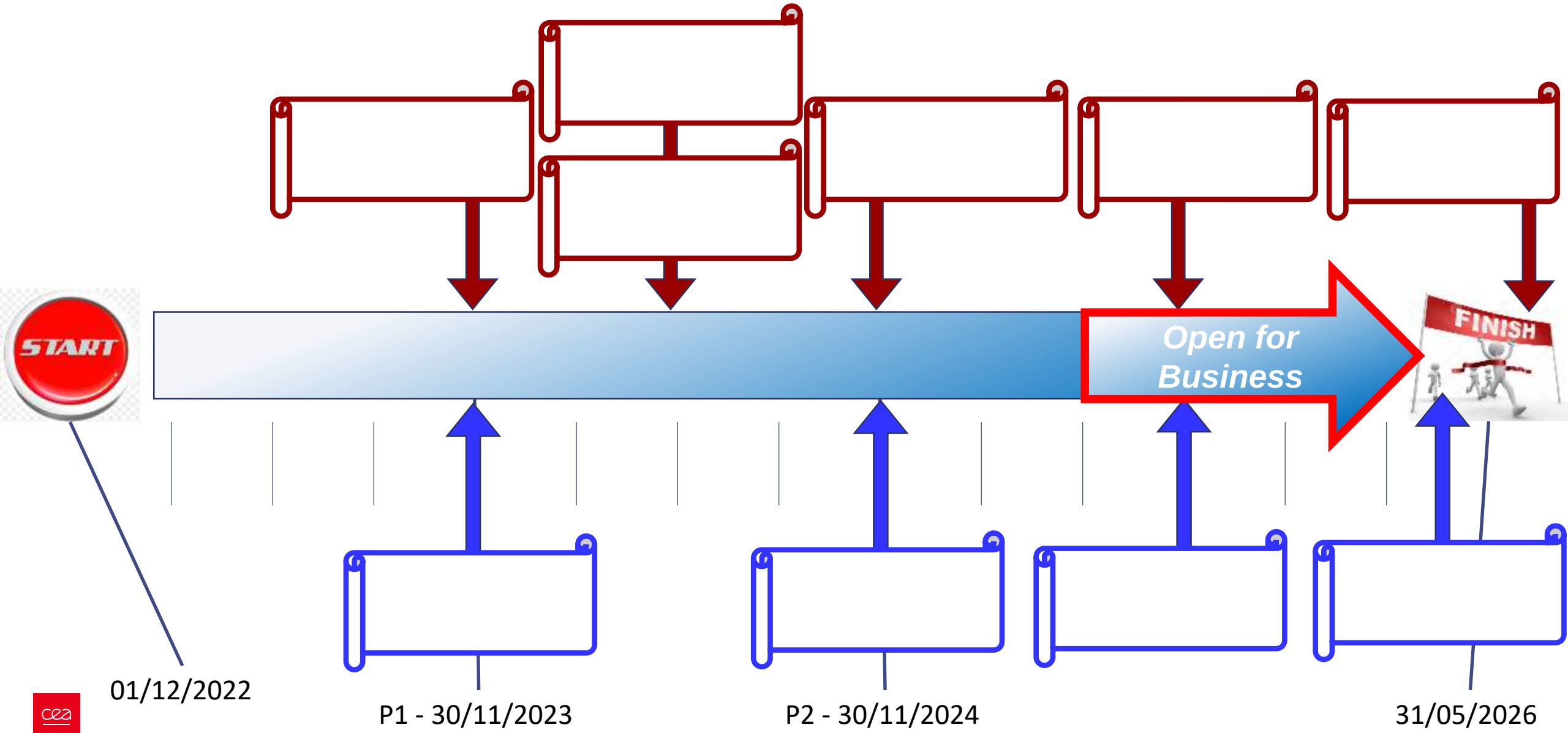
	non-volatile embedded memories			3D heterogeneous integration and assembling			photonics and connectivity	
	MRAM	OxRAM	FeRAM	die to die	die to wafer	wafer to wafer	integrated photonics	RF
CEA		✓			✓	✓	✓	
imec	✓				✓	✓	✓	
FhG			✓ (IPMS, IIS)		✓ (EMFT)	✓ (IZM-ASSID)		
VTT				✓	✓			✓

Possible Demonstrator 1

- **NVM demonstrator**
  - One memory chip (MRAM) coming from IMEC
  - One AI chip coming from LETI (full digital compute chiplet)
  - Assembly on package (BGA) for functionnal tests
  - Sub-system assy on FPGA
  - Final demo ➔ smart camera

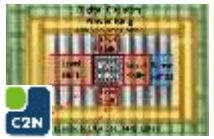


Timeline - demonstration



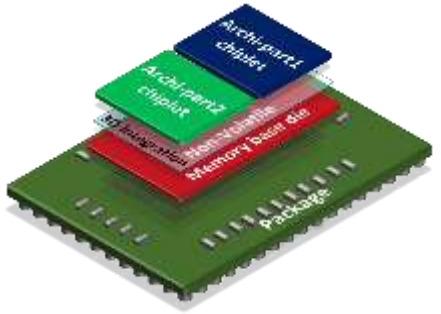
AI Research axis @CEA

Smart sensors



Bayesian machine

Esperanto



MOSAIC: Modular AI systems composed of heterogeneous components

Classification

BNN
digital popcount

SPIRIT

X10000 more neurons
X10 lower power

Spiking SNN

LARGO

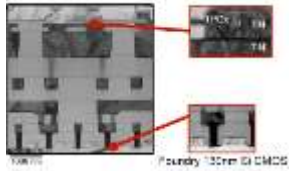
CNN
X100 lower power

Feature extractor of HD images

NeuroCORGI

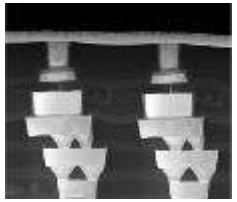
Technologies

22 FDSOI



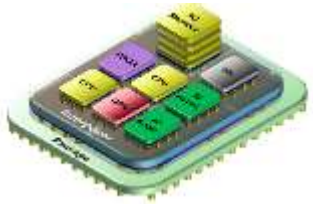
130nm CMOS / RRAM

sensors



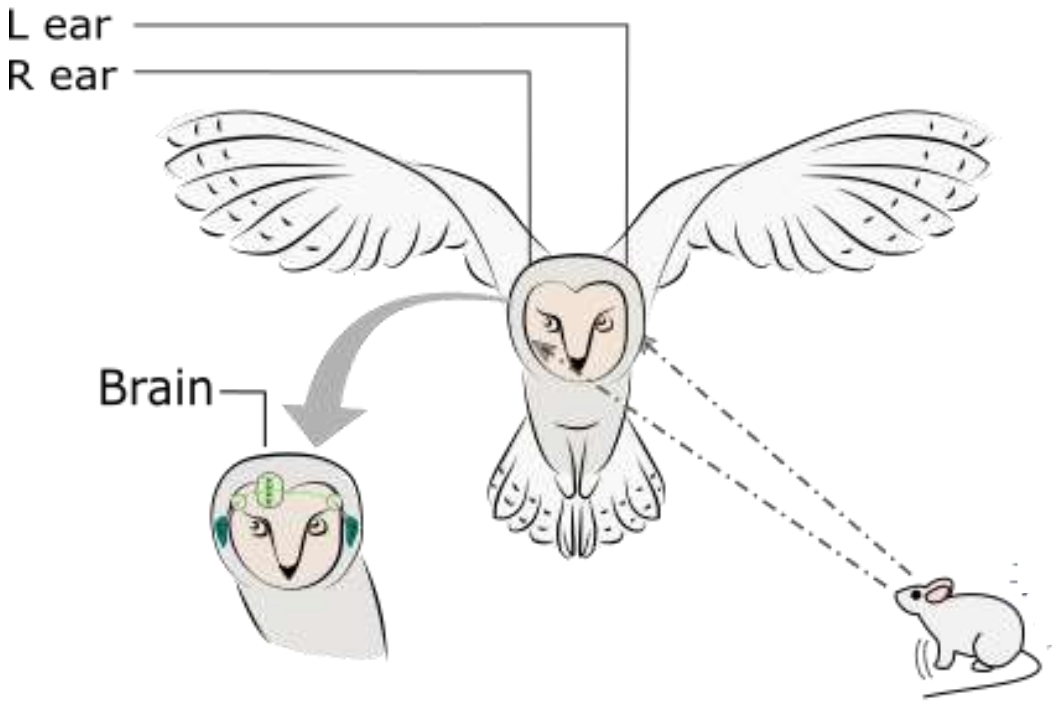
28nm FDSOI / RRAM

22nm FDSOI
&
22nm FDSOI / RRAM



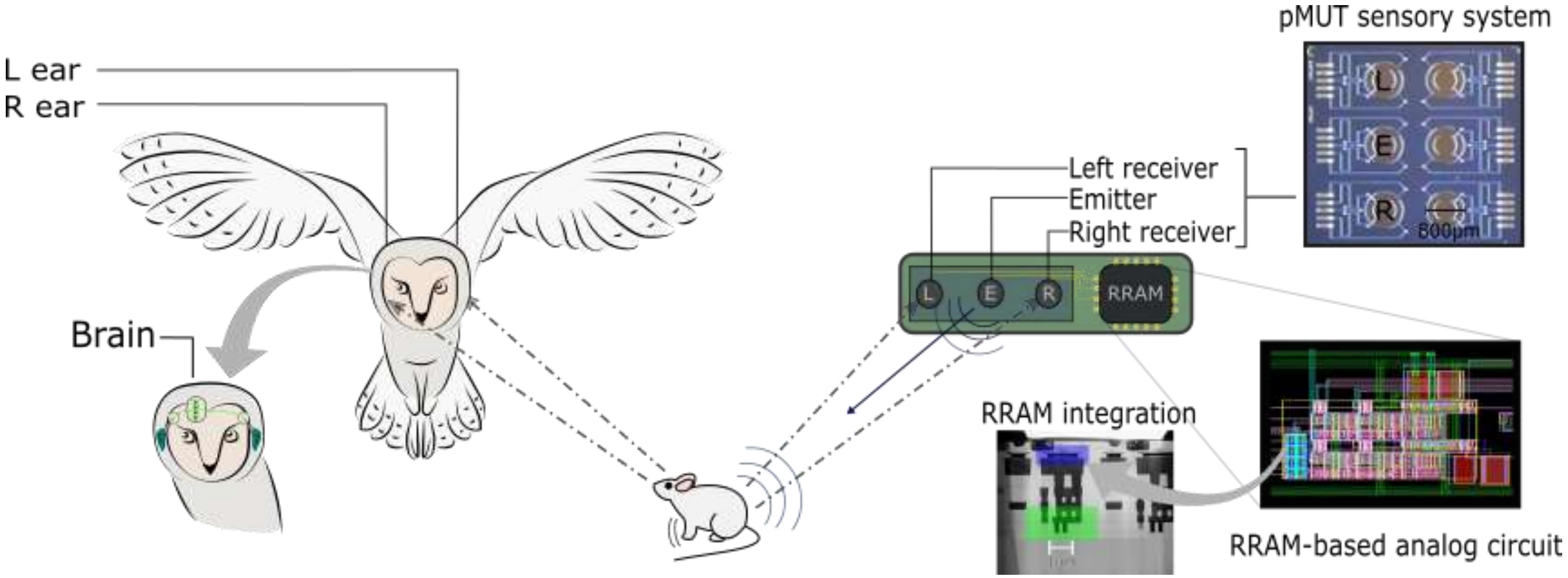
Multi-die (chiplet)

Barn owl-inspired object localization detector



- **Event-driven, local processing** – spikes only when pMUTs sense, and RRAM-based IMC
- **All-analog** – no ADCs, RRAM conductance adjusted to compensate CMOS variability

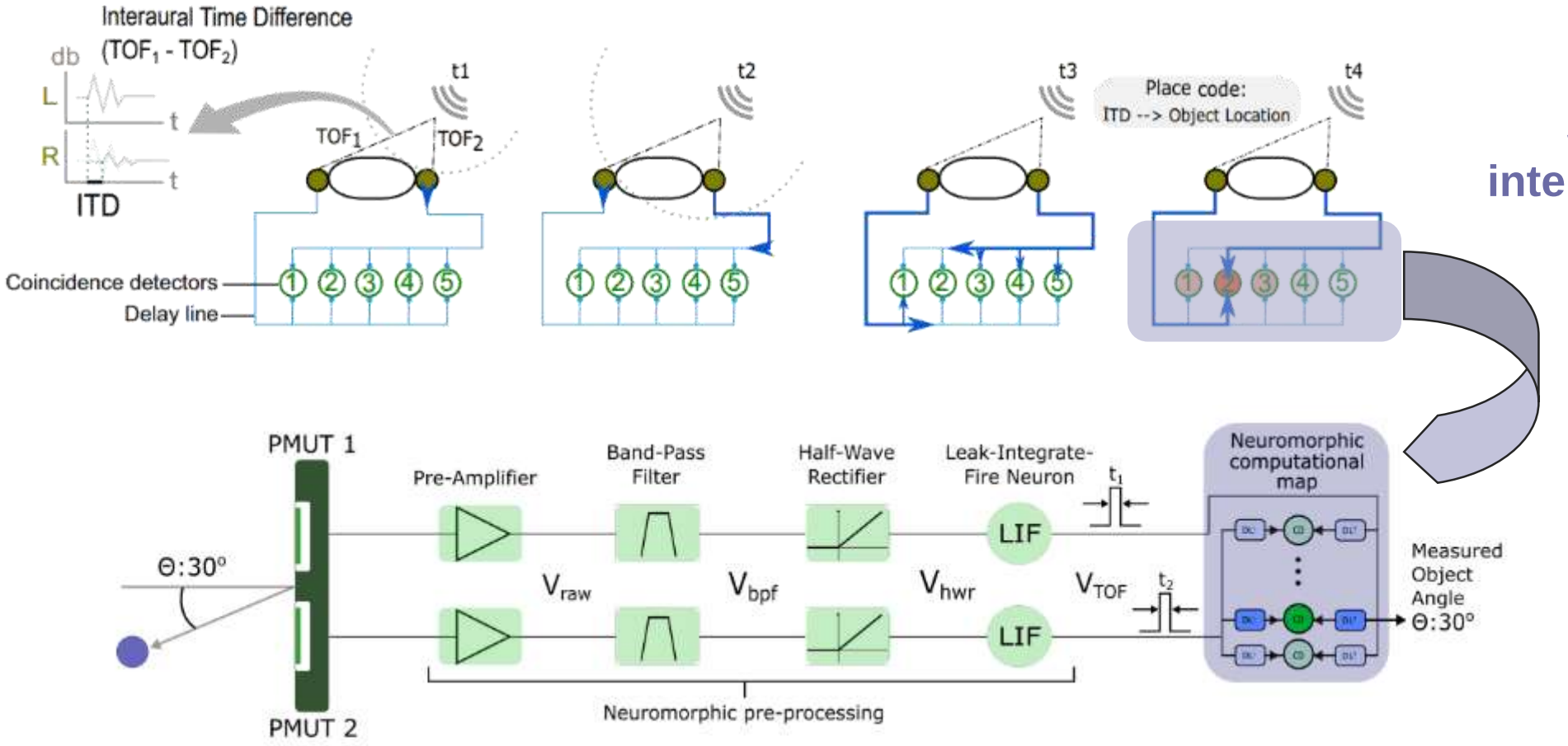
Barn owl-inspired object localization detector



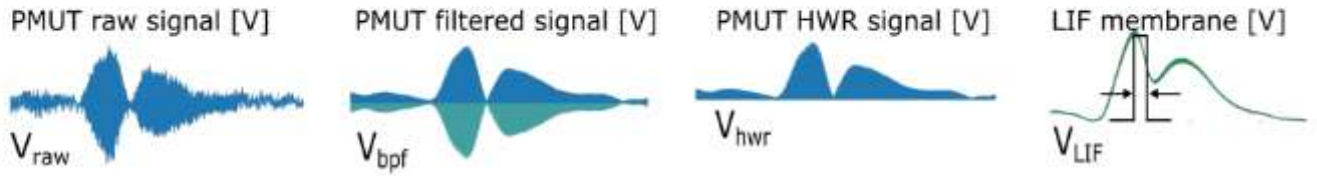
nature COMMUNICATIONS

[F. Moro et al., Nat Comm, 2022]

Coincidence detection and pre-processing

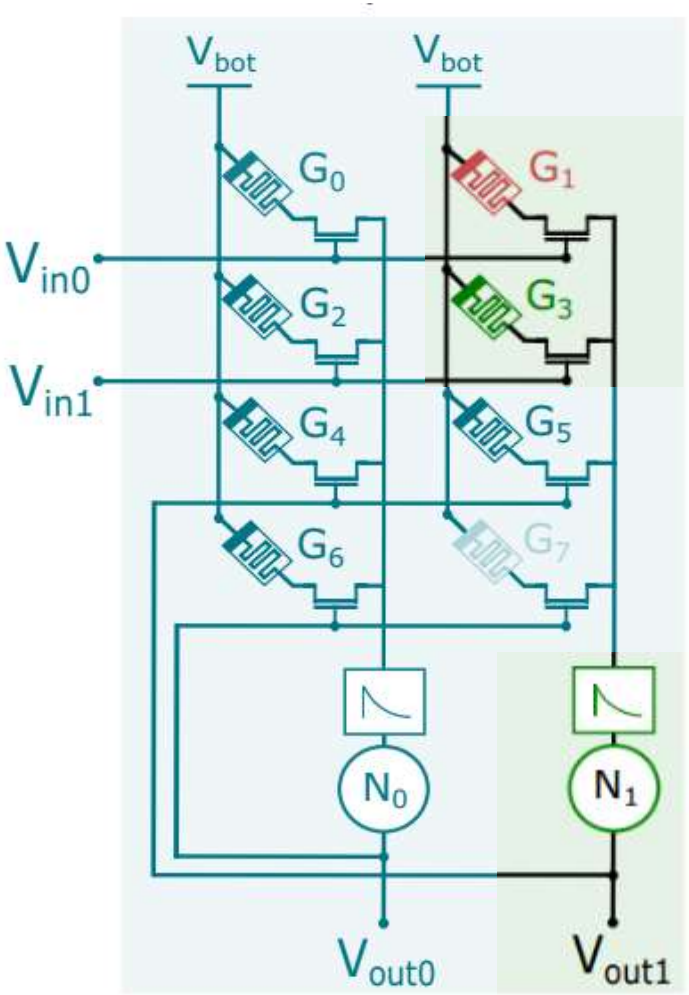


Jeffress model for inter-aural time difference



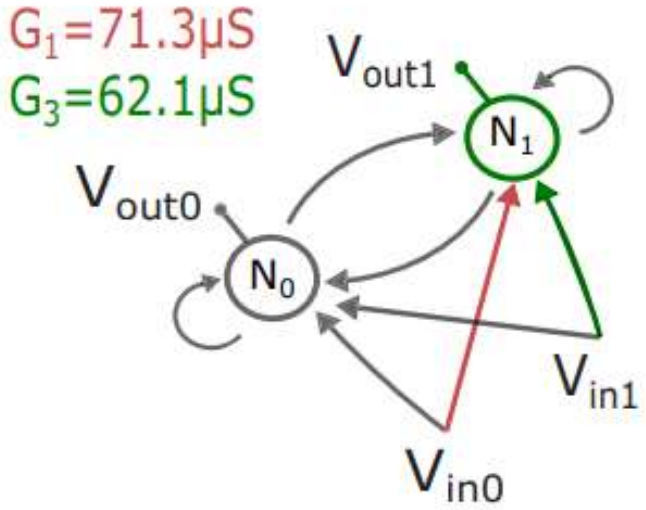
Neuromorphic pre-processing

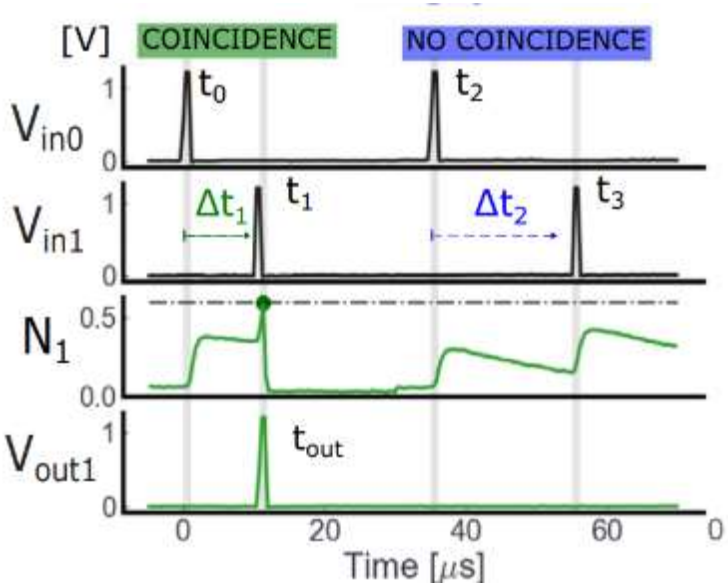
RRAM-based coincidence detectors



RRAMs route and weigh incoming pulses
(+ can be tweaked to compensate analog CMOS variability)

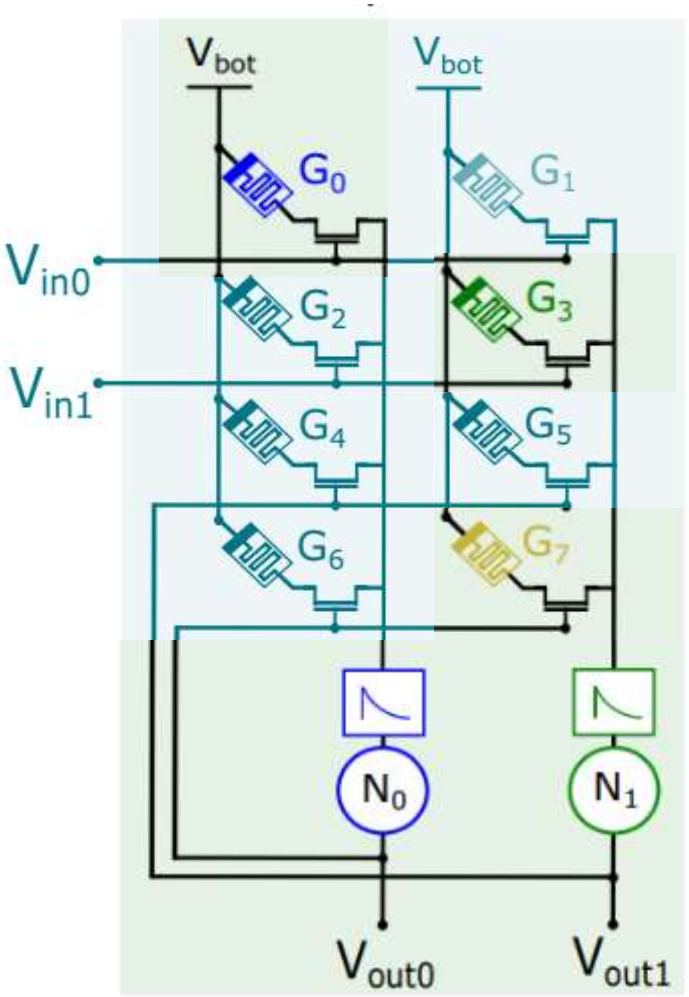
Detector fires if spikes from paths 0 and 1 reach N1 within less than Δt





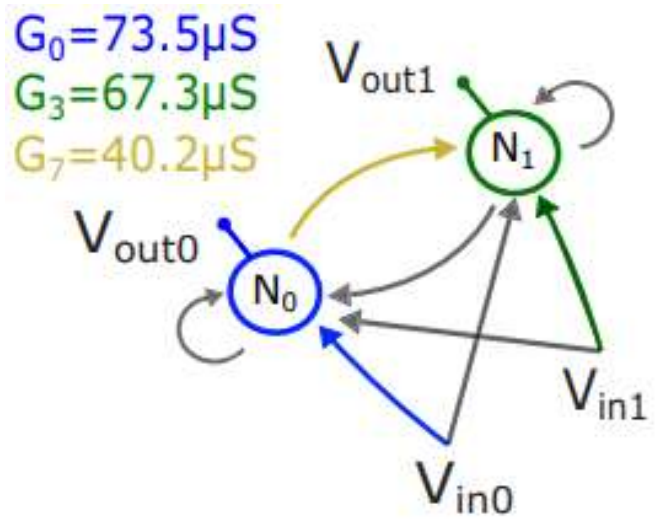
Direction-insensitive

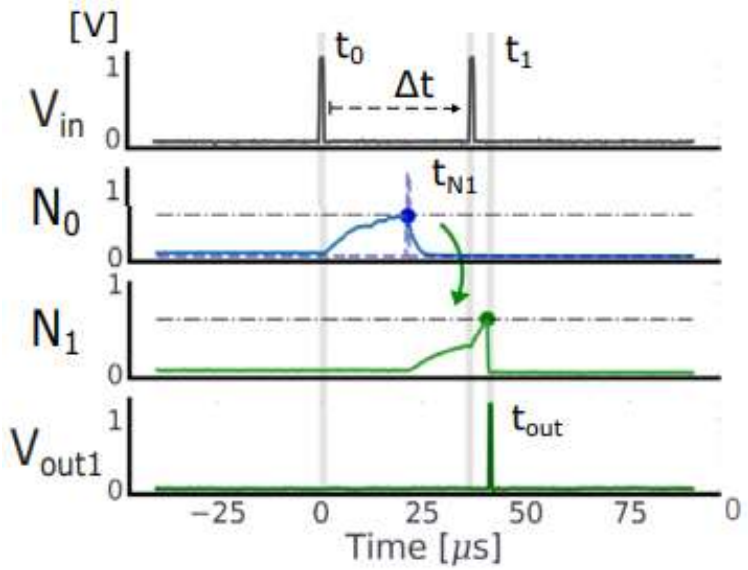
RRAM-based coincidence detectors



RRAMs route and weigh incoming pulses
(+ can be tweaked to compensate analog CMOS variability)

Detector fires if spikes from paths 0 and 1 reach N1 within less than Δt and path 0 was the first





Direction-sensitive

Power, performance, perspectives

- ***Power consumption:***

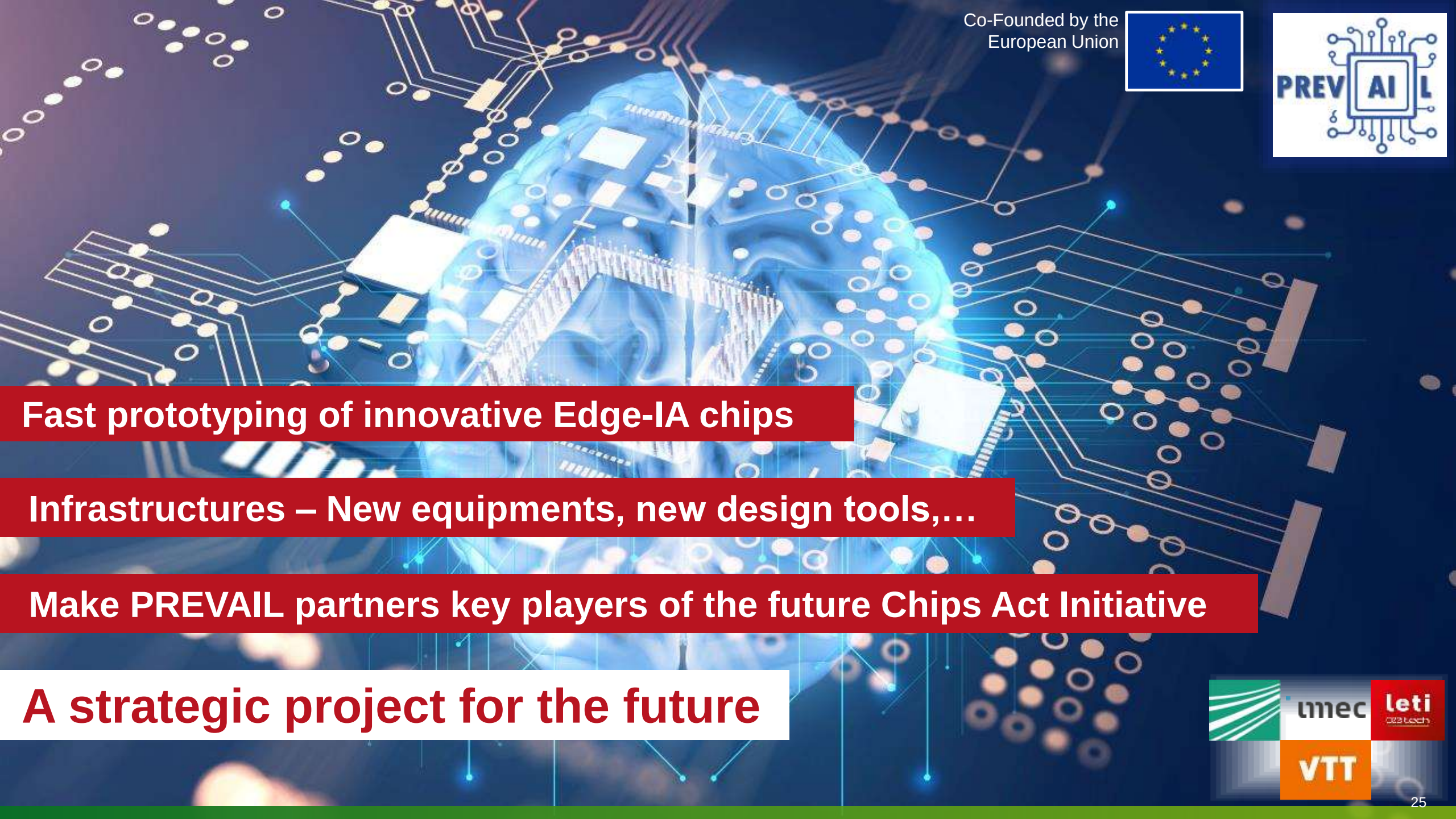
83.3 nW vs. 244.7 µW for MCU; **~3000 x smaller**

- ***Angular resolution:***

computational map 4° (delays of neurons and synapses),
pMUT sensing 10° (at 50cm, using this setup)

- ***To go further:***

sensor fusion to relax precision requirements
(ex: coarse ultrasound sensing + visual sensing)


Co-Founded by the
European Union
PREVAIL
Fast prototyping of innovative Edge-IA chips
Infrastructures – New equipments, new design tools,…
Make PREVAIL partners key players of the future Chips Act Initiative
A strategic project for the future
imec
leti
VTT