Gate All Around Nanowire FETs: Operation From RT To Cryogenic Temperatures

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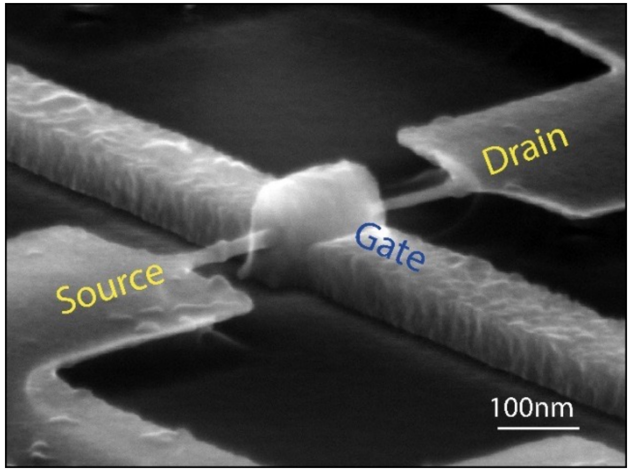
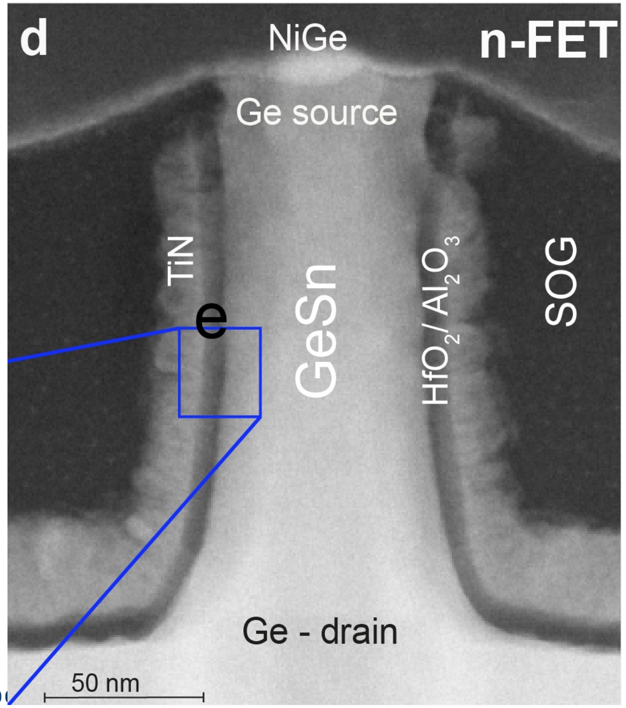
OUTLINE

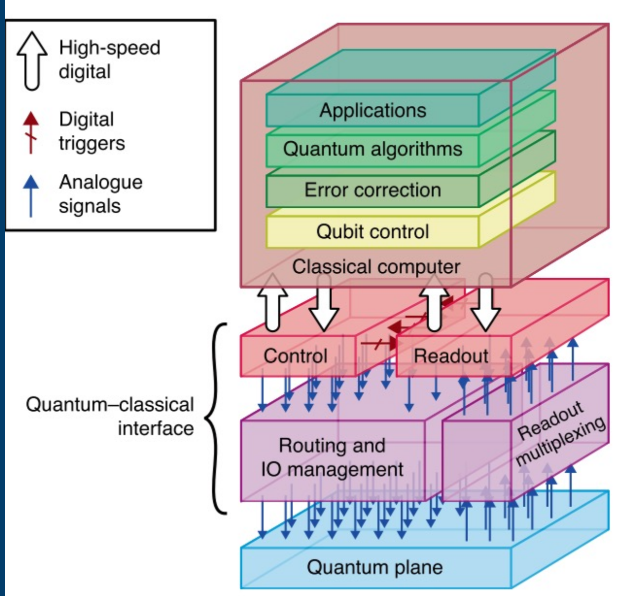




Horizontal Si NW GAA FETs

Vertical Ge/GeSn NW GAA FETs

Electronics working at low T

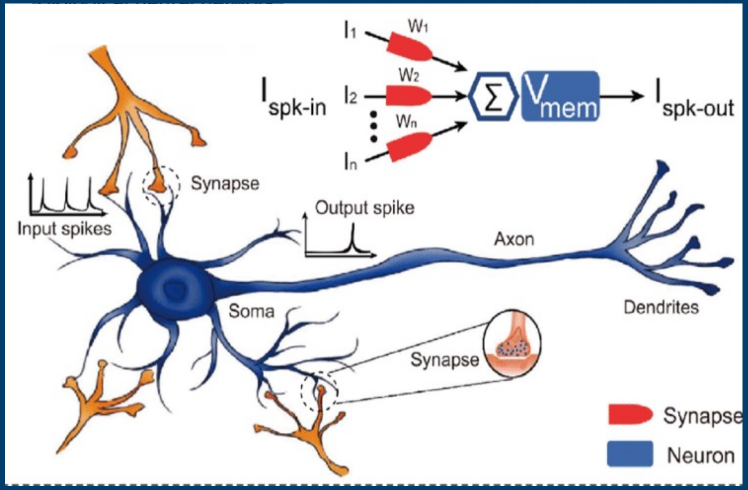


Quantum computing
Classical controller: 1-4K

Spacecraft
300-20K

Cryogenic Electronics

High performance computing:
300~77K



Cryogenic neuromorphic computing: 300-77K?

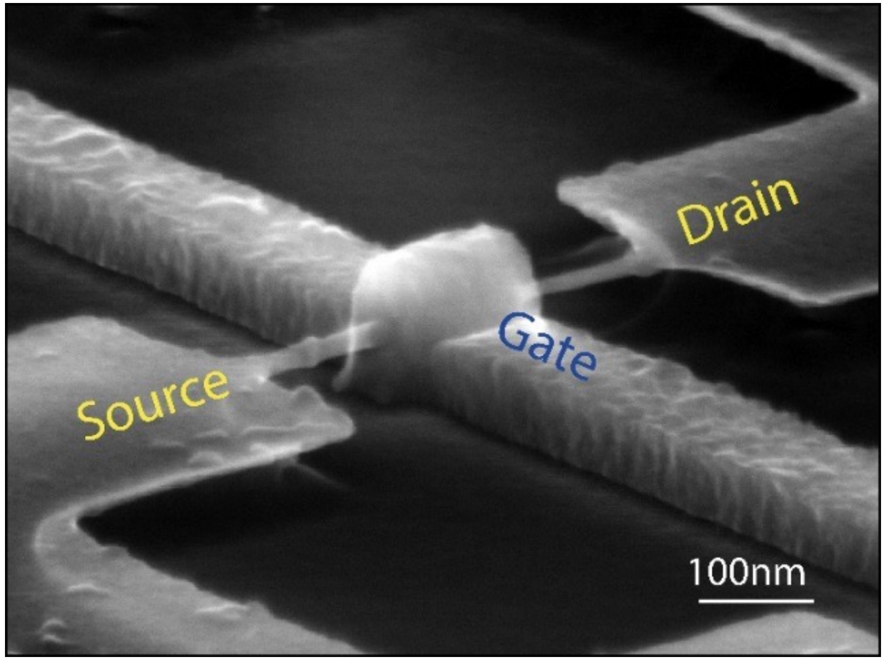
Ultra-Low Power

Introduction-why GAA NW?

Power consumption

$$P_{tot} = AC_{tot}{V_{DD}}^2 f + V_{DD}I_{off}$$

$$P_{stat} = V_{DD}I_{off} = V_{DD}I_{Vth}10^{\frac{-V_{th}}{SS}}$$



$$\mathrm{SS} = \frac{kT}{q}\ln(10)\,(1 + \frac{C_d + C_{it}}{C_{ox}})$$

$$C_d \approx \varepsilon_0\varepsilon_{NW}\frac{\pi D^2}{4\mathrm{L}}$$

$$C_{it} \approx e^2\, D_{it}\pi DL$$

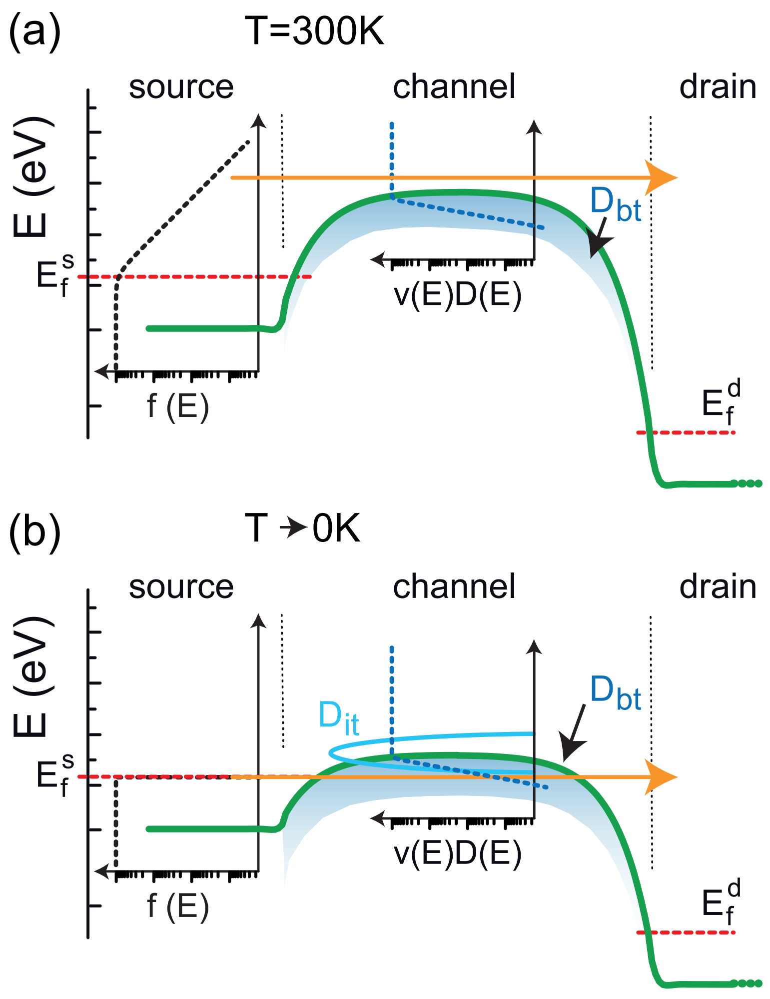
NW diameter D decreases, SS is smaller!

Introduction: temperature dependence

$$D(E)_{\mathrm{bt}} \propto \exp\left(-\frac{\Phi_c - E}{\Delta E}\right)$$

$$I_{\mathrm{d}} = \frac{2e}{h}\int dE D(E) v(E) f_s(E_f^s) \approx \frac{2e}{h}\int_{-\infty}^{E_f^s} dE v_f^s D_{\mathrm{bt}}$$

$$\propto v_f^s \Delta E \exp\left(-\frac{\Phi_c - E_f^s}{\Delta E}\right). \qquad (4)$$



J. Knoch, … Q.T. Zhao, PSS(a), 2023

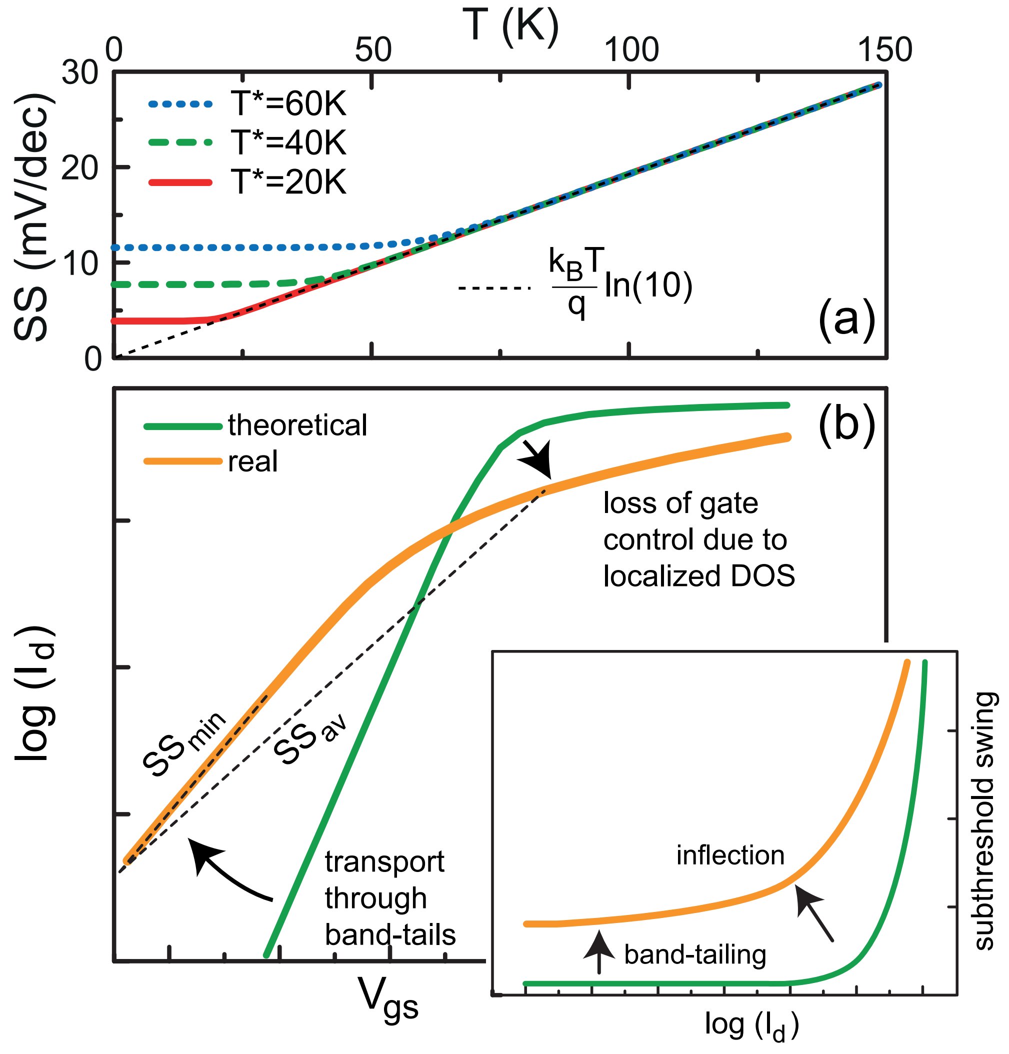
Introduction: Band Tailing

$$SS_{\mathrm{real}} = \frac{k_B T^\star}{e} \ln(10) \left(1 + \frac{C_{\mathrm{it}}}{C_{\mathrm{ox}}} + \frac{C_{\mathrm{depl}}}{C_{\mathrm{ox}}}\right)$$

$$\left[1 + \alpha \ln\left(1 + \exp\left(\frac{T - T^\star}{\alpha T^\star}\right)\right)\right],$$

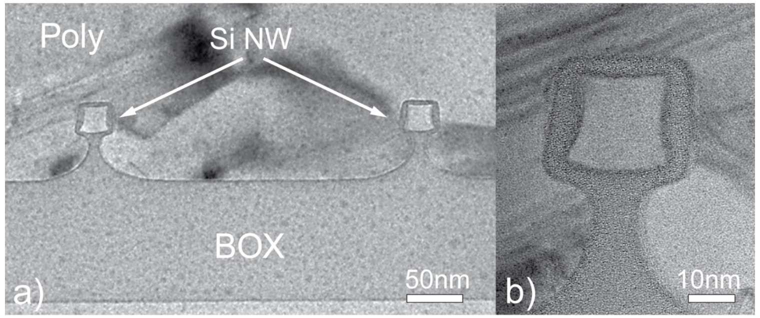
G. Ghibaudo et al., SSE 170, 2020

Locallized states cause the depdendence of SS on Vg, the inflection phenomenon (states at the band edge).

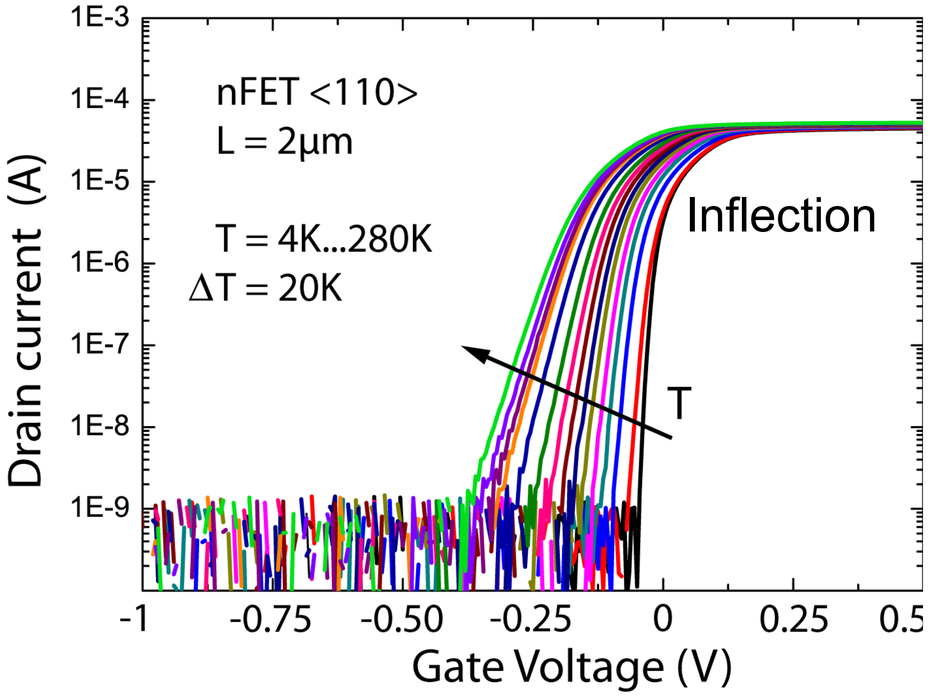


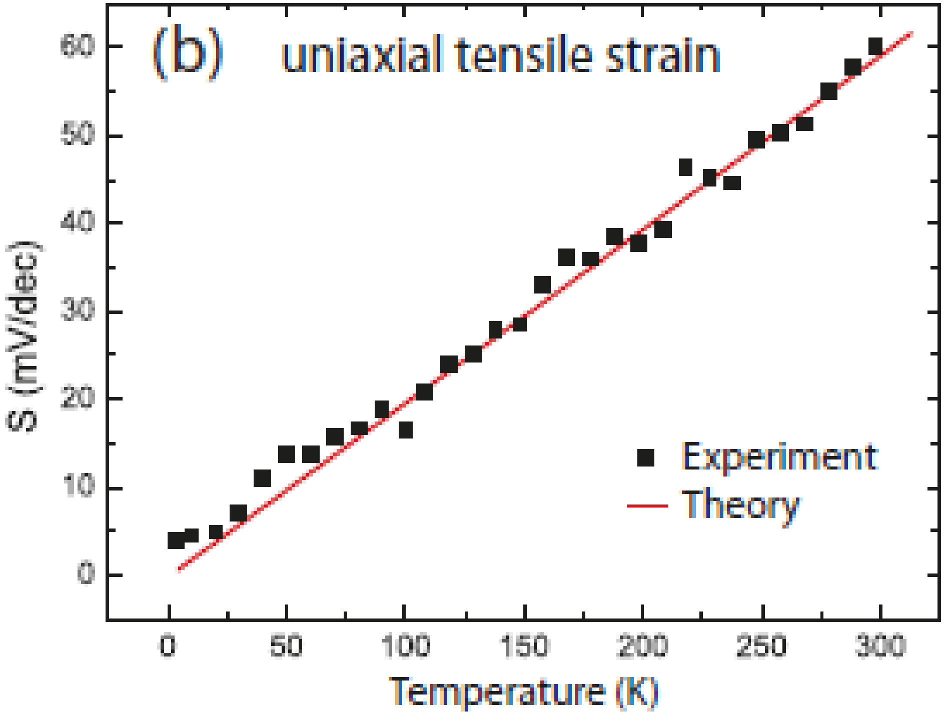
J. Knoch, … Q.T. Zhao, PSS(a), 2023

Si NW Ω-GATE FET



- Strained Si Nanowire
- Gate oxide: SiO2
- Source/drain: by ion implantation



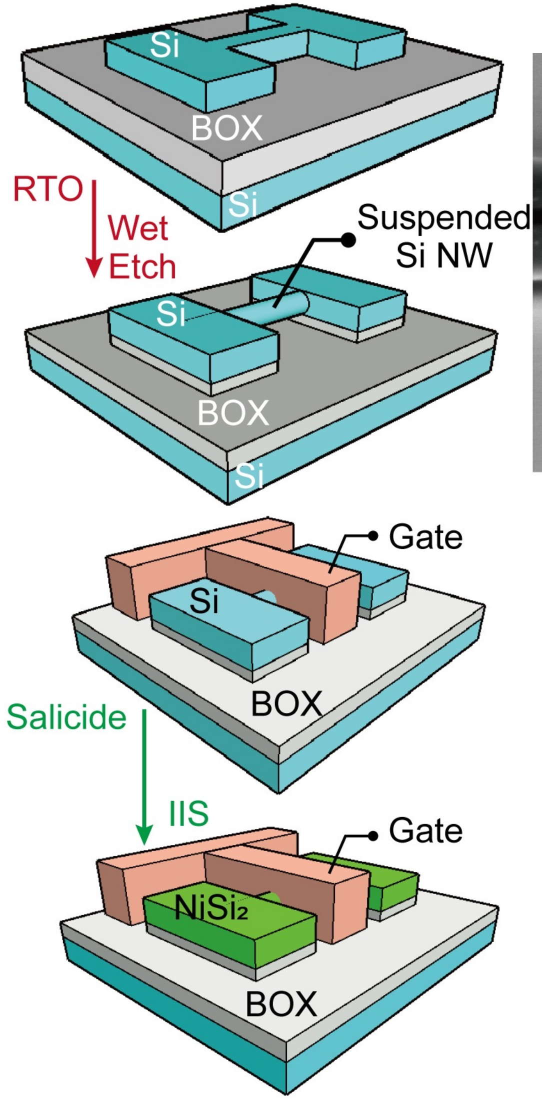


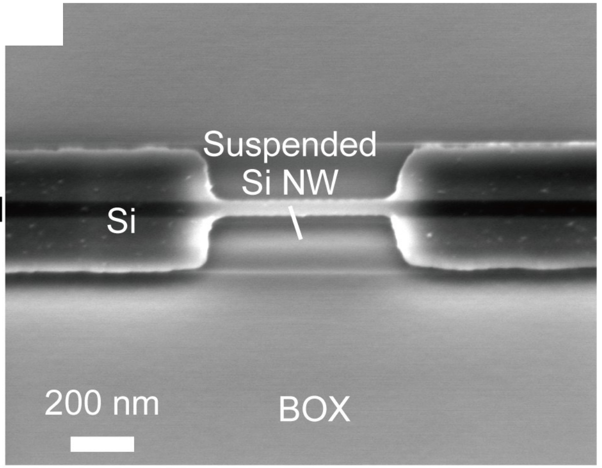
S. Habicht et al., Thin Solid Films, 2012

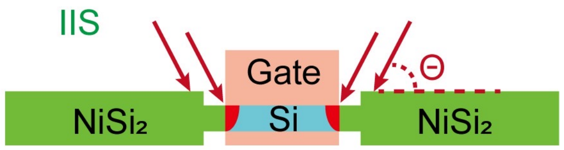
- SS= 60 mV/dec
- SS= 4mV/dec @4.2K
- SS saturation at T<20 K
- Still high inflection,

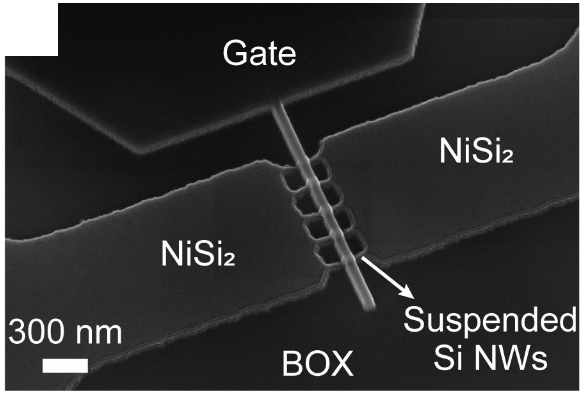
Nanowire GAA FETs

Process and devices



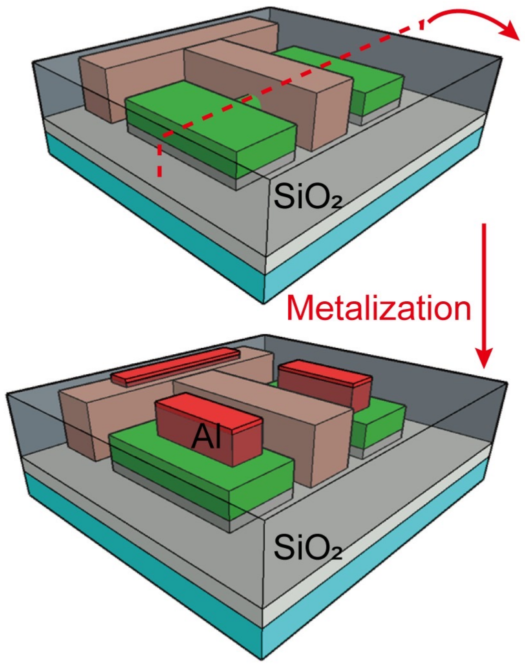


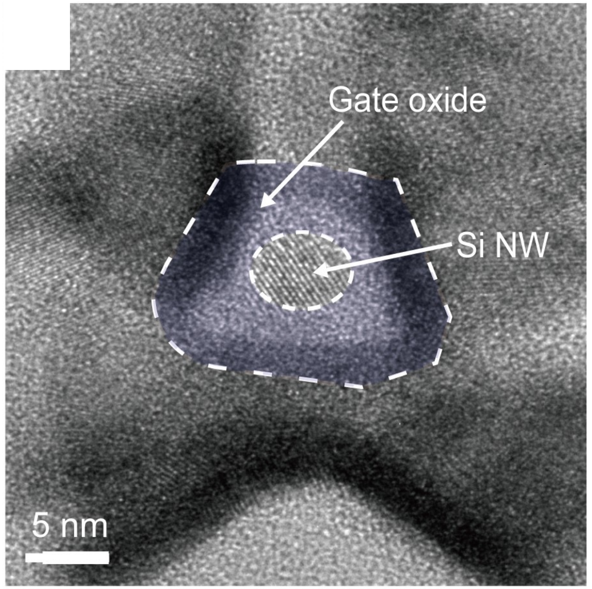




Fully silicided source/drain Si NW FETs by implantation into silicide (IIS)

The diameter is 5 nm.





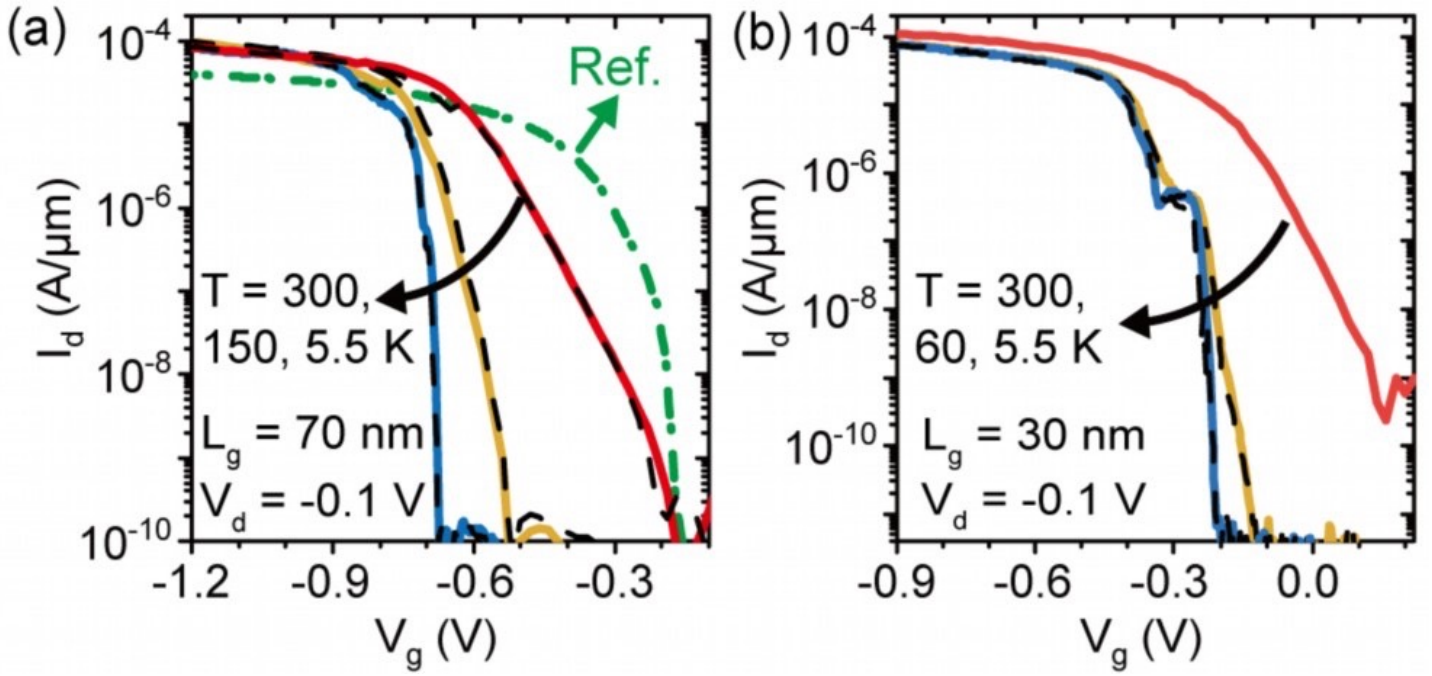
Y. Han *et al.*, *IEEE Electron Device Lett.*, 2022.

Cryogenic Characteristics

GAA Si NW FETs

❖ Suppressed band tail effects

- Narrow transition region and steep SS at 5.5 K



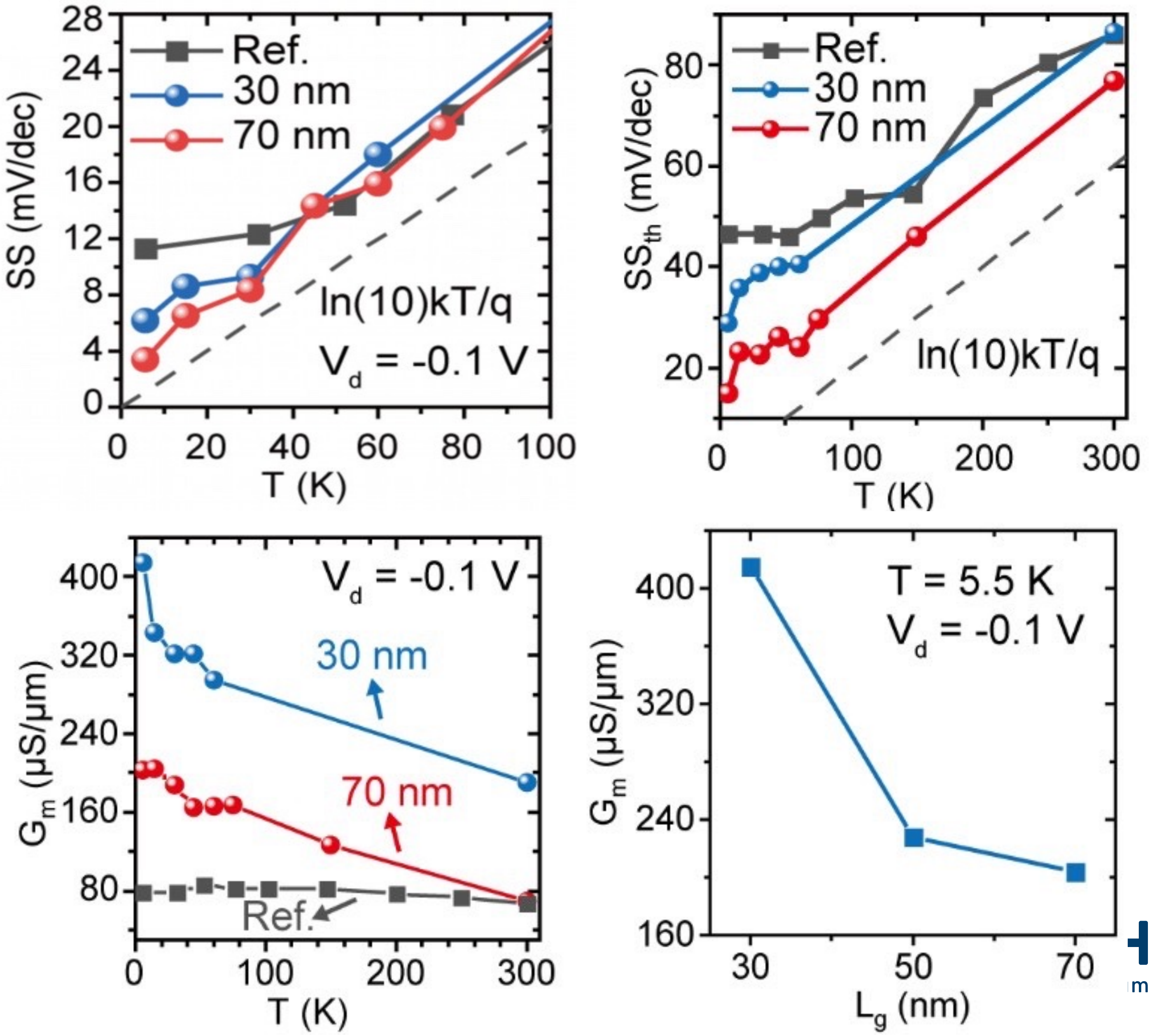
SS of 2.3 mV/dec
Average SS_{th} of 10.1 mV/dec

Cryogenic Characteristics: SS

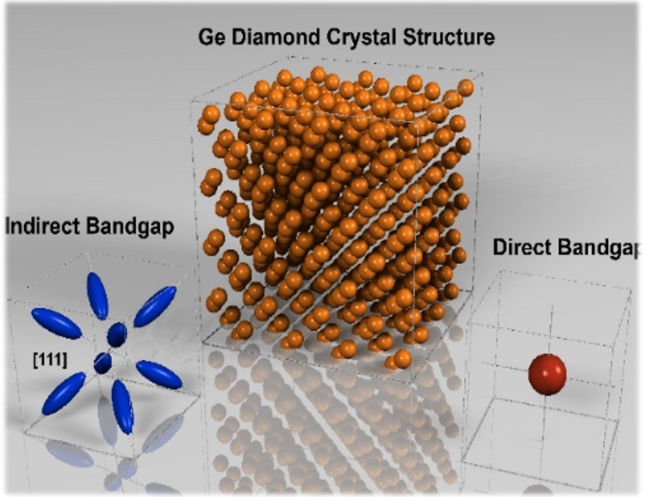
GAA Si NW FETs

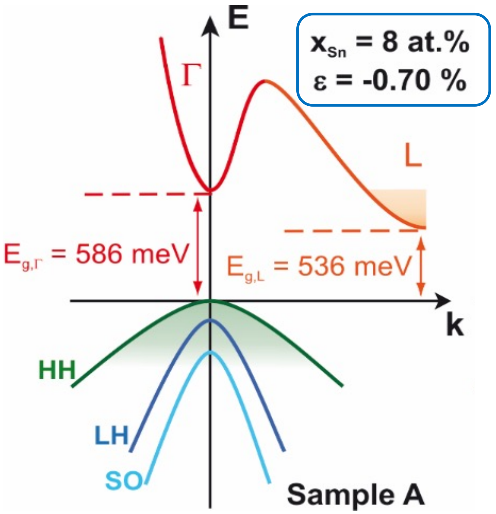
- No SS and SS_{th} saturation at Cryo-T
- Increased G_m as T decreases

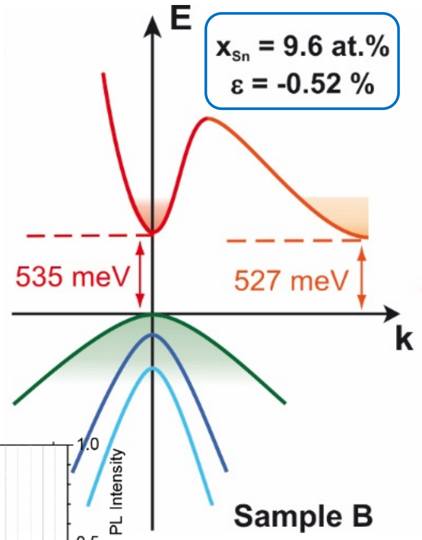
Y. Han et al., to be published



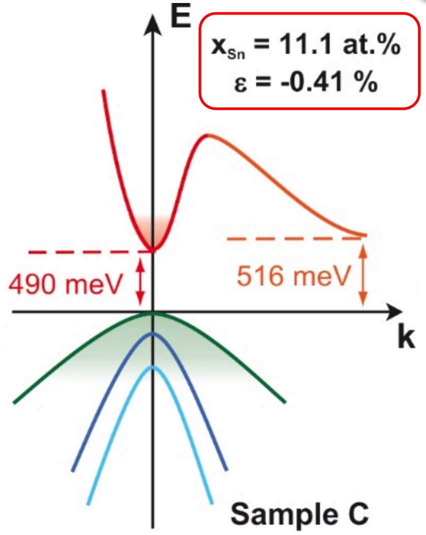
GeSn: from indirect to direct



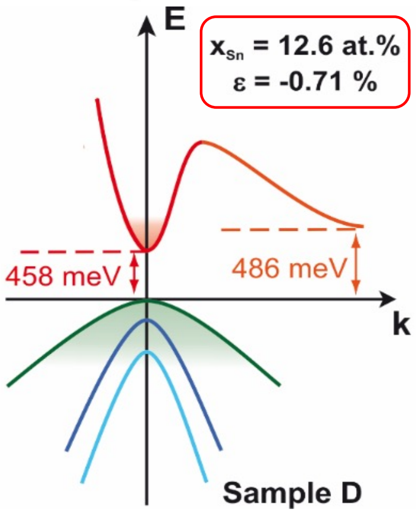


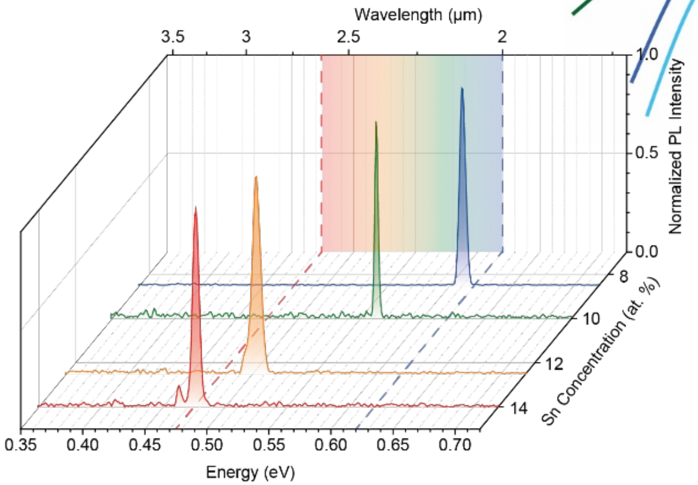


Indirect Bandgap



Direct Bandgap





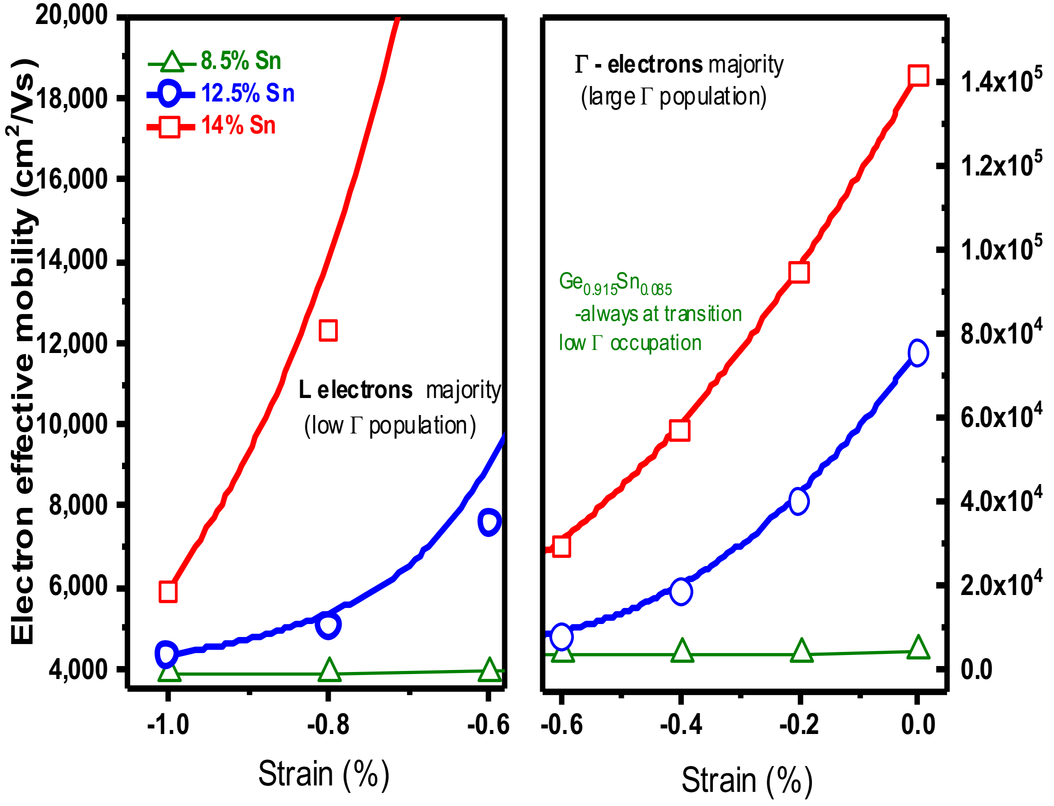
GeSn lasing

S. Wirth et al, Nature Photonics 2015

Calculations based on Bahder: *Phys. Rev. B* **41**, 11992-12001 (1990)

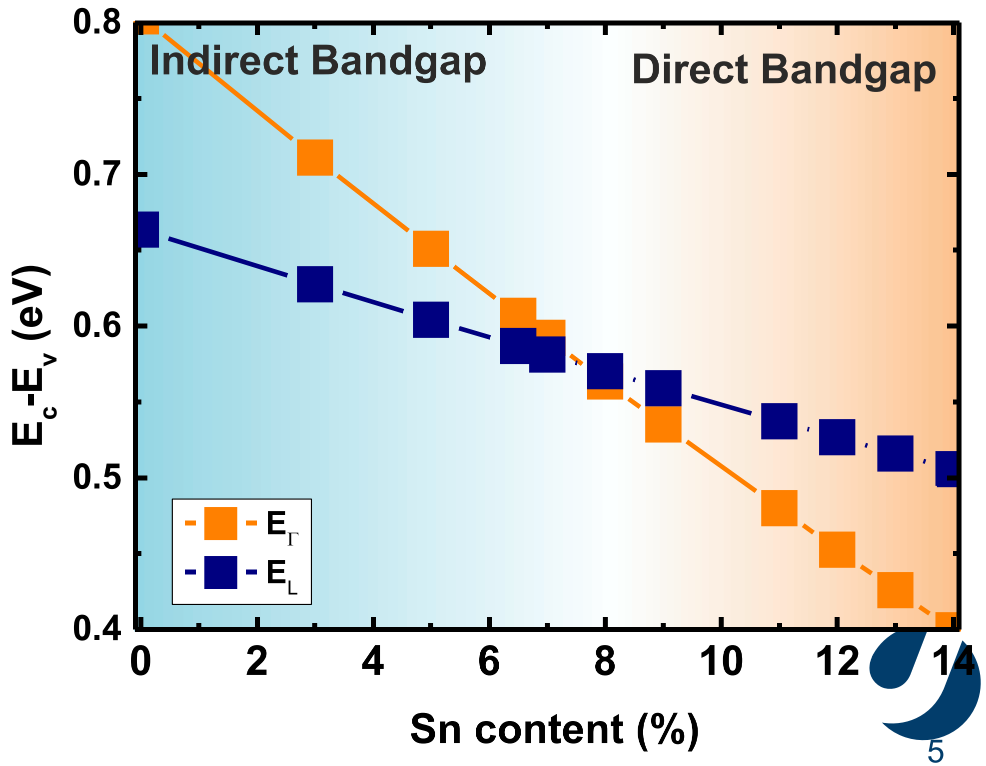
S. Wirth, PhD thesis @ FZJ

Group IV- GeSn: high mobility

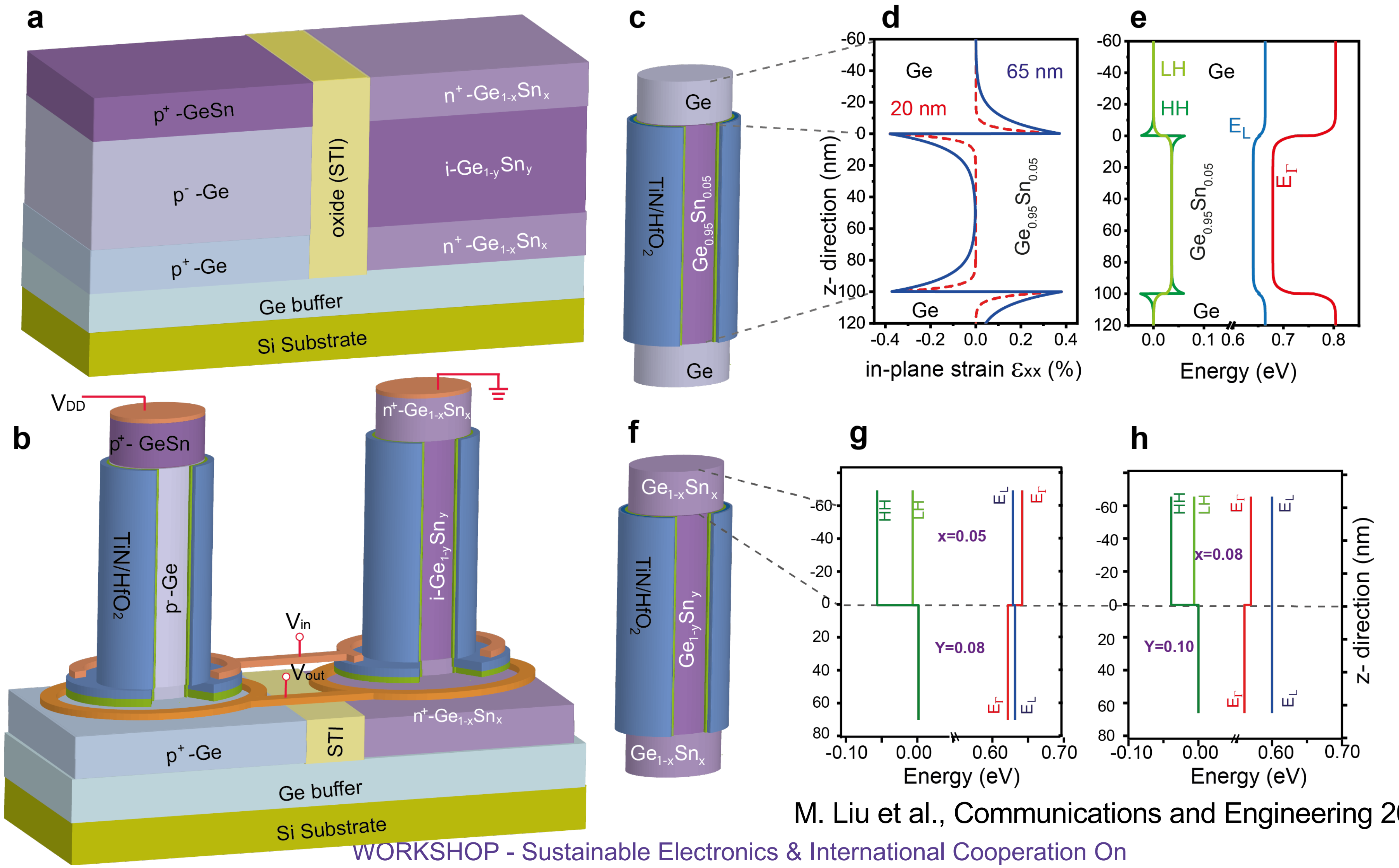


Calculated elecron mobility in GeSn
(Zoran Ikonic @Univ. Leeds)

- „Bandgap-Engineering“ → Heterostructurs
- Compatible with CMOS process technology
- Integration into existing processes



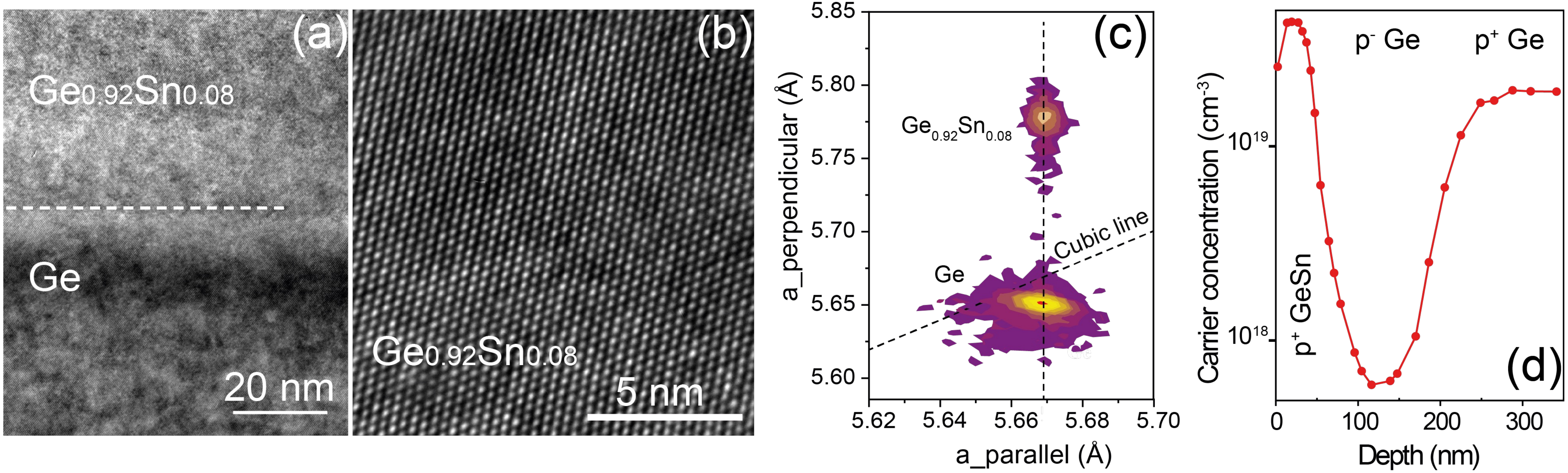
Vertical GeSn/Ge heterostructure NW FETs



M. Liu et al., Communications and Engineering 2023

GeSn/Ge Material Growth for p-FETs

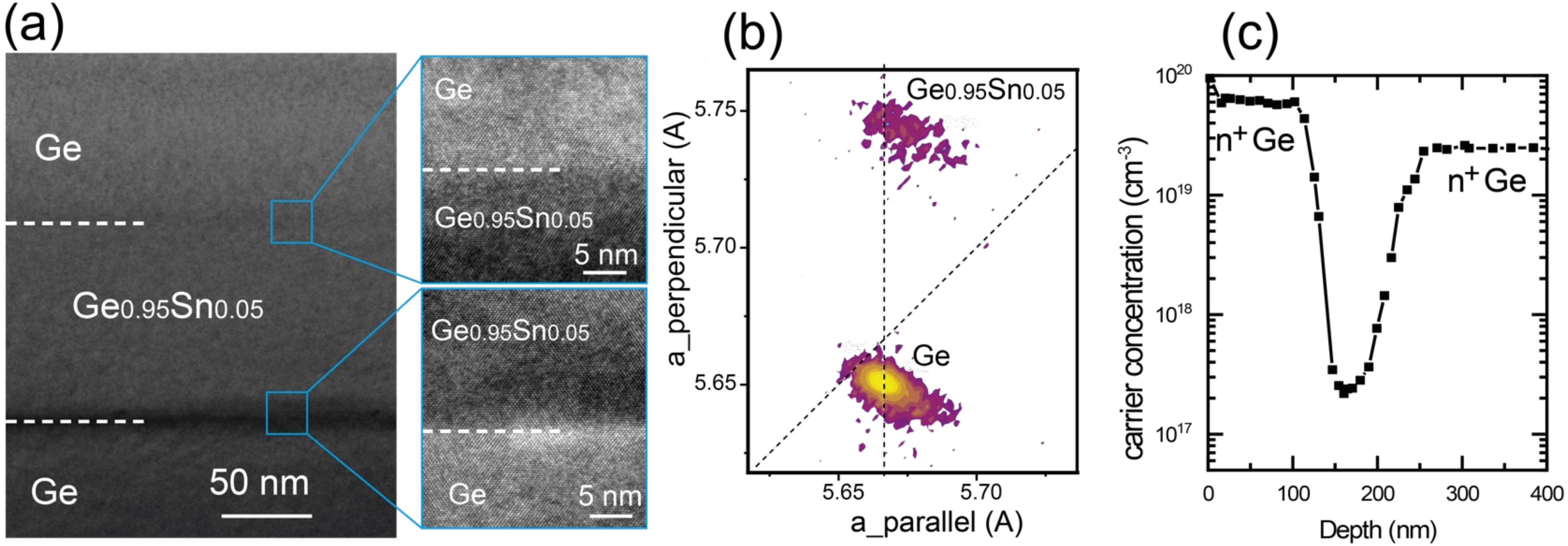
- Epitaxial $Ge_{0.92}Sn_{0.08}$ layer on Ge virtual substrate by CVD
  - Good Crystalline quality of strained $Ge_{0.92}Sn_{0.08}$
  - Defect-free interface



Pseudomorphic growth

Ge/GeSn/Ge Growth for n-FETs

- Epitaxial $Ge_{0.92}Sn_{0.05}$ layer on Ge virtual substrate by CVD
  - Good Crystalline quality of strained $Ge_{0.92}Sn_{0.05}$
  - Defect-free interface



Pseudomorphic growth

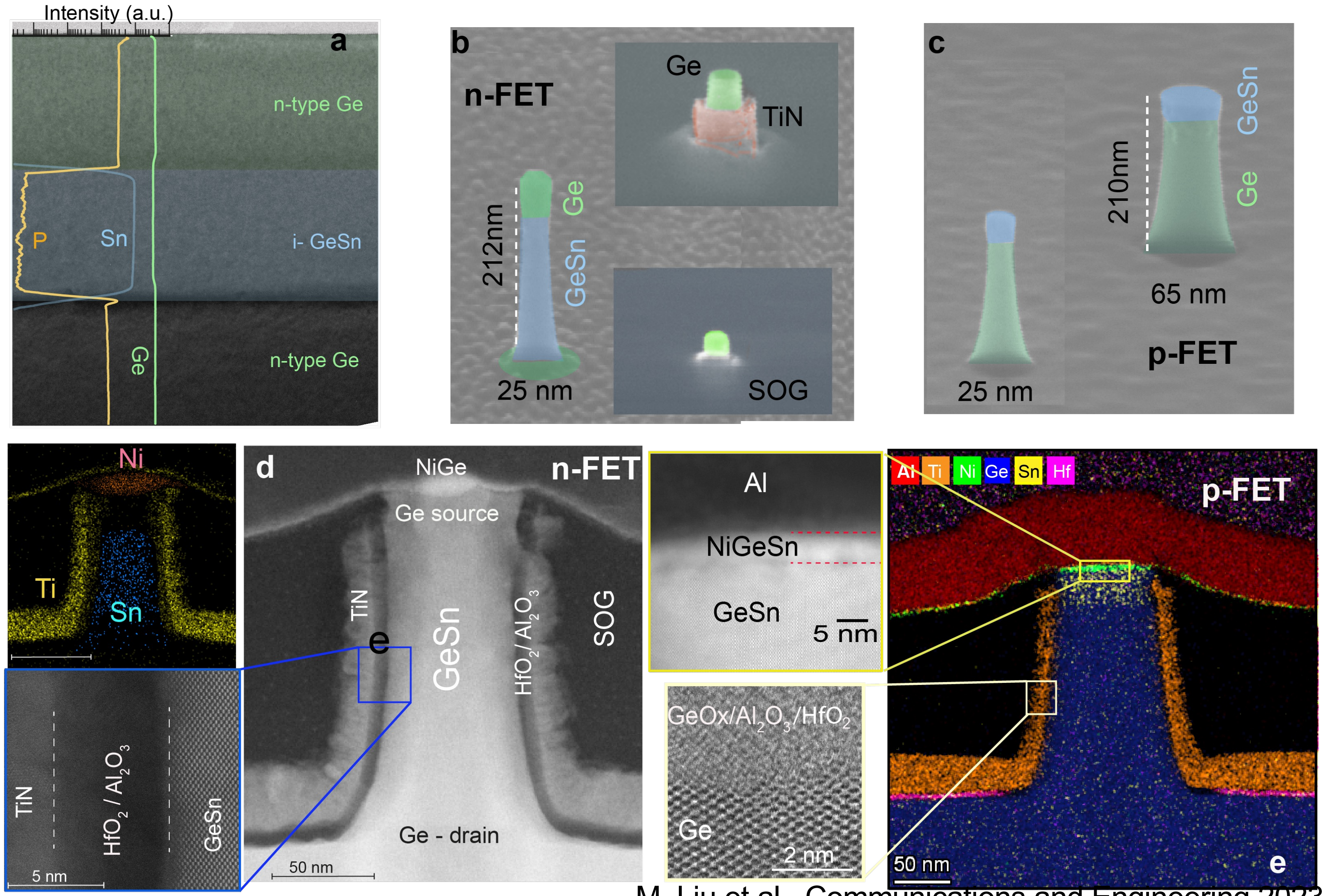
Vertical GeSn NW CMOS

n-VFET:

- GeSn channel
- Ge S/D
- In situ doping

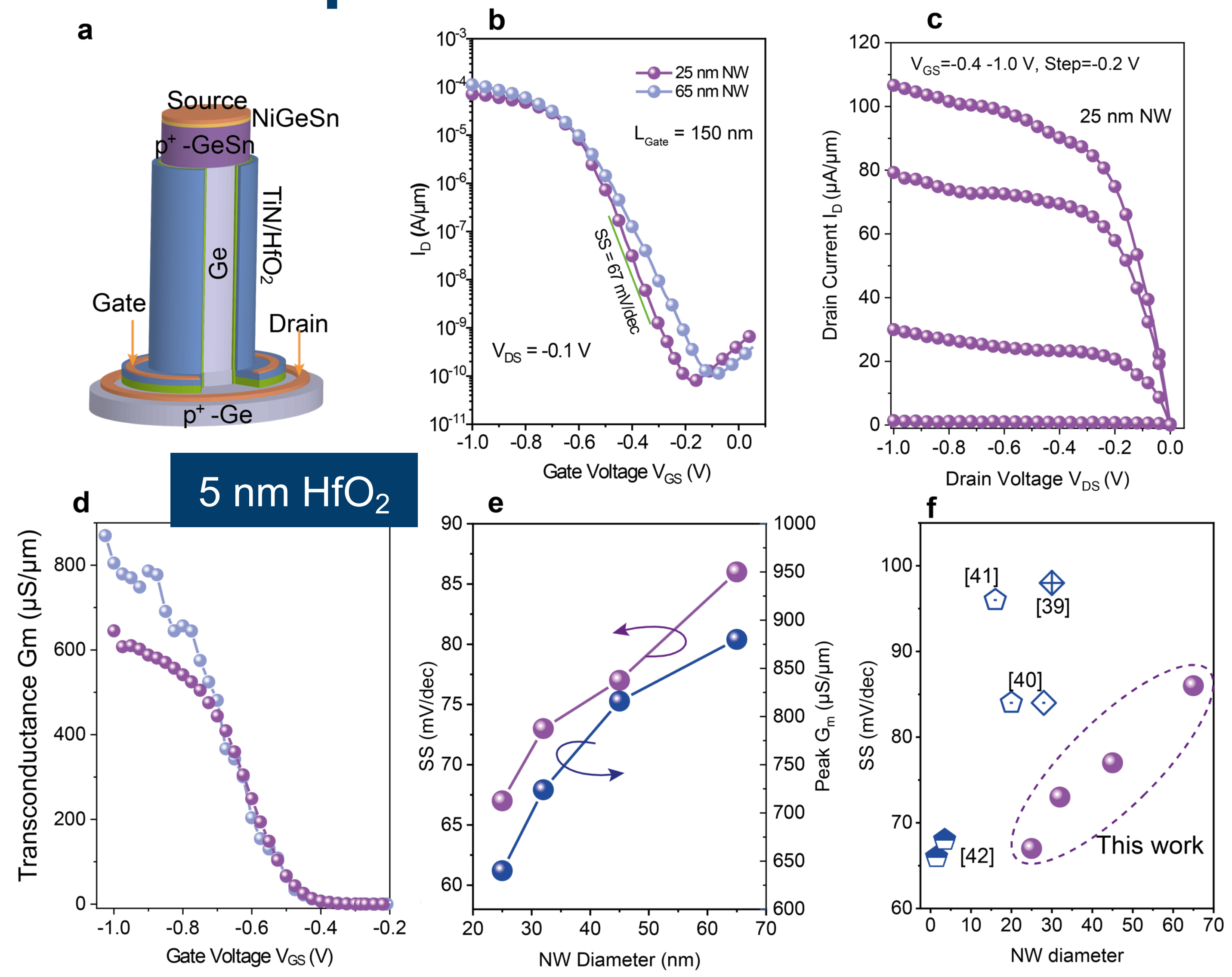
P-VFET:

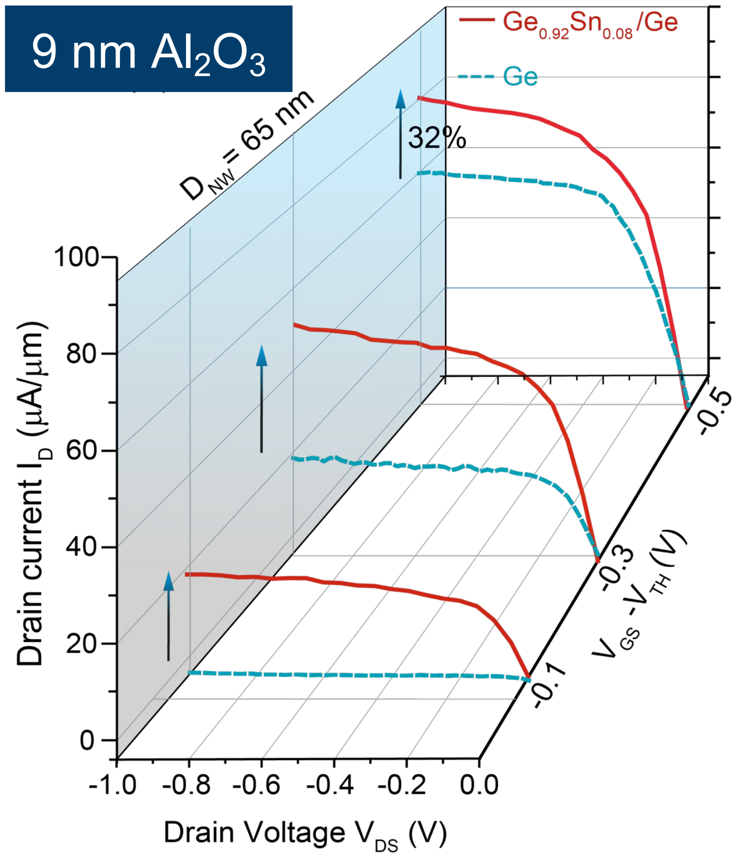
- Ge channel
- GeSn top source



M. Liu et al., Communications and Engineering 2023

GeSn/Ge p-VFETs

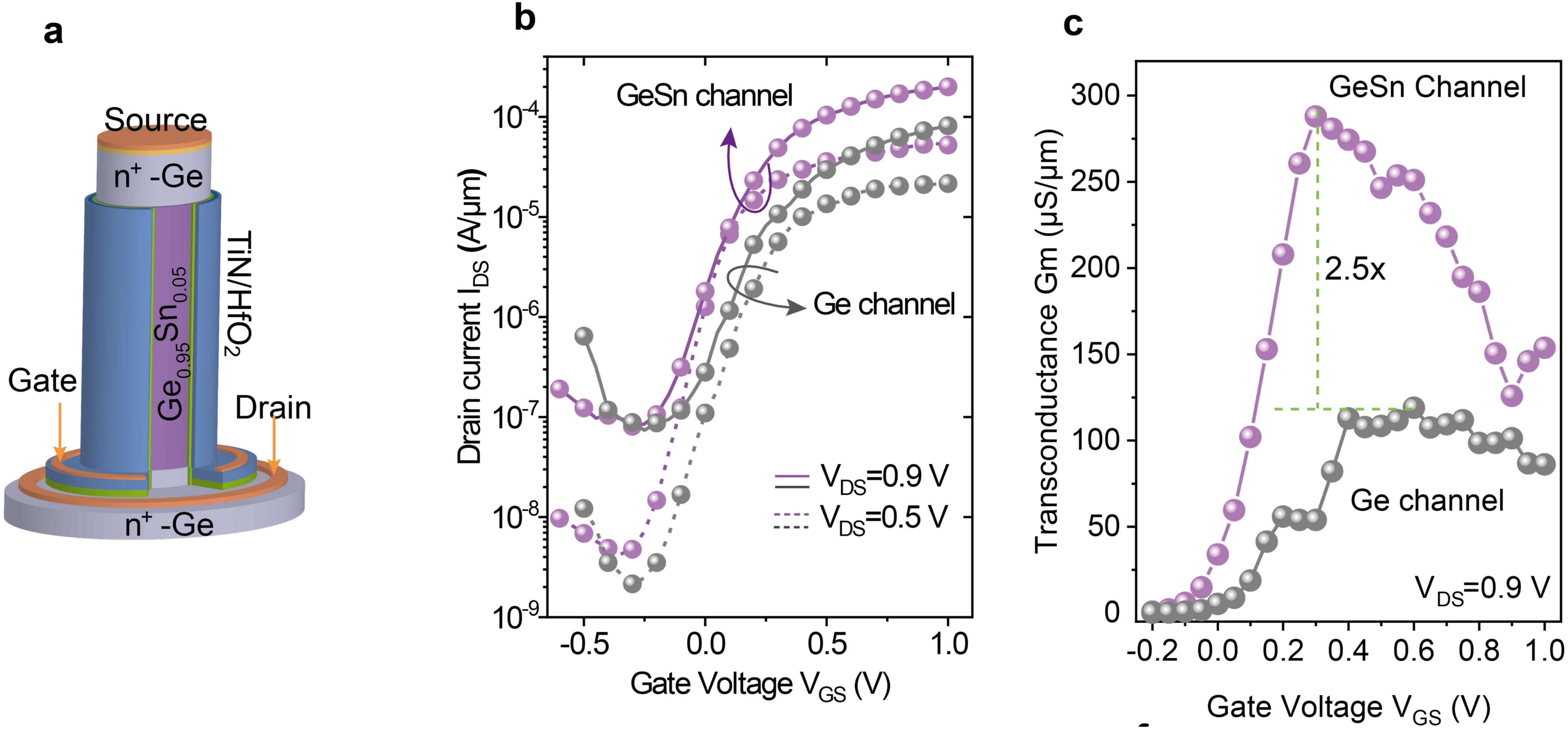




~32% I_{ON} enhancement for $Ge_{0.92}Sn_{0.08}$/Ge device at V_{ov} = -0.5V.

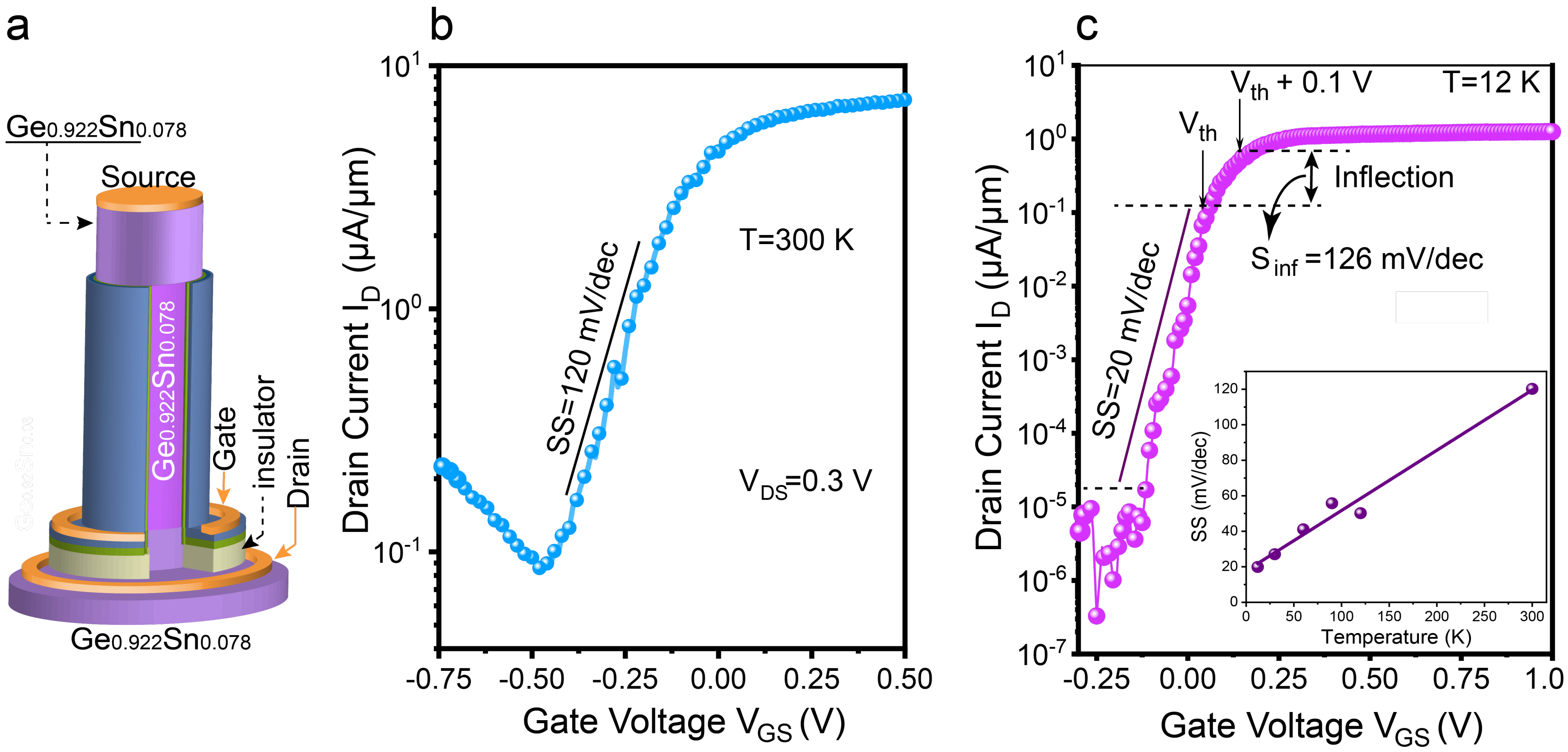
M. Liu et al., ACS Appl. Nano Materials 2021

Vertical GeSn Nanowire nFETs



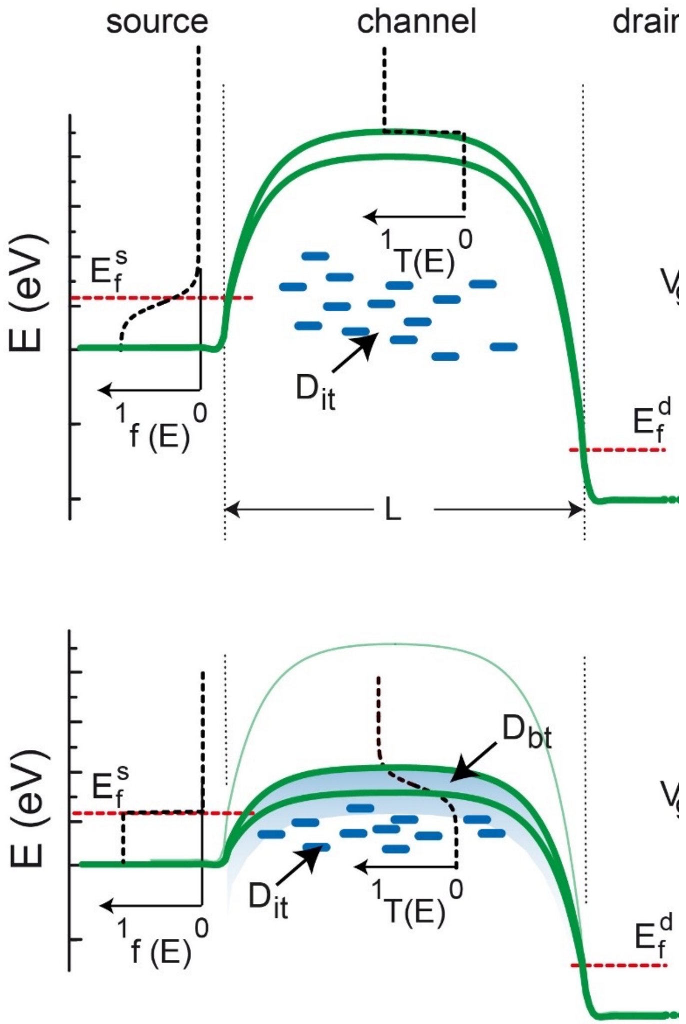
M. Liu et al, Communications Engineering 2023

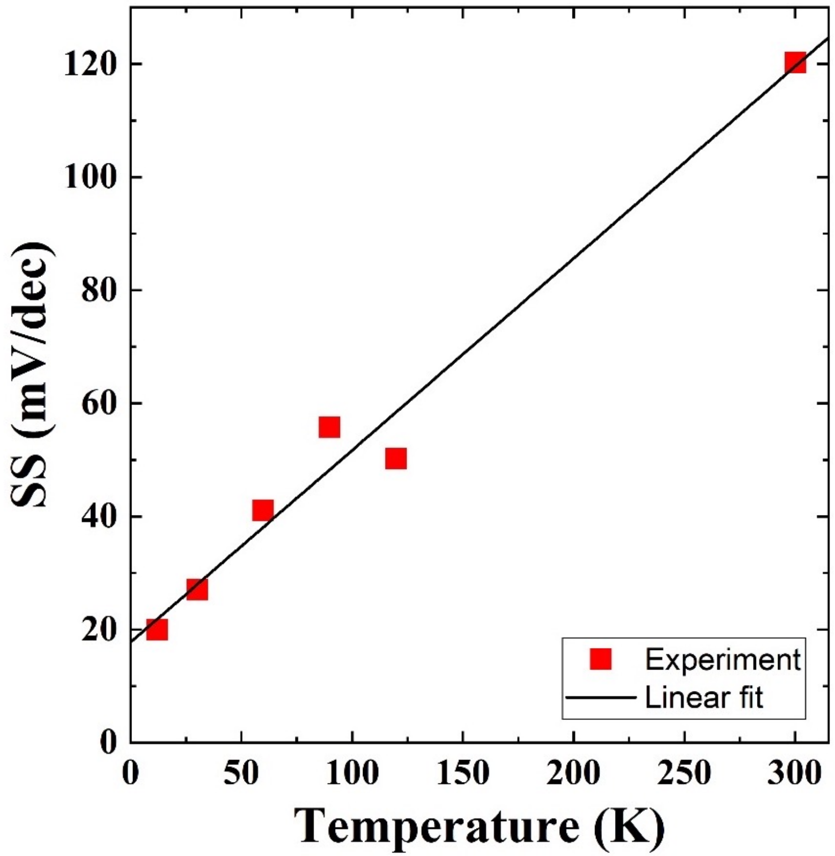
Vertical All-GeSn Nanowire nFETs

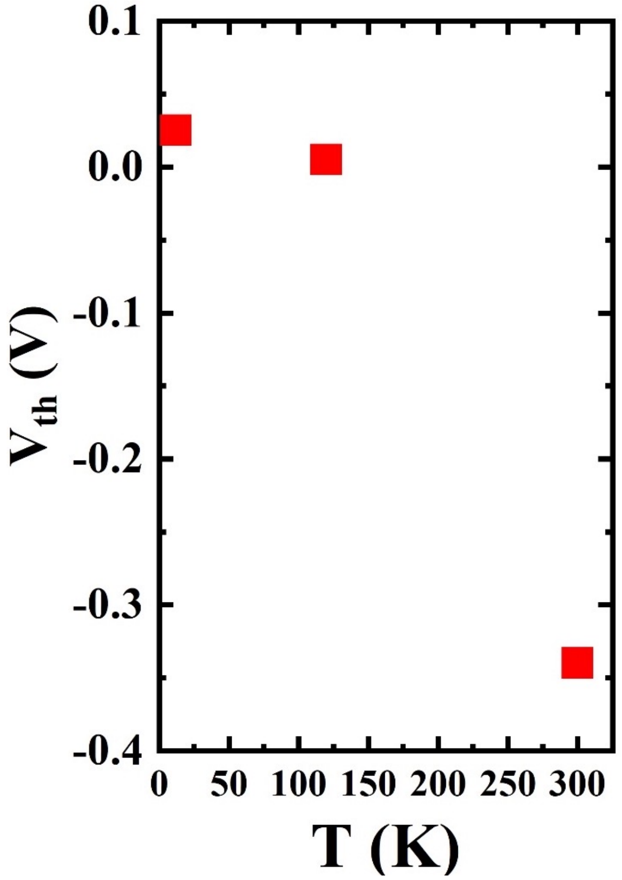


M. Liu et al, Communications Engineering 2023

GeSn Cryogenic n-FETs





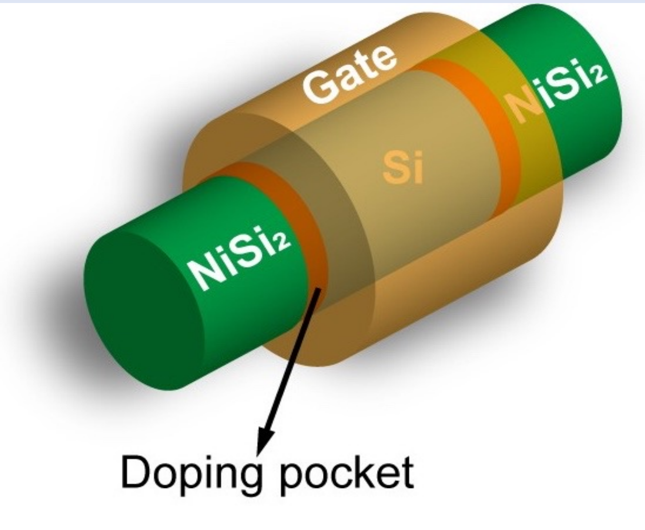


- SS linearly dependent on temperature
- V_{th} increases at lower temperatures, close to 0 V

M. Liu et al, Communications and Engineering, 2023

SUMMARY

Si NW FETs



1. SS~ 60 mV/dec at 300K
2. Suppressed band tails effect by IIS
3. Lowest SS, SS_{th}, and high G_m

GeSn Vertical NW GAA FETs

1. Heterostructure design for n- and p-FETs
2. Higher hole and electron mobilities than Ge
3. Improved SS at cryo-T and inflection

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- **Ionut Radu**