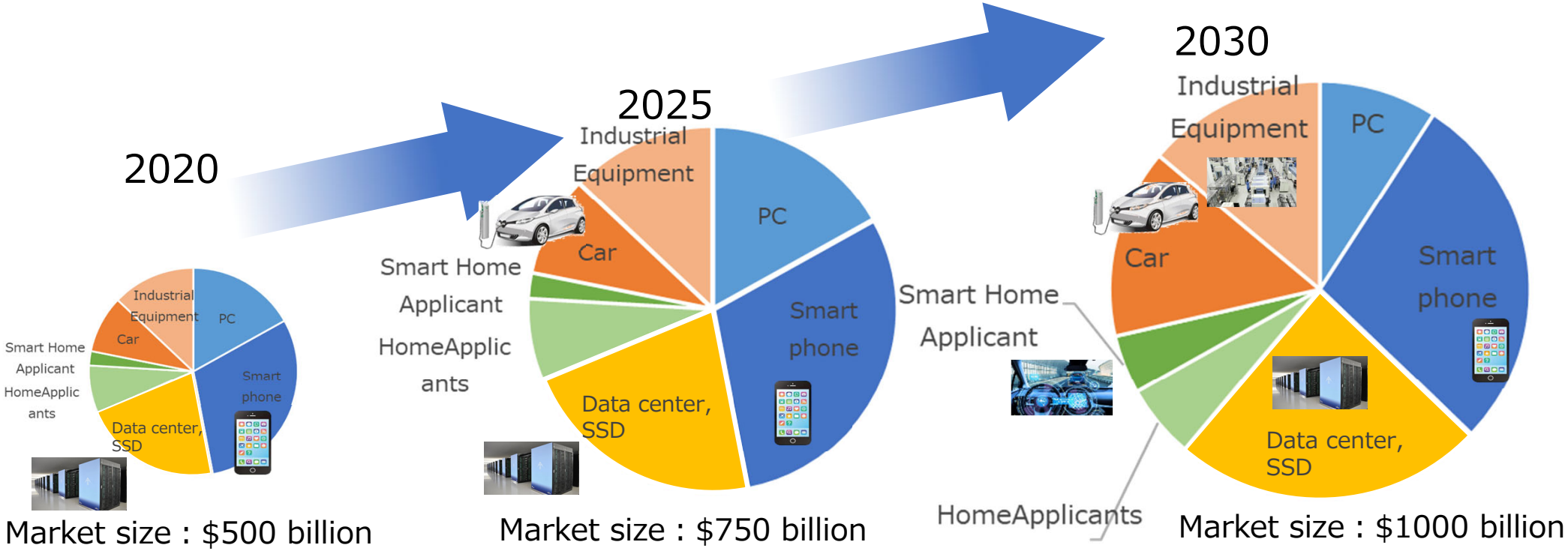
Basic Semiconductor Revitalization Strategy in Japan

Step 1 : Enhancement of Basic Production Capacity for IoT



Step 2 : Realization of Next Gene Semiconductor Technology through US – JP Collaboration

Step 3 : R&D For Future technology

Photonics-Electronics Convergence, Quantum Computing through Global Collaboration

(Reference) : prepared by METI, based on data from OMDIA

Step1:Advanced Semiconductor Production Capacity

1．JASM（Joint Venture of TSMC（TW）, Sony（JP） and Denso（JP））
【June 17, 2022】
- ✓Up to approx **US$3.5 billion** subsidy
- ✓New-Fab for Logic Semiconductor (12–28 nm)

2．KIOXIA（JP） and Western Digital（US） 【July 26, 2022】
- ✓Up to approx **US$700 million** subsidy
- ✓Advanced 3D NAND Flash Memory Investment

3． Micron (US) 【September 30, 2022】
- ✓Up to approx **US$320 million** subsidy
- ✓Advanced DRAM(1β) Investment

+Additional

450 billion JPN yen (US$ 3.2 billion)

Step1:General Semiconductor Production Capacity

Challenge

- 20% Demand Growth in 2021 from 2019
- Only 8% Supply Growth (Operation Rate is 95%)

Solution

- Production Capacity Expansion

  For Power Chip, Analog Chip, etc, (Low Investment Incentive in Private)

“Subsidy Program for Indispensable Semiconductors” ($340M)

- Support Capital Investment in 27 Factories out of 81 in Japan (33%)

Profile of Economic Security Promotion Act*(ESPA)

* "Act for the Promotion of Ensuring National Security through Integrated Implementation of Economic Measures"

- The first legislation which includes **the concept of "economic security"** "Basic act" for economic security measures under the one legislative purpose bundling the four policy issues:
  - **1) Ensuring Stable Supply of Critical Items**
  - **2) Ensuring the Stable Provision of Essential Infrastructure Services**
  - **3) Enhancing Development of Advanced Critical Technologies**
  - **4) Non-Disclosure of Selected Patent Applications**
- Named as the **Economic Security "Promotion" Act** under the presumption that the government of Japan must promptly enact from policy fields ready to be legislated and continue to revise, while recognizing remaining policy challenges, including the necessity of improving information security of technologies supported by government funds.

To strengthen supply capabilities of semiconductor supply chain

- Based on ESPA law, after **designating semiconductors as Critical Items**, it aims to strengthen the domestic production capacity of semiconductors by enhancing the manufacturing capacity of **legacy chips and the manufacturing equipment, materials, and raw materials** that make up the semiconductor supply chain.
- The budget (FY2022 supplementary budget) is **368.6 B JPN Yen（2.6B＄）**.

Measures to stable supply of semiconductors	
①Legacy Chips （Power MCU Analong）	✓Support for large-scale capital investment, etc. to strengthen domestic manufacturing capacity ✓For power chips, this program provides intensive support for investments of a considerable scale with a focus on SiC power semiconductors, while also taking into consideration the efforts to procure key materials.
②Manufacturing Equipment	✓ Support for large-scale capital investment, etc. to strengthen domestic manufacturing capacity
③Materials	✓ Support for large-scale capital investment, etc. to strengthen domestic manufacturing capacity ✓ For SiC wafers, consideration is also given to whether or not the initiatives contribute to ensuring the international competitiveness of the power semiconductor industry.
④Raw Materials	✓Support for capital investment, etc. to promote recycling of semiconductor raw materials, strengthen domestic production, stockpiling, and transportation systems

Step2:Beyond 2nm Next Generation Semicon Tech

Drastic Technology Change **from Fin-Fet to GAA**

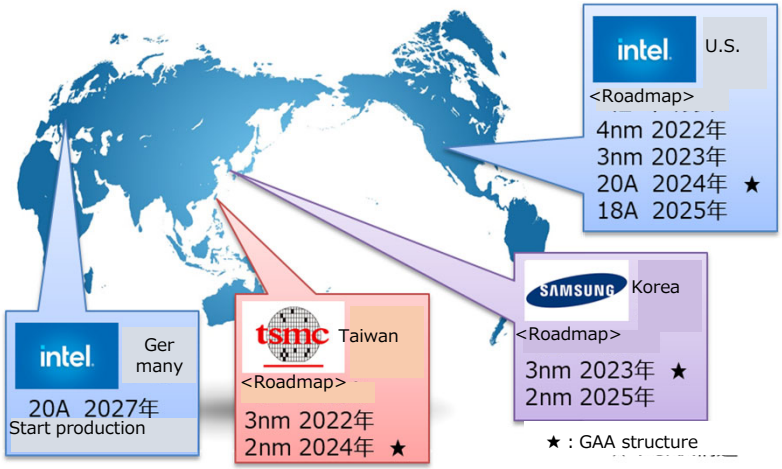
abroad

Japan

tsmc SAMSUNG intel IBM

Japan is 10 years behind from Global Trend

Challenges
- ✓ Development of use cases utilizing next-generation semiconductors
- ✓ Establish knowledge of next-generation semiconductor development and manufacturing
- ✓ Education of human resources



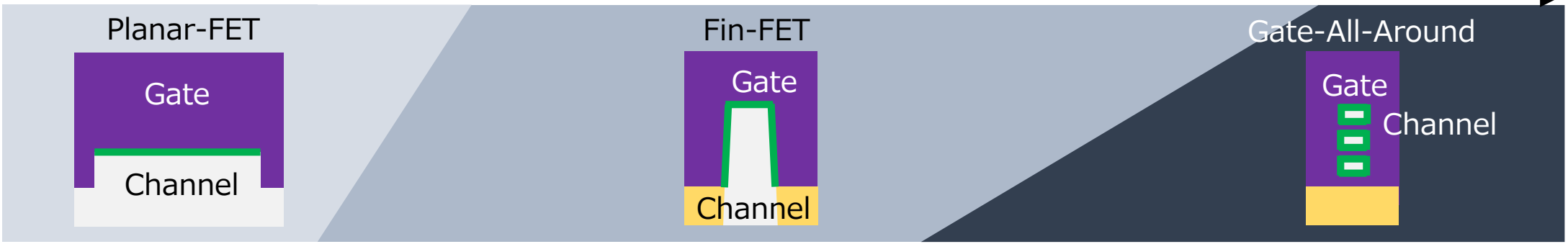
TSMC Japan

Next Generation Semiconductor

Fin-FET introduction

GAA introduction (plan)

45nm 28nm 22nm 16/12nm 7nm 5nm 3nm 2nm Beyond

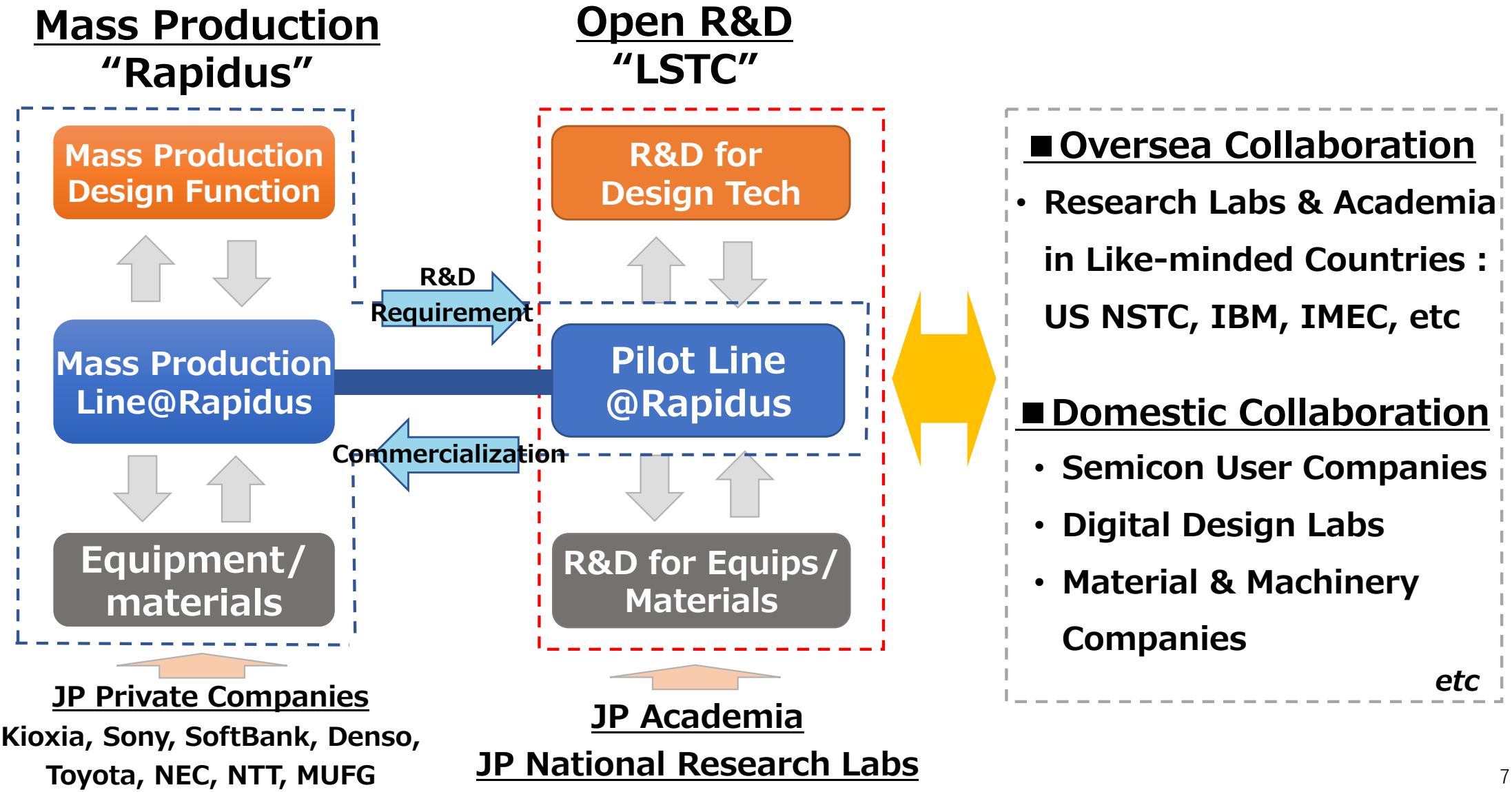


Same gate width in smaller area ＝high integration

Project Framework for Next Generation Beyond 2nm Project (B2P)

<METI announcement on 11th Nov.>: Establishment of Two Entities for B2P

1. "LSTC": Open Collaborative R&D Platform ※Leading-Edge Semiconductor Technology Center
2. "Rapidus": Mass Production Entity (Inc.)



Process for Next-Generation Semiconductor R&D Project

- **70B JPN Yen** will be allocated to Rapidus (announced on Nov. 11)
- **New additional budget of 260B JPN Yen** will be allocated to Rapidus (announced on Apr. 25)
- R&D Theme by Rapidus; **2nm-node Transistor Integration Technology and Short TAT [*1] Production Technology** through the Cooperation between Japan and the US
  - Will **cooperate with IBM and others** to develop technologies for **2 nm-node logic semiconductors**, build **short TAT pilot lines** in Japan and conduct verifications using test chips.
  - In FY2022, will **acquire the elemental technologies for 2nm-node semiconductors**, **begin installing EUV lithography equipment**, **formulate specifications** for production equipment, transport systems, and production management systems **necessary for short TAT** production system, and deploy the **initial design for pilot line** (**70 B JPN Yen**[*2]).
  - Will aim to **commercialize** next generation logic foundry after the R&D project

※1 TAT: Turn Around Time
※2 $1 = 140 JPN Yen

Mass production base: Rapidus Corporation

- A company established **with the endorsement of major Japanese companies that gathers top-level engineers from all over Japan in order to create a mass production base for next-generation semiconductors.**
- It has been selected to carry out the research and development project toward **the establishment of design and manufacturing bases for next-generation semiconductors in the latter half of the 2020s.**
- **Together with LSTC, Rapidus will aim to build a mass production base for next-generation semiconductors in Japan**.

■ Investing Companies

Company	Investment amount(Billion)
Kioxia	1 billion
Sony	1 billion
Soft Bank	1 billion
Denso	1 billion
Toyota	1 billion
NEC	1 billion
NTT	1 billion
MUFG Bank	0.3 billion

■ Rapidus Corporation main principal officers

Position	Name
Executive Chairman	HIGASHI Tetsuro
President and Representative Director	KOIKE Atsuyoshi

The system may be expanded in the future in accordance with Rapidus Corporation's activities.

LSTC（Leading-edge Semiconductor Technology Center : Japan NSTC）

LSTC was established in 2022, leaders of each teams were assigned.
R&D items along a needs from industry are under discussion in each teams.

Chairman
HIGASHI Tetsuro

Committee for R&D planning
ISHIMARU Kazunari（Rapidus）
MASAHARA Meisyoku（AIST）
KURODA Tadahiro（University of Tokyo）
HIRAMOTO Toshiro（University of Tokyo）
SUGAWA Shigetoshi（Tohoku University）
CHIKYO Toyohiro（NIMS）
SUGANUMA Katsuaki（Osaka Univ.）
KOIKE Atsuyoshi（Rapidus）

Chief in Academia
GONOKAMI Makoto

Chip Design
KURODA Tadahiro

Physical Transistor Design
HIRAMOTO Toshiro

Productization Technology
SUGAWA Shigetoshi

Materials Technology
CHIKYO Toyohiro

Advanced Packaging
SUGANUMA Katsuaki

Use-Case Creation
TBD

Human-Resource Development
TBD.

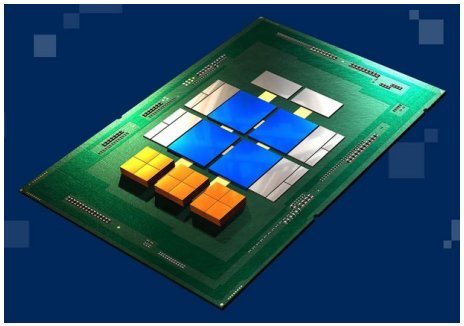
参画機関

AIST NATIONAL INSTITUTE OF ADVANCED INDUSTRIAL SCIENCE AND TECHNOLOGY (AIST)
RIKEN
NIMS 国立研究開発法人 物質・材料研究機構 National Institute for Materials Science
Rapidus
東京大学 THE UNIVERSITY OF TOKYO
東北大学 TOHOKU UNIVERSITY
東京工業大学 Tokyo Institute of Technology
大阪大学 OSAKA UNIVERSITY
名古屋大学 NAGOYA UNIVERSITY
KEK

Advanced Packaging Development

- Japanese techs like substrate, material and equipment can contribute to chiplet tech.
- TSMC opened new 3DIC RD center in Tsukuba.

■New standard of a Chiplet “UCIe”



AMD arm ASE GROUP
Google Cloud intel Meta
Microsoft Qualcomm
SAMSUNG tsmc

Reference: “UCIe” website

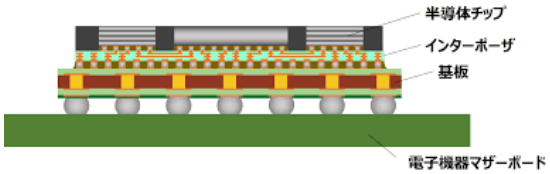
to invite/cooperate

■Technology of advanced packaging

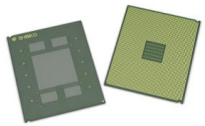
TSMC Japan
3DIC R&D Center

to cooperate

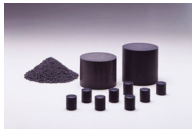
2.5D/3DIC



Reference: “DNP” website



Substrates



Materials

Manufacturing technology

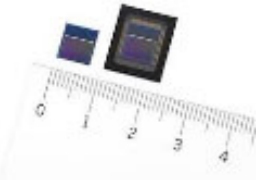
Next Generation Computing Platform

DX Trend

GX Trend

High Functional Low power semiconductors

AI semiconductor



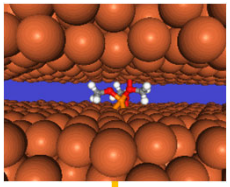
Sensor ×AI semicon

Simulation Needs

Nation security

Natural disaster

Material R&D



・・・

High Functional Edge Devices

5G/Post 5G
Beyond 5G

On-board

Autonomous vehicle

Smart factory

Robotics

・・・

【Computing Resource manager】

(Optimally combining and controlling various and distributed computing infrastructure)

High speed Low Pewer semiconductors

Ultra high performance CPU

AI accelerator

Ultra-high-speed, high-capacity optical network

Quantum gate

Quantum annealing

【 Quantum】

Supercomputer

AI computer

・・・

High performance computer

・・・

【 Classical】

On-board

Overview of Semiconductor human resource development

- Develop the professional human resources to supply of next-generation semiconductor and create the use cases through global collaboration.
- Expand to the regional basis in consideration of the characteristics of each region and private sector is expanding these efforts nationwide.

Efforts of Each Regional Basis

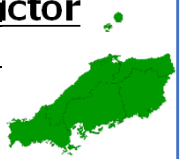
Kyushu Human Resource Development Consortium

(Industry) SONY, JASM
(Academia) Kyushu univ., Kumamoto univ.
(Government) Kyushu Bureau of Economy, Trade and Industry, METI

Tohoku Semiconductor and Electronics Design Study Group

(Industry) KIOXIA Iwate,
(Academia) Tohoku univ.
(Government) Tohoku Bureau of Economy, Trade and Industry, METI

Chugoku Region Semiconductor Industry Promotion Council



(Industry) Micron
(Academia) Hiroshima univ.
(Government) Chugoku Bureau of Economy, Trade and Industry, METI

Considering the development of professionals and global human resources

- ✓ In order to establish the design and manufacturing base for next-generation semiconductors in the latter half of the 2020s, there is an urgent need to develop professional and global human resources.
- ✓ Development of human resources responsible for all processes from design to cutting-edge packaging and mass production processes.