Chips Acts and IRDS Building Pillars And Bridges over Valleys of Death

Paolo Gargini

Chairman IRDS

Life-Fellow IEEE, Fellow I-JSAP

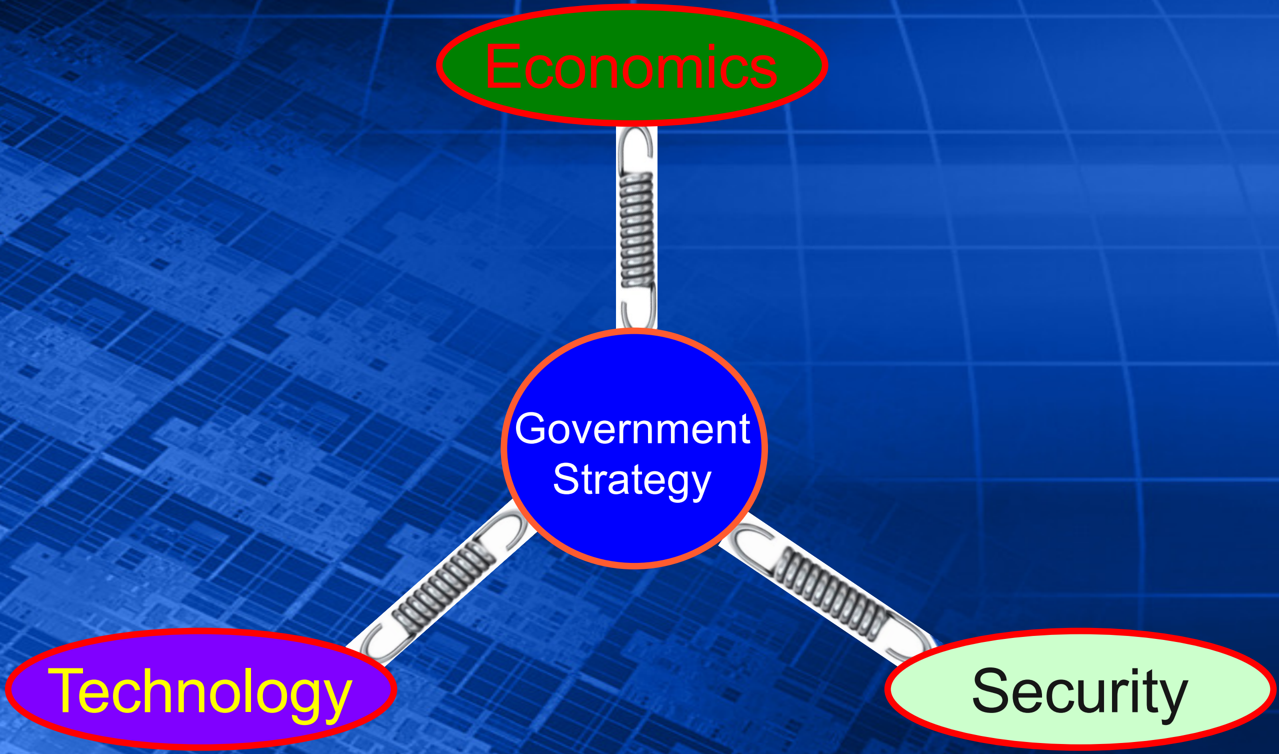
Former Intel Fellow
and
Director of Technology Strategy (1978-2012)

A Message from Dr, Laurie Locascio
Director of NIST and Undersecretary of Commerce

The US CHIPS R&D program looks forward to explore opportunities to cooperate with allied and partner nations on semiconductor technology innovation. We see value where Interest in technology roadmaps and grand challenges might align.

The Script

- 1957: Act 1
- 1987: Act 2
- 1997: Act 3
- 2020: Act 4



Economics

Government Strategy

Technology

Security

Electronics Industry Drivers

- Economic Success
  - Obtain the maximum return with the smallest possible investment (e.g., most Companies)
- Technology Leadership
  - Master the most advanced technology no matter how much it costs (i.e., first man on the Moon)
- Security Requirements
  - Keep the most advanced technology completely exclusive (i.e., many governments)

These requirements are completely inconsistent with each other

Nothing is New

But

Never is the Same

First Act

THE FAIRCHILD EIGHT: From left, Gordon Moore, Sheldon Roberts, Eugene Kleiner, Robert Noyce, Victor Grinich, Julius Blank, Jean Hoerni, and Jay Last.

October 3, 1957

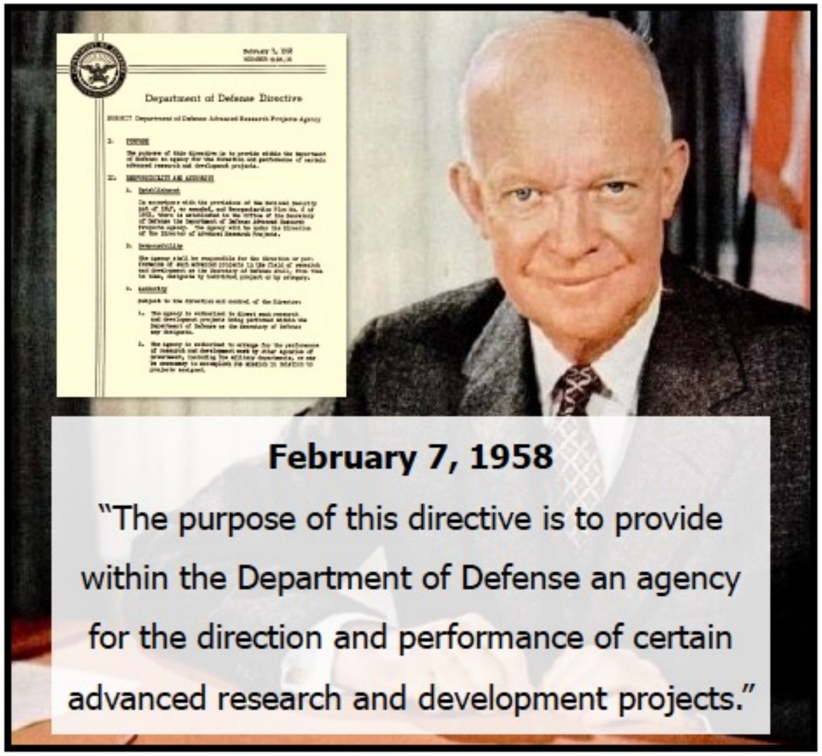
First Shocker

DARPA Origins

Defense Advanced Research Projects Agency

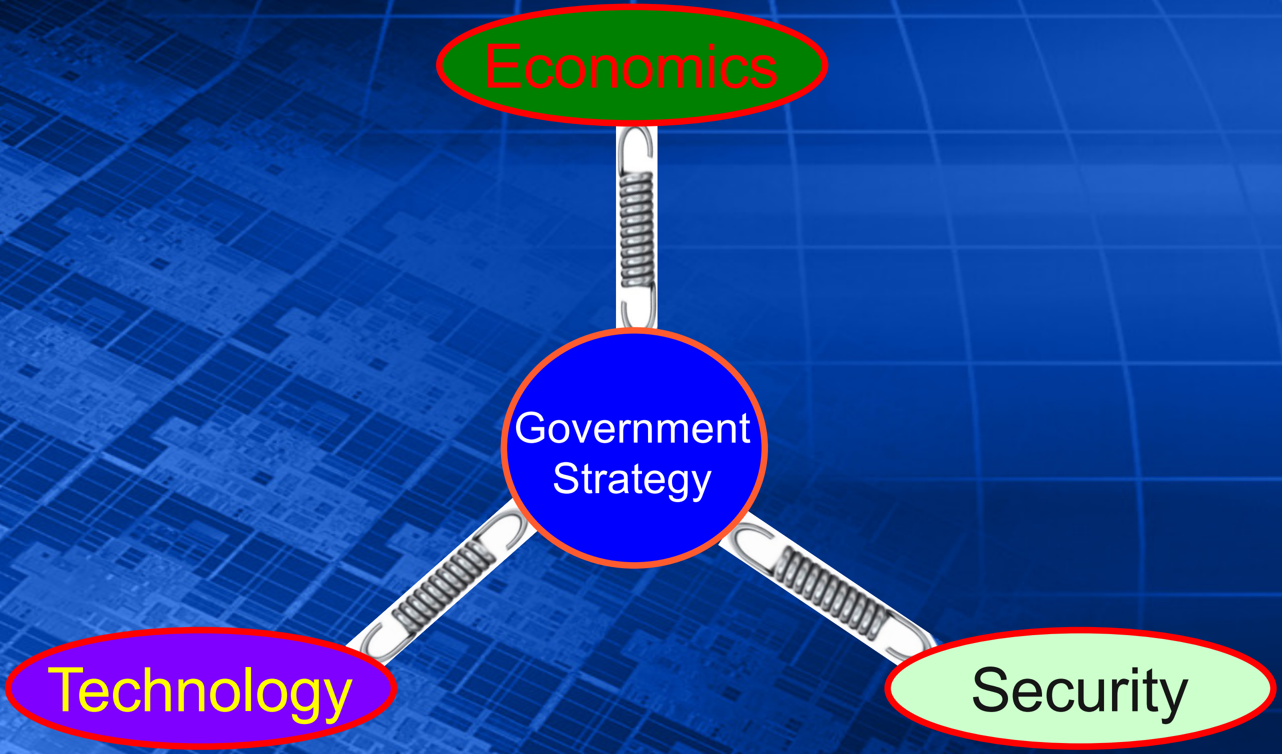
October 4, 1957

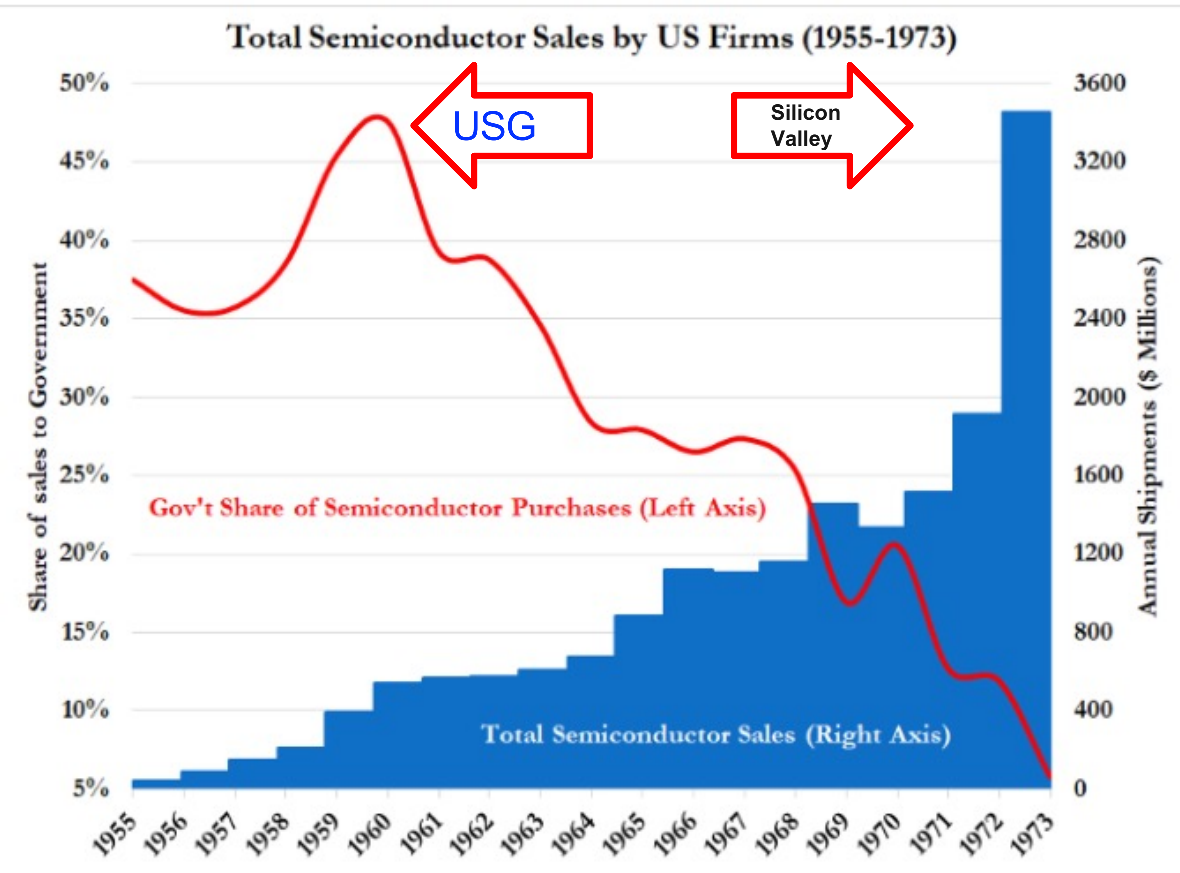
U.S.S.R. beats U.S. to space with Sputnik satellite; U.S. should never again be surprised by technology.



February 7, 1958

"The purpose of this directive is to provide within the Department of Defense an agency for the direction and performance of certain advanced research and development projects."


Economics
Government Strategy
Technology
Security



Total Semiconductor Sales by US Firms (1955-1973)

Second Act

IBM selected Intel and Microsoft for PC

(August 1980-August 1981)

August 12, 1981

JUNE 2, 1981

TEST STRATEGIES HELP USERS CHECK BUBBLE MEMORIES/145

Letter from San Diego: the boom is waning/100

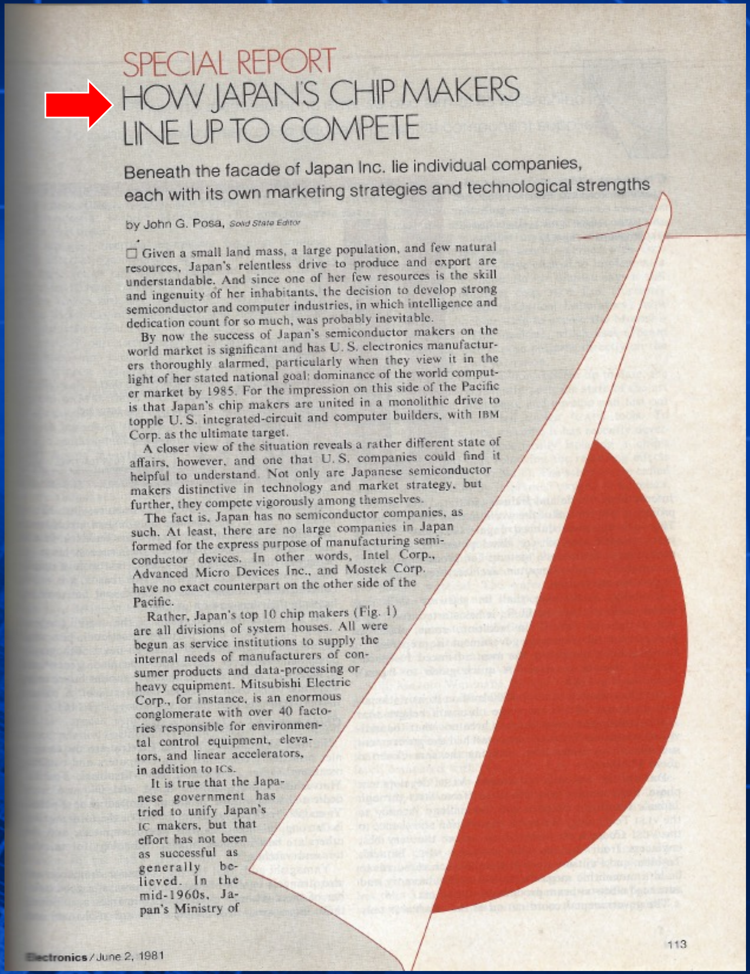
16-bit processor adds virtual memory to minicomputer line/134

SIX DOLLARS A McGRAW-HILL PUBLICATION

Electronics

INSIDE JAPANESE SEMICONDUCTOR TECHNOLOGY

1420 GRG306 MFPA1 JUL81
PA GARGINI
3005 [illegible] RD
PALO ALTO CA 94303



SPECIAL REPORT

HOW JAPAN'S CHIP MAKERS LINE UP TO COMPETE

Beneath the facade of Japan Inc. lie individual companies, each with its own marketing strategies and technological strengths

by John G. Posa, *Solid State Editor*

☐ Given a small land mass, a large population, and few natural resources, Japan's relentless drive to produce and export are understandable. And since one of her few resources is the skill and ingenuity of her inhabitants, the decision to develop strong semiconductor and computer industries, in which intelligence and dedication count for so much, was probably inevitable.

By now the success of Japan's semiconductor makers on the world market is significant and has U. S. electronics manufacturers thoroughly alarmed, particularly when they view it in the light of her stated national goal: dominance of the world computer market by 1985. For the impression on this side of the Pacific is that Japan's chip makers are united in a monolithic drive to topple U. S. integrated-circuit and computer builders, with IBM Corp. as the ultimate target.

A closer view of the situation reveals a rather different state of affairs, however, and one that U. S. companies could find it helpful to understand. Not only are Japanese semiconductor makers distinctive in technology and market strategy, but further, they compete vigorously among themselves.

The fact is, Japan has no semiconductor companies, as such. At least, there are no large companies in Japan formed for the express purpose of manufacturing semiconductor devices. In other words, Intel Corp., Advanced Micro Devices Inc., and Mostek Corp. have no exact counterpart on the other side of the Pacific.

Rather, Japan's top 10 chip makers (Fig. 1) are all divisions of system houses. All were begun as service institutions to supply the internal needs of manufacturers of consumer products and data-processing or heavy equipment. Mitsubishi Electric Corp., for instance, is an enormous conglomerate with over 40 factories responsible for environmental control equipment, elevators, and linear accelerators, in addition to ICs.

It is true that the Japanese government has tried to unify Japan's IC makers, but that effort has not been as successful as generally believed. In the mid-1960s, Japan's Ministry of

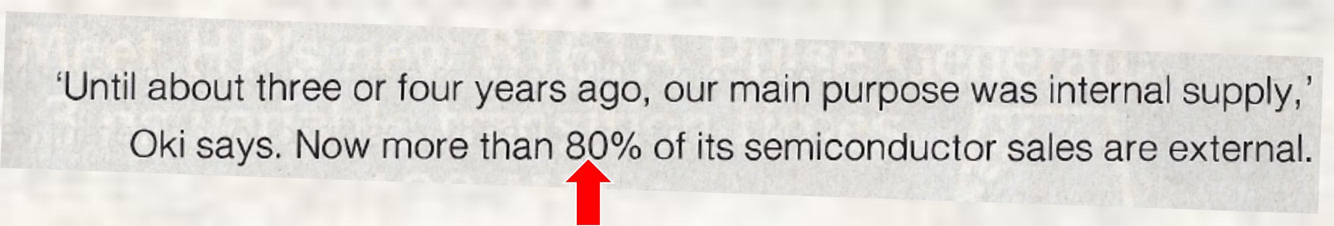
Electronics / June 2, 1981

113

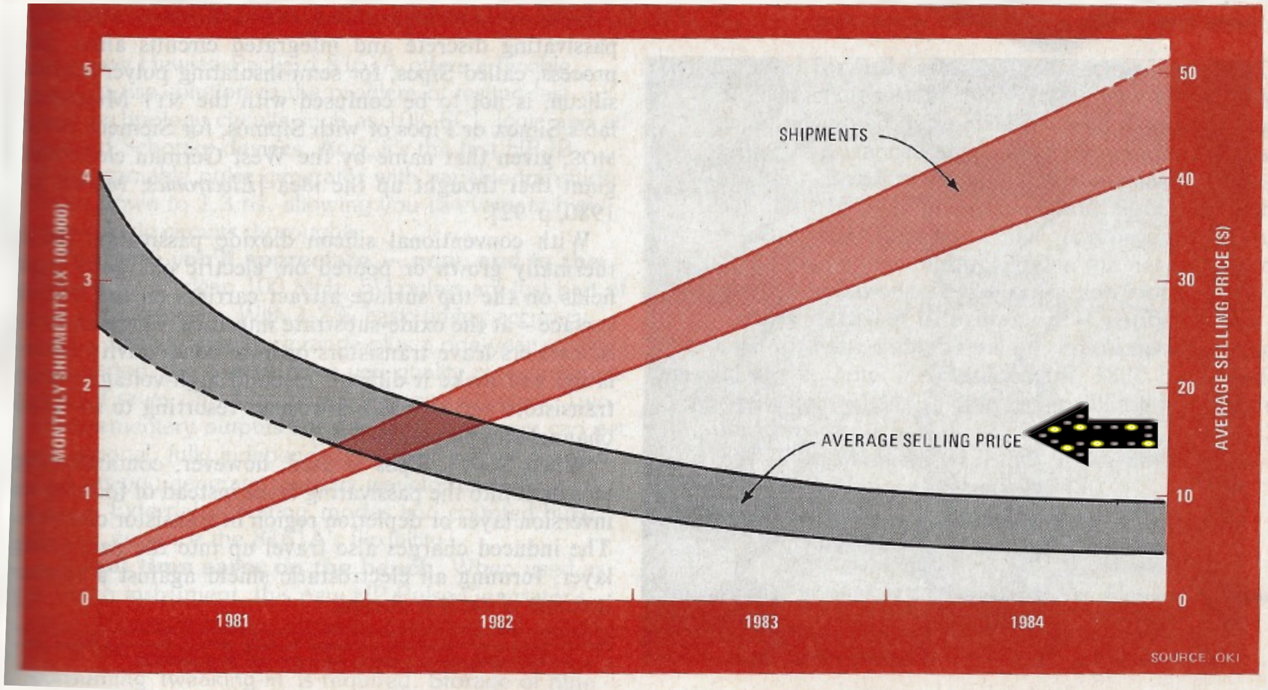
2023

IEEE NTRS ITRS ITRS 2.0 IRDS INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS

P.Gargini



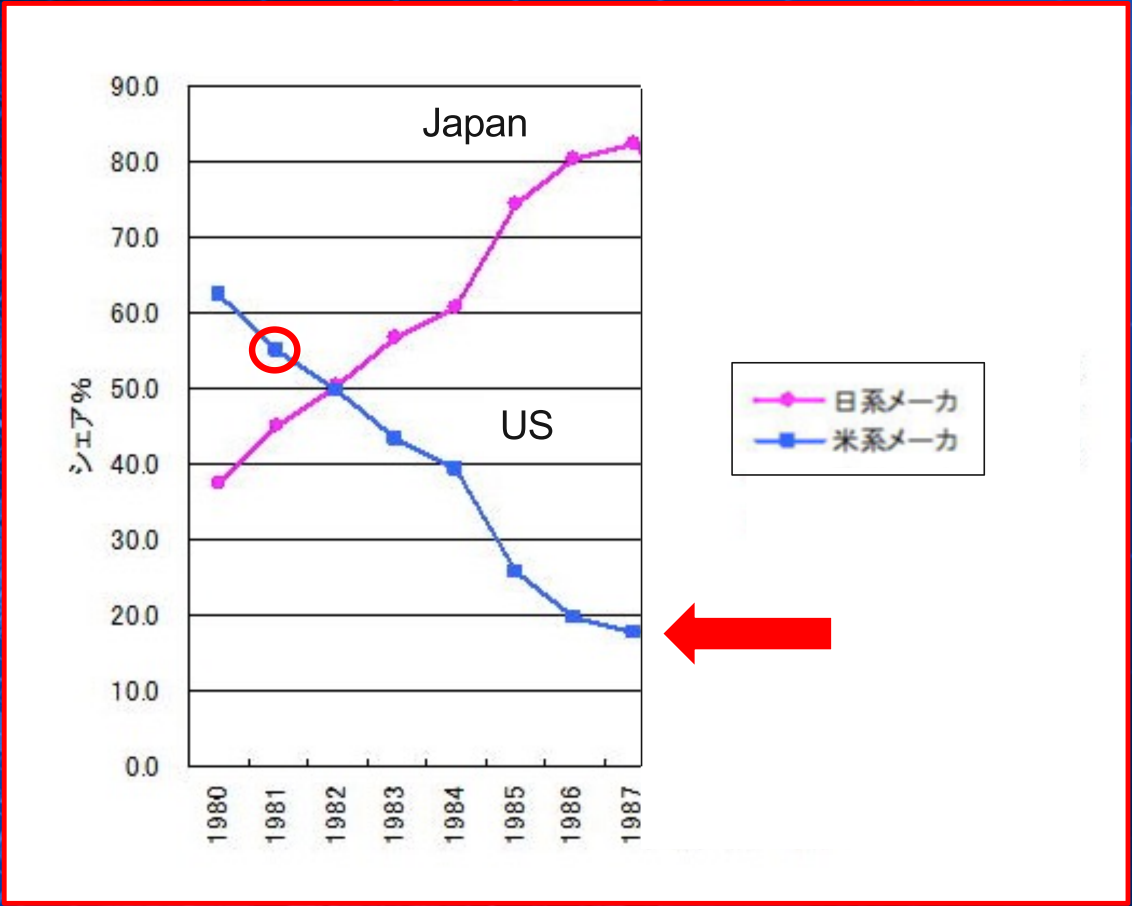
‘Until about three or four years ago, our main purpose was internal supply,’ Oki says. Now more than 80% of its semiconductor sales are external.



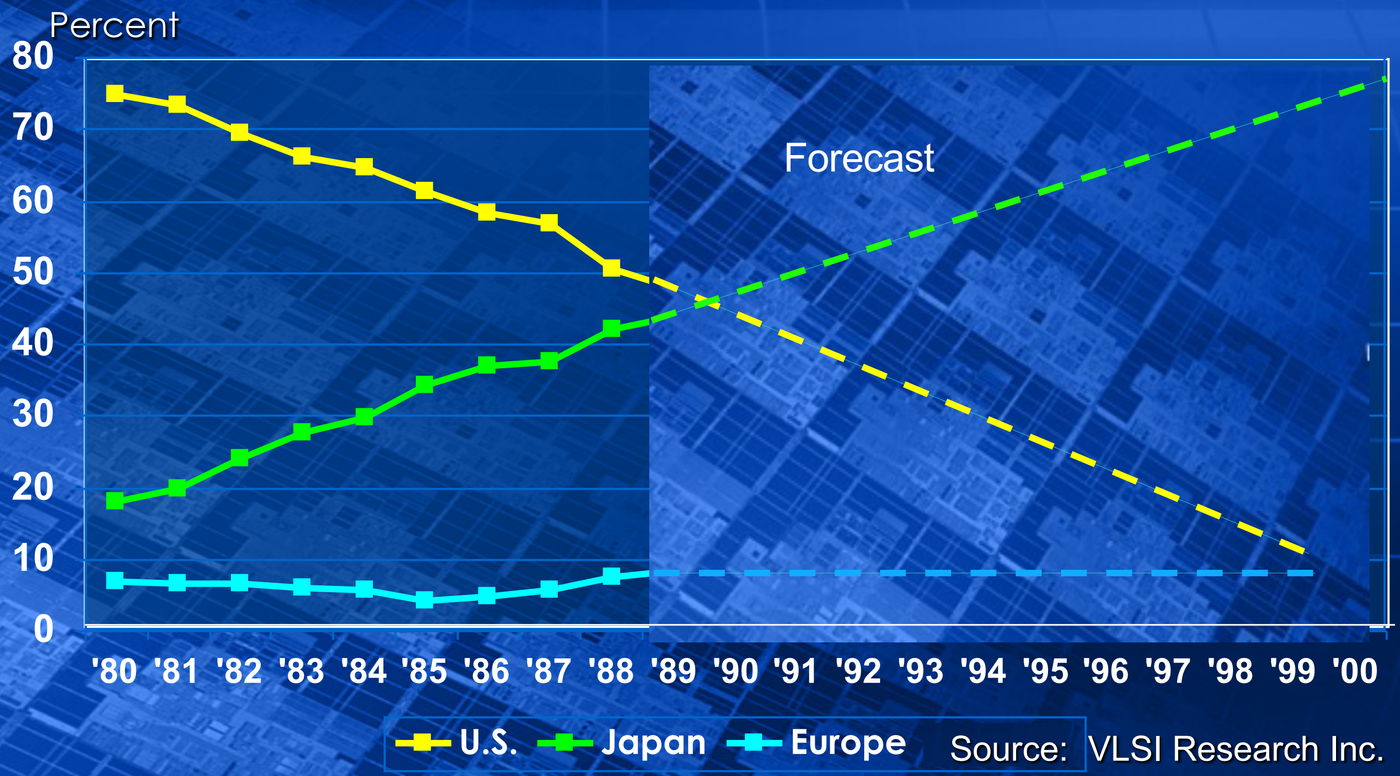
SOURCE: OKI

Second Shocker

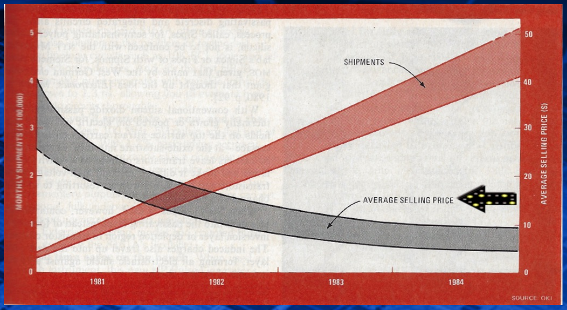
US-Japan Semiconductor Actual Market Share



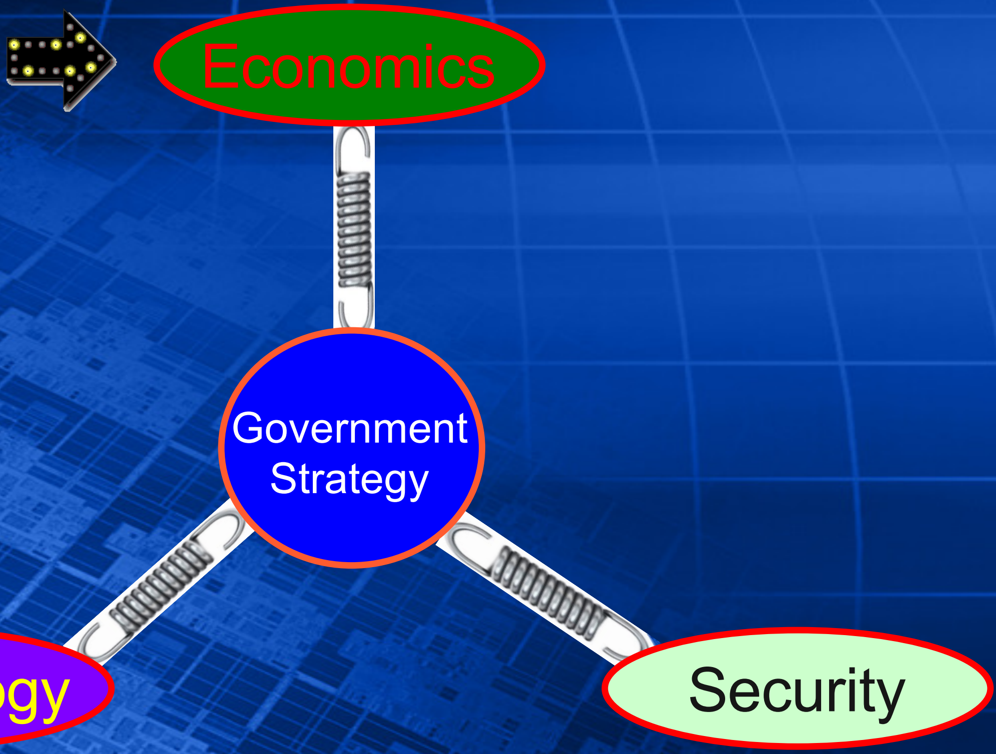
Semiconductor Equipment Market Share



Source: VLSI Research Inc.



SOURCE: OKI



Economics

Government Strategy

Technology

Security

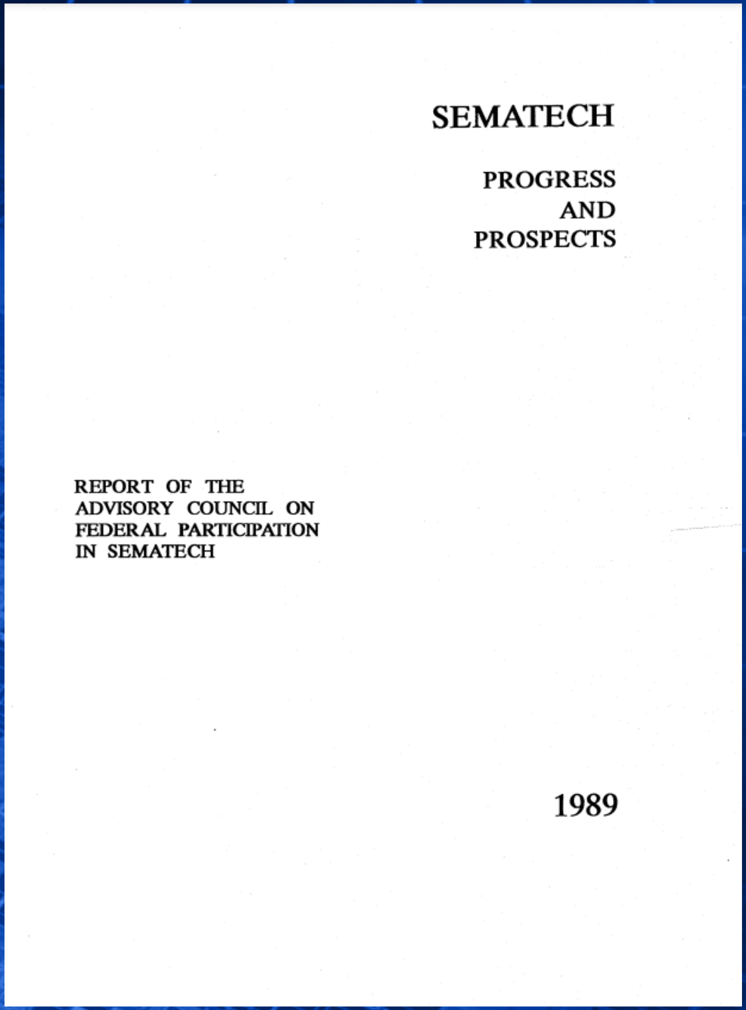
IEEE

NTRS

ITRS

ITRS 2.0

IRDS International Roadmap for Devices and Systems



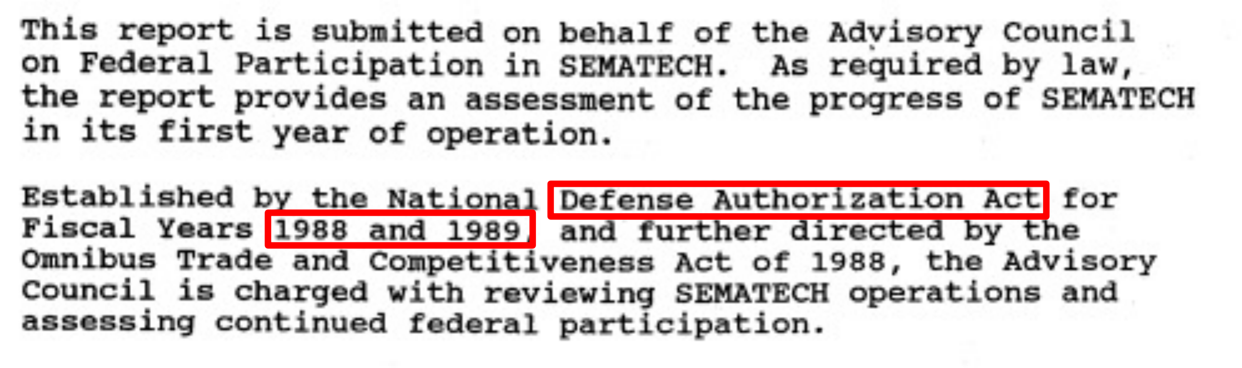
SEMATECH

PROGRESS
AND
PROSPECTS

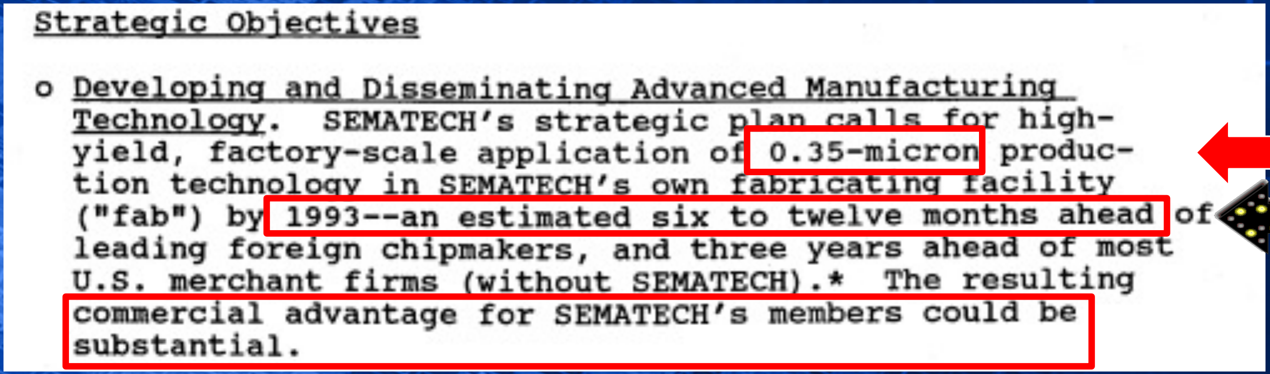
REPORT OF THE
ADVISORY COUNCIL ON
FEDERAL PARTICIPATION
IN SEMATECH

1989

Sematech Objectives


This report is submitted on behalf of the Advisory Council on Federal Participation in SEMATECH. As required by law, the report provides an assessment of the progress of SEMATECH in its first year of operation.

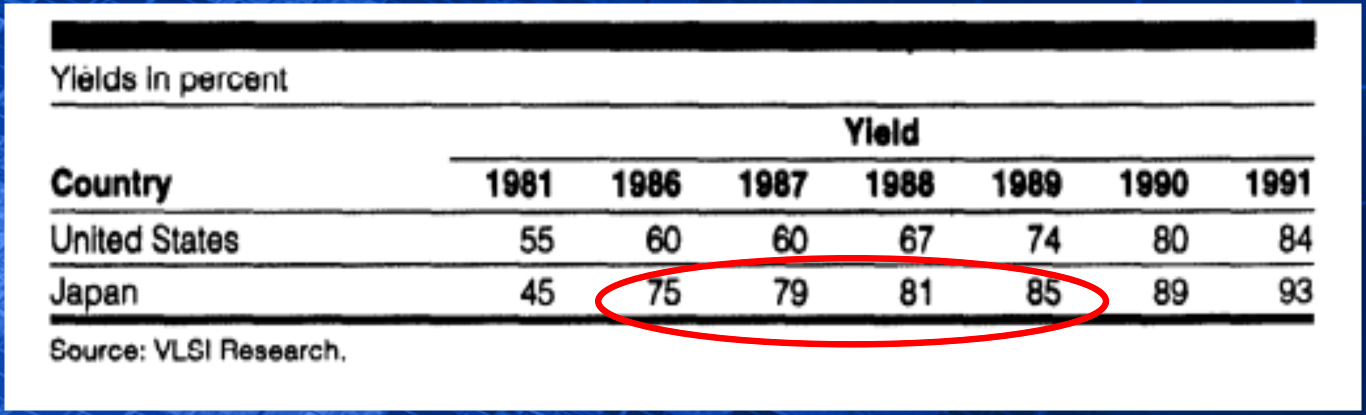
Established by the National Defense Authorization Act for Fiscal Years 1988 and 1989, and further directed by the Omnibus Trade and Competitiveness Act of 1988, the Advisory Council is charged with reviewing SEMATECH operations and assessing continued federal participation.


Strategic Objectives

o Developing and Disseminating Advanced Manufacturing Technology. SEMATECH's strategic plan calls for high-yield, factory-scale application of 0.35-micron production technology in SEMATECH's own fabricating facility ("fab") by 1993--an estimated six to twelve months ahead of leading foreign chipmakers, and three years ahead of most U.S. merchant firms (without SEMATECH).* The resulting commercial advantage for SEMATECH's members could be substantial.

Correct Problem Statement

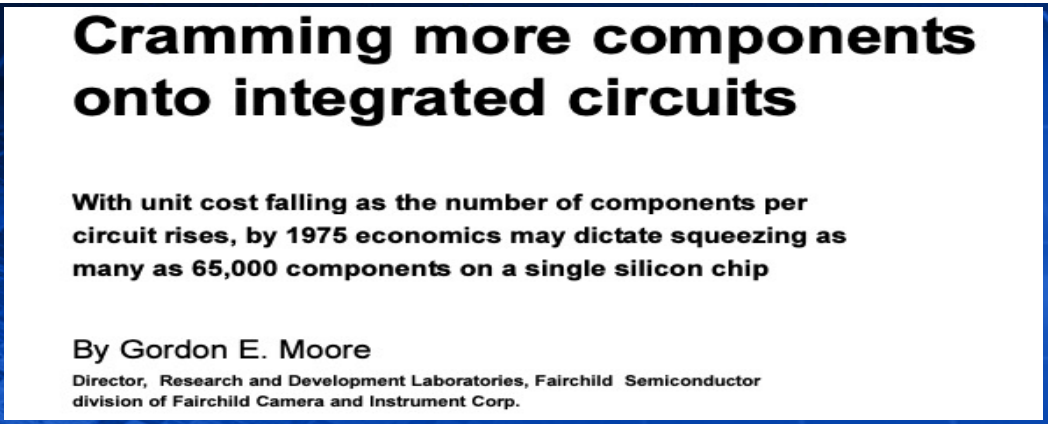
1. US and Japanese companies had at the time the same technology capabilities
2. Japanese equipment was superior in quality, accuracy and reliability to US equipment
3. Manufacturing methods of Japanese companies were superior to US



Yields in percent

	Yield						
Country	**1981**	**1986**	**1987**	**1988**	**1989**	**1990**	**1991**
United States	55	60	60	67	74	80	84
Japan	45	75	79	81	85	89	93

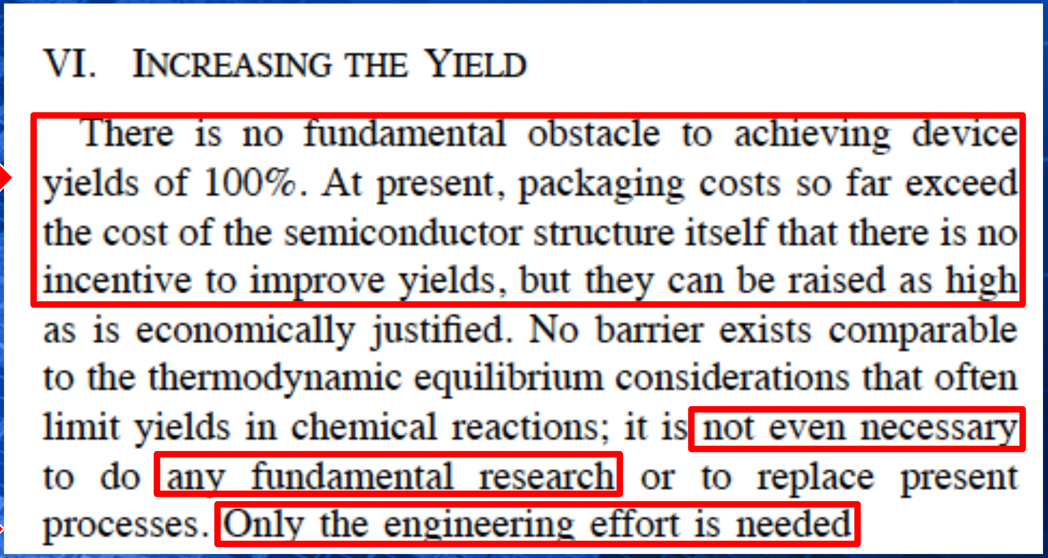
Source: VLSI Research.



Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore
Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.



VI. INCREASING THE YIELD

There is no fundamental obstacle to achieving device yields of 100%. At present, packaging costs so far exceed the cost of the semiconductor structure itself that there is no incentive to improve yields, but they can be raised as high as is economically justified. No barrier exists comparable to the thermodynamic equilibrium considerations that often limit yields in chemical reactions; it is not even necessary to do any fundamental research or to replace present processes. Only the engineering effort is needed

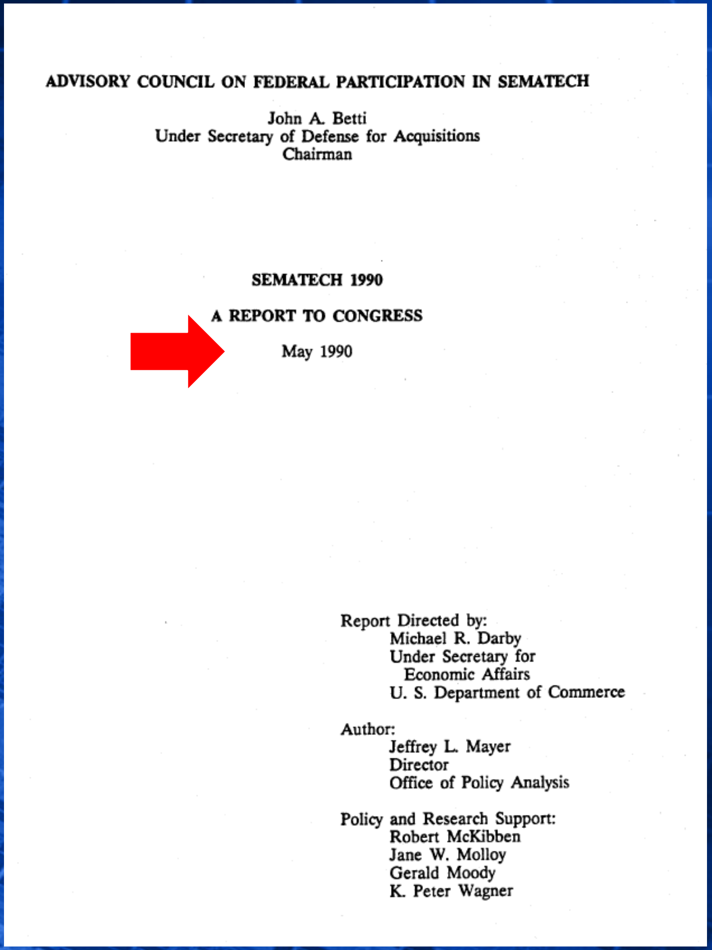
Electronics, Volume 38, Number 8, April 19, 1965

Scaling Continues beyond Imagination

Production	1989	1991	1993	1995	1997	1999
Generation	1.00	0.80	0.50	0.35	0.25	0.18
Gate Length	1.00	0.80	0.50	0.35	0.20	0.13
SRAM Cell	220	111	44	21	10.6	5.6
Power Supply	5.0	5.0	3.3	2.5	1.8	1.5
# Metal	2	3	4	4	5	6

New generation every 2 years

IEEE NTRS ITRS ITRS 2.0 IRDS INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS



ADVISORY COUNCIL ON FEDERAL PARTICIPATION IN SEMATECH

John A. Betti
Under Secretary of Defense for Acquisitions
Chairman

SEMATECH 1990

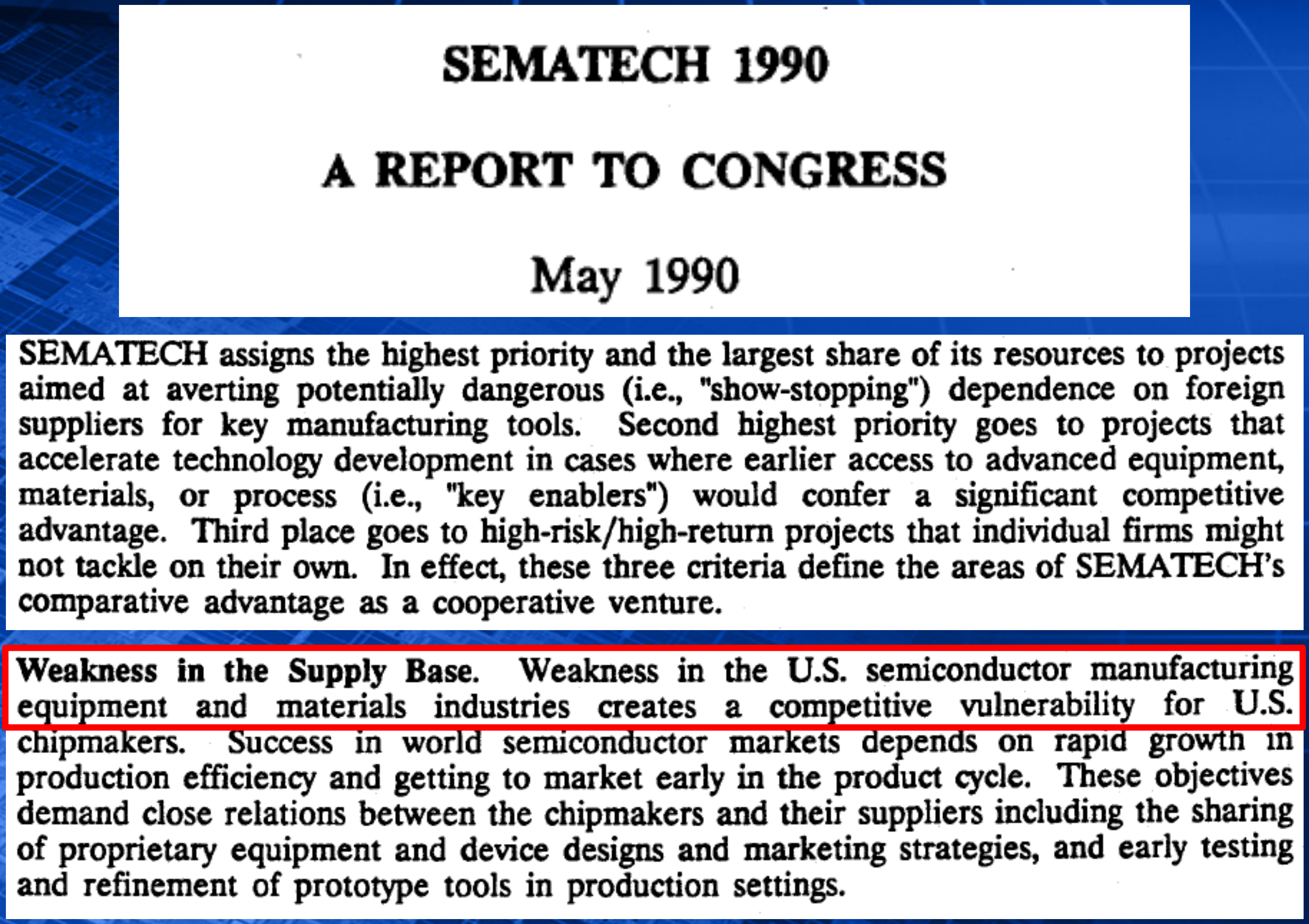
A REPORT TO CONGRESS

May 1990

Report Directed by:
Michael R. Darby
Under Secretary for
Economic Affairs
U. S. Department of Commerce

Author:
Jeffrey L. Mayer
Director
Office of Policy Analysis

Policy and Research Support:
Robert McKibben
Jane W. Molloy
Gerald Moody
K. Peter Wagner



SEMATECH 1990

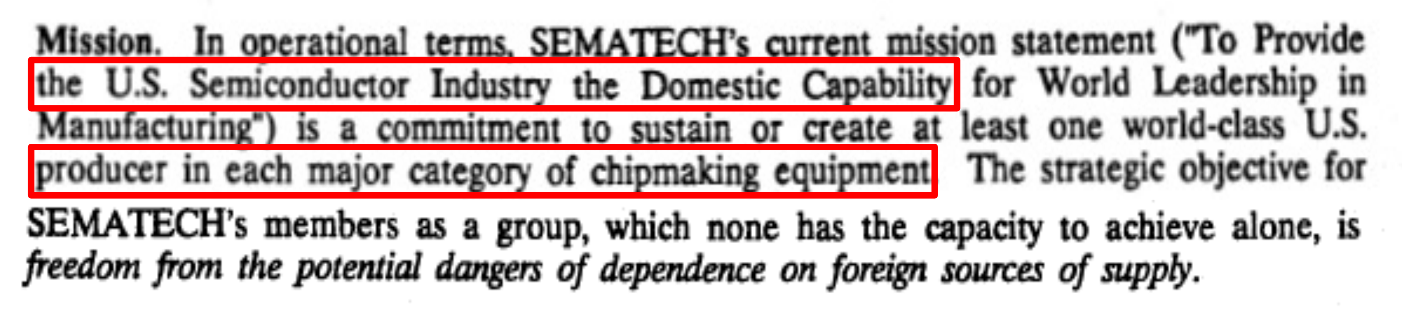
A REPORT TO CONGRESS

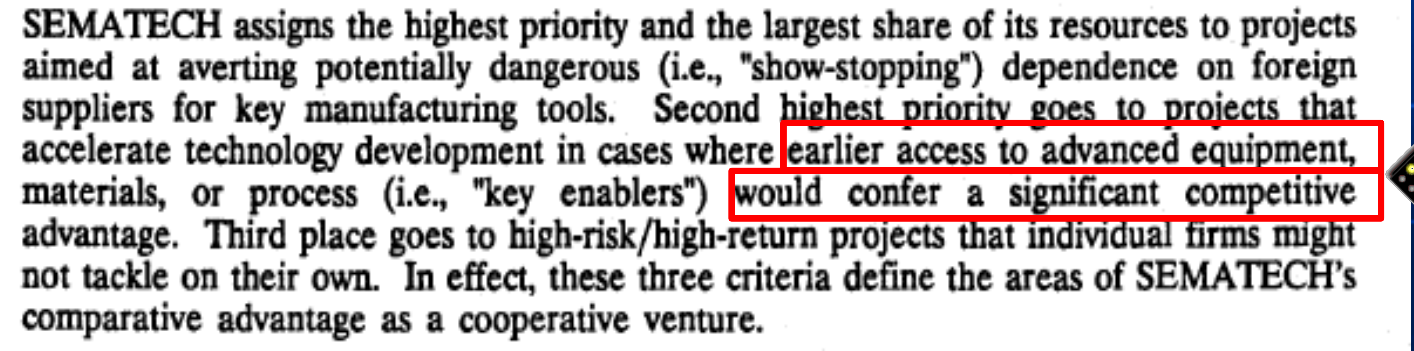
May 1990

SEMATECH assigns the highest priority and the largest share of its resources to projects aimed at averting potentially dangerous (i.e., "show-stopping") dependence on foreign suppliers for key manufacturing tools. Second highest priority goes to projects that accelerate technology development in cases where earlier access to advanced equipment, materials, or process (i.e., "key enablers") would confer a significant competitive advantage. Third place goes to high-risk/high-return projects that individual firms might not tackle on their own. In effect, these three criteria define the areas of SEMATECH's comparative advantage as a cooperative venture.

Weakness in the Supply Base. Weakness in the U.S. semiconductor manufacturing equipment and materials industries creates a competitive vulnerability for U.S. chipmakers. Success in world semiconductor markets depends on rapid growth in production efficiency and getting to market early in the product cycle. These objectives demand close relations between the chipmakers and their suppliers including the sharing of proprietary equipment and device designs and marketing strategies, and early testing and refinement of prototype tools in production settings.

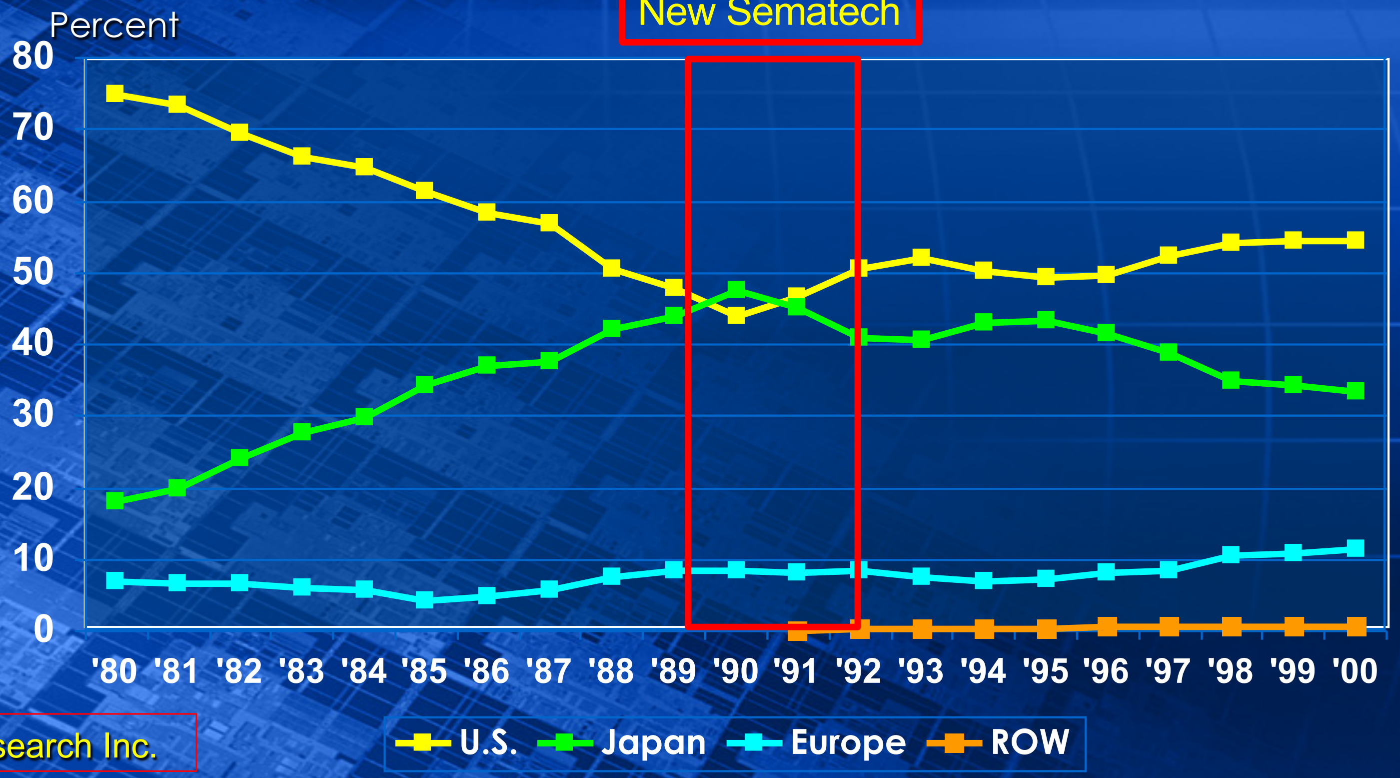
Revised Sematech Mission


Mission. In operational terms, SEMATECH's current mission statement ("To Provide the U.S. Semiconductor Industry the Domestic Capability for World Leadership in Manufacturing") is a commitment to sustain or create at least one world-class U.S. producer in each major category of chipmaking equipment. The strategic objective for SEMATECH's members as a group, which none has the capacity to achieve alone, is *freedom from the potential dangers of dependence on foreign sources of supply*.


SEMATECH assigns the highest priority and the largest share of its resources to projects aimed at averting potentially dangerous (i.e., "show-stopping") dependence on foreign suppliers for key manufacturing tools. Second highest priority goes to projects that accelerate technology development in cases where earlier access to advanced equipment, materials, or process (i.e., "key enablers") would confer a significant competitive advantage. Third place goes to high-risk/high-return projects that individual firms might not tackle on their own. In effect, these three criteria define the areas of SEMATECH's comparative advantage as a cooperative venture.

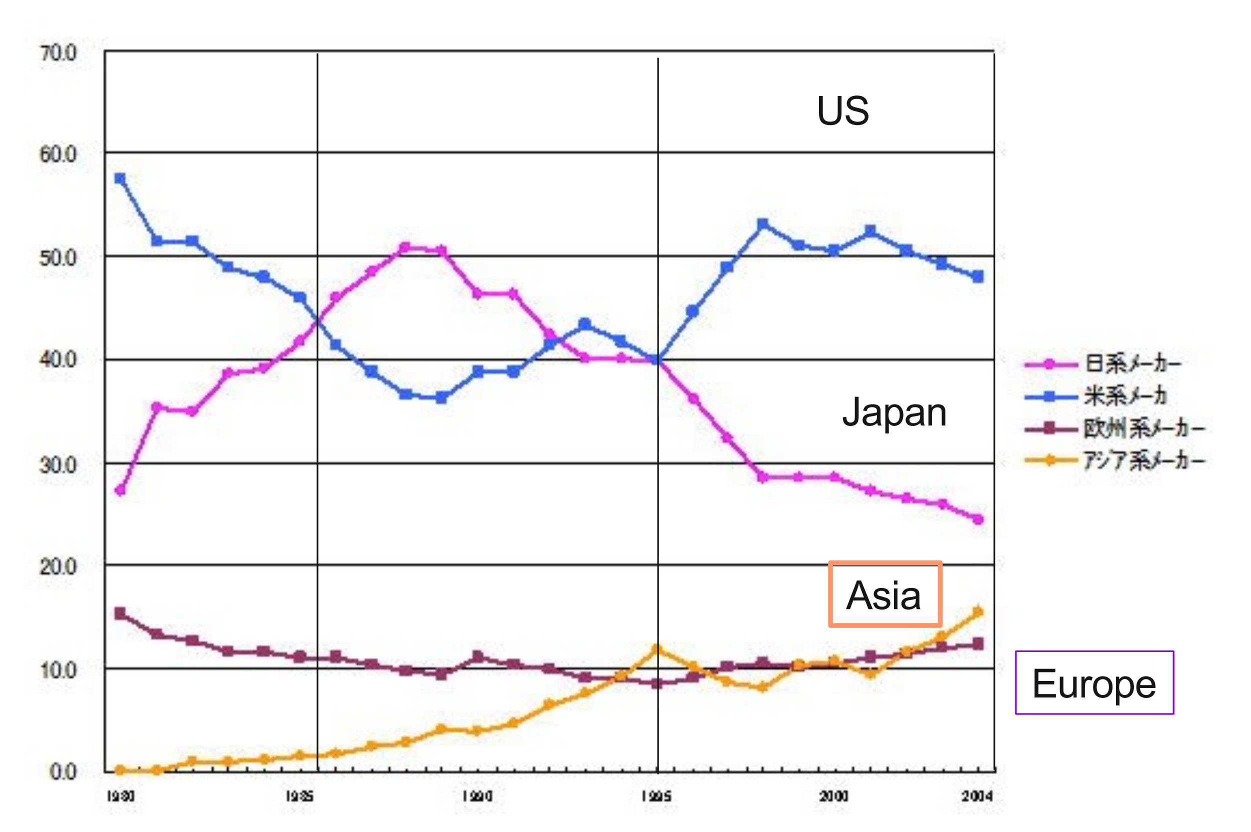
Semiconductor Equipment Market Share

New Sematech

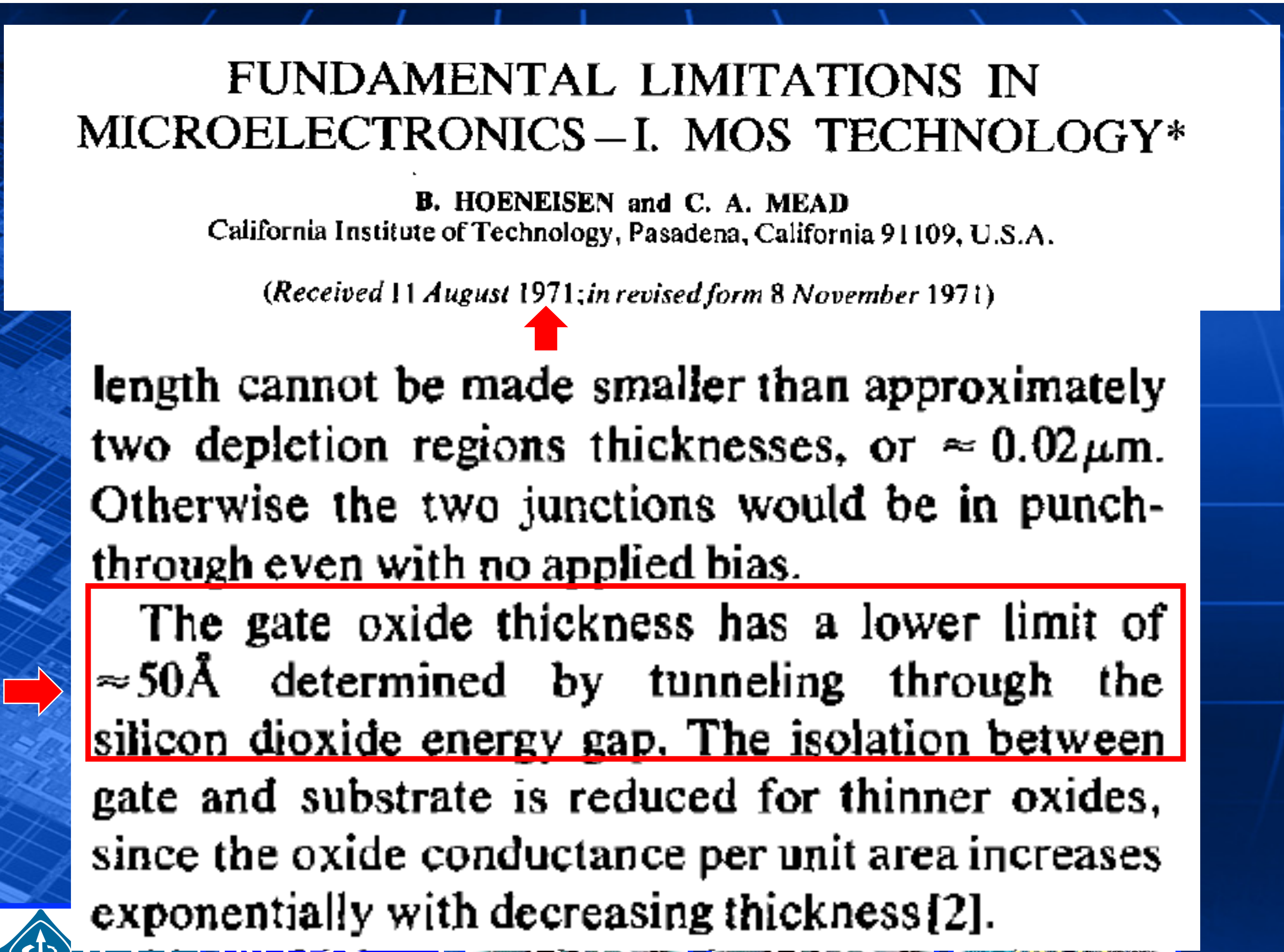


Source: VLSI Research Inc.

Semiconductor Market Share



Third Act



FUNDAMENTAL LIMITATIONS IN MICROELECTRONICS—I. MOS TECHNOLOGY*

B. HOENEISEN and C. A. MEAD
California Institute of Technology, Pasadena, California 91109, U.S.A.

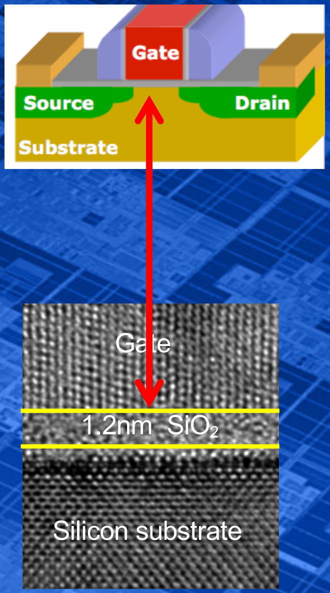
(*Received* 11 *August* 1971; *in revised form* 8 *November* 1971)

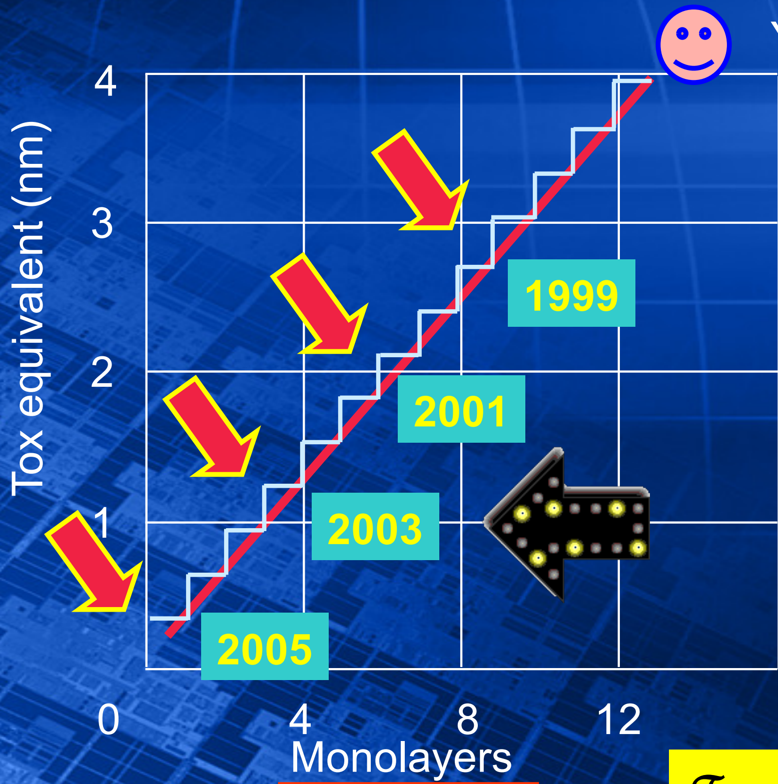
length cannot be made smaller than approximately two depletion regions thicknesses, or ≈ 0.02 μm. Otherwise the two junctions would be in punch-through even with no applied bias.

The gate oxide thickness has a lower limit of ≈50Å determined by tunneling through the silicon dioxide energy gap. The isolation between gate and substrate is reduced for thinner oxides, since the oxide conductance per unit area increases exponentially with decreasing thickness[2].

Third Shocker

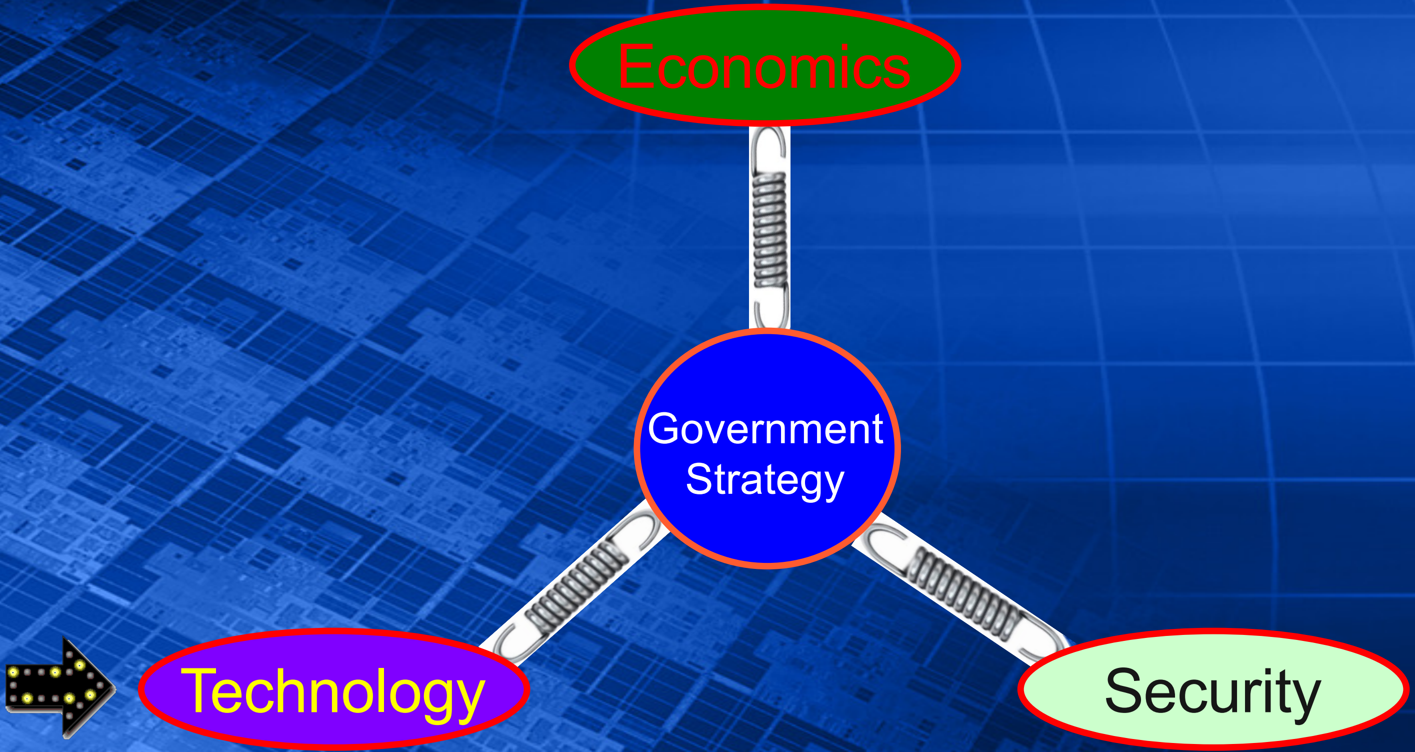
Gate Dielectric Scaling





1997 NTRS

From My Files



Economics

Government Strategy

Technology

Security

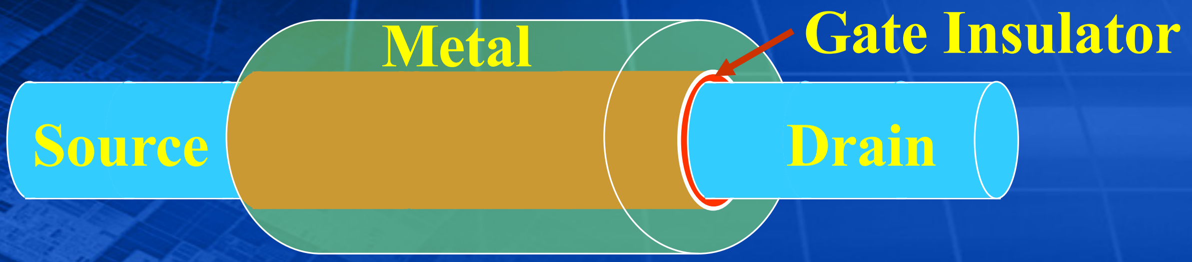
ITRS 1.0

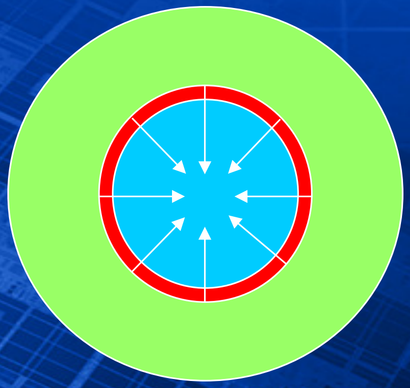
Europe **Japan** **Korea** **Taiwan** **USA**

International Technology Roadmap for Semiconductors

1998

The Ideal MOS Transistor





Fully Surrounding Metal Electrode

Fully Enclosed, Depleted Semiconductor

High-K Gate Insulator

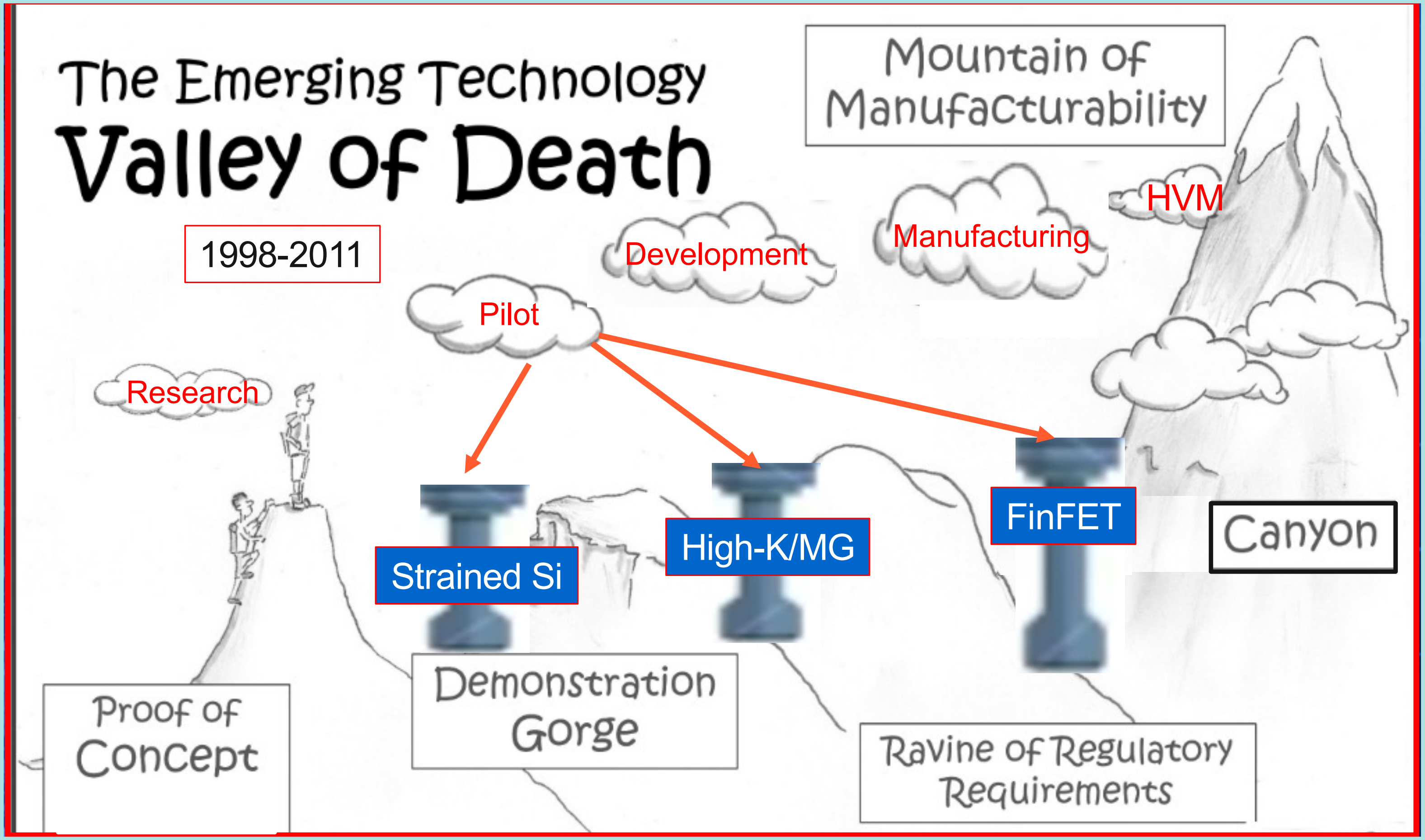
Low Resistance Source/Drain

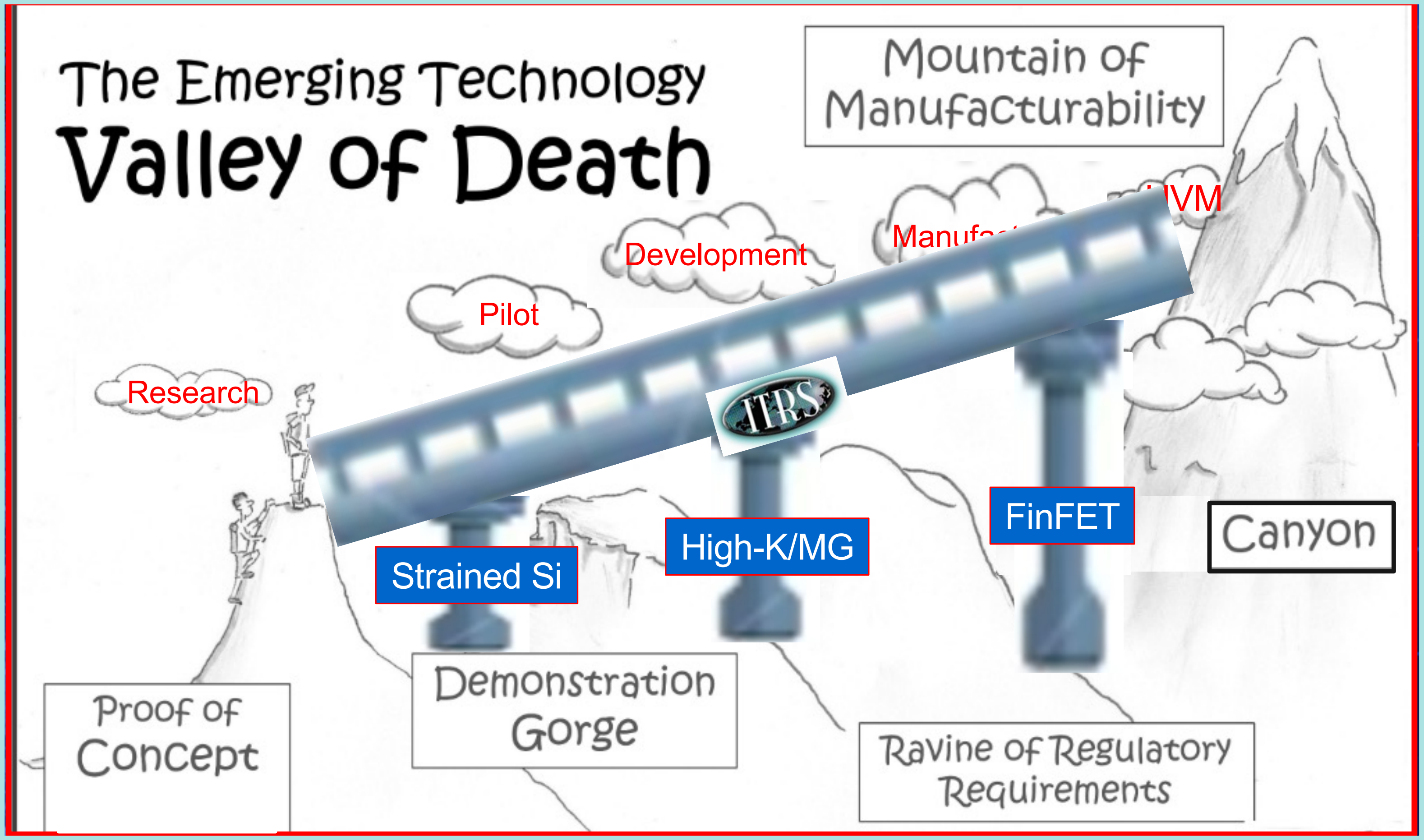
Band Engineered Semiconductor

From My Files

IEEE NTRS ITRS ITRS 2.0 IRDS International Roadmap for Devices and Systems

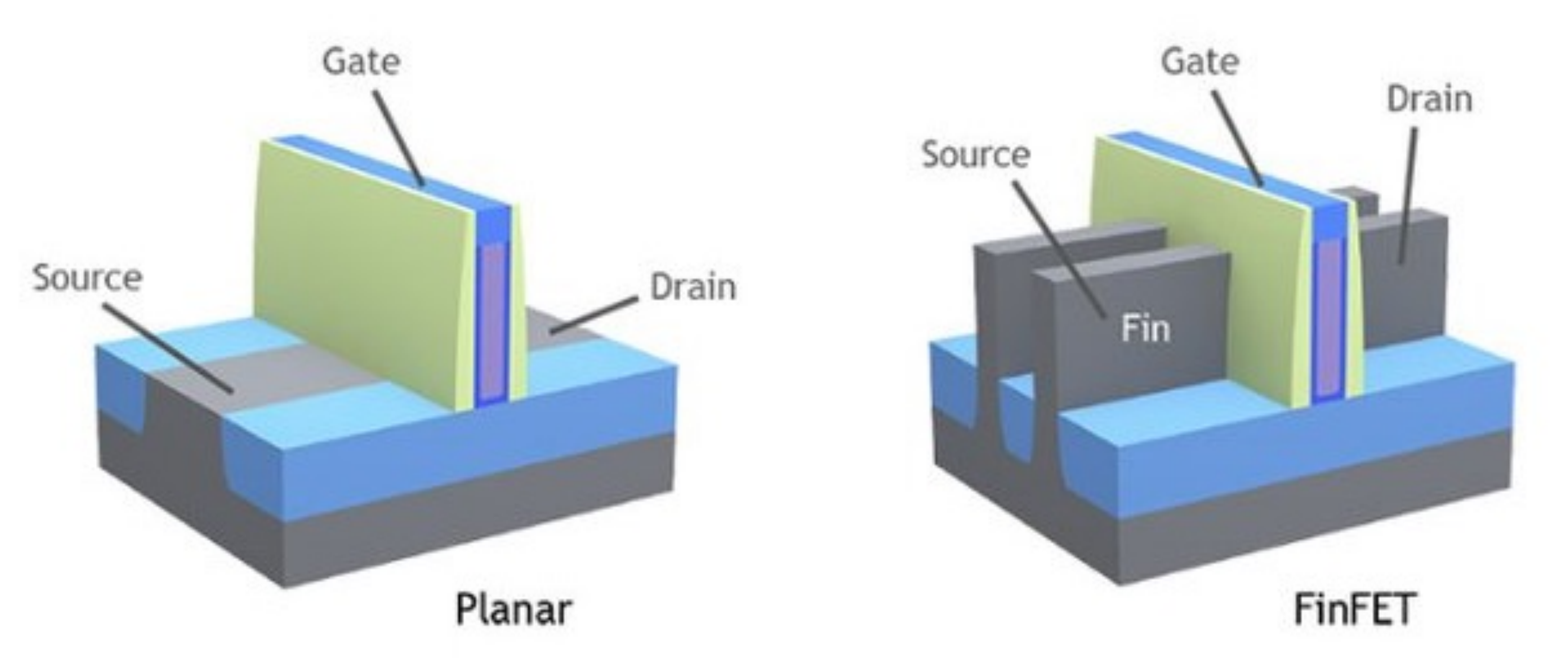
The Emerging Technology Valley of Death




The Emerging Technology
Valley of Death
Mountain of Manufacturability
VM
Manufac
Development
Pilot
Research
ITRS
FinFET
Canyon
High-K/MG
Strained Si
Demonstration Gorge
Proof of Concept
Ravine of Regulatory Requirements

Fourth Act

1965-2011: From Planar Transistor to FinFET



IRDS

IRDS

INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS

http://irds.ieee.org/

IEEE

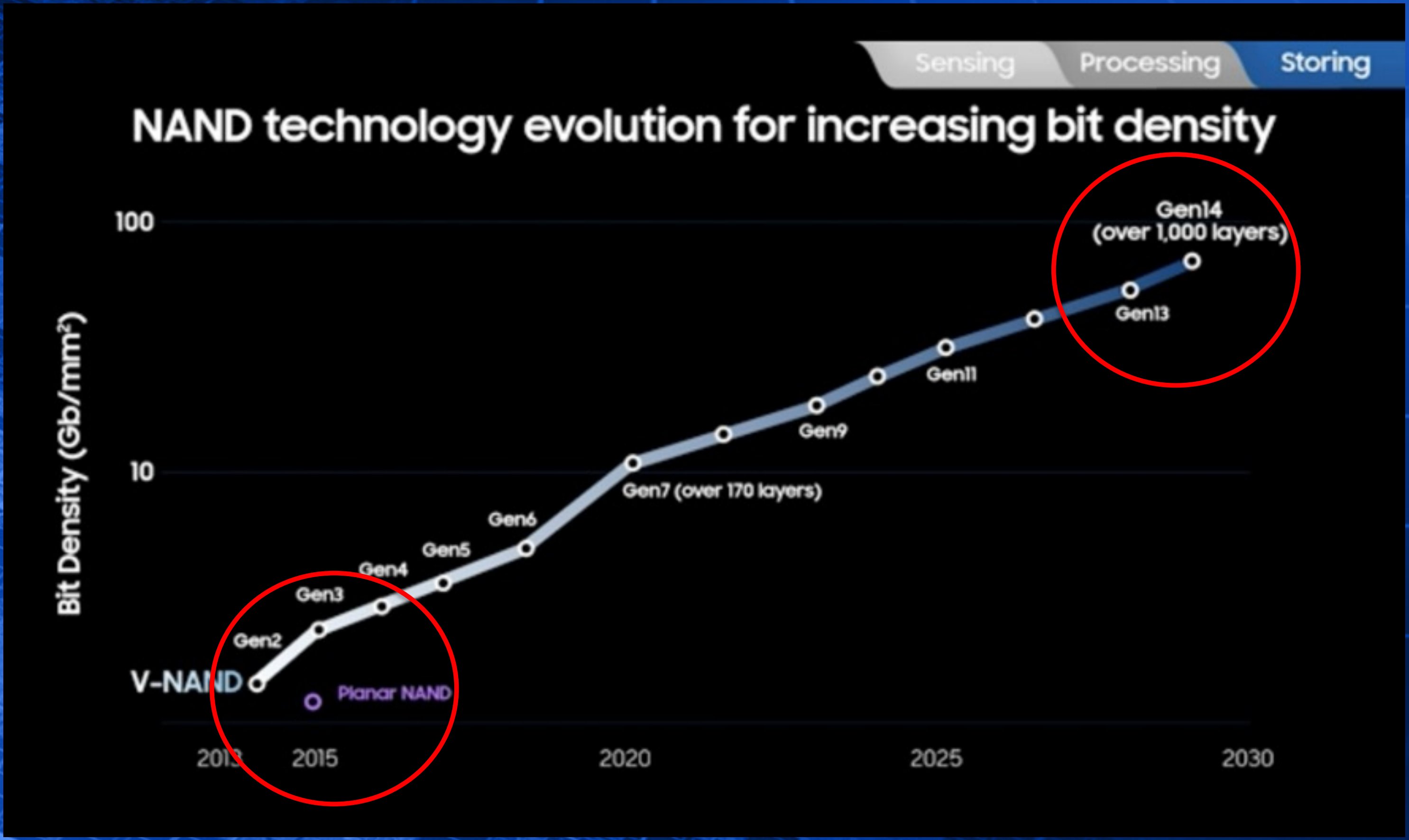
3D Power Scaling

2015->2025-2040

↑ MEMORY

↑ LOGIC

Samsung, IEDM 2021



NAND technology evolution for increasing bit density

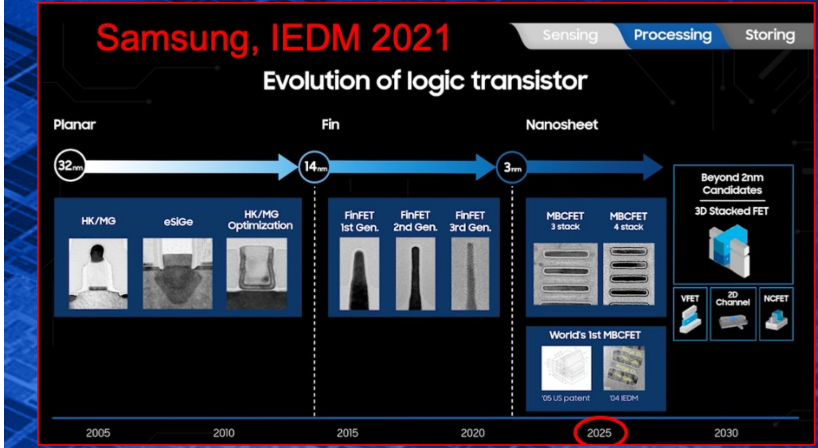
3D Power Scaling

2015->2025-2040

MEMORY

LOGIC

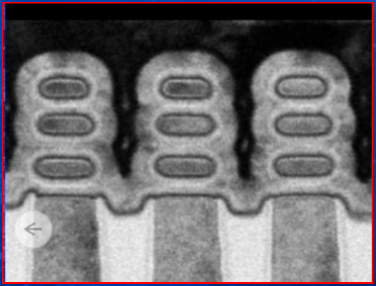
Gate All Around (GAA) by nanosheets technology in 2025

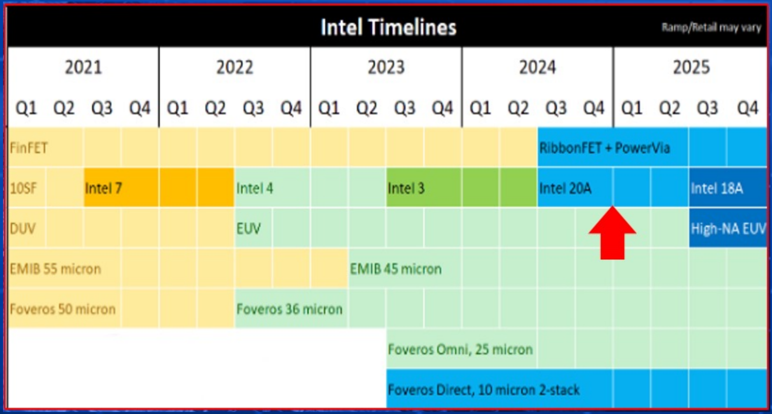


Samsung, IEDM 2021

Sensing Processing Storing

Evolution of logic transistor

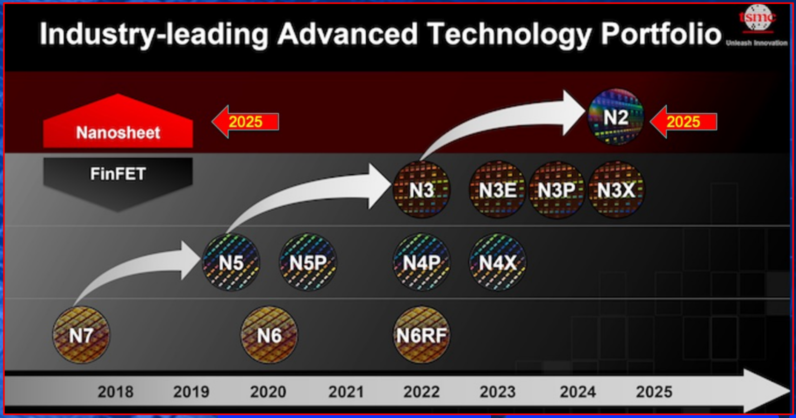




Intel Timelines

Ramp/Retail may vary

2021				2022				2023				2024				2025			
Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4	Q1	Q2	Q3	Q4
FinFET														RibbonFET + PowerVia					
10SF		Intel 7				Intel 4				Intel 3				Intel 20A				Intel 18A	
DUV						EUV												High-NA EUV	
EMIB 55 micron									EMIB 45 micron										
Foveros 50 micron						Foveros 36 micron													
										Foveros Omni, 25 micron									
										Foveros Direct, 10 micron 2-stack									

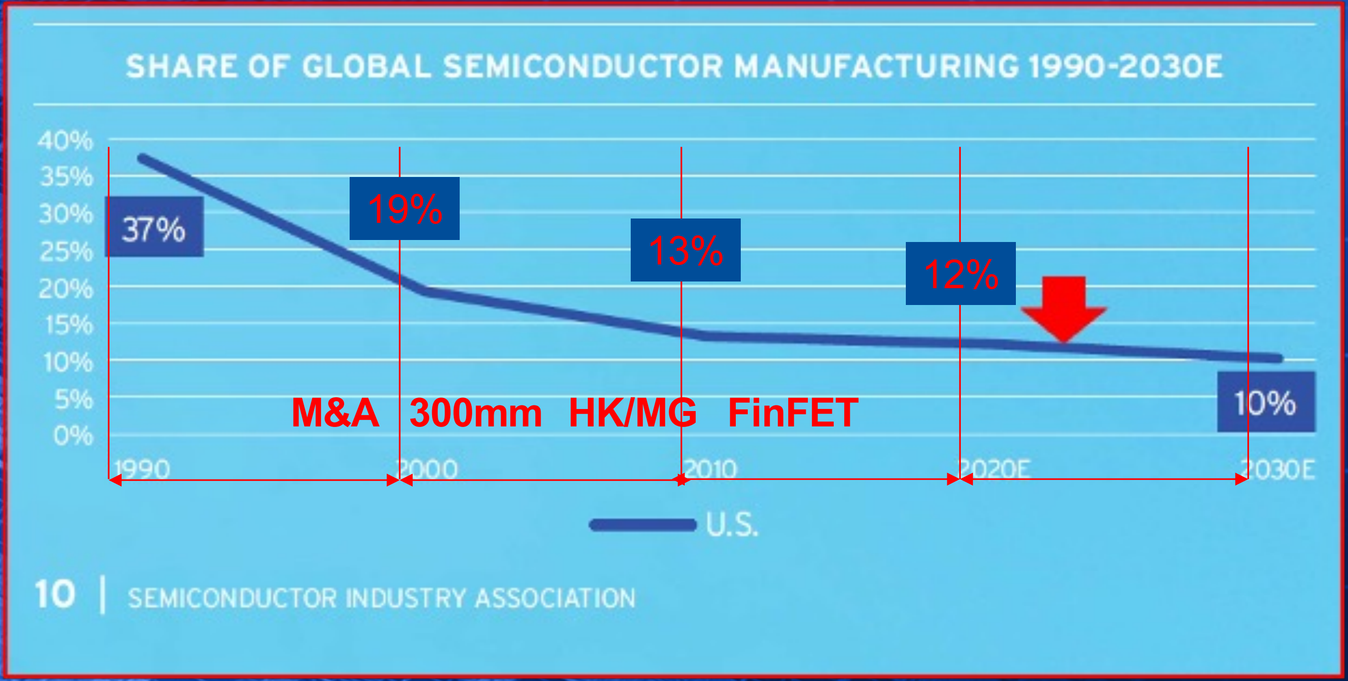


Industry-leading Advanced Technology Portfolio

Fourth Shocker

January 2020

Semiconductor Manufacturing Investments in US



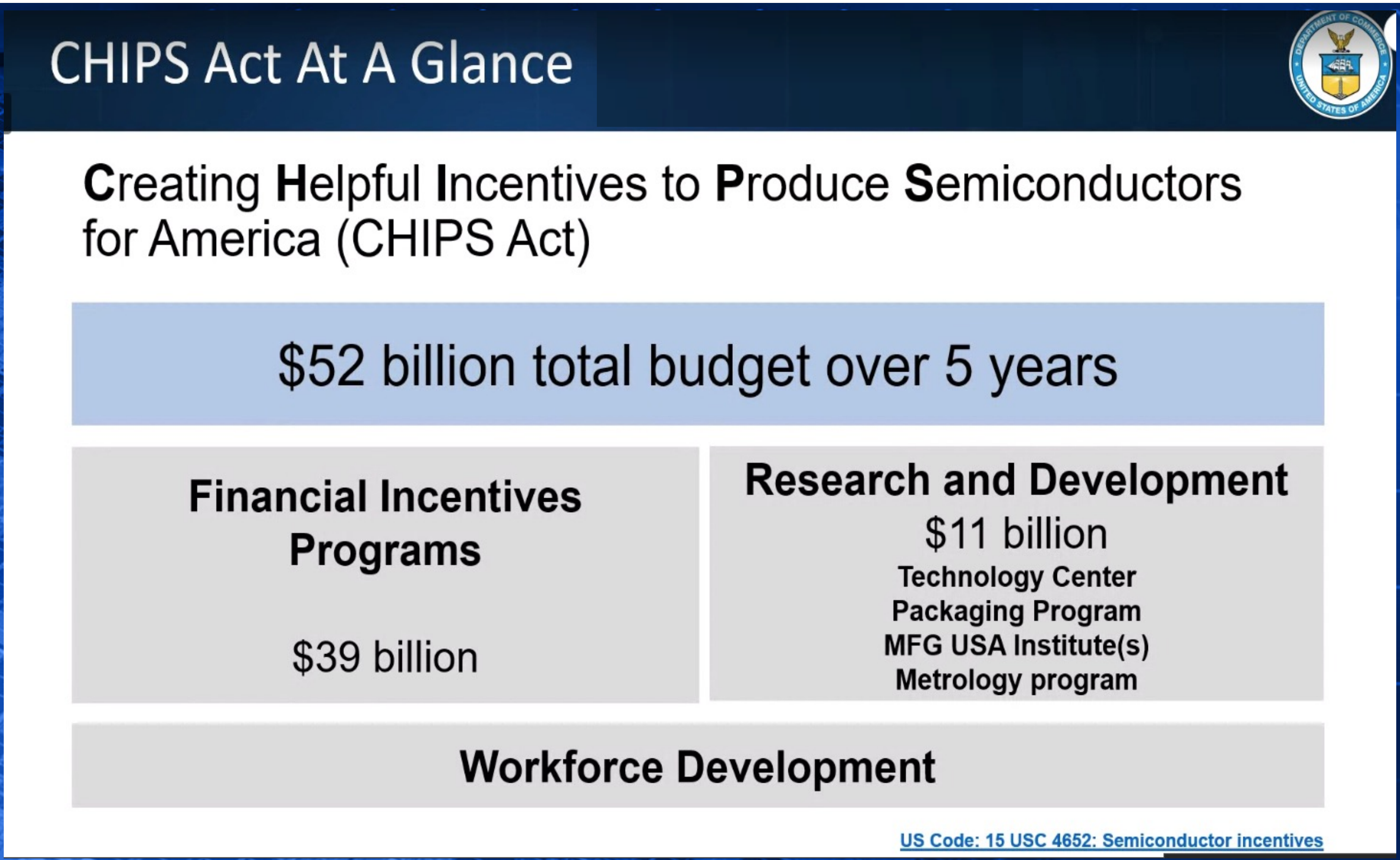
Economics

Government Strategy

Technology

Security

CHIPS
for AMERICA



CHIPS Act At A Glance

Creating **H**elpful **I**ncentives to **P**roduce **S**emiconductors for America (CHIPS Act)

$52 billion total budget over 5 years

Financial Incentives Programs

$39 billion

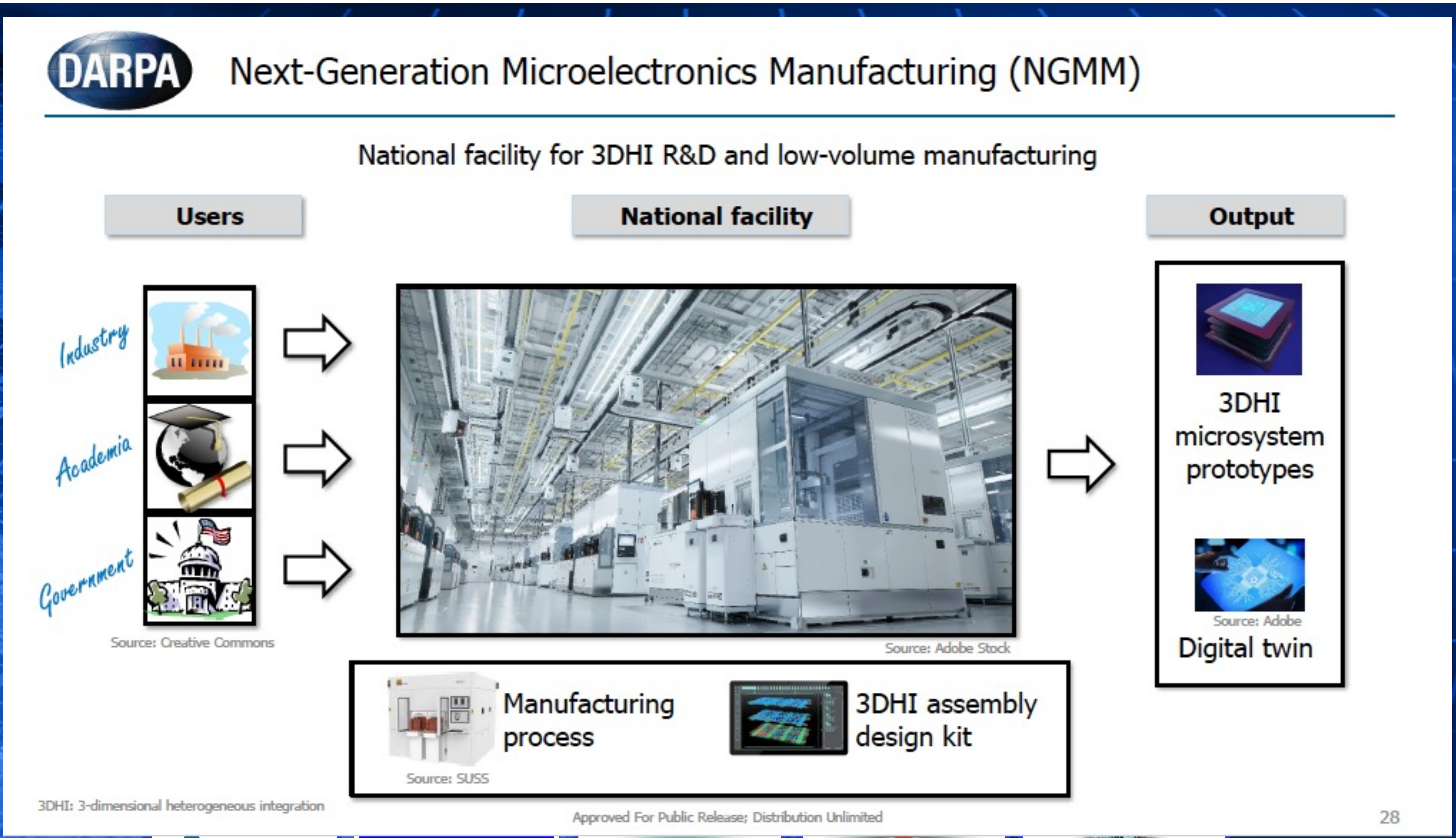
Research and Development

$11 billion

Technology Center
Packaging Program
MFG USA Institute(s)
Metrology program

Workforce Development

US Code: 15 USC 4652: Semiconductor incentives



Next-Generation Microelectronics Manufacturing (NGMM)

National facility for 3DHI R&D and low-volume manufacturing

Users

National facility

Output

Industry

Academia

Government

Source: Creative Commons

Source: Adobe Stock

3DHI microsystem prototypes

Source: Adobe

Digital twin

Manufacturing process

Source: SUSS

3DHI assembly design kit

3DHI: 3-dimensional heterogeneous integration

Approved For Public Release; Distribution Unlimited

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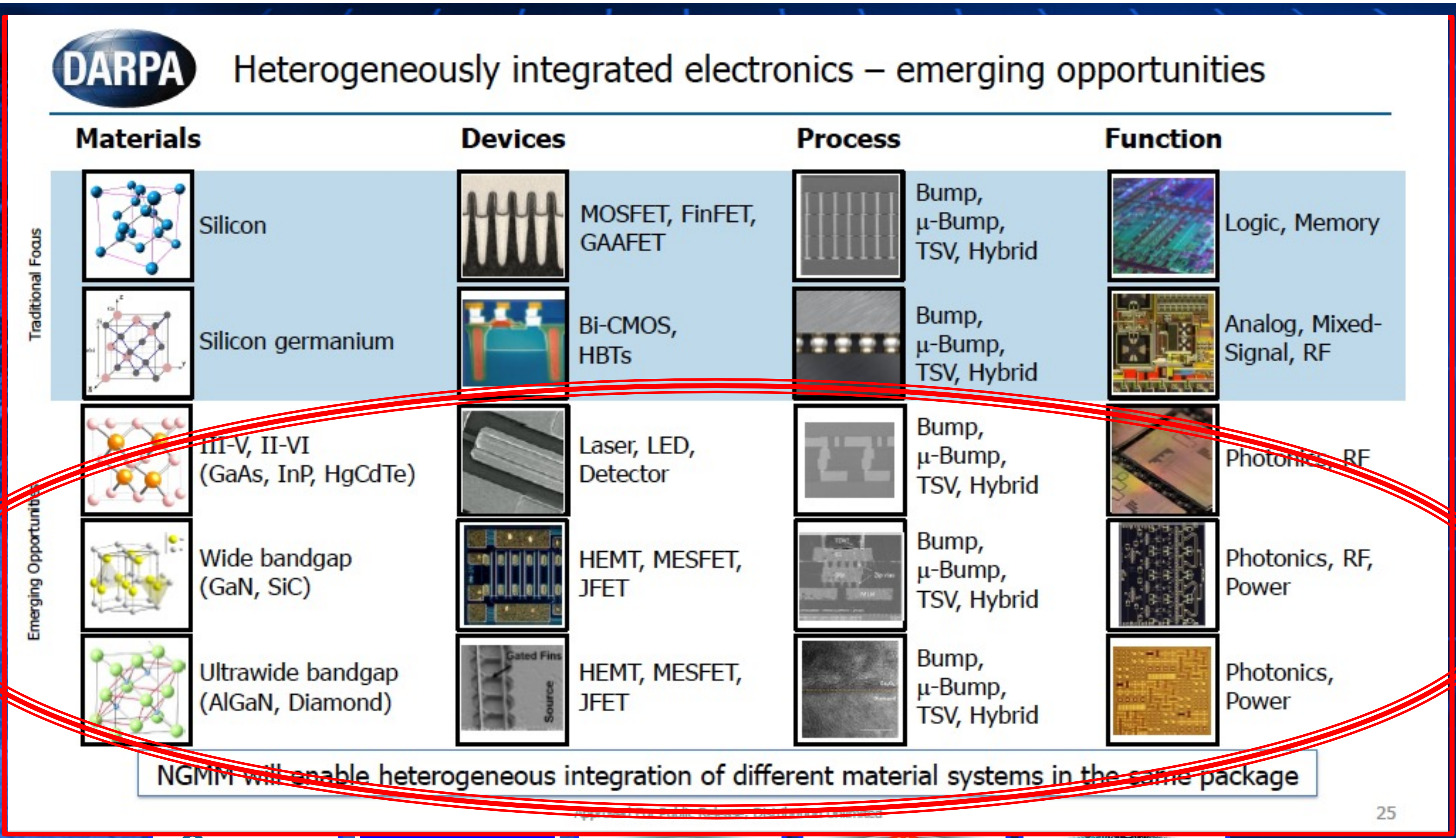
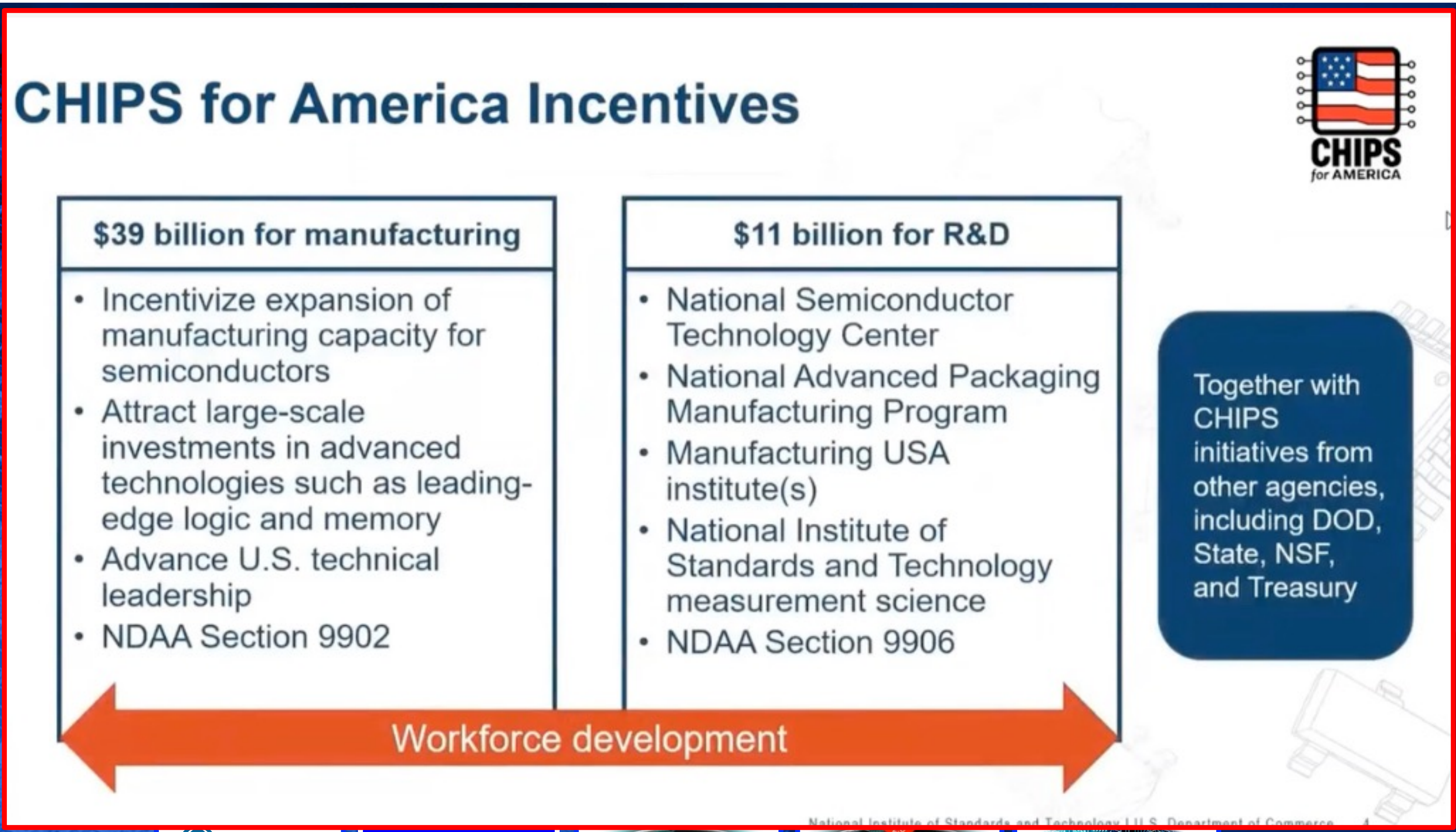


Heterogeneously integrated electronics – emerging opportunities

	Materials	Devices	Process	Function
Traditional Focus	Silicon	MOSFET, FinFET, GAAFET	Bump, μ-Bump, TSV, Hybrid	Logic, Memory
	Silicon germanium	Bi-CMOS, HBTs	Bump, μ-Bump, TSV, Hybrid	Analog, Mixed-Signal, RF
Emerging Opportunities	III-V, II-VI (GaAs, InP, HgCdTe)	Laser, LED, Detector	Bump, μ-Bump, TSV, Hybrid	Photonics, RF
	Wide bandgap (GaN, SiC)	HEMT, MESFET, JFET	Bump, μ-Bump, TSV, Hybrid	Photonics, RF, Power
	Ultrawide bandgap (AlGaN, Diamond)	HEMT, MESFET, JFET	Bump, μ-Bump, TSV, Hybrid	Photonics, Power

NGMM will enable heterogeneous integration of different material systems in the same package



CHIPS for America Incentives

$39 billion for manufacturing

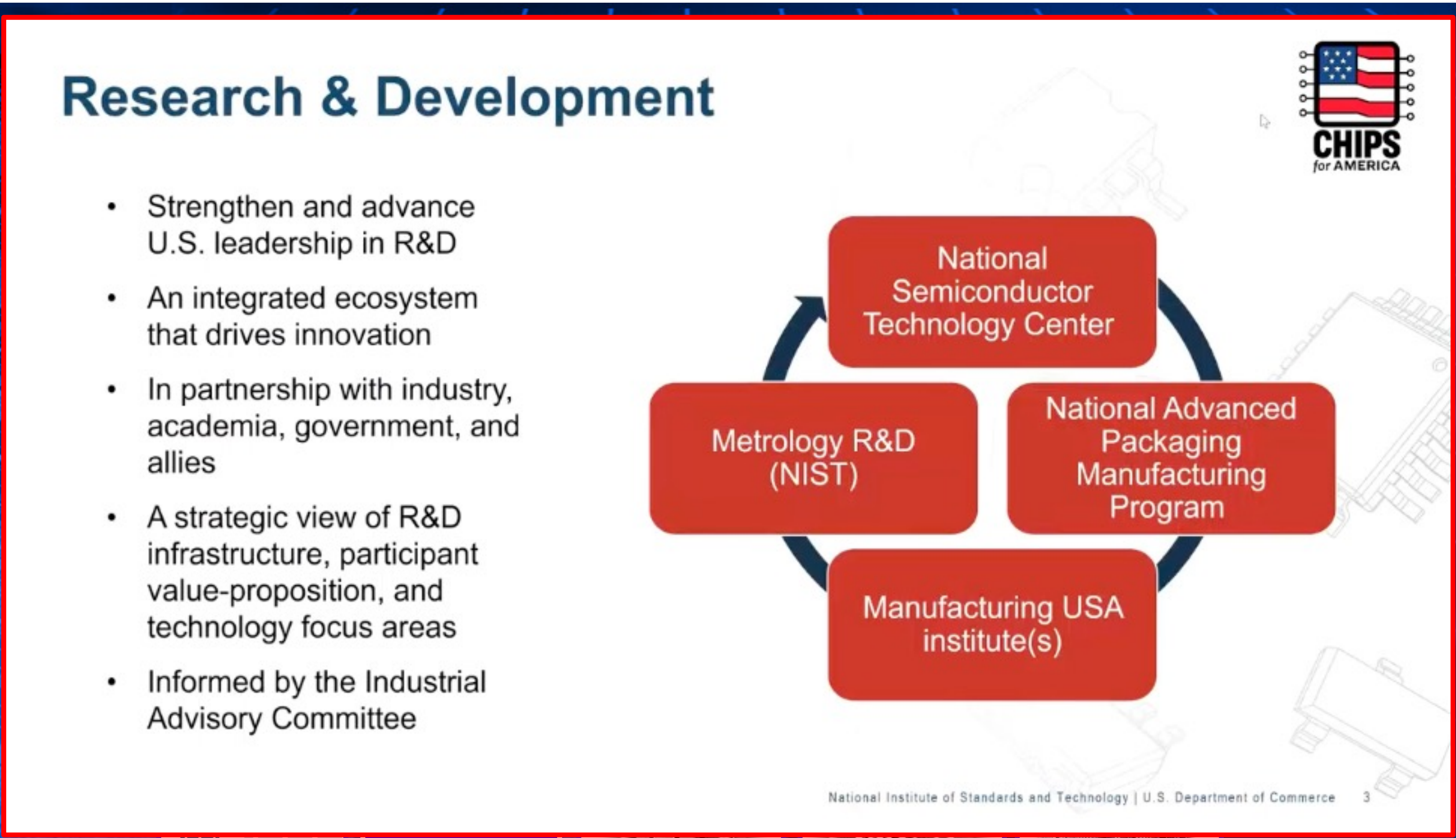
- Incentivize expansion of manufacturing capacity for semiconductors
- Attract large-scale investments in advanced technologies such as leading-edge logic and memory
- Advance U.S. technical leadership
- NDAA Section 9902

$11 billion for R&D

- National Semiconductor Technology Center
- National Advanced Packaging Manufacturing Program
- Manufacturing USA institute(s)
- National Institute of Standards and Technology measurement science
- NDAA Section 9906

Workforce development

Together with CHIPS initiatives from other agencies, including DOD, State, NSF, and Treasury



Research & Development

- Strengthen and advance U.S. leadership in R&D
- An integrated ecosystem that drives innovation
- In partnership with industry, academia, government, and allies
- A strategic view of R&D infrastructure, participant value-proposition, and technology focus areas
- Informed by the Industrial Advisory Committee

National Semiconductor Technology Center

Metrology R&D (NIST)

National Advanced Packaging Manufacturing Program

Manufacturing USA institute(s)

National Institute of Standards and Technology | U.S. Department of Commerce 3

National Semiconductor Technology Center

CHIPS for AMERICA

Vision: Will serve as the **focal point** for research and engineering throughout the semiconductor ecosystem, advancing and enabling disruptive innovation to provide U.S. leadership in the industries of the future.

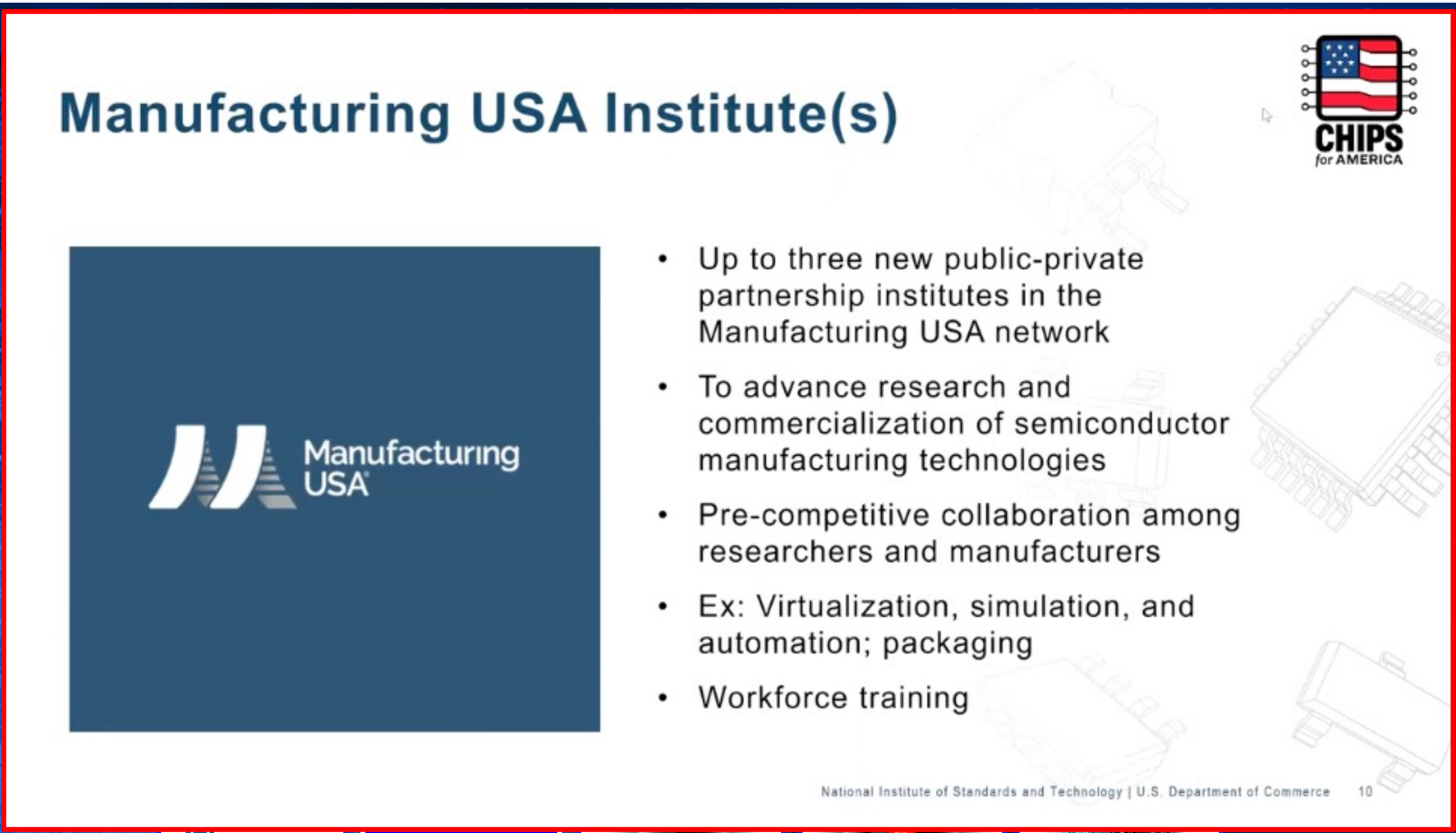
Structure: A public-private consortium as an independent entity with a governing board informed and advised by industry, academia, government, and key stakeholders.

National Institute of Standards and Technology | U.S. Department of Commerce 6

National Advanced Packaging Manufacturing Program

CHIPS for AMERICA

- Strengthen semiconductor advanced test, assembly, and packaging capability in the domestic ecosystem
- Leverage public-private partnerships, that can include support for facilities managed by the NSTC and MUSA
- Broad range of technologies:
    - Heterogeneous integration
    - Wafer and panel-based approaches
    - Tooling and automation
    - Substrate technology



Manufacturing USA Institute(s)

- Up to three new public-private partnership institutes in the Manufacturing USA network
- To advance research and commercialization of semiconductor manufacturing technologies
- Pre-competitive collaboration among researchers and manufacturers
- Ex: Virtualization, simulation, and automation; packaging
- Workforce training

NIST Metrology R&D

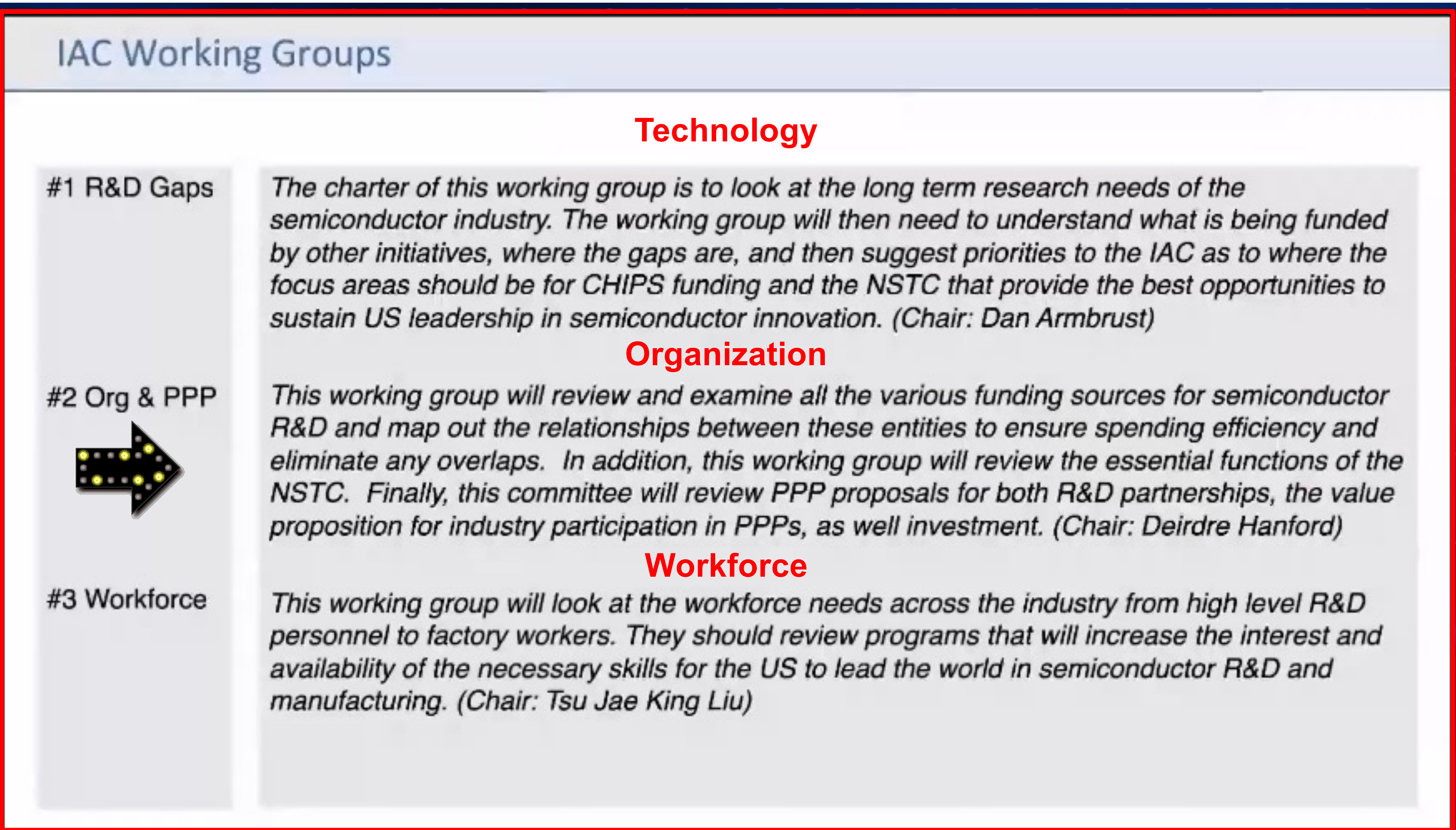
Strategic Opportunities for U.S. Semiconductor Manufacturing

Facilitating U.S. Leadership and Competitiveness through Advancements in Measurements and Standards

August 2022

- Measurement science for new materials and packaging
- Physical metrology for next-generation microelectronics
- Computation and data
- Virtualization and automation
- Reference materials and data, and calibrations
- Standards for processes, cybersecurity, and test methods

National Institute of Standards and Technology | U.S. Department of Commerce 13



IAC Working Groups

Technology

#1 R&D Gaps

The charter of this working group is to look at the long term research needs of the semiconductor industry. The working group will then need to understand what is being funded by other initiatives, where the gaps are, and then suggest priorities to the IAC as to where the focus areas should be for CHIPS funding and the NSTC that provide the best opportunities to sustain US leadership in semiconductor innovation. (Chair: Dan Armbrust)

Organization

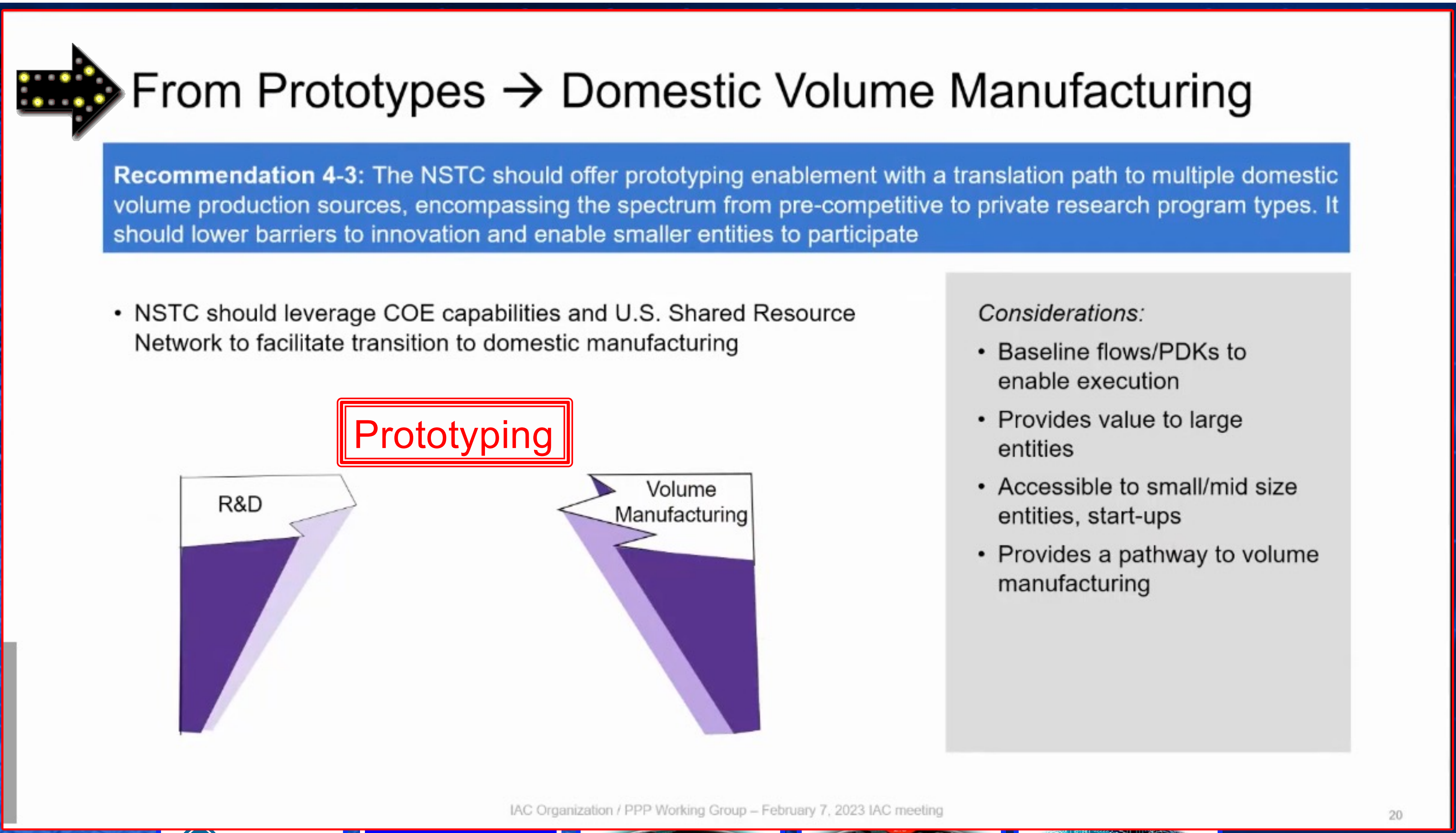
#2 Org & PPP ➡

This working group will review and examine all the various funding sources for semiconductor R&D and map out the relationships between these entities to ensure spending efficiency and eliminate any overlaps. In addition, this working group will review the essential functions of the NSTC. Finally, this committee will review PPP proposals for both R&D partnerships, the value proposition for industry participation in PPPs, as well investment. (Chair: Deirdre Hanford)

Workforce

#3 Workforce

This working group will look at the workforce needs across the industry from high level R&D personnel to factory workers. They should review programs that will increase the interest and availability of the necessary skills for the US to lead the world in semiconductor R&D and manufacturing. (Chair: Tsu Jae King Liu)



From Prototypes → Domestic Volume Manufacturing

Recommendation 4-3: The NSTC should offer prototyping enablement with a translation path to multiple domestic volume production sources, encompassing the spectrum from pre-competitive to private research program types. It should lower barriers to innovation and enable smaller entities to participate

- NSTC should leverage COE capabilities and U.S. Shared Resource Network to facilitate transition to domestic manufacturing

Considerations:

- Baseline flows/PDKs to enable execution
- Provides value to large entities
- Accessible to small/mid size entities, start-ups
- Provides a pathway to volume manufacturing

Proposal

NSTC Sustainable Business Model

Lesson from Act 1

Recommendation 4-2: The NSTC should develop a sustainable business model, with increased funding by industry over time. Government funding should provide risk capital to facilitate broad participation of firms and research institutions of all sizes and means

- Industry and Government must **co-invest for the long term** to ensure sustainability and ongoing success

Lesson from Act 1

Funding model based on insights provided by Dr. Paolo Gargini

Considerations:

- Successful PPPs strike a good **balance** between Industry and Government investment
- Sustained government investment ensures **broad access** (start-ups, universities, small businesses) and increased **risk tolerance**
- Sustained Industry investment ensures **relevance and evergreen capabilities**
- Compared organizational models IMEC, SRC, SEMATECH, etc.

IAC Organization PPP Working Group – February 7, 2023 IAC meeting

NSTC PPP Organization

Proposal

Recommendation 4-1: The NSTC should be a leading and convening public private partnership, led by an independent CEO reporting to a fiduciary board, with the advice of a Technical Advisory Board (TAB).

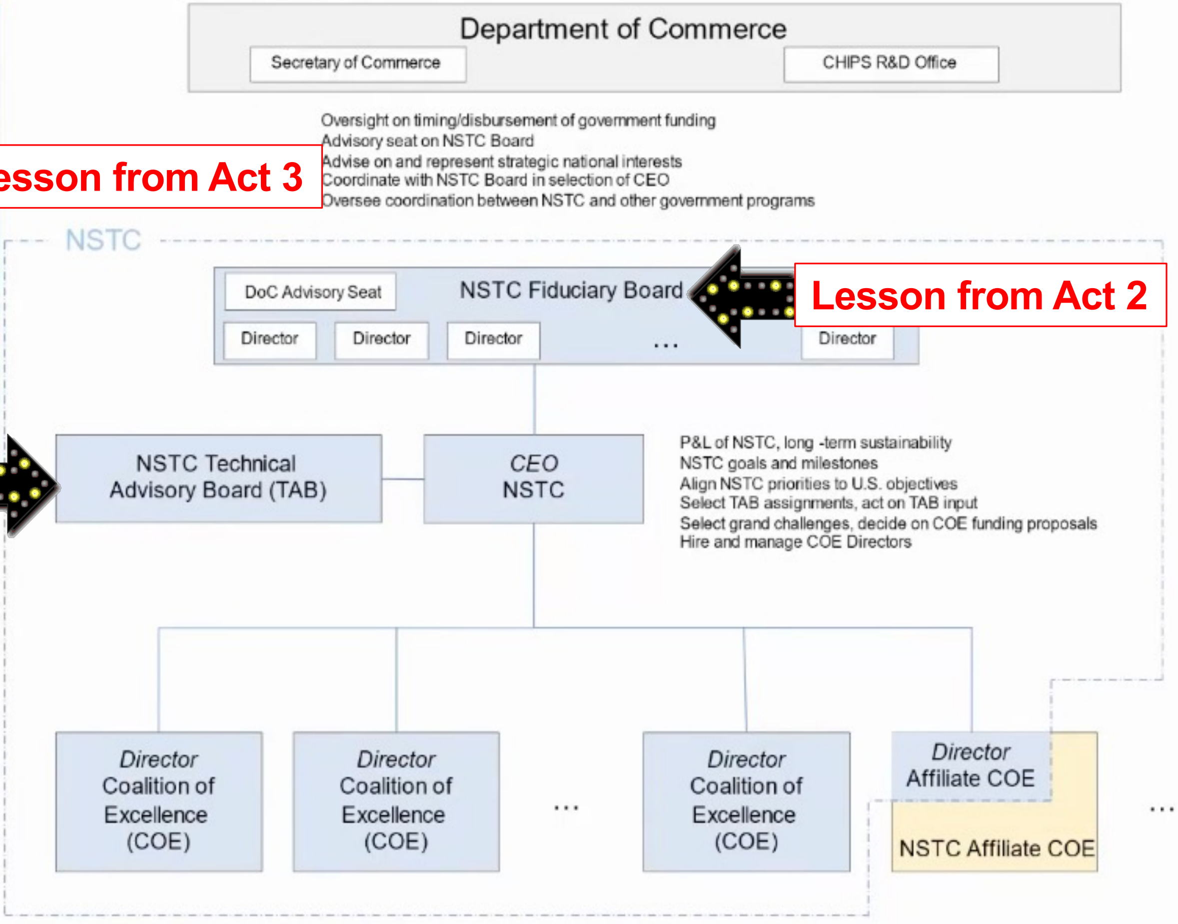
The CEO oversees Multiple Coalitions of Excellence (COEs), each with an Executive Director who oversees specific work sectors

Lesson from Act 3

Lesson from Act 3

Considerations:

- CEO appointment process
- CEO authority & reporting structure
- COE specialization areas



Oversight on timing/disbursement of government funding
Advisory seat on NSTC Board
Advise on and represent strategic national interests
Coordinate with NSTC Board in selection of CEO
Oversee coordination between NSTC and other government programs

Lesson from Act 2

P&L of NSTC, long -term sustainability
NSTC goals and milestones
Align NSTC priorities to U.S. objectives
Select TAB assignments, act on TAB input
Select grand challenges, decide on COE funding proposals
Hire and manage COE Directors

IAC Organization / PPP Working Group – February 7, 2023 IAC meeting

CHIPS *for* AMERICA

A VISION AND STRATEGY FOR THE NATIONAL SEMICONDUCTOR TECHNOLOGY CENTER

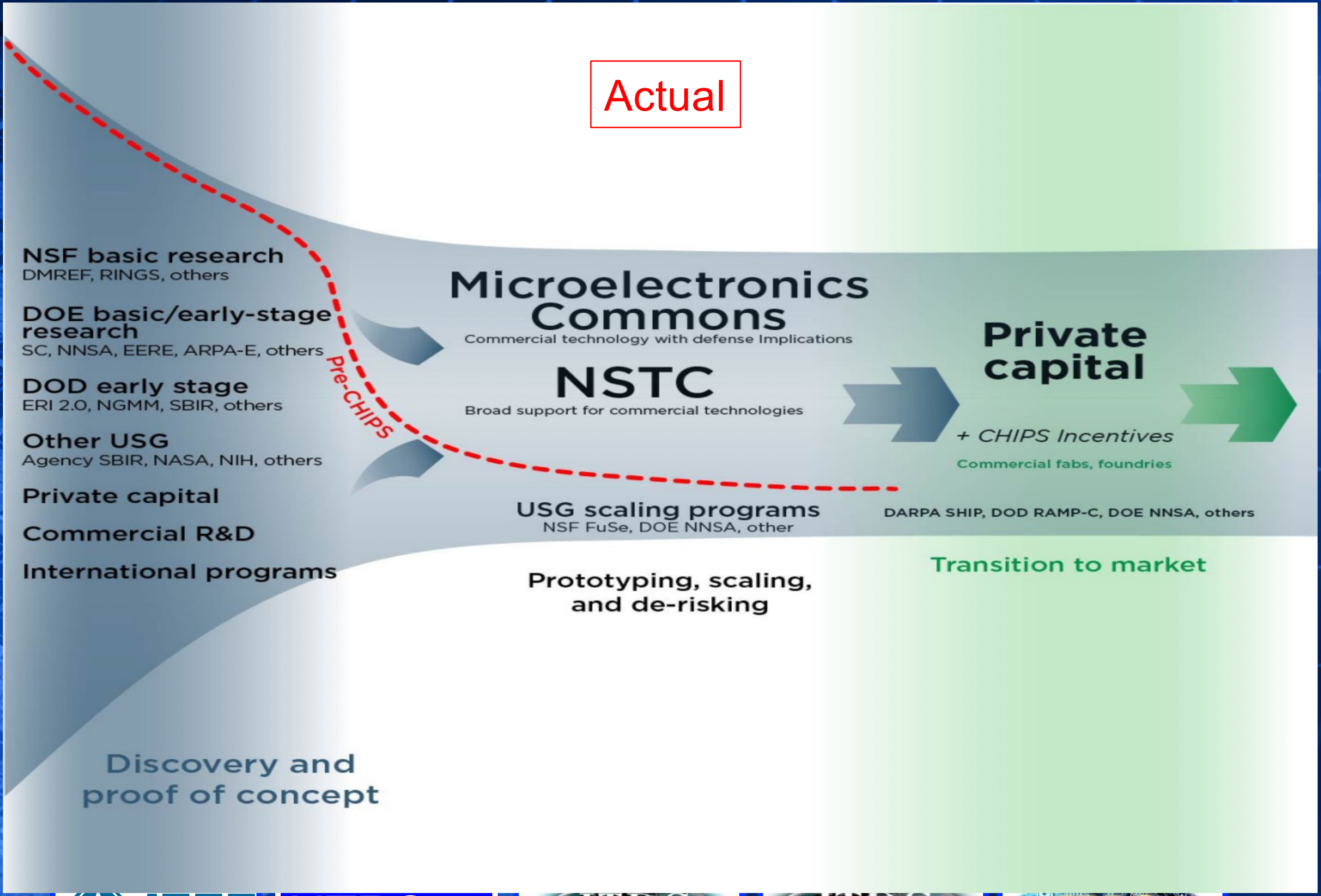
CHIPS Research and Development Office

April 25, 2023

CHIPS *for* AMERICA

NIST NATIONAL INSTITUTE OF STANDARDS AND TECHNOLOGY
U.S. DEPARTMENT OF COMMERCE

Actual



NSF basic research
DMREF, RINGS, others

DOE basic/early-stage research
SC, NNSA, EERE, ARPA-E, others

DOD early stage
ERI 2.0, NGMM, SBIR, others

Other USG
Agency SBIR, NASA, NIH, others

Private capital

Commercial R&D

International programs

Pre-CHIPS

Discovery and proof of concept

Microelectronics Commons
Commercial technology with defense Implications

NSTC
Broad support for commercial technologies

USG scaling programs
NSF FuSe, DOE NNSA, other

Prototyping, scaling, and de-risking

Private capital

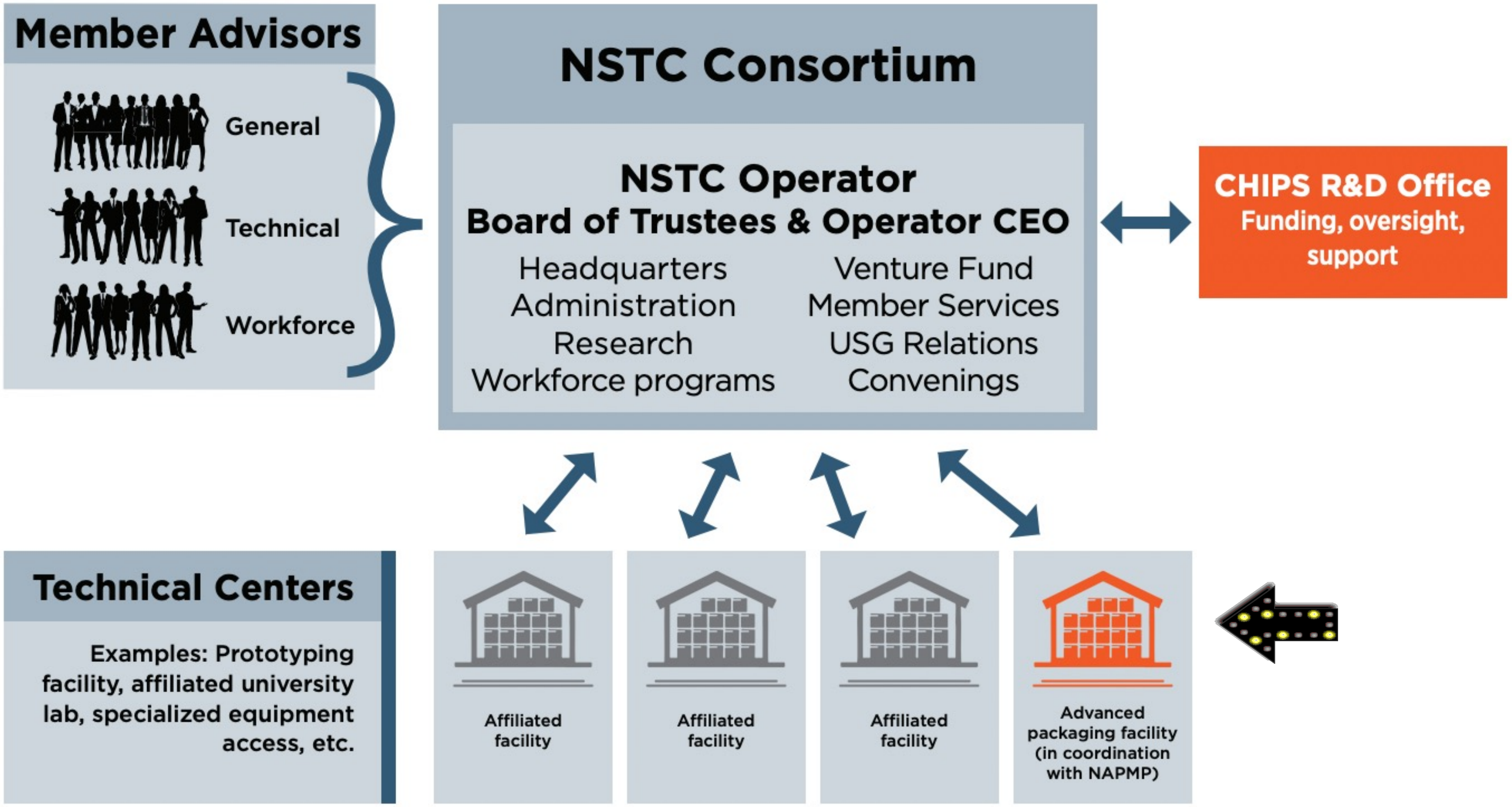
+ CHIPS Incentives
Commercial fabs, foundries

DARPA SHIP, DOD RAMP-C, DOE NNSA, others

Transition to market

NSTC OPERATING STRUCTURE

Actual



Member Advisors

- General
- Technical
- Workforce

NSTC Consortium

NSTC Operator

Board of Trustees & Operator CEO

Headquarters	Venture Fund
Administration	Member Services
Research	USG Relations
Workforce programs	Convenings

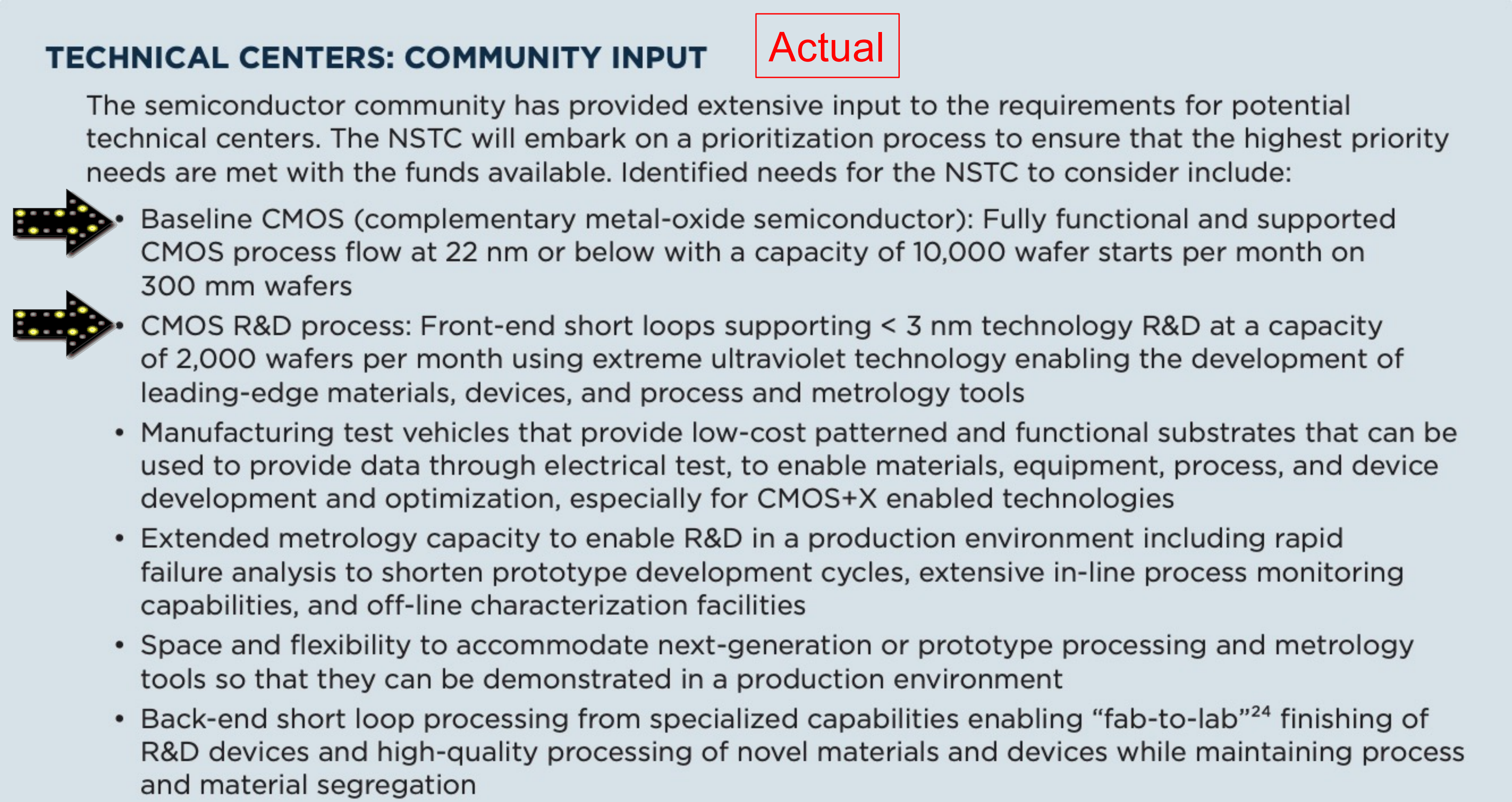
CHIPS R&D Office

Funding, oversight, support

Technical Centers

Examples: Prototyping facility, affiliated university lab, specialized equipment access, etc.

- Affiliated facility
- Affiliated facility
- Affiliated facility
- Advanced packaging facility (in coordination with NAPMP)



Actual

TECHNICAL CENTERS: COMMUNITY INPUT

The semiconductor community has provided extensive input to the requirements for potential technical centers. The NSTC will embark on a prioritization process to ensure that the highest priority needs are met with the funds available. Identified needs for the NSTC to consider include:

- Baseline CMOS (complementary metal-oxide semiconductor): Fully functional and supported CMOS process flow at 22 nm or below with a capacity of 10,000 wafer starts per month on 300 mm wafers
- CMOS R&D process: Front-end short loops supporting < 3 nm technology R&D at a capacity of 2,000 wafers per month using extreme ultraviolet technology enabling the development of leading-edge materials, devices, and process and metrology tools
- Manufacturing test vehicles that provide low-cost patterned and functional substrates that can be used to provide data through electrical test, to enable materials, equipment, process, and device development and optimization, especially for CMOS+X enabled technologies
- Extended metrology capacity to enable R&D in a production environment including rapid failure analysis to shorten prototype development cycles, extensive in-line process monitoring capabilities, and off-line characterization facilities
- Space and flexibility to accommodate next-generation or prototype processing and metrology tools so that they can be demonstrated in a production environment
- Back-end short loop processing from specialized capabilities enabling “fab-to-lab”[24] finishing of R&D devices and high-quality processing of novel materials and devices while maintaining process and material segregation

NSTC+APMP

2021 IRDS Proposal

6G
$f>$400GHz

META
AR/VR

Sensors
Edge Comp

NSTC
APMP

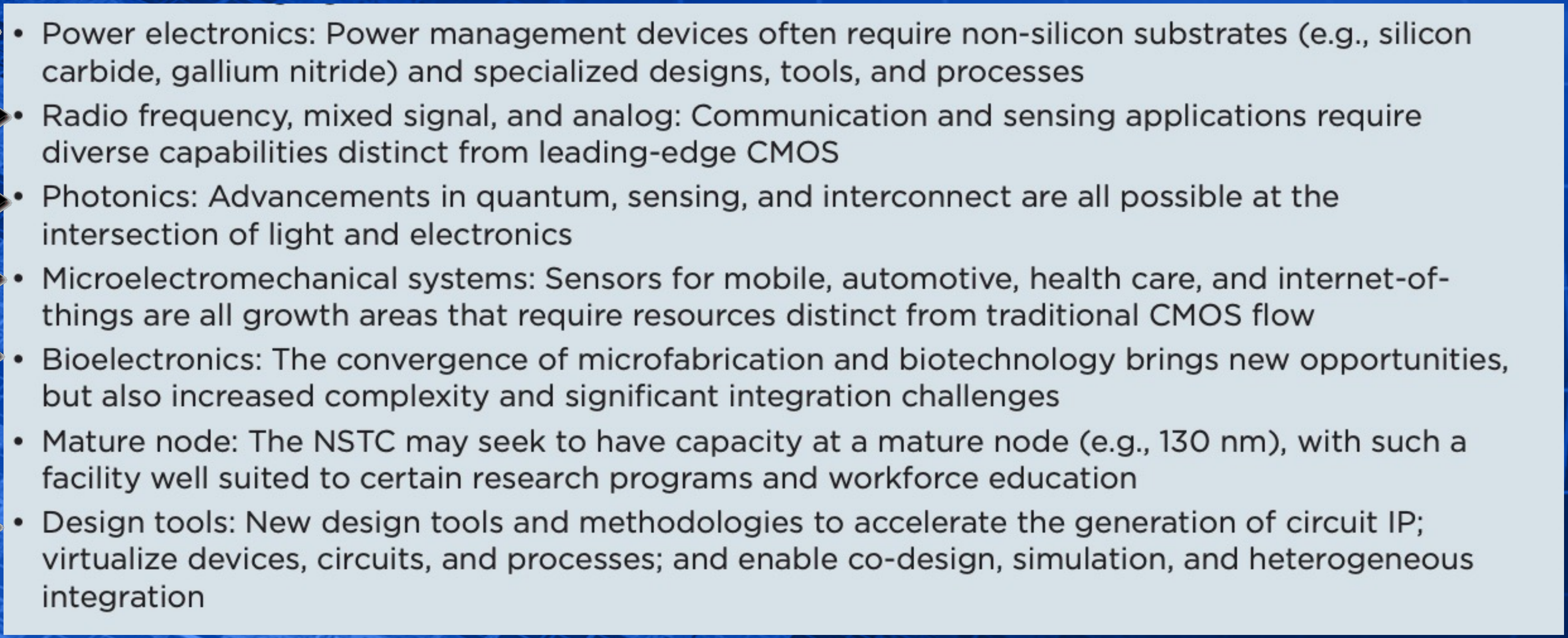
Self
Driving
Vehicles

Holography
Avatar

Power
Devices
GaN, SiC

Beyond CMOS

Actual



- Power electronics: Power management devices often require non-silicon substrates (e.g., silicon carbide, gallium nitride) and specialized designs, tools, and processes
- Radio frequency, mixed signal, and analog: Communication and sensing applications require diverse capabilities distinct from leading-edge CMOS
- Photonics: Advancements in quantum, sensing, and interconnect are all possible at the intersection of light and electronics
- Microelectromechanical systems: Sensors for mobile, automotive, health care, and internet-of-things are all growth areas that require resources distinct from traditional CMOS flow
- Bioelectronics: The convergence of microfabrication and biotechnology brings new opportunities, but also increased complexity and significant integration challenges
- Mature node: The NSTC may seek to have capacity at a mature node (e.g., 130 nm), with such a facility well suited to certain research programs and workforce education
- Design tools: New design tools and methodologies to accelerate the generation of circuit IP; virtualize devices, circuits, and processes; and enable co-design, simulation, and heterogeneous integration

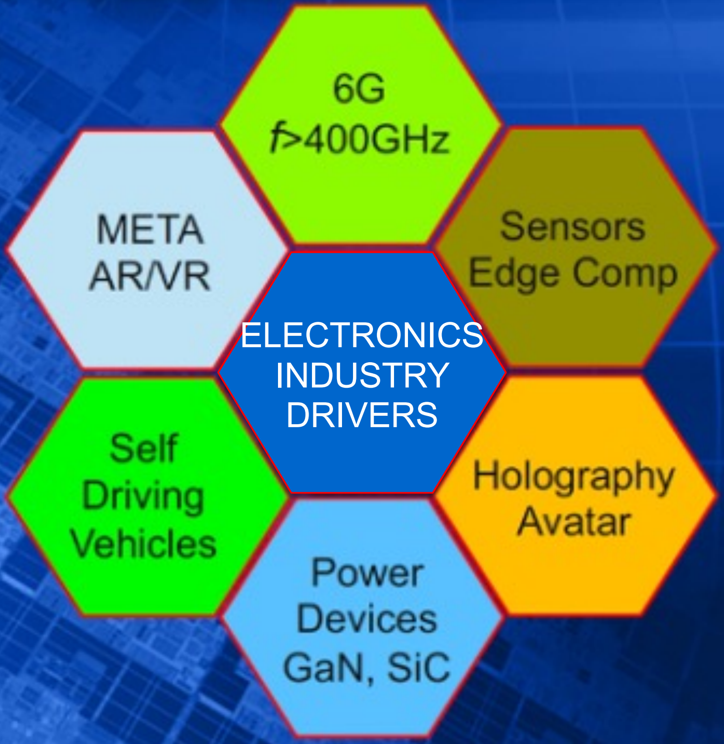
IRDS

http://irds.ieee.org/

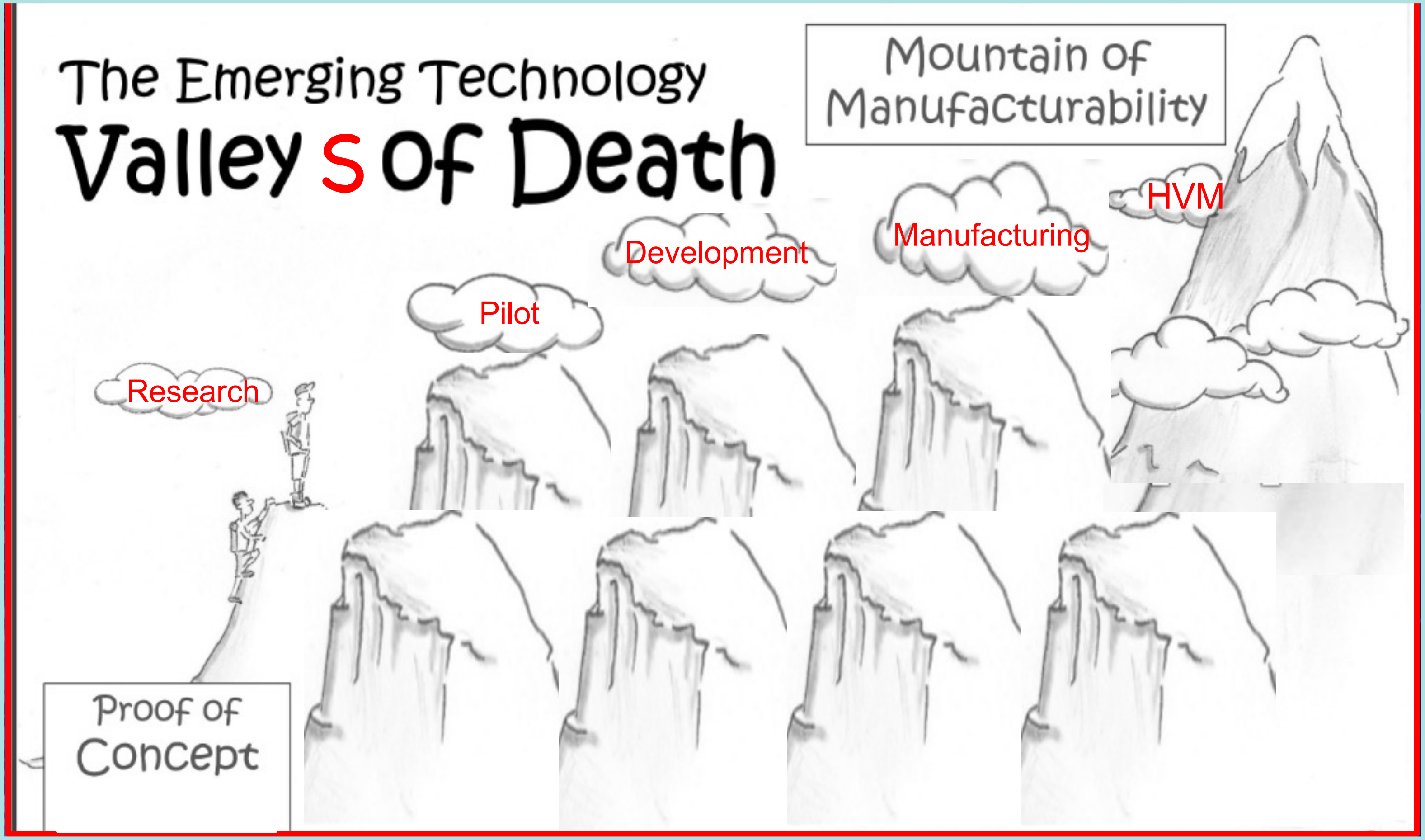
IEEE

IRDS Plans

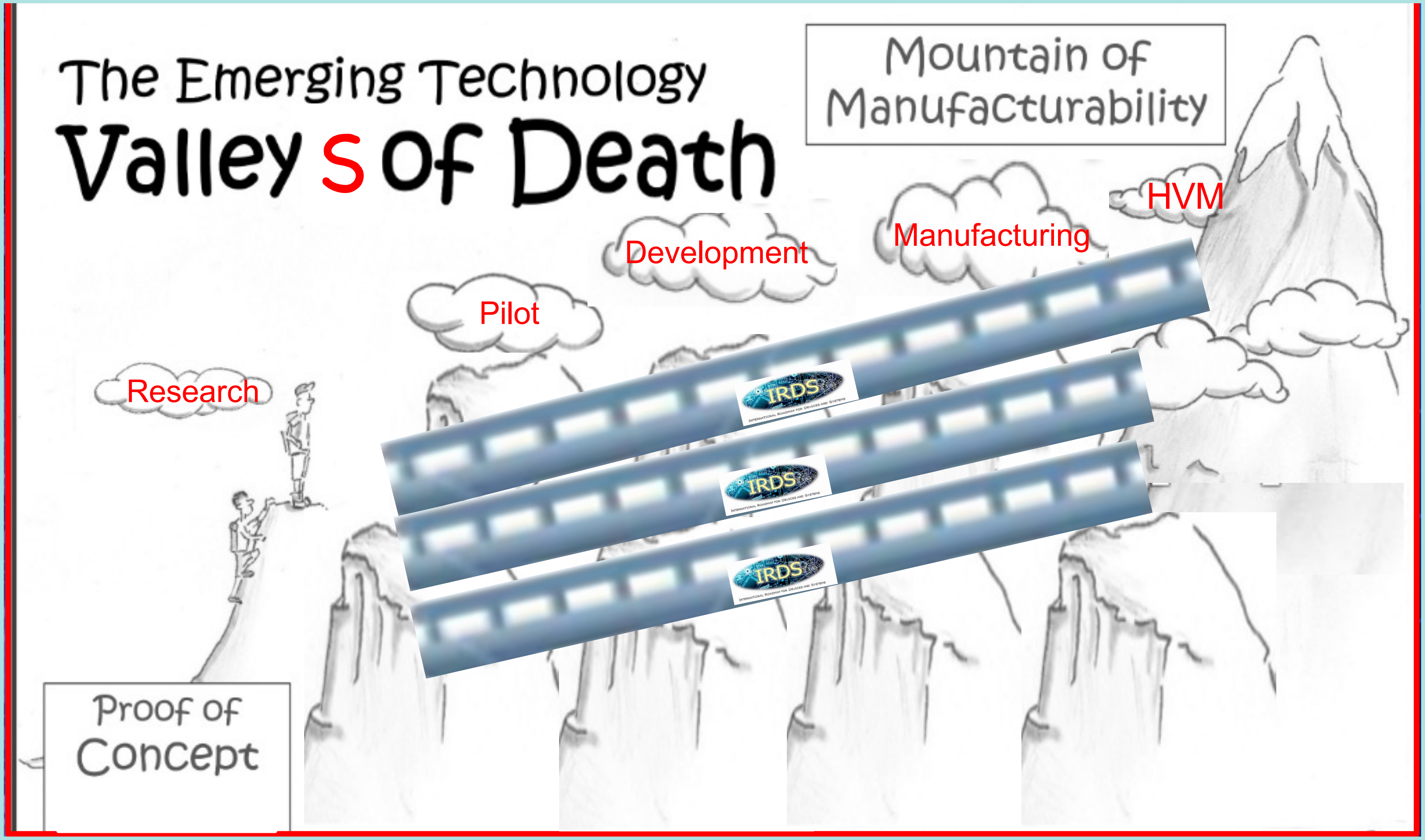
2023 IRDS VISION

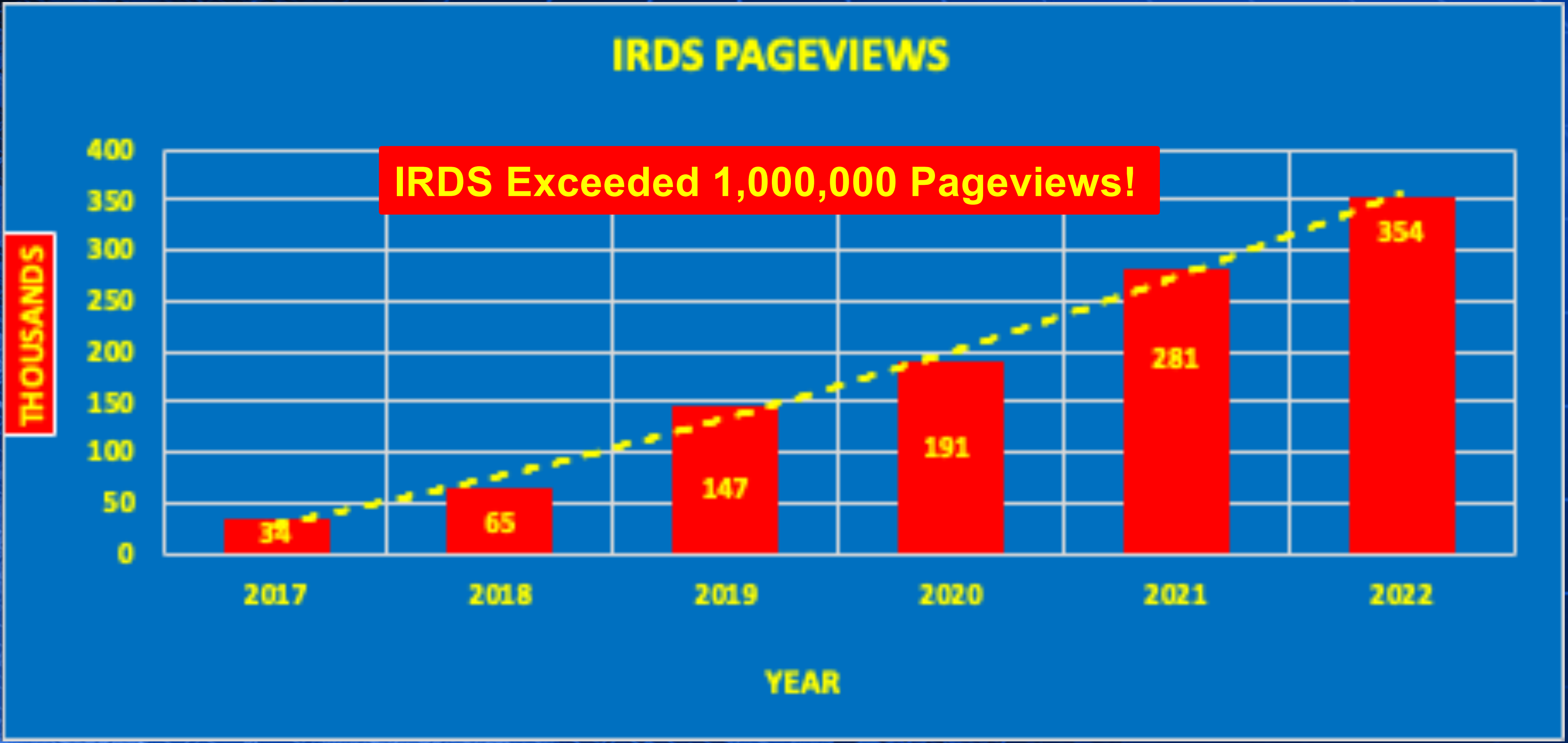


Multidimensional Challenges



Multidimensional Bridges





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