Silicon Photonics: (a, b) current state, future evolution, and (c) trends

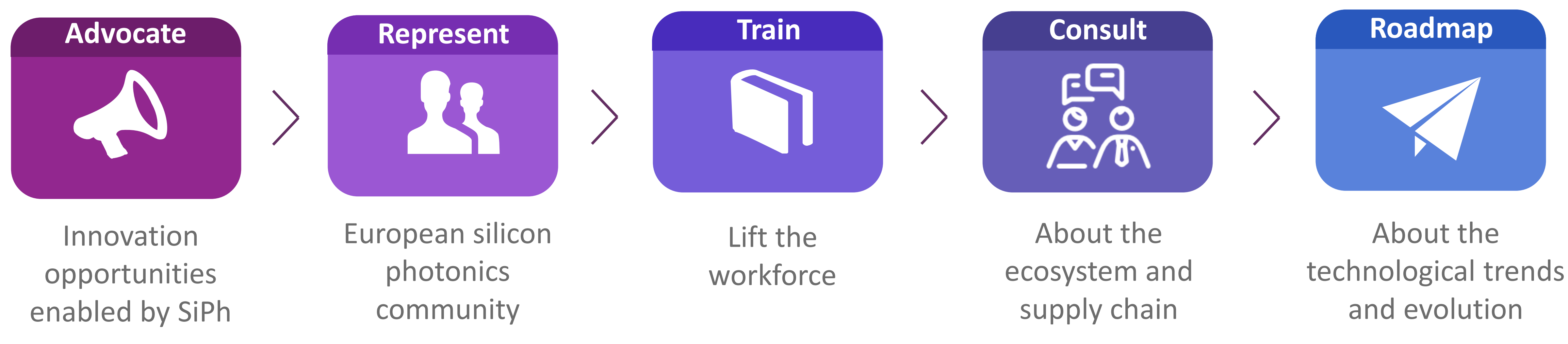
Dr. Abdul Rahim (Program Manager)

ePIXfab – the European Silicon Photonics Alliance

Ghent University, Belgium

ePIXfab - The European Silicon Photonics Alliance

ePIXfab's mission is to act as a catalyst for European academia and industry to strengthen the worldwide silicon photonics ecosystem.



Global Photonics Market

Photonics worldwide market size

Source: Tematys/Photonics21

Courtesy: EPIC

€ billion

1000
800
600
400
200
0

2005 2006 2007 2008 2009 2010 2011 2012 2013 2014 2015 2016 2017 2018 2019 2020 2021 2022 2023 2024 2025

+7.5%
+6.3%
+7%
+6% (est)

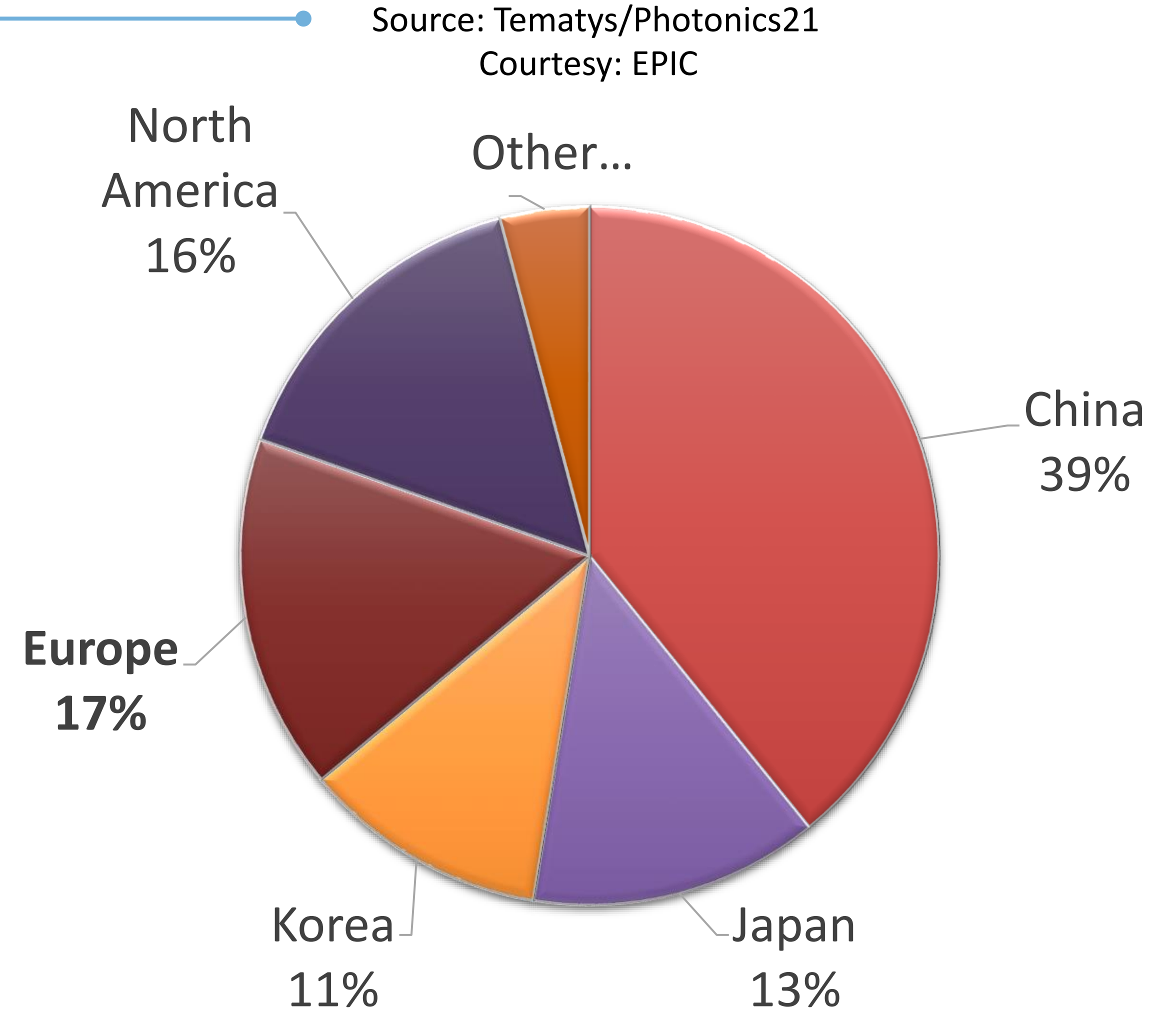
All OECD industry: 0.48%
China: 13.3%

All OECD industry: 1.07%
China: 7.4%

All OECD industry: 1.3%
China: (est) 6.0%

Global Photonics market expected to reach €900 billion in 2025

Global Photonics Market



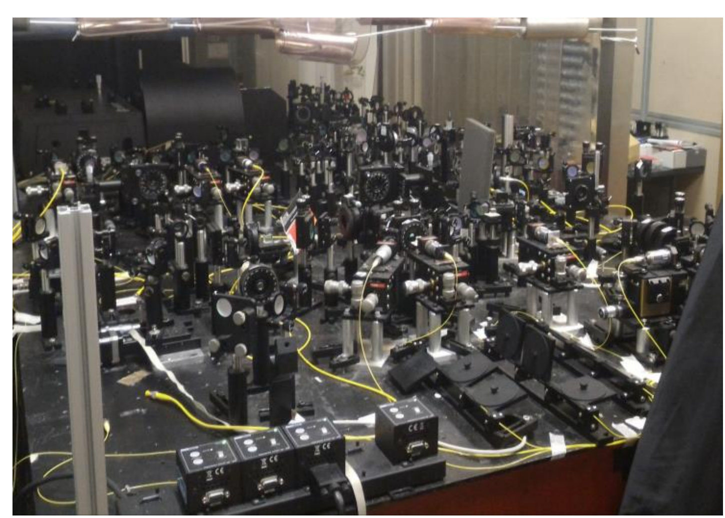
Global photonics market share:

- From 2015 to 2019, the share of the **European photonics industry has been maintained at 17%** of the global market thanks to the creativity of the European Research and the dynamism of companies active in "mid-size" markets.
- Asia photonics industry is mainly focus in displays, PV, and LED production

Photonics in Europe

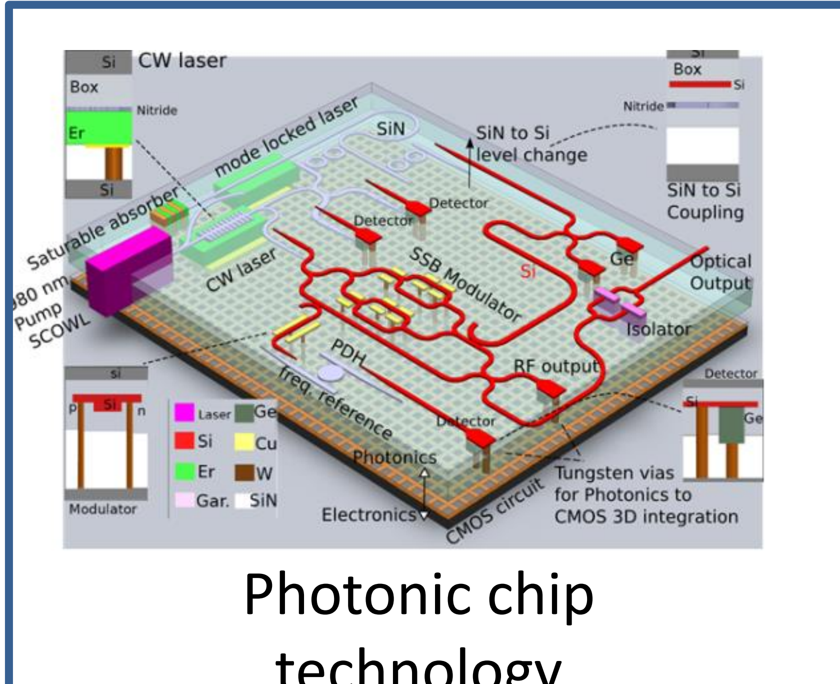
Source: Tematys/Photonics21
Courtesy: EPIC

Different forms of photonics



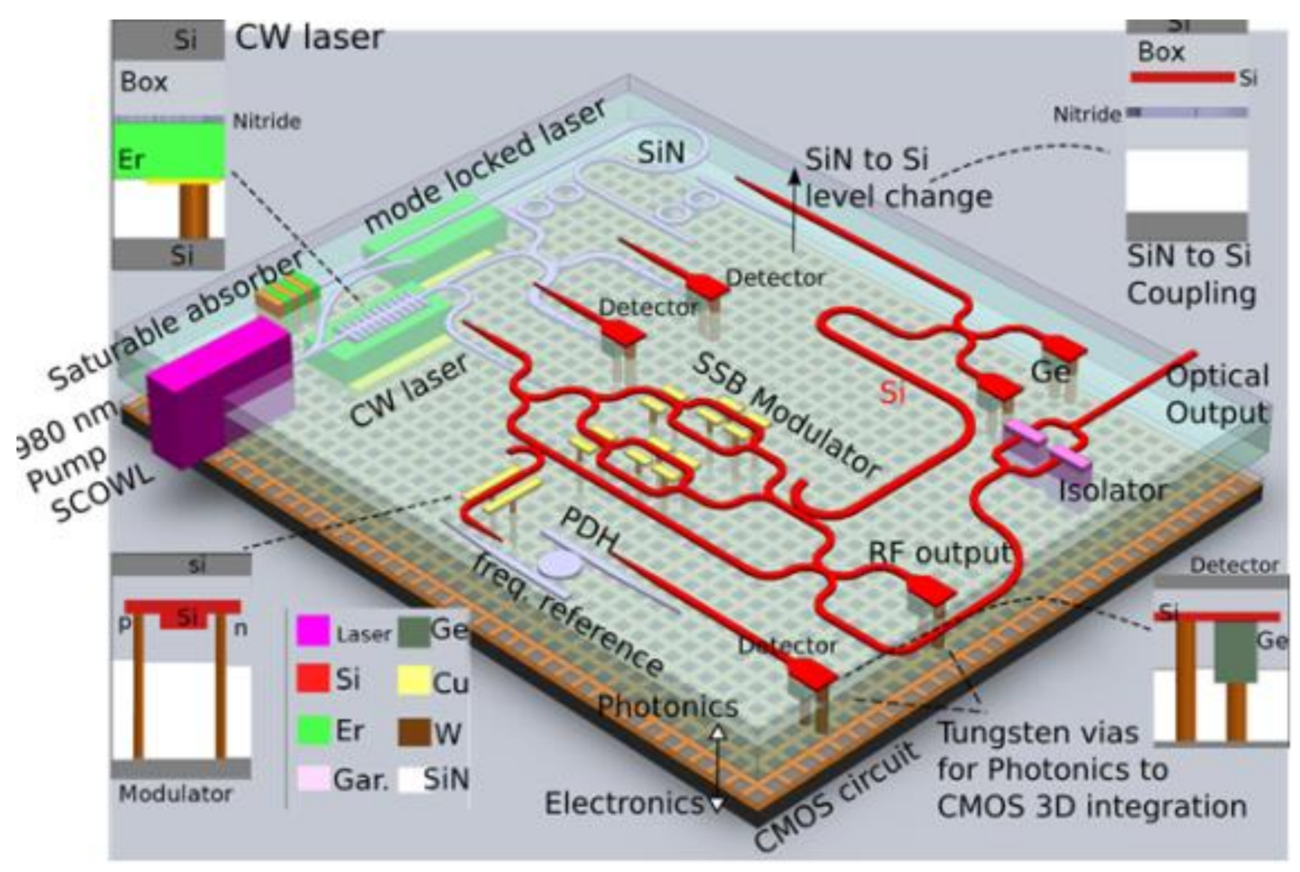
Free space optical technology

Optical fiber technology



Photonic chip technology

Photonics Integrated Circuits (PICs)



Source: EECS Berkeley

PICs provide a route to commoditize photonics at larger volumes and lower costs

PICs: platforms & application landscape

Not exhaustive

Transparency Window

- Indium phosphide
- Silicon nitride on insulator
- Silicon on insulator
- Aluminium Oxide on insulator
- Germanium-based platforms (GeOI, SiGe on Si, Ge-rich SiGe, etc.)
- Lithium niobate on insulator

Today's Mainstream platforms

0.0 0.5 1.0 1.5 2.0 2.5 3.0 3.5 4.0 4.5 5.0

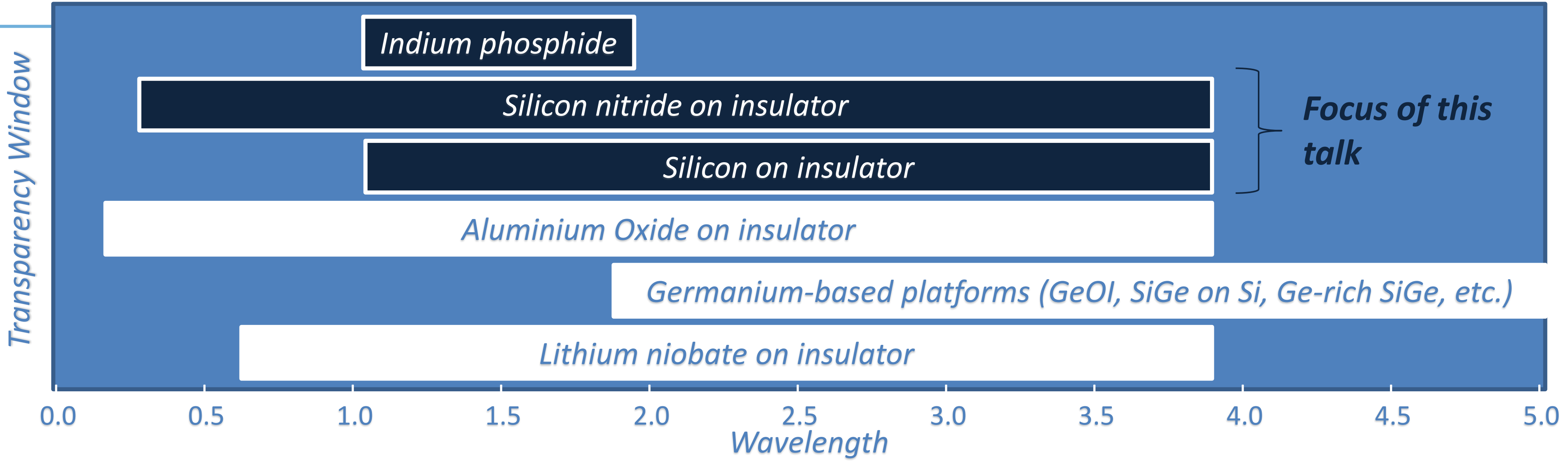
Wavelength

Applications

- Datacom
- Datacom/Telecom
- LiDAR
- Optical interconnects and optical processing
- Medical devices/consumer health/bio-sensing
- Industrial sensing (Gyroscopes, Fiber Interrogators)
- Quantum processing/communication
- Fiber RF and microwave photonics
- Precision metrology and spectroscopy
- Sensing and Defence applications

PICs: platforms & application landscape

Not exhaustive



What else is not covered in this talk:

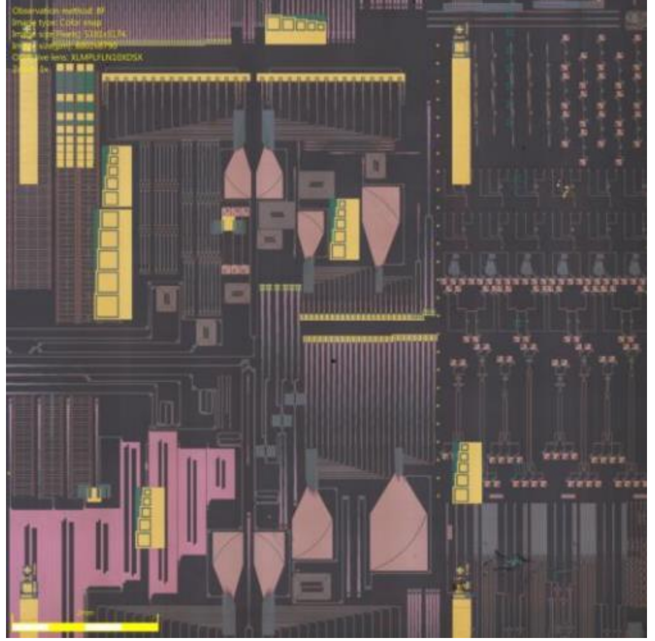
X PICs based on Compound semiconductors, R&D platforms, emerging platforms

X Imager chips

X VCSEL Arrays

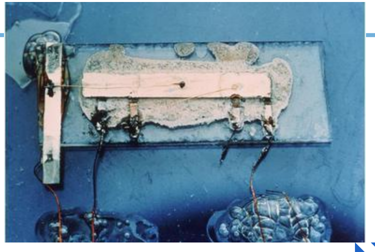
What is silicon photonics?

The implementation of high density photonic integrated circuits by means of CMOS process technology in a CMOS fab



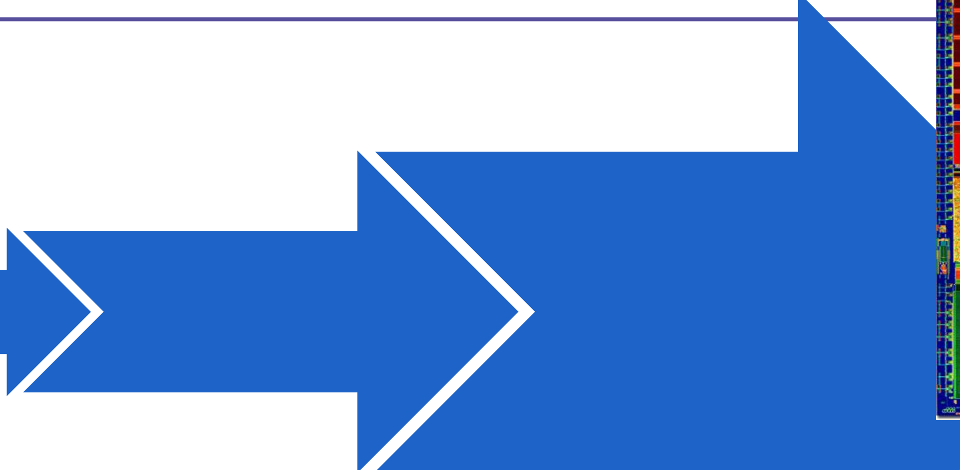
Enabling complex optical functionality on a compact chip at low cost

From discrete functions to circuits

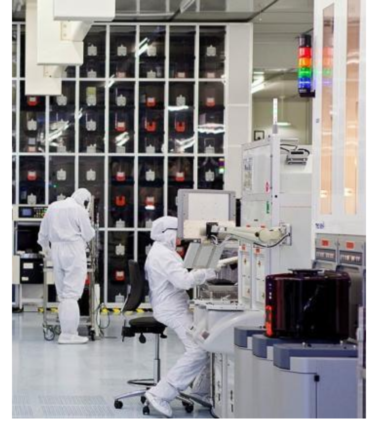


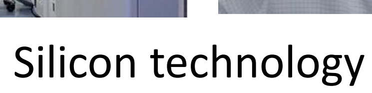
Jack Kilby

1958

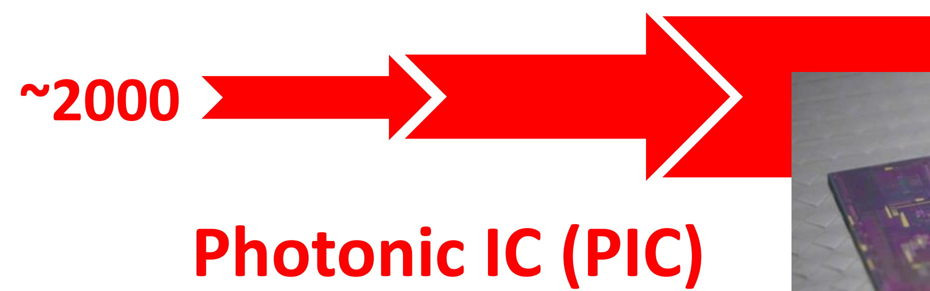


Electronic IC (EIC)



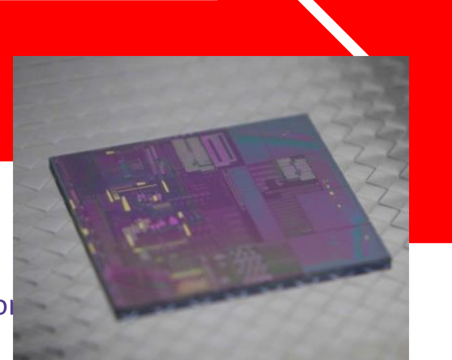


Silicon technology



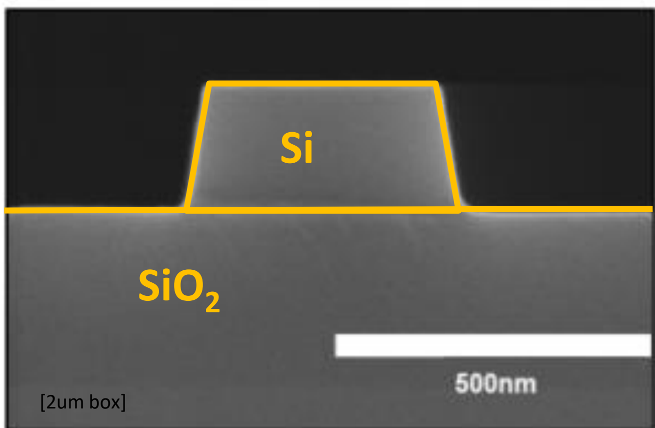
~2000

Photonic IC (PIC)

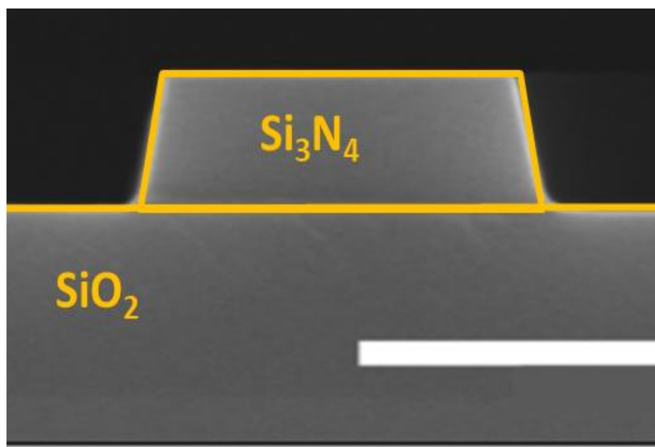


Silicon photonics: Two CMOS –fab compatible families

Silicon-on-Insulator (SOI)	Silicon nitride (SiN)



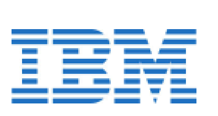
Silicon: n=3.5
Silicon oxide: n=1.45
Very high index contrast

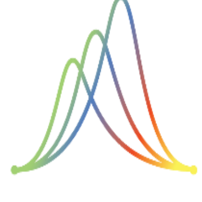


Silicon nitride: n=2
Silicon oxide: n=1.45
Moderately high index contrast

Not exhaustive

Main product today: transceivers for datacom and telecom

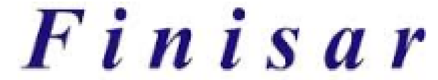




Under development:

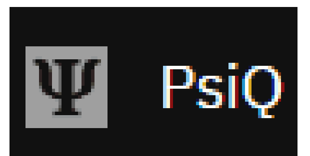
Data rate: 800 Gb/s

Symbol rate: 100 Gbaud



Not exhaustive

Silicon photonics going beyond transceivers



2021-2027 SILICON PHOTONIC DIE FORECAST BY APPLICATION

Source: Silicon Photonics 2022 Report, Yole Intelligence, 2022

- Data center transceivers
- Long haul transceivers
- 5G transceivers
- Co-packaged engines
- Immunoassay
- Consumer health
- Fiber-optic gyroscope
- Automotive LiDAR
- Photonic processing
- Optical interconnects

2021
$151M

$148M
$2.6M
$0.6M
$0.1M
$0.002M

CAGR$_{21-27}$: 36%

2027
$972M

$468M CAGR 22%
$244M CAGR 142%
$240M CAGR 30%
$1.7M CAGR 259%
$1.6M CAGR 56%
$2.2M CAGR 27%
$7.2M CAGR 302%
$5.5M CAGR 13%
$0.4M CAGR 194%
$1.5M CAGR 108%

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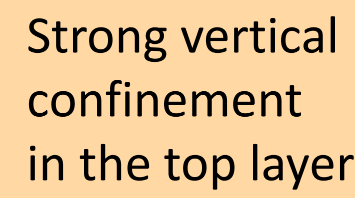
Current state & future evolution of silicon photonics

- From technological lens
- From value chain lens + Europe's position

Silicon photonics waveguide stack



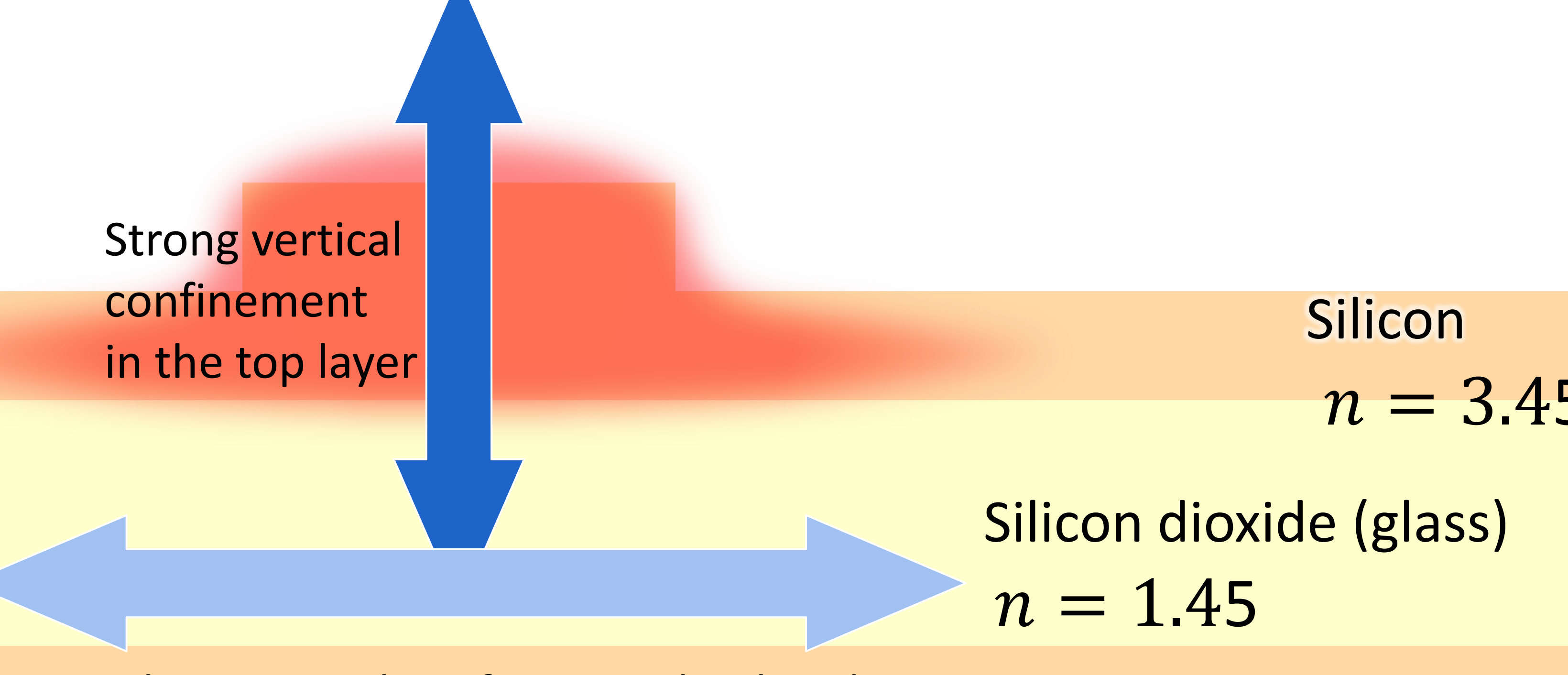
Strong vertical confinement in the top layer

Silicon
$n = 3.45$

Silicon dioxide (glass)
$n = 1.45$

Silicon
$n = 3.45$

Silicon photonics rib waveguide



Silicon photonics strip waveguide

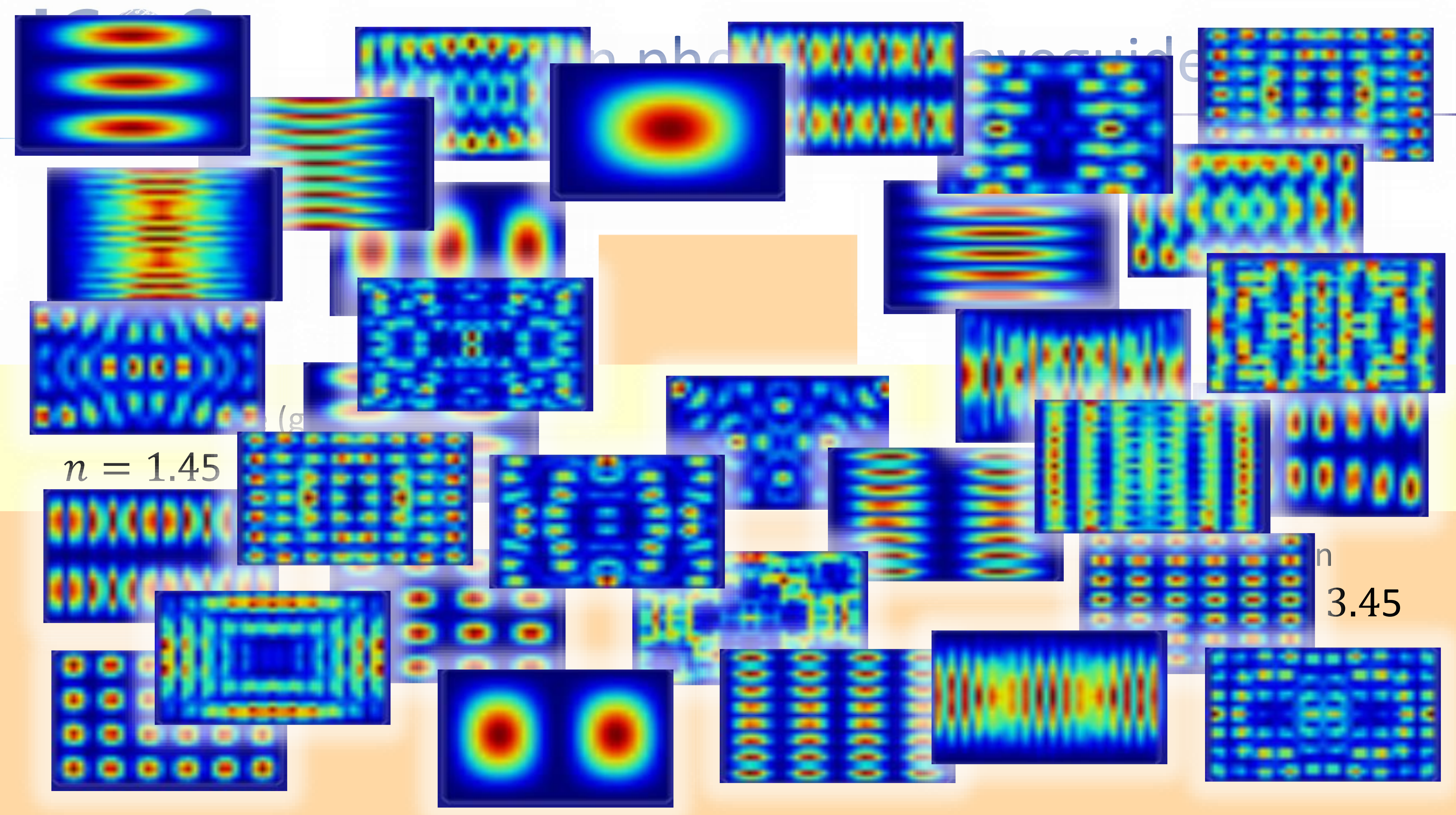
Strong vertical
confinement
in the top layer

Silicon
$n = 3.45$

Silicon dioxide (glass)
$n = 1.45$

Strong Horizontal confinement by the strip

Silicon
$n = 3.45$


$n = 1.45$
n
3.45

Shrinking SOI waveguides

Silicon

$n = 3.45$

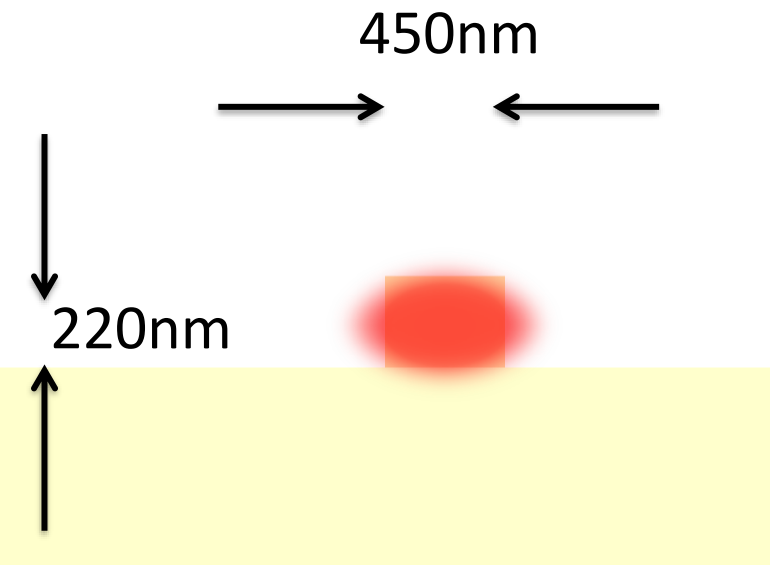
Silicon dioxide (glass)

$n = 1.45$

Silicon

$n = 3.45$

Shrinking SOI waveguides



Silicon

$n = 3.45$

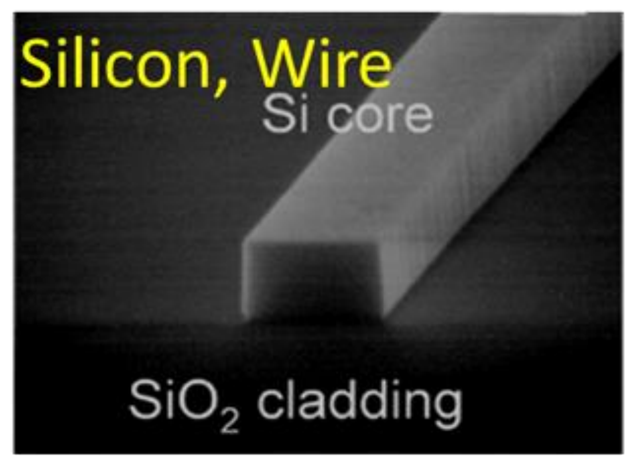
Silicon dioxide (glass)

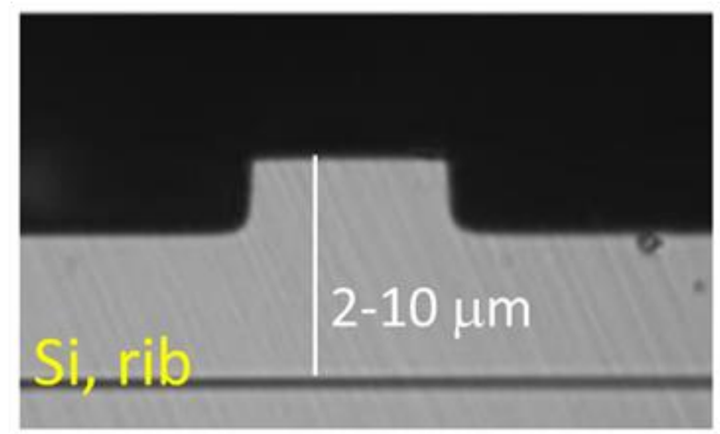
$n = 1.45$

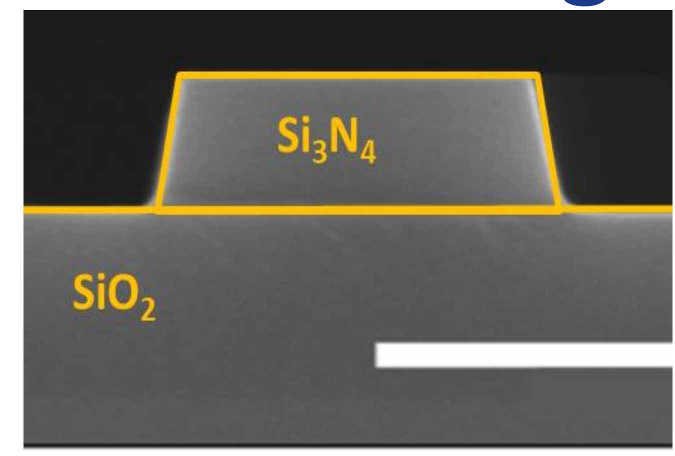
Silicon

$n = 3.45$

Current state and future evolution: Waveguides



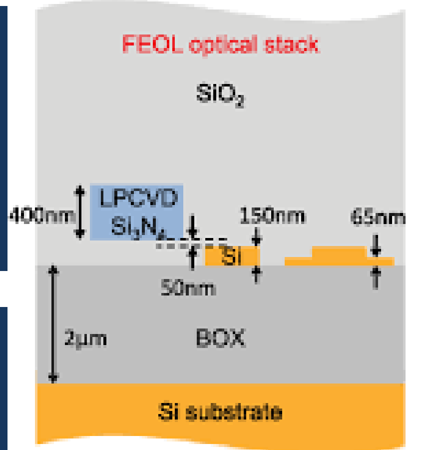


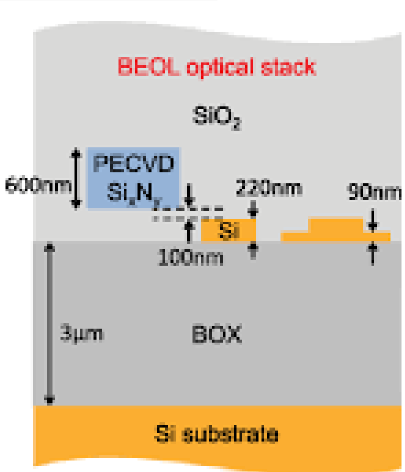


Performance:

Propagation loss: ~0.5– 2 dB/cm

Bending radius: 5 – 20 micron



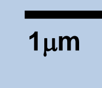


Source: J. Poon, JLT

Future evolution:

- Better process control (every nm^3 matters)
- Substrate quality
- Multilayer platforms with medium index contrast guiding layers

Fiber coupling to WG



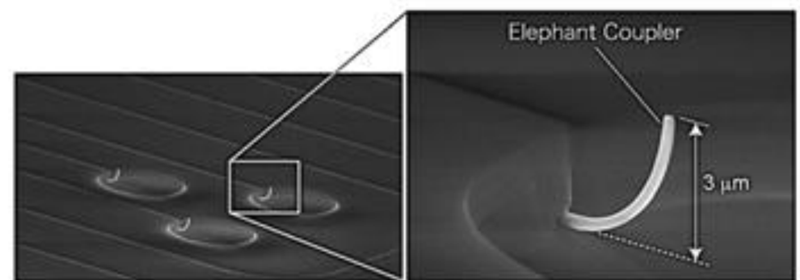
Requirements

- Low loss
- Broadband
- High coupling tolerance
- No facet reflections
- Wafer-scale testability
- Easy to fabricate

Current state and future evolution: I/O devices

	Inverted taper	Grating coupler
Loss (best)	<1dB	<1dB
Loss (in real live)	2dB-7dB	3dB-7dB
Broadband	> 100nm	35nm (1dB)
Misalignment tolerance	1um (1dB)	2.5um (1dB)
Facet reflections	Low	-20dB
Waferscale testing	No	Yes

T.Yoshida, IPR



Future evolution:

- Better process control
- Substrate quality WiW and WtW
- New designs

Current state and future evolution: High-speed phase modulators

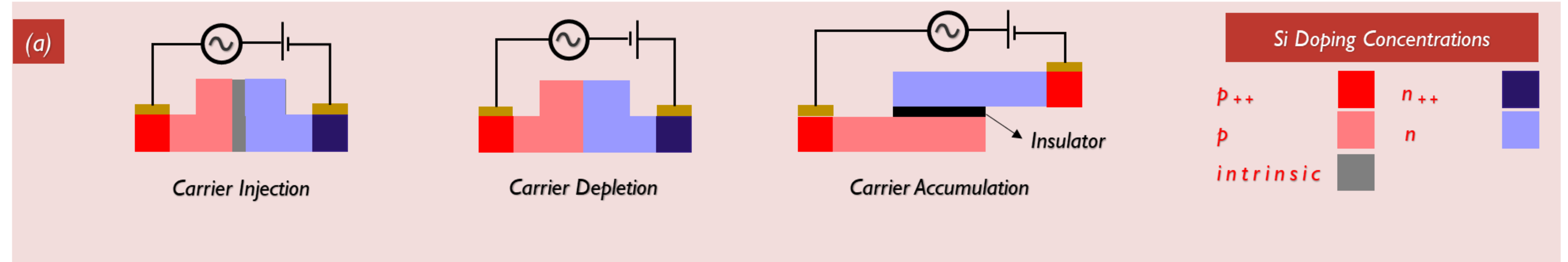


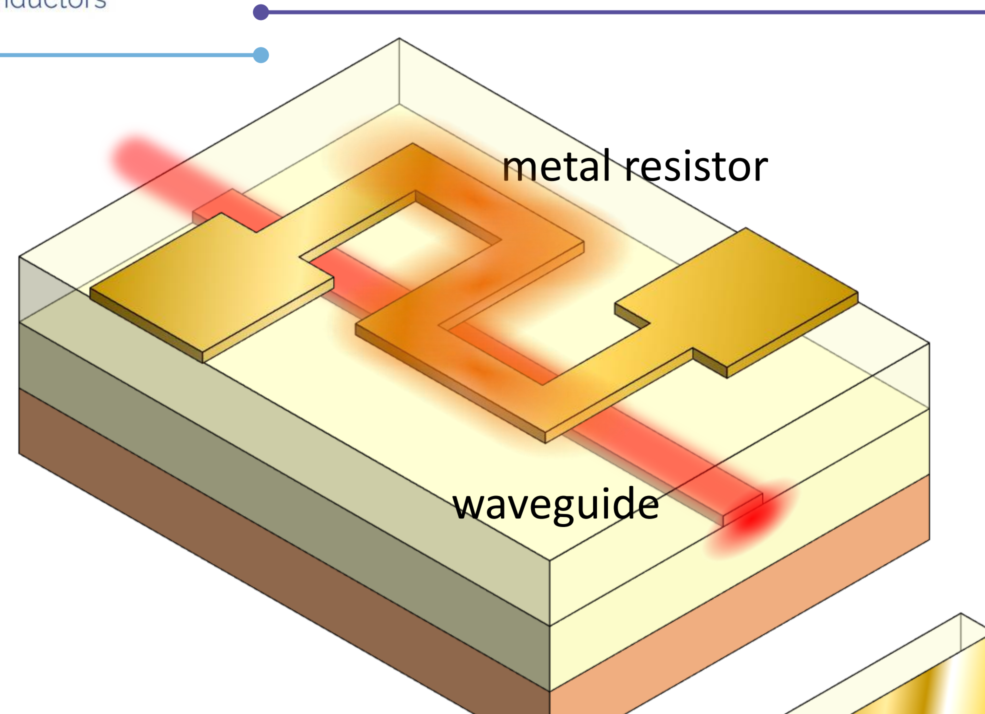
Table 2 Typical and state-of-the-art performance matrix for the plasma dispersion high-speed phase modulators. The parentheses contain the best-reported result for a performance attribute. The matrix includes the results reported for O-band and C-band demonstrations.

Principle	Modulation efficiency $V_\pi \cdot L$ (V · cm)	Loss (dB/cm)	Length[a] of phase shifter (mm)	Data rate[b] (Gb/s)	Energy/bit (fJ/bit)
Carrier injection[c]	<0.5 (0.058[8])	∼70 (28[7])	≥0.1 to <0.3	<40 (70[7])	∼1000 for MZMs and RMs (0.1[f,98])
Carrier accumulation[d]	<0.3 (0.16[69])	50 to 80 (∼35[69])	≤0.5	∼40 (40[5])	>200 for MZMs, <200 (3[105]) for SLMs[g]
Carrier depletion[e]	∼2 (0.52[9])	10 to 30 (2.6[10])	>1	>40 (100[122,123])	∼200 for MZMs (32.4[19]), <40 for RMs (0.9[18])

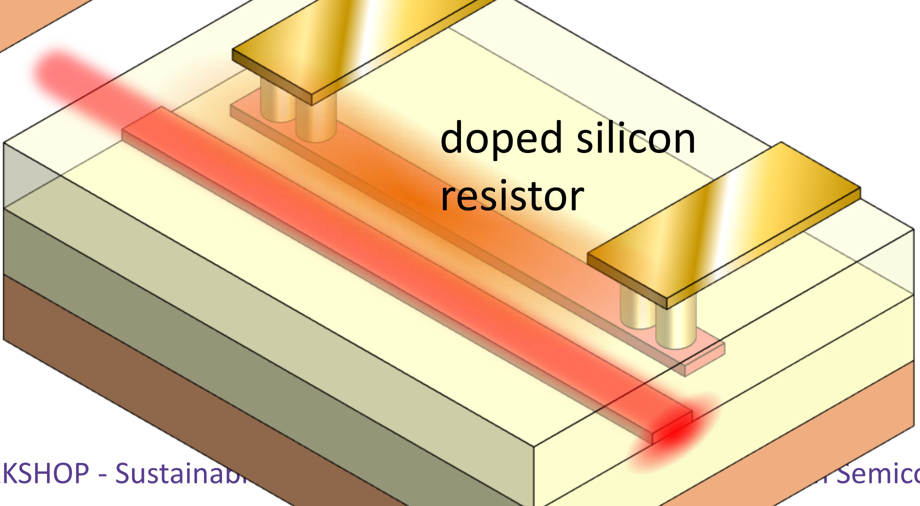
Future evolution:

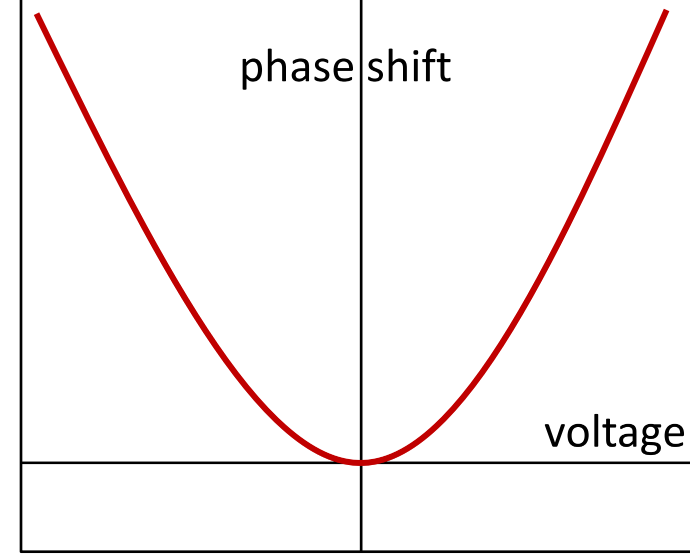
Integration of novel materials (Ferroelectrics, 2D, Polymers, SiGe, III-Vs, etc.) for low Vpi, low loss, high bandwidth, and low energy pure phase shift

Low-speed phase shifter by heaters

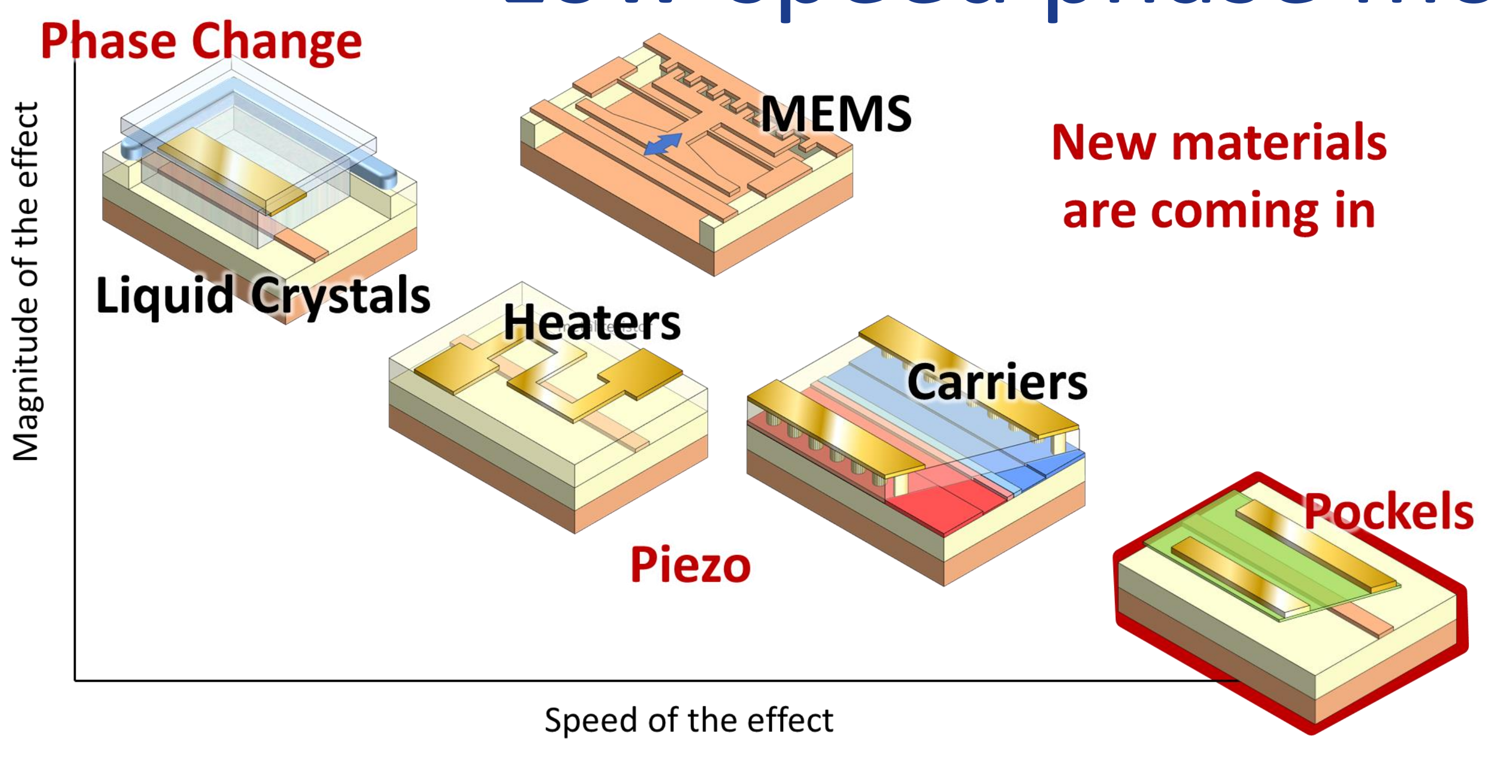


- Waveguides are thermally sensitive:
  $\Delta\phi \sim \Delta n_{eff} \sim T \sim P_{elec} \sim V^2 \sim I^2$
- Integrate resistor close to the waveguide
- efficiency: $P_\pi \approx 5 - 30mW$ (for silicon waveguides)

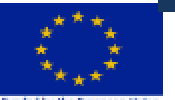




Current state and future evolution: Low-speed phase modulators

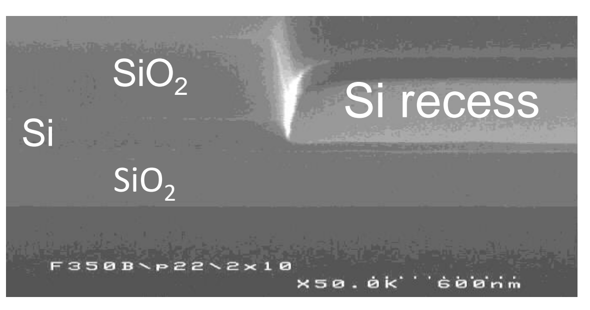


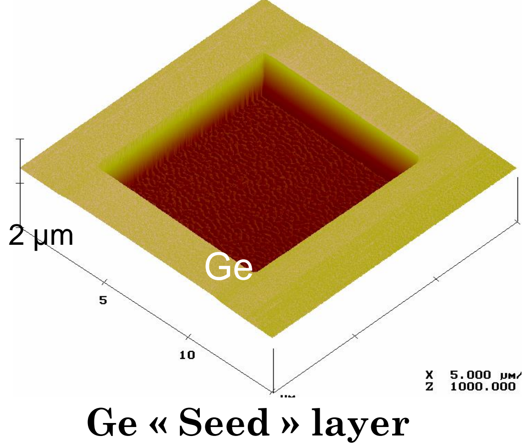
Future evolution:
Integration of novel materials for more efficient (power, loss, crosstalk) low-speed phase shifters



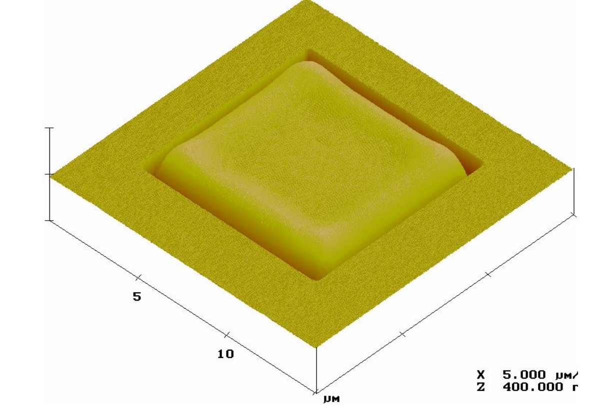
Current state and future evolution:

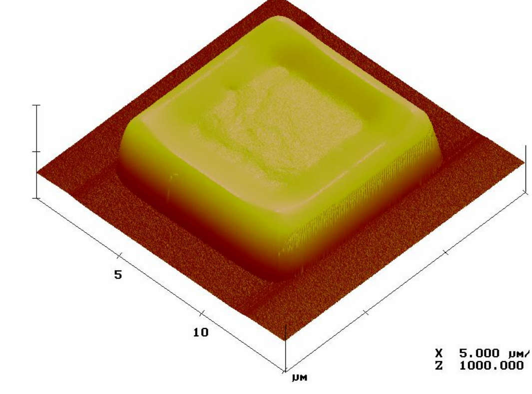
Two RPCVD steps to overcome lattice mismatch issue





Ge « Seed » layer
400° C, 60s

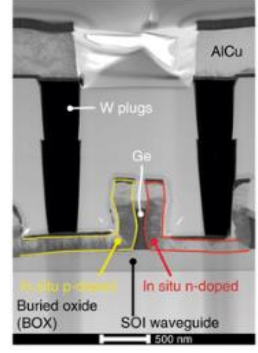




Photodetectors	[unit]	
Absorption	α (cm^{-1})	10^3
Dark Current	I (nA)	0.2
Responsivity (p-i-n)	R (A/W)	1
Bandwidth (p-i-n)	B (GHz)	>100
Gain x Bandwidth (APD)	GB (GHz)	300
Guided Power*	mW	30

Future evolution:

- Better process control for narrower intrinsic regions
- Lower defect density for lower dark currents



S. Lischke,
Nat. Photonics

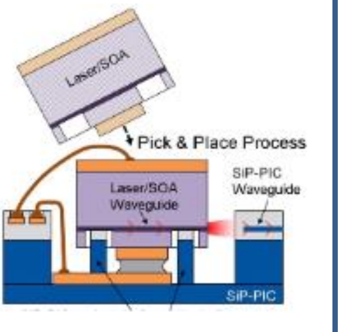
Current state and future evolution: Light sources

LaMP

- ✓ Use mature III-V technology
- ✓ Wafer level test on source
- ✓ Known good die
- — No waveguide-in / waveguide-out devices
- — Sequential population of SiPhwafer

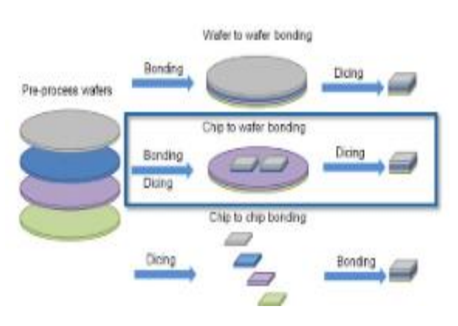
Flip-chip Integration

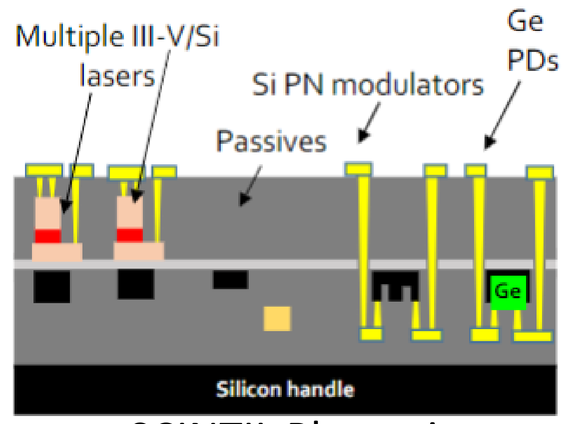
- ✓ Use mature III-V technology
- ✓ Wafer-level test on source
- ✓ Known good die
- ✓ Fairly efficient optical coupling
- — Sequential population of SiPhwafer
- — Requires local back-end removal



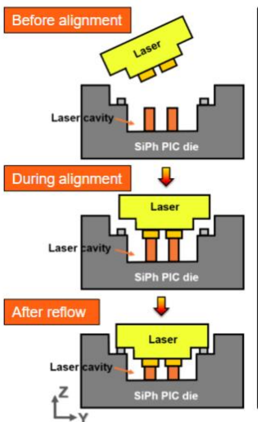
Die-to-wafer bonding

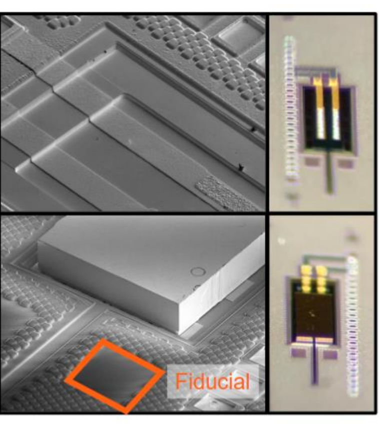
- ✓ Efficient optical coupling
- ✓ Parallel processing of devices
- ✓ Wafer-level test on target wafer
- — III-V processing on target wafer
- — No known good III-V die



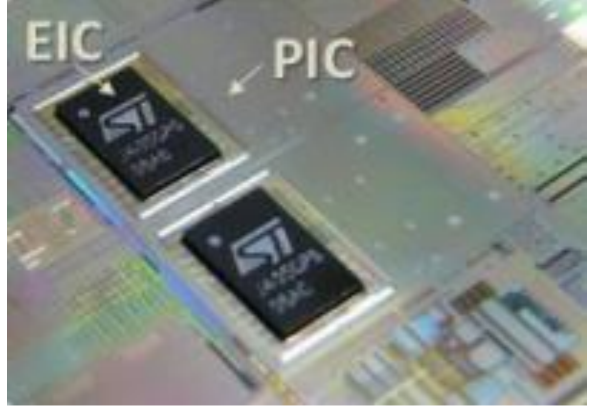


SCINTIL Photonics

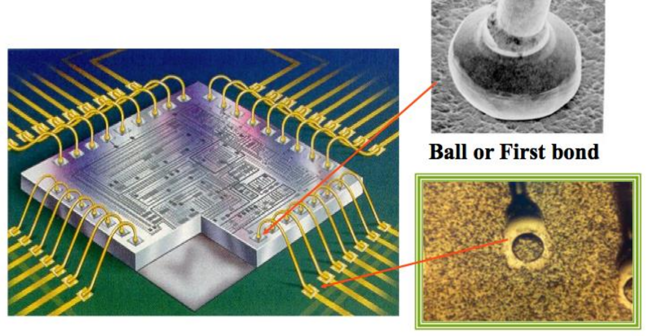




Current state and future evolution : electronic-photonic integration

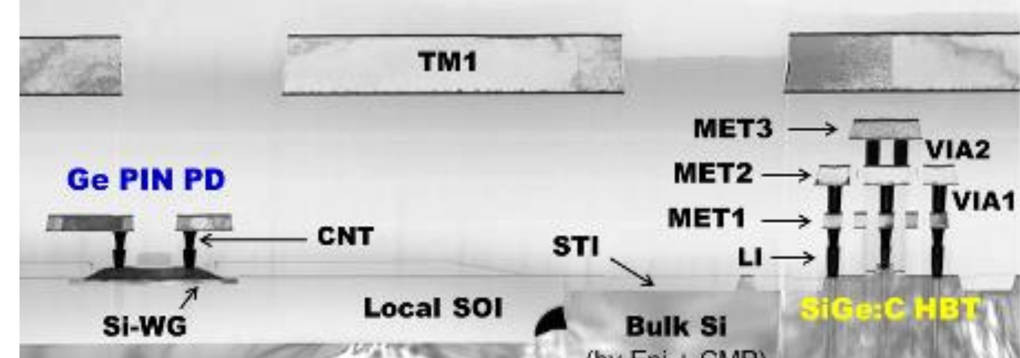


STMicro.



Tyndall

IHP



GlobalFoundries

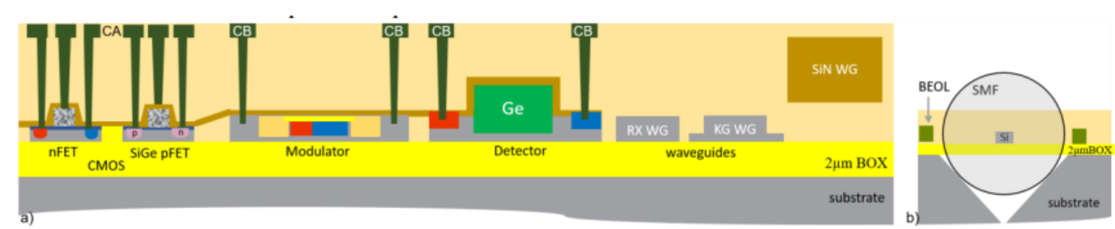


Fig. 1. (a) Cross-section showing front end and middle of line of 45CLO technology. (b) Cross-section diagram of the IOSMF with v-groove and the attached fiber.

Future Evolution: Higher intimacy between electronics and photonics becoming more important

A generic cross-section of a silicon photonics platform

Representative cross-section of a silicon photonics process

Representative cross-section of a silicon photonic process combing photonics with electronics (b) with BICMOS process (c) with Bulk Si or PD-SOI

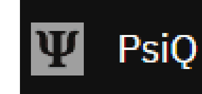
(a)
(b)
(c)
Al Pad
Al Pad
Al Pad
Oxide Cladding
WGs
P.S
HS Mod.
HS Det.
EPICs
Metal Layer
SiN Waveguide Layer
I/O
Heater
Rib Waveguide
Edge coupler
Grating Coupler
Strip Waveguide
Depletion Modulator
Germanium Photodiode
HBT Transistor
CMOS Transistor
Metal Layer
Photonic Isolation Layer or BOX
Transistor Isolation
Selective silicon epitaxy
Silicon Handle

Current state & future evolution of silicon photonics

- From technological lens
- From value chain lens + Europe's position

Silicon photonics value chain

and others …



and others …

Fabs

Chip Companies

Wafer Fab Equipment

Materials and Subsystem

Design Automation Tools

Chip Intellectual Property Cores

and many others …

and many others …

and many others …

Inspired from: Steve Blank: The Semiconductor Ecosystem – Explained

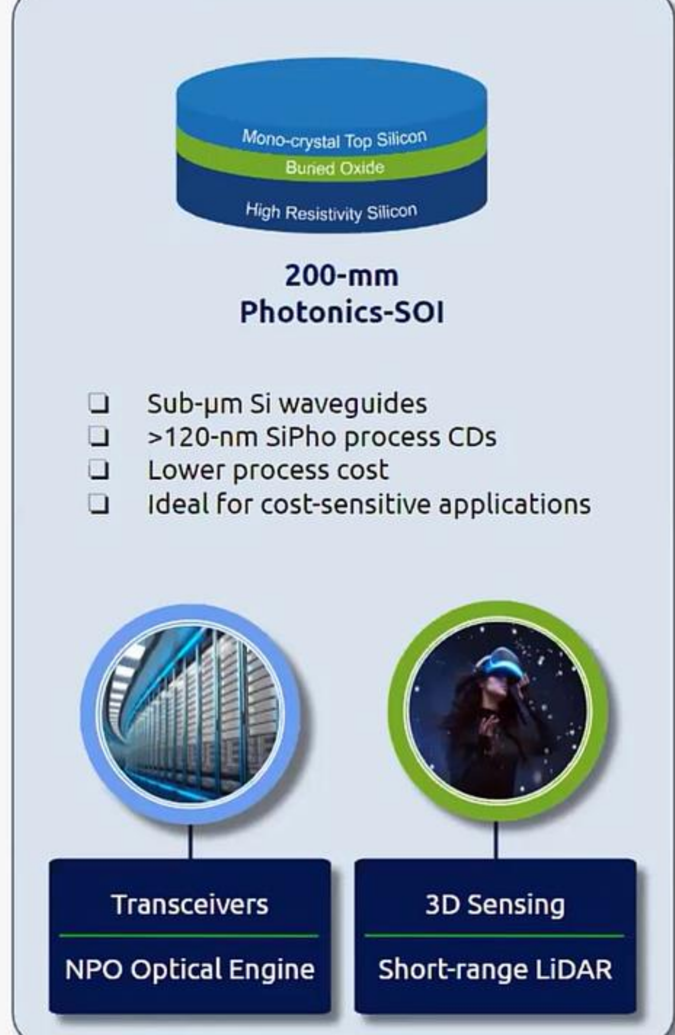
White Paper on Integrated Photonics

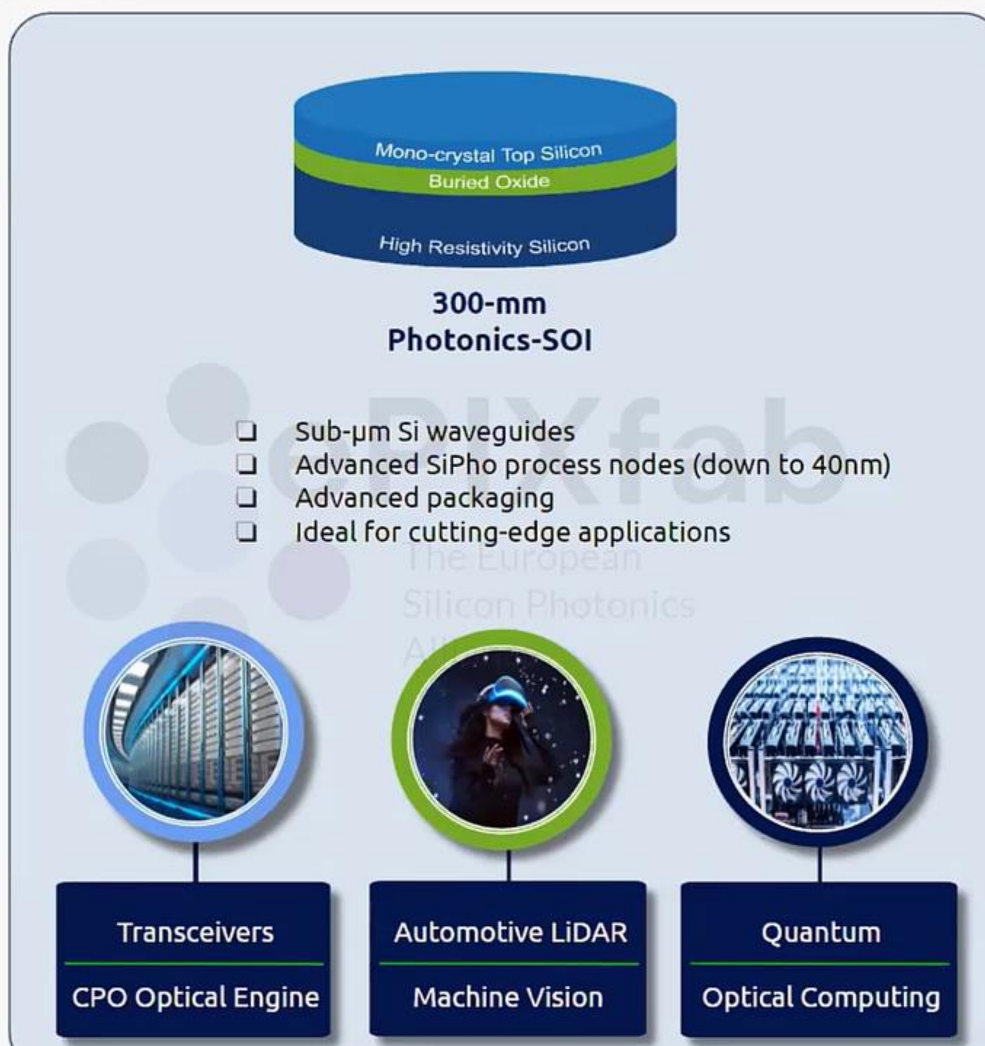
authored by a Joint Focus Group of the
European Association on Smart Systems Integration (EPoSS)
and
Photonics21

Michael Scholles, Michael J. Wale, Timo Aalto, Mohand Achouche, Luc Augustin, David Bitauld, Sonia Garcia Blanco, Patrick Cogez, Marcus Dahlem, Paul van Dijk, Gerhard Domann, Amir Ghadimi, Martijn Heck, Thomas Hessler, Andreas Klug, Renaud de Langlade, Martin Martens, Christian Meyne, Clifford Murray, Sybille Niemeier, Ruud Oldenbeuving, Mehmet Cengiz Onbaşlı, Joseph Pankert, Ryszard Piramidowicz, Abdul Rahim, Graham Reed, Jelmer Renema, Ewit Roos, Martin Schell, Elisabeth Steinmetz, Martin Strassburg, Bertrand Szelag, Tolga Tekin, Dao Thang Duy, Dries van Thourhout, Marija Trajkovic, Gintaras Valusis, Lennart de Vreede, Markus Wilkens, Martina Wisniewski, Benjamin Wohlfeil, Lars Zimmermann

April 2023

Ecosystem status: materials and substrates





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Ecosystem status: materials and substrates

Europe's position

- ✓ One of the largest SOI wafer manufacturer is based in Europe (SOITEC)
- ✓ Close collaboration of EU fabs and substrate manufactures to meet future substrate demands (wafer sizes, uniformity)
- — Diversity of material systems makes it difficult for substrate manufactures to make a bet (a lot of parallel R&D)
- — Access to novel material likes TFLN and EUs push to include novel materials with SiPh.

Ecosystem status: electronic photonic design automation

- Large EDA vendors (that are mostly US-centric organizations) offer integrated photonics design frameworks
- The fab PDKs are getting rich but still lack compact models and not at-par with electronic PDKs
- Lack of unified process flow for electronic-photonic co-design
- Lack of standardization and no incentive in doing that
- Limited number of design houses and IP vendors

Ecosystem status: electronic photonic design automation

Europe's position

✓A number of smaller but collaborative companies offering best-in-class for various aspects of photonic design flow

✓Close relationship of the stakeholders with EU and non-EU foundries to support various PIC platforms

—Challenges in attracting and retaining talented HR, limited scale-up funding, limited business in EU

—Asia and US driving the narrative and winning the business

Ecosystem status: manufacturing

NORTH AMERICA

1. **ULL Technologies (USA)**
2. Applied Nanotools Inc. (Canada)
3. Intel (USA)
4. **Tower Semicon. (USA)**
5. **Globalfoundries (USA)**
6. **AIM Photonics (USA)**
7. Skorpios Technologies (USA)
8. Skywater (USA)
9. **C2MI (Canada)**

EUROPE

10. VTT (Finland)
11. SiPhotonic (Denmark)
12. **Imec (Belgium)**
13. **Cornerstone (UK)**
14. IHP (Germany)
15. **LIGENTEC (Swiss.)**
16. **LETI (France)**
17. **CNM-IMB (Spain)**
18. **LioniX Int. (Netherlands)**
19. **STMicro. (France)**
20. **AMO GmbH (Germany)**
21. **CNIT (Italy)**
22. **X-FAB (Germany/France)**

ASIA

23. **CUMEC (China)**
24. **AMF (Singapore)**
25. **CompoundTek (Singapore)**
26. **SilTerra (Malaysia)**
27. PETRA (Japan)
28. IMECAS (China)
29. SAMSUNG (Korea)
30. Australian Silicon Ph. (Australia)
31. TSMC (Taiwan)

IDM
Pure-play Foundry
R&D + Small volume

View Interactive map:
https://www.google.com/maps/d/edit?mid=1zHWNDRO0Ol0M_bh6eGerY7ddVOjl8ohE&usp=sharing

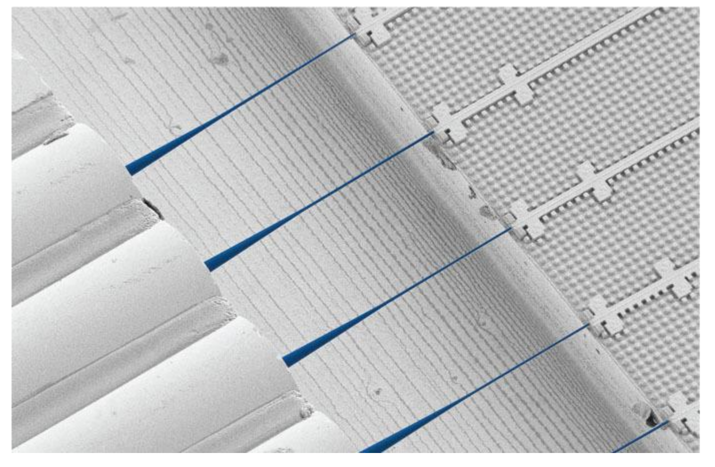
Ecosystem status: manufacturing

Europe’s position

- ✓ Renowned R&D institutes with a an established track record in integrated photonics offering open-access pilot-scale manufacturing of silicon photonics
- ✓ Rich portfolio of platforms with their complementary strengths
- ✓ Full value chain in EU: electronics, photonics, packaging
- — No pure-play high-volume and high-end silicon photonics fab today

Ecosystem status: assembly and packaging

- 70% of the costs associated with silicon photonic device production arise during this packaging process
- Rapid evolution of technologies and solutions
- Toolmakers have emerged
- Less investment and lack of standardization



Photonics Spectra

Ficontec PIC Assembly Tool

Ecosystem status: assembly and packaging

Europe's position

✓ Know-how, expertise both a pilot-scale and beyond

✓ EU equipment providers for assembly and packaging

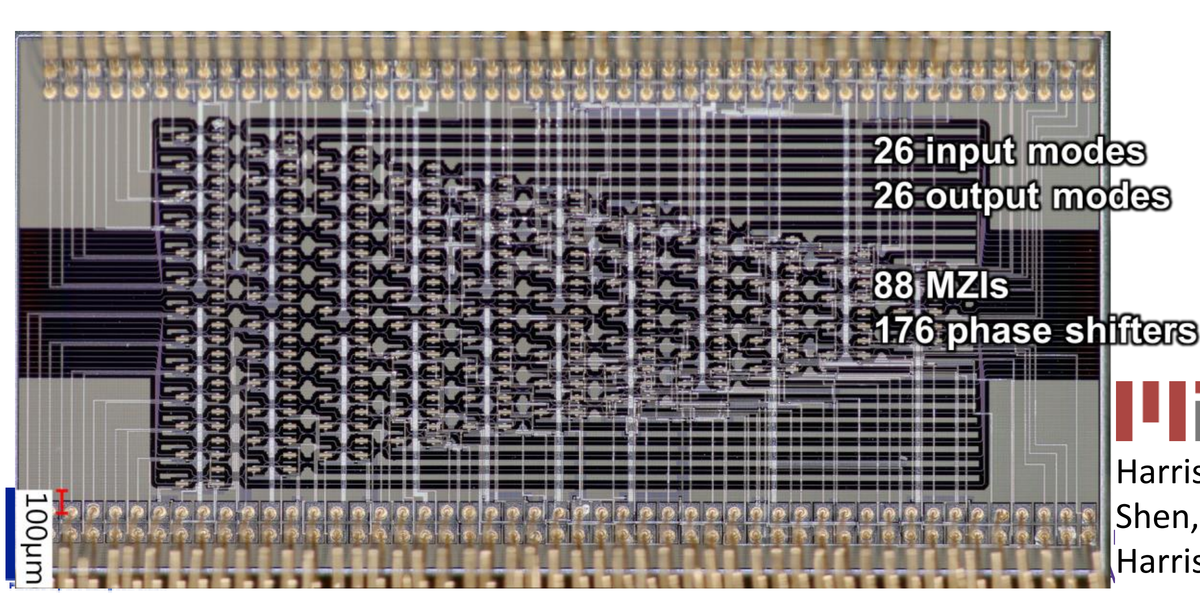
— Lack of co-design tools and lack of experts

— Dominance of outsourcing to Asian suppliers

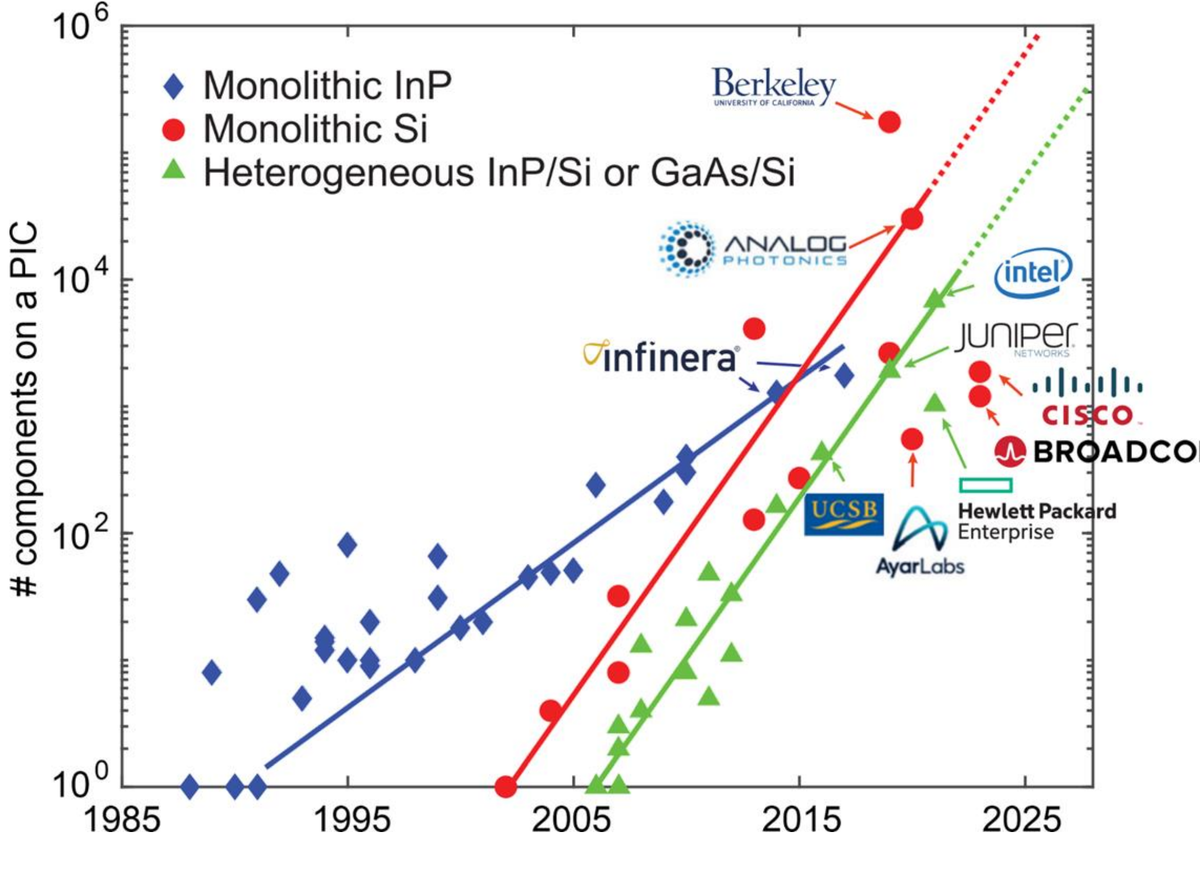
Future trends in silicon photonics

Future Trends - Large-scale photonic integration

- Growing order of integration; 10Ks of components
- photonics + electronic drivers
- different applications (AI, ML, LiDARs, Computing)
- Small chip volumes (compared to electronics)



Harris et al, Nature Photonics 2017
Shen, Harris et al, Nature Photonics 2017
Harris et al, Optica 2018

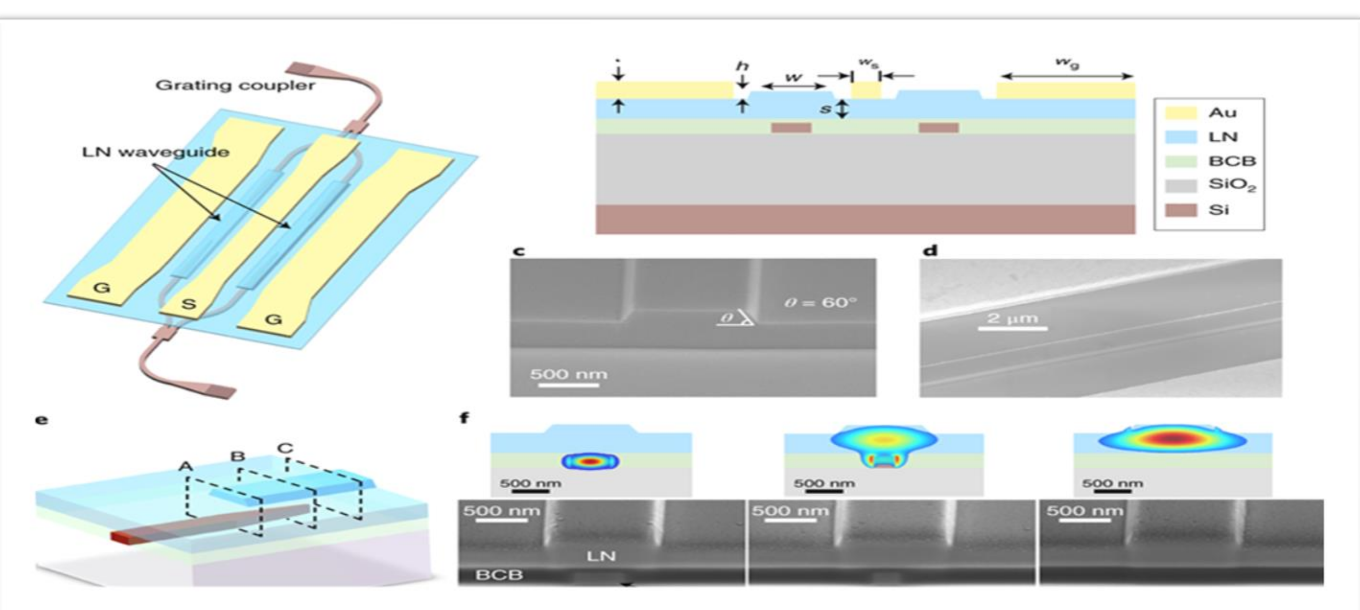


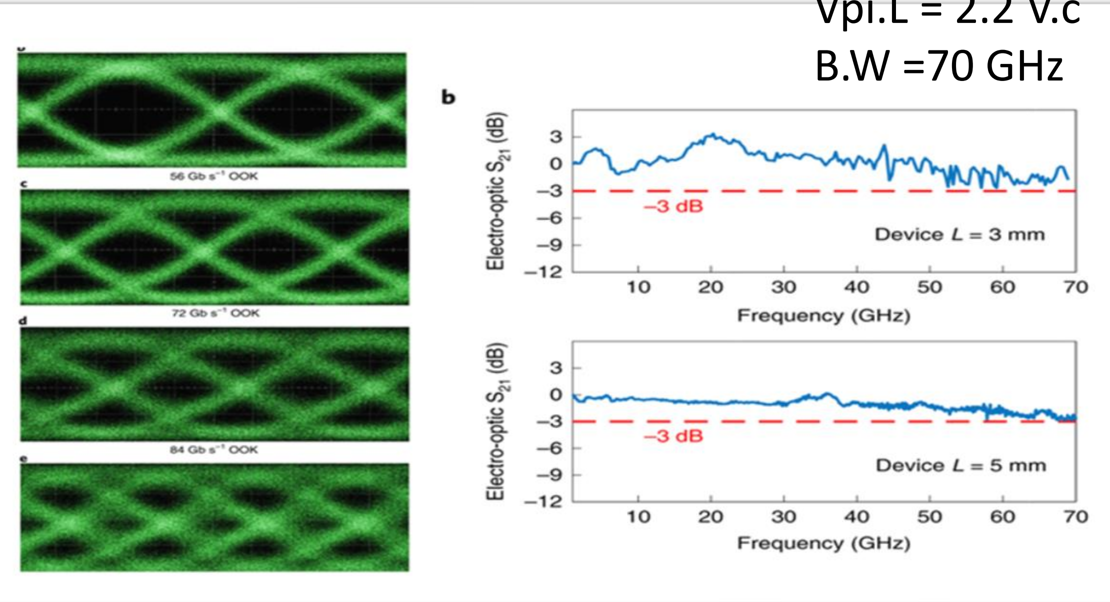
Margalit et al, APL, 2021

Future Trends - Heterogenous silicon photonics

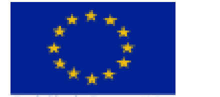
- Wafer-scale integration of novel materials to boost the performance of silicon photonics building blocks
  - Example: high-speed phase modulator

I.L = 2.5 dB
Vpi.L = 2.2 V.c
B.W =70 GHz



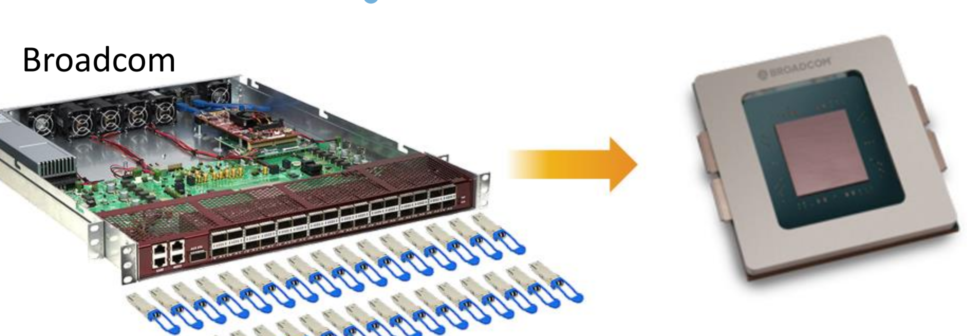


https://www.nature.com/articles/s41566-019-0378-6



Future Trends - Enhanced intimacy b/w electronics and photonics

Broadcom



Co-Packaged Optics

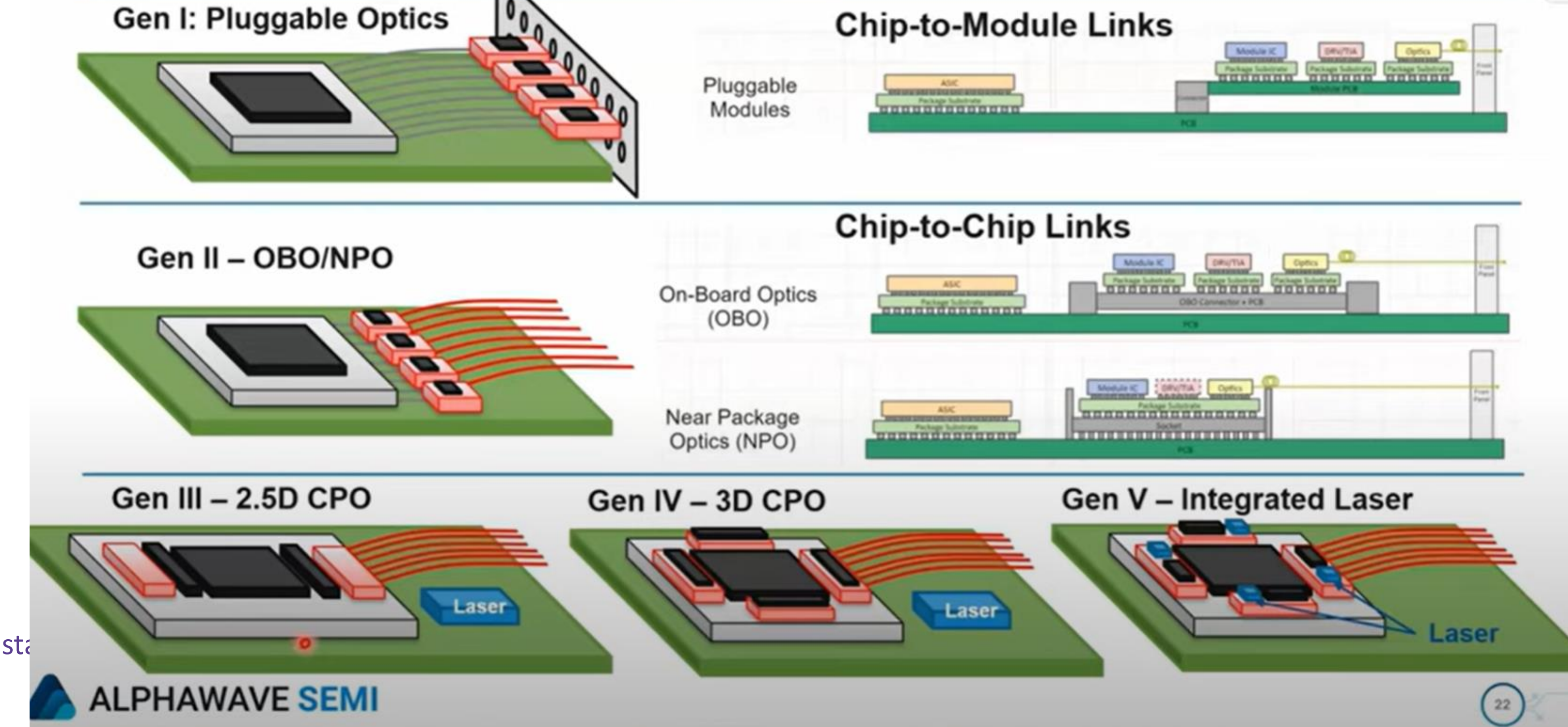
- Integration of optical engines on a common package substrate
- Objective: alleviate the "interconnect density bottleneck"

→

- Low power
- Low cost
- Low latency
- Higher IO bandwidth

Challenges:

- Power heat management in ASIC
- Complex assembly
- Difficult field service
- Restricts competition with concentrated R&D to a few companies



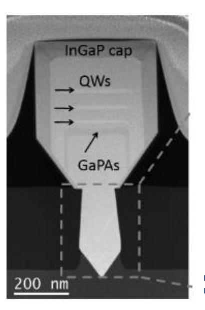
Future Trends - Light source integration

LaMP

- ✓ Use mature III-V technolog…
- ✓ Wafer level test on source…
- ✓ Known good die
- — Fairly efficient optical cou…
- — No waveguide-in / wavegu…
- — Sequential population of S…
- — Can be integrated on back…

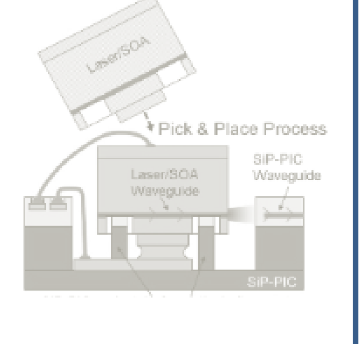
III-V integration using hetero-epitaxy

- ✓ Front end monolithic integration
- ✓ Efficient evanescent coupling
- — Develop completely new process flow
- — Demonstrate yield and reliability



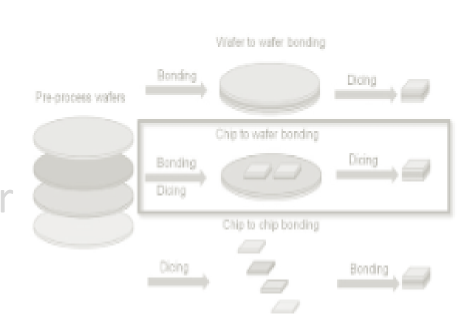
Flip-chip Integration

- …logy
- …rce
- …upling
- …f SiPhwafer
- …es difficult
- … removal



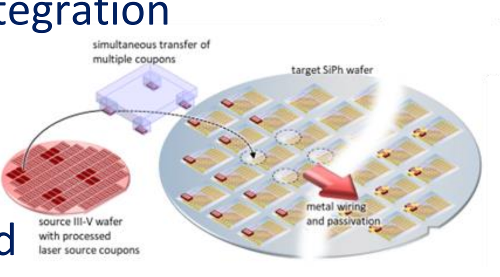
Die-to-wafer bonding

- ✓ Efficient optical coupling
- ✓ Waveguide in-out devices
- ✓ Parallel processing of devices
- ✓ Wafer-level test on target wafer
- — III-V processing on target wafer
- — No known good III-V die
- — Front-end / back-end NRE



Micro-transfer printing

- ✓ III-V process & test prior to integration
- ✓ Back-end integration
- ✓ High throughput integration
- ✓ Efficient evanescent coupling
- — Supply chain being established
- — To demonstrate yield and reliability



Summary

- There is a diversity of platforms available in silicon photonics
- Heterogeneous integration provide routes to boost the performance of silicon PIC building blocks
- Datacom/telecom is the major driver today. Other applications are on the horizon
- European silicon photonics eco-system is in a decent shape but has limited design houses, and also lacks an open-access high-volume commercial foundry service.

THANK YOU

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