EU Chips Act

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European Commission

ICOS Workshop

Grenoble, 26 April 2023

Semiconductor in EU
Design and production

- Post-pandemic **chip shortages** revealed **fragility** of supply chain
- Concentration in Asia and geopolitical tensions expose EU to supply **disruptions**
- **Capex** investments in EU have stagnated, share falling below 10%
- EU has no fab (and few designs) in **advanced nodes**: weaknesses in the most relevant stages of the value chain
- Demand will keep growing steadily, market reaching USD 1 Trillion by 2030

Digital Decade Target: **Double EU share** in global **semiconductor production** to **20% by 2030**

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The EU Chips Act

> *We will present a European Chips Act…*
> *This is not just a matter of our competitiveness.*
> *This is also a matter of **tech sovereignty**.*
>
> *Commission President Ursula von der Leyen*

Vision

To jointly create a **state-of-the-art** European chip ecosystem, that includes world-class **research**, **design** and **production** capacities

Key objectives

- strengthen **research and technology** leadership
- build and reinforce **innovation capacity** in design, manufacturing and packaging
- put in place framework to increase substantially **production capacity** by 2030
- address the acute **skills** shortage, attract new talent
- develop mechanism to monitor **supply chain** and intervene if needed

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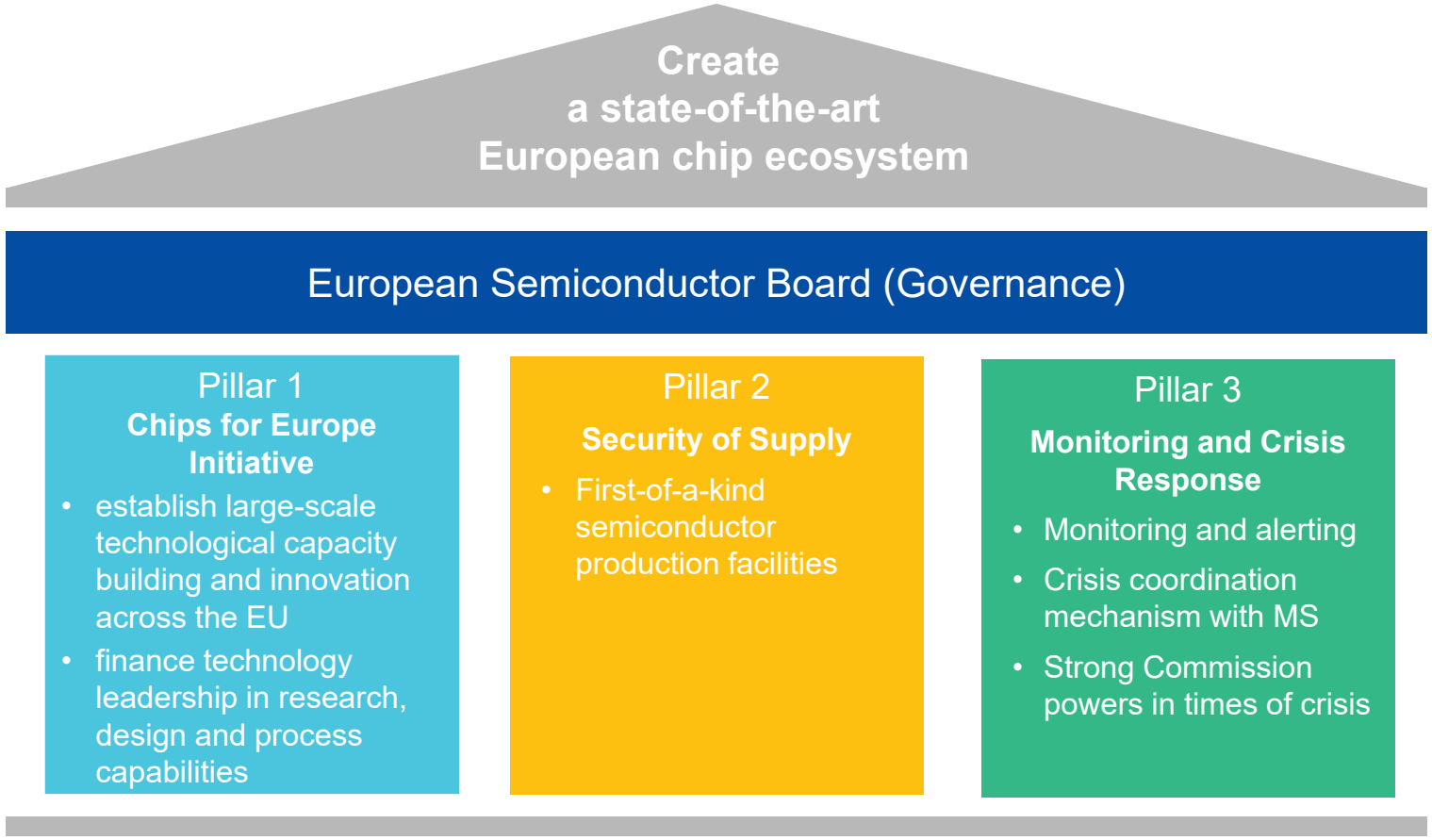
Three pillars of the Chips Act



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EU Chips Act

- Context
- Pillar 1
  1. Design Platform
  2. Pilot Lines
  3. Quantum
  4. Competence Centres
  5. Chips Fund

- Pillar 2
  - Security of supply
- Pillar 3
  - Supply chain monitoring
  - International cooperation

European Commission

Pillar 1

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Chips for Europe Initiative
Rationale for the Initiative

Situation today

- EU is strong in R&D, RTOs and in manufacturing equipment
- R&D supported by EU and Member States with ~4 B€ in MFF programmes

What is the EU missing

- Capability for translating R&D excellence into new markets
- Industrial capabilities in leading-edge design and manufacturing
- Market pull

- EU + MS programmes cover R&D and innovation
- Measures to help **bridge the gap to market** are required

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Chips for Europe Initiative
Aim: bridging the gap from lab to fab

5 Objectives

1. Reinforce design capacity by providing a **virtual design platform**
2. Enhance existing and developing new **pilot lines**
3. Accelerate the development of **quantum chips**
4. Expand **skills** and set up a network of **competence centres**
5. Facilitate SME access to **equity and loans** through a dedicated **Chips Fund**

Chips JU

EIC
I-EU

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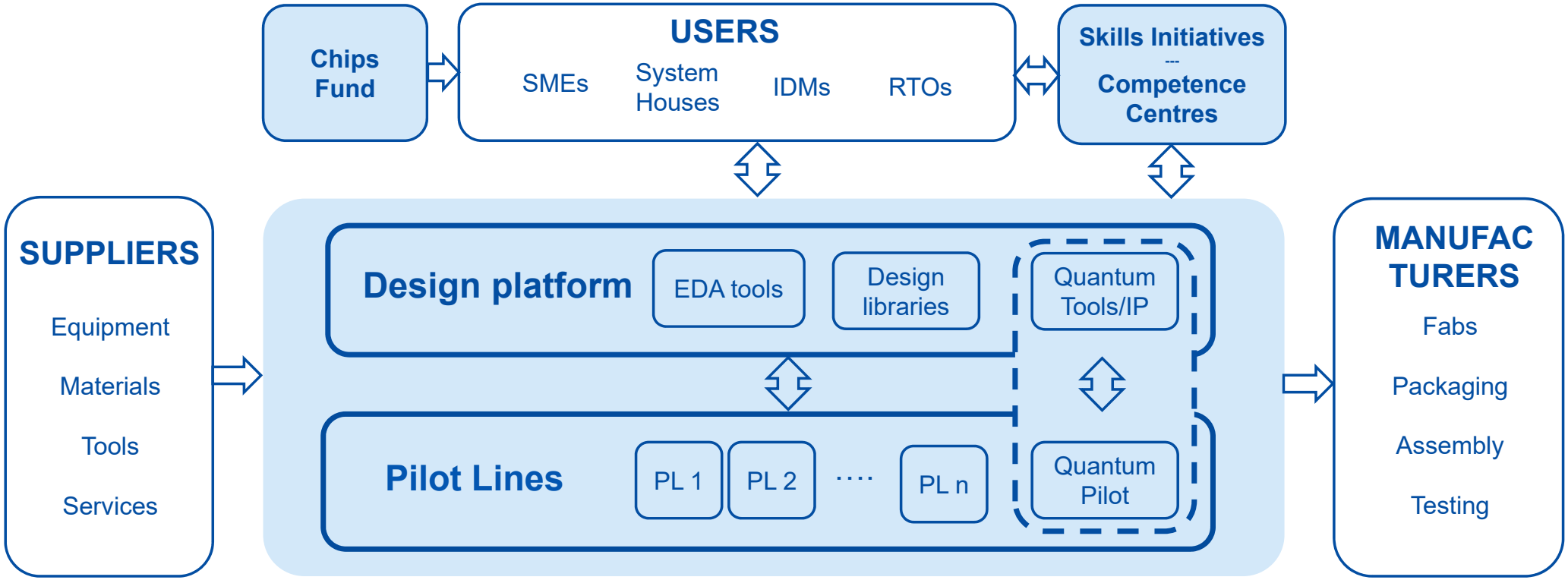
Chips for Europe Initiative
Bridging the gap from lab to fab



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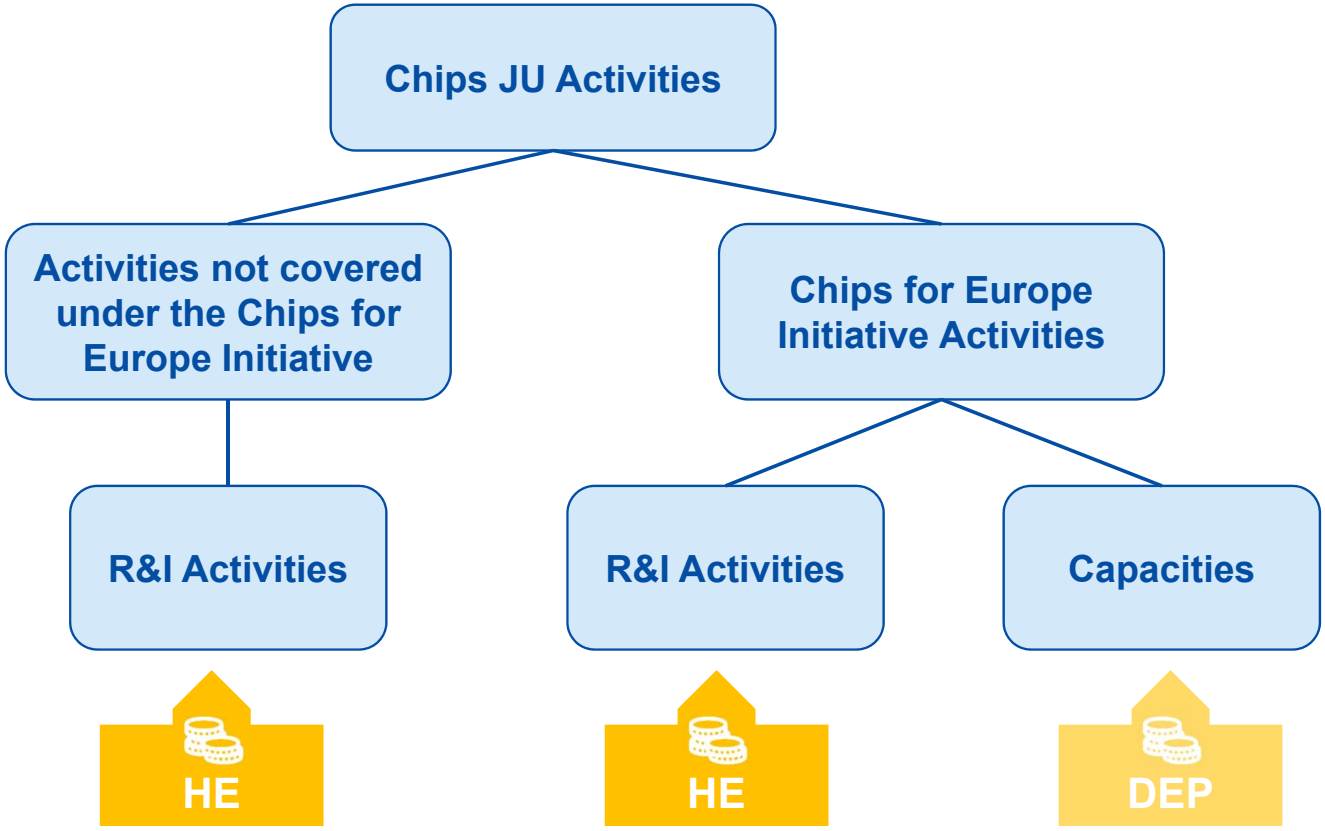
Future “Chips JU” Activities

Chips for Europe Initiative



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Pillar 1

1- Design Platform

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Design platform - scope

Ambition

Foster the development of the semiconductor **design ecosystem** in EU, reinforcing capacity to innovate and create European Intellectual Property through IC design

Main scope

- **Reduce entry barriers** and administrative burden for EU companies engaging in chip design
- **Facilitate access** to pilot lines and manufacturing facilities
- Foster **collaboration** among EU stakeholders, also on new IP and tools (incl. open-source, quantum)
- **Access** to network of **competence centers** offering **training** and support to boost design skills

Instrument

Develop a **virtual design platform,** offering **cloud-based** access to tools, libraries and support services to accelerate development and reduce time-to-market

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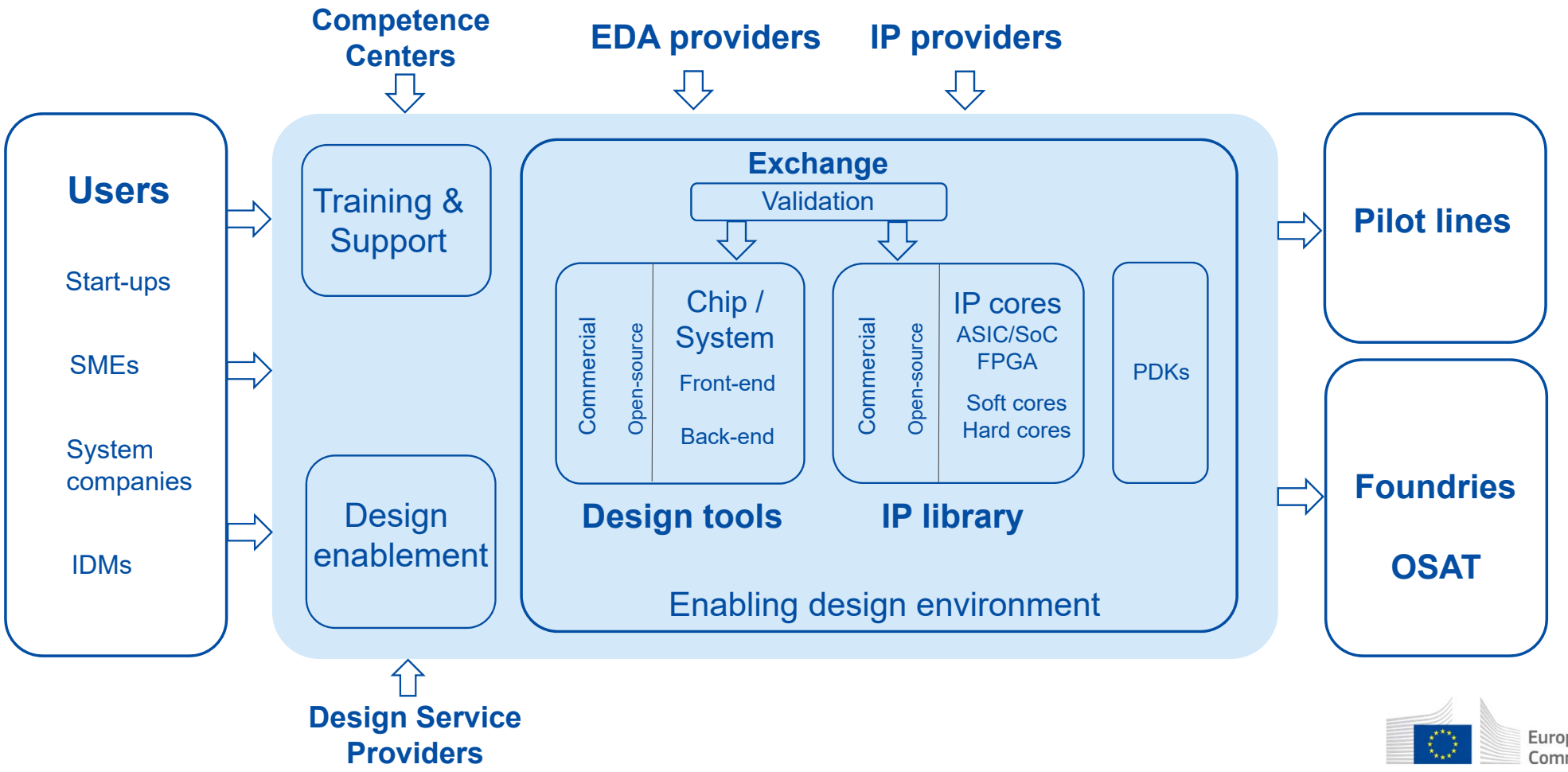
Design platform



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Pillar 1

2 - Pilot Lines

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Pilot Lines
Semiconductors R&I challenges

EU semiconductor ecosystem: limited capability to convert **excellence in research** into **industrial innovation**

- *Existing R&D **instruments** not offering a path **from lab to industrialisation***
- *Semiconductor development is **costly and risky,** particularly in early stages*
- *Opportunities in **emerging trends** not always seized on time*

Pilot Lines can be the response to these challenges

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Pilot Lines in the Chips Act

1. Support development of advanced pilot lines for deployment of next-generation semiconductors
2. Provide industry a facility to test, experiment and validate novel semiconductor technologies
3. Public investments required to accelerate uptake by offsetting the risk of new technologies

- **Access conditions**: Open, non discriminatory, cost efficient
- **Design support**: PDK, ADK, (virtual) prototyping, functional experimentation, validation…
- **Skills**: contribution of pilot lines to on-the-job training, mobility of researchers

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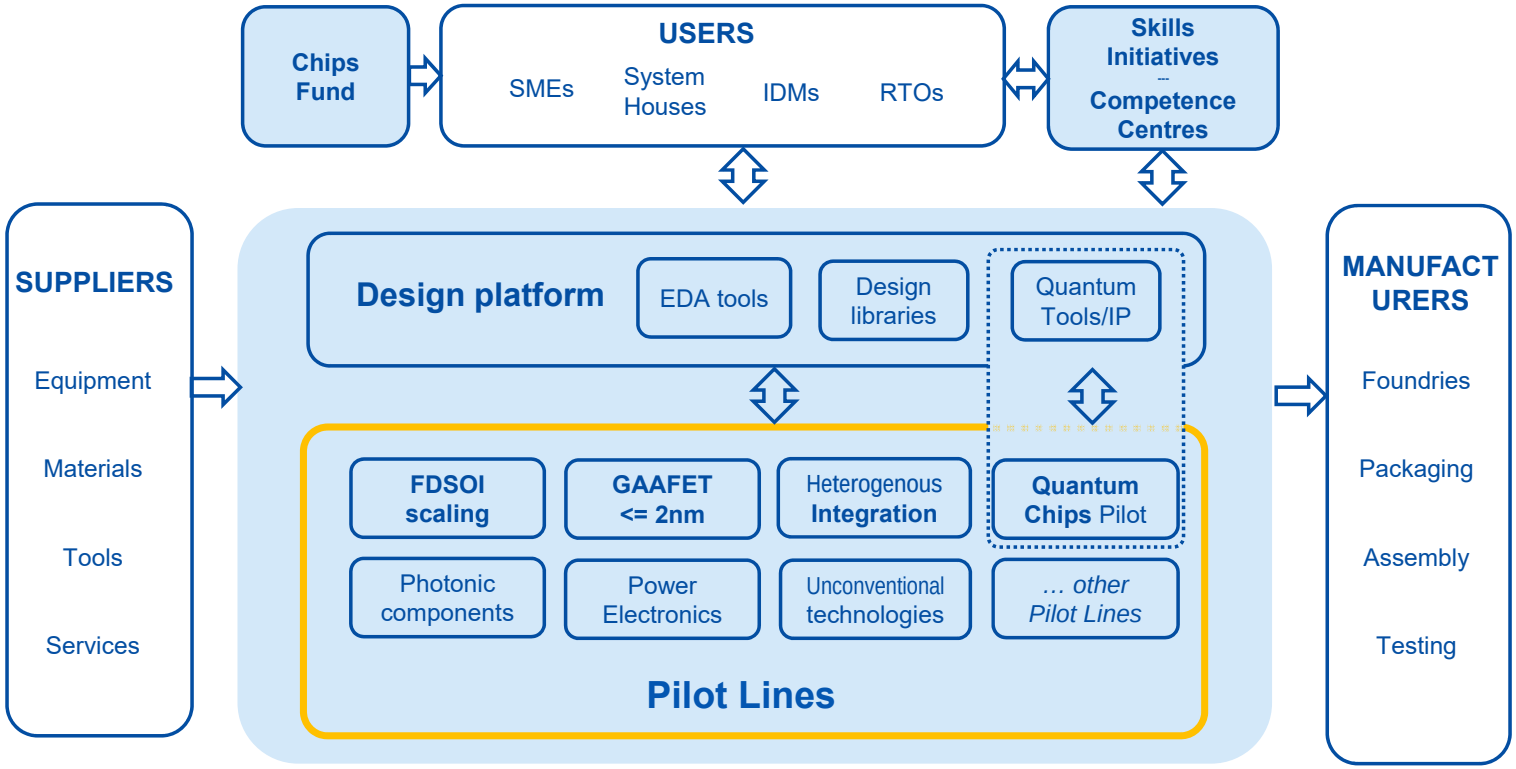
Pilot Lines in the Chips Act



Pilot Line Infrastructure

Central role:

- *Scaled FD-SOI down to 10nm and below*
- *Leading-edge process at 2nm and below*
- *Advanced Het. System Integration*

Other technologies:

- *Quantum*
- Photonics
- Power
- …

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Pillar 1
4 – Competence Centre / Skills

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Skills in the Chips Act

- **Chips JU** dedicated calls, in collaboration with **Member States**:
  - Public awareness campaigns
  - Scholarships and Traineeships
  - Free training, upskilling and reskilling programmes
  - Training and support programmes for SMEs
  - Link with complementary mobility under Erasmus+
- Many actions will be coordinated by the **Competence Centres**

*A **DEP call** on the above topics is already foreseen in Q3 2023*

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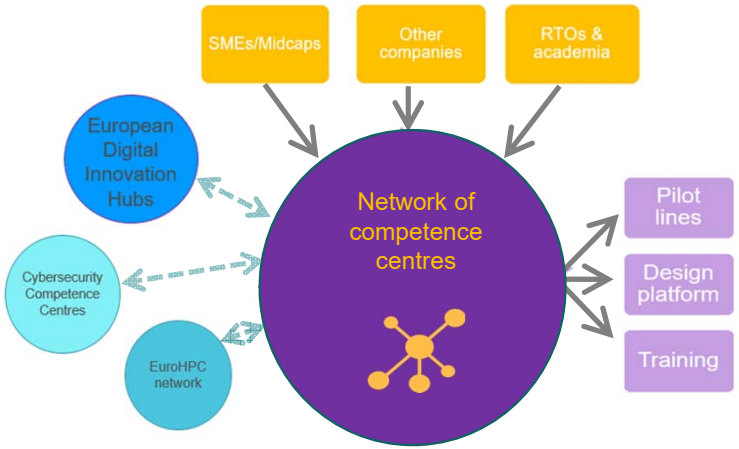
EU Network of Competence centers



Role of Competence Centers

- Provide access to **training**, including upskilling and reskilling
- Act as reference for own area of **expertise**
- Match **user needs** with available expertise in the network
- Facilitate access to **design platform** and **pilot lines**
- Support technology **transfer**
- Raising **awareness** on international programmes, promoting **services**, **funding** opportunities

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EU Network of Competence centers

- Member States designate candidates
- Single organisation or coordinated group with complementary expertise
- Non profit organisation (RTOs, Uni's)

- Synergies with EDIHs, can become CCs
- Governance autonomy, in line with objectives of the Initiative

EU support for at least one centre per Member State

Co-investment with Member States and Regions

Supporting industry and public services

Access to design platform and pilot lines

Focus on Semiconductors Skills

A strong European network of Competence Centres

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Pillar 1
5 – Chips Fund

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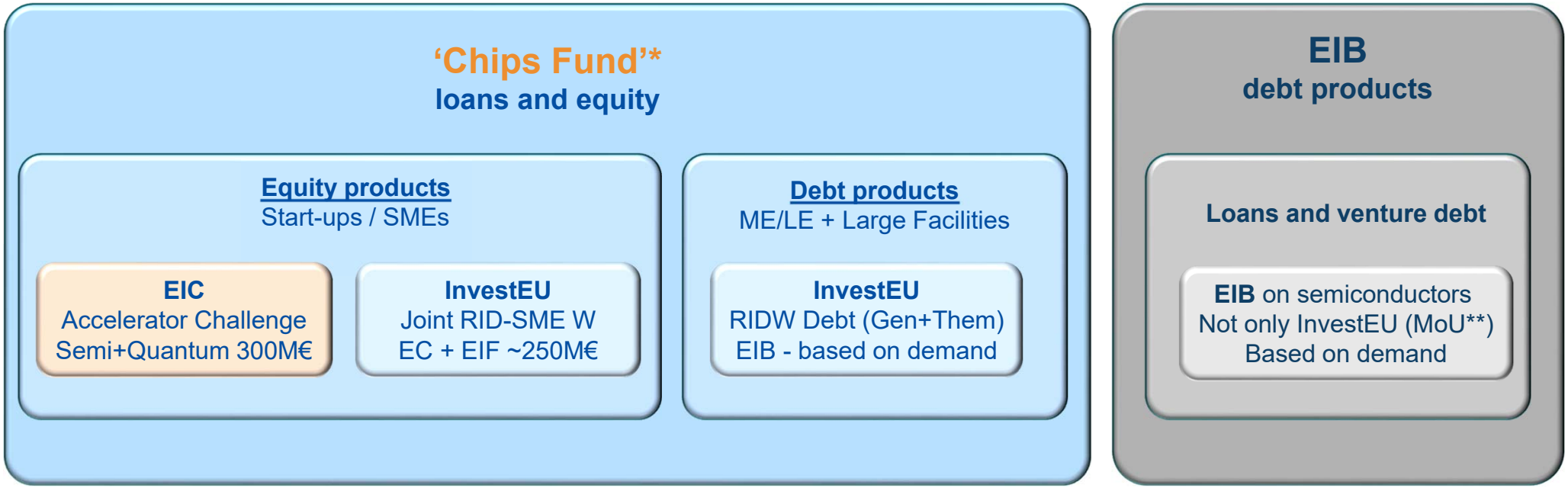
The “Chips fund” investment facility



* The “Chips Fund” will be implemented through an investment facility Fund and eligibility criteria are in current EIB group mandates

** An MOU between EIB and EC for investments in semiconductors has been signed upon the Chips Act presentation (8/2/’22)

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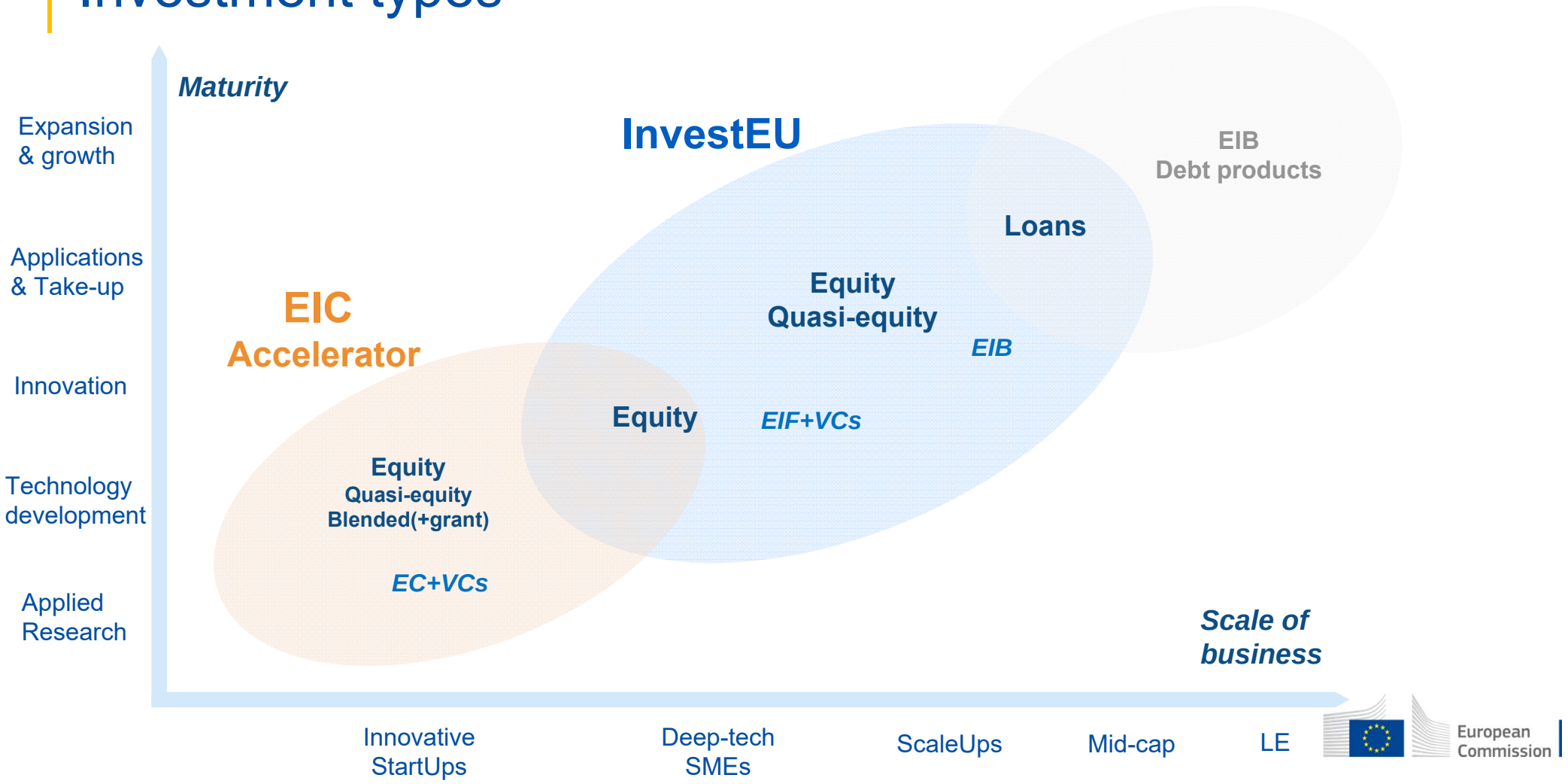
Chips Fund
Investment types



Pillar 2

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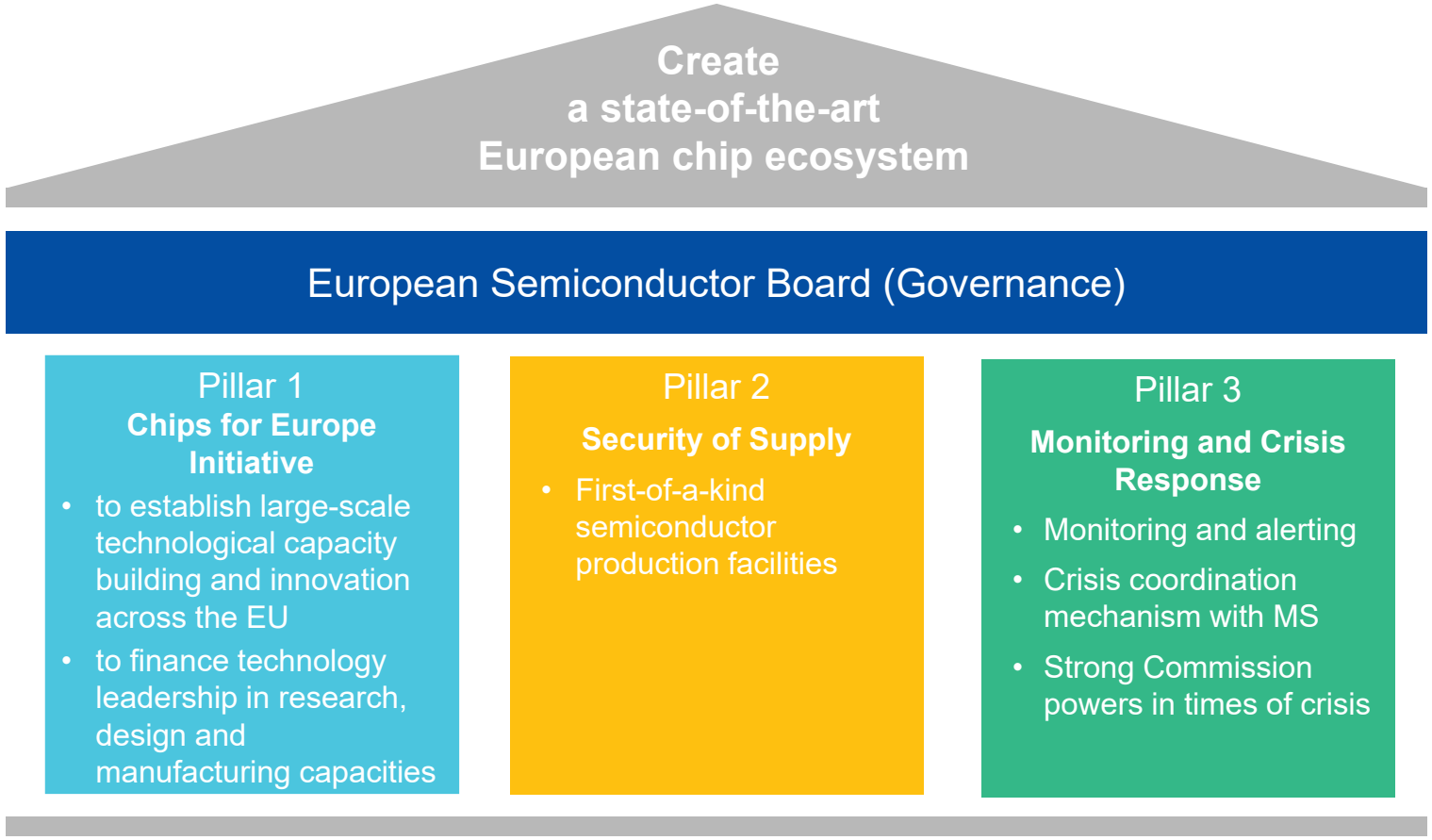
Three pillars of the Chips Act



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Pillar 2 - Security of supply and resilience
Facilitate investments in manufacturing facilities

State aid *distorts competition and is prohibited in the Union (TFEU) - unless justified by economic development needs*

First-of-a-kind facility: to qualify, facility needs to offer innovation in terms of products or process that is not yet present in the Union (not to distort competition)

Conditions: positive impact, security of supply and commitment to next generation

Integrated Production Facility (IPF)

First-of-a-kind facility which produces the chips (mostly) for the same undertaking

Open EU Foundry (OEF)

First-of-a-kind facility that produces chips (mostly) for unrelated undertakings

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Pillar 2 – Security of supply and resilience
First of a Kind facilities: what qualifies

The main stages of semiconductor production may be eligible

Innovation can be in terms of:

- technological performance
- process innovation
- energy and environmental performance

Not only miniaturisation

Relevant projects have been announced already by Intel, ST-Microelectronics, GlobalFoundries, Infineon…

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Pillar 3

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Pillar 3: Monitoring and crisis response

Monitoring stage

- Regular **monitoring** by Member States and update mechanism for alerts by stakeholders
- Coordinated assessment of crisis response measures by **Semiconductor Board**

Crisis trigger

When **assessment of EC provides evidence** of serious supply disruptions entailing significant negative effects on one or more important sectors

Crisis stage

Emergency Toolbox activated: Information gathering, priority-rated orders, export control

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Pillar 3: Monitoring and crisis response

International partnerships

- Semiconductor value chain is global and spread over different world regions
- We need to **cooperate** with like-minded partner countries, proactively managing **interdependencies** to ensure:
  - a reliable global **marketplace** for EU products
  - **security of supply** including in crisis situations

Example: **EU-US Trade and Technology Council**

- Coordinate measures to secure supply
- Exchange information and coordination on:
  - Early warning systems to detect supply issues
  - Industry-led methods to estimate demand
  - Avoid subsidy races
  - Improve understanding of global demand

Digital partnerships with Japan and other Asian countries

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Chips Act – Process

Commission

Chips Act proposal in Feb 2022

Council

- **Industry** CWP and **Research** CWP
- **General Approach in** Dec 2022

Parliament

- ITRE leading 6 Parliamentary **Committees**
- **Plenary vote** in Feb 2023

Trilogue negotiation

Agreement 18 April 2023

Chips Act Adoption

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Thank you

Q&A

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