Nanosheet-based Device Architectures for Enabling Advanced CMOS Logic Scaling

Anabela Veloso

Imec, Kapeldreef 75, 3000 Leuven, Belgium

Email: Anabela.Veloso@imec.be

ICOS International Cooperation On Semiconductors

Outline

- Introduction – CMOS scaling trends
- Nanosheet FET based device architectures:
  - as enabler of further CMOS logic scaling
  - some key device fabrication aspects
  - extension to further scaling options, e.g.,
    - ✓ forksheet configuration
    - ✓ stacking of different polarity devices (CFET)
- Device connectivity using both wafer sides ⇒ towards CMOS 2.0
- Summary

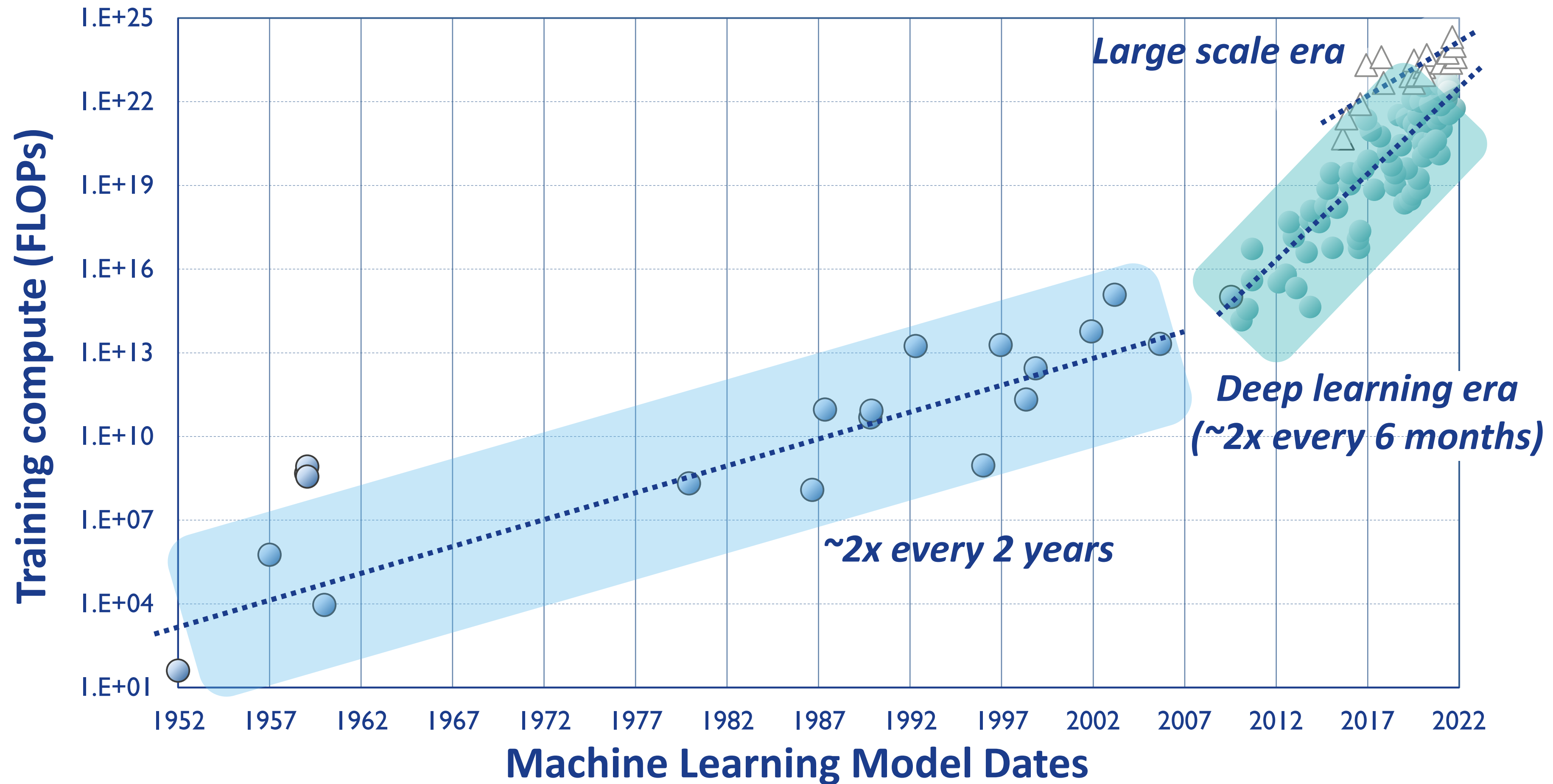
ICOS
International Cooperation On Semiconductors

Outline

- ❑ Introduction – CMOS scaling trends
- ❑ Nanosheet FET based device architectures:
  - as enabler of further CMOS logic scaling
  - some key device fabrication aspects
  - extension to further scaling options, e.g.,
    - ✓ forksheet configuration
    - ✓ stacking of different polarity devices (CFET)
- ❑ Device connectivity using both wafer sides ⇒ towards CMOS 2.0
- ❑ Summary

ICOS International Cooperation On Semiconductors

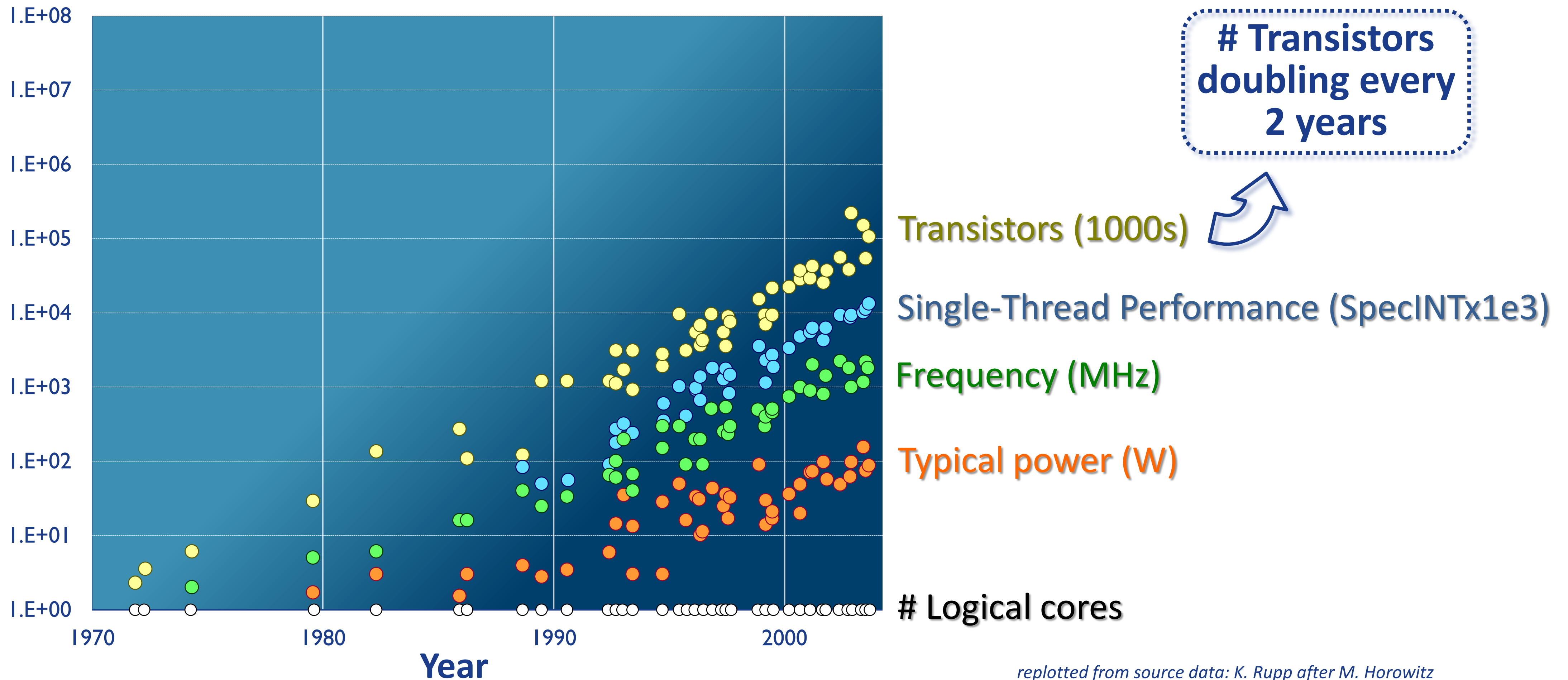
Compute Needs Continue to Grow



Data source: Sevilla et al. https://doi.org/10.48550/arXiv.2202.05924

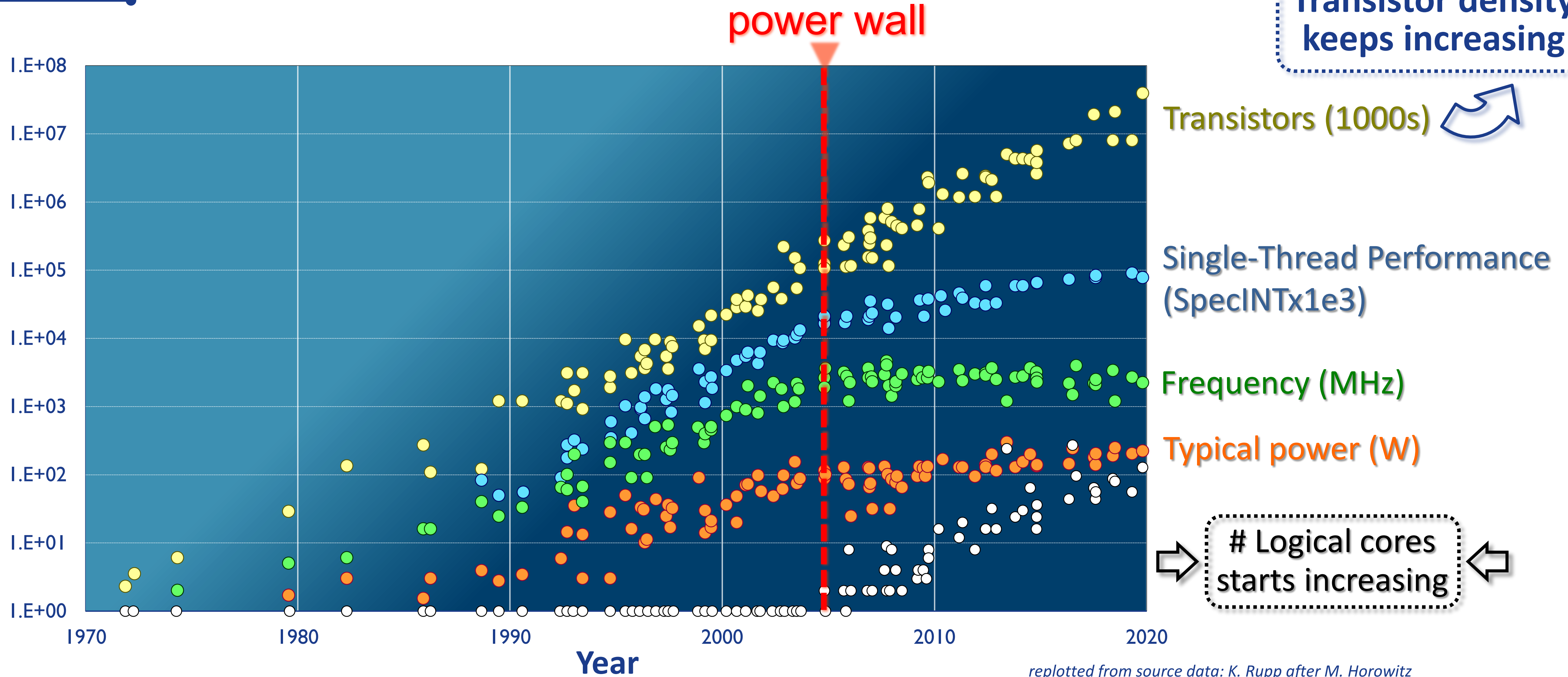
ICOS
International Cooperation
On Semiconductors

Happy Scaling until 2005...



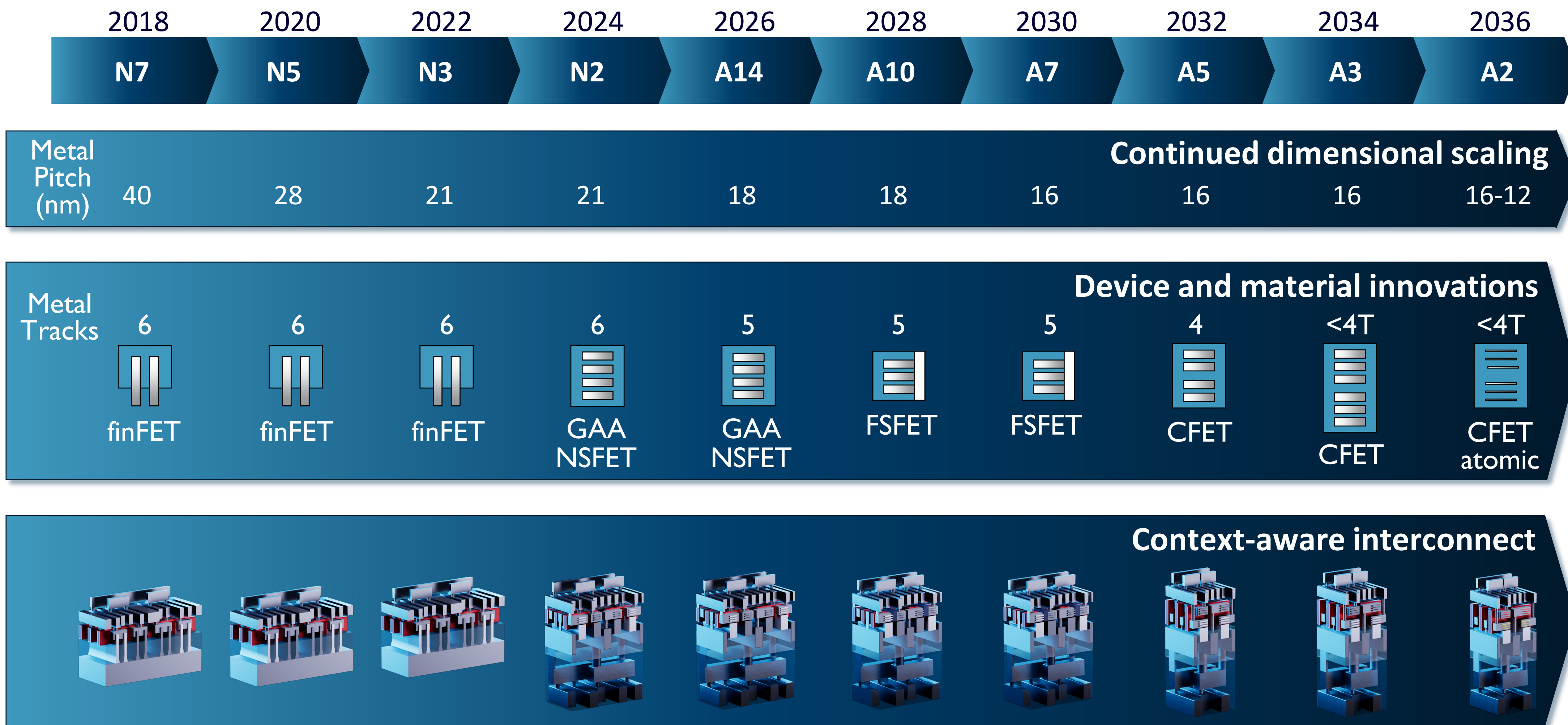
replotted from source data: K. Rupp after M. Horowitz

then Something Changed...



ICOS International Cooperation On Semiconductors

Potential Logic Scaling Roadmap Extension



ICOS International Cooperation On Semiconductors

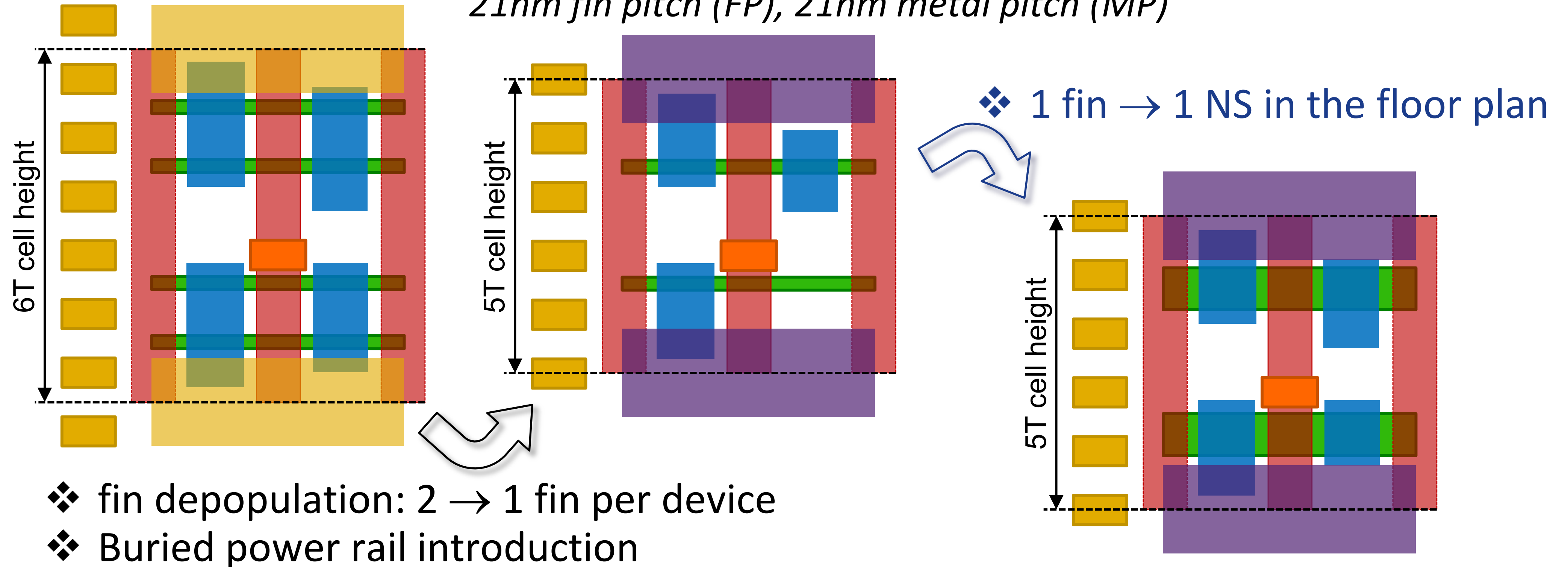
Outline

- ❑ Introduction – CMOS scaling trends
- ❑ Nanosheet FET based device architectures:
  - ❖ as enabler of further CMOS logic scaling
  - ❖ some key device fabrication aspects
  - ❖ extension to further scaling options, e.g.,
    - ✓ forksheet configuration
    - ✓ stacking of different polarity devices (CFET)
- ❑ Device connectivity using both wafer sides ⇒ towards CMOS 2.0
- ❑ Summary

ICOS International Cooperation On Semiconductors

Standard Cell Layout Evolution: FinFETs → NSFETs

N3 design rules assumption: 45nm contacted-gate-pitch (CGP), 21nm fin pitch (FP), 21nm metal pitch (MP)

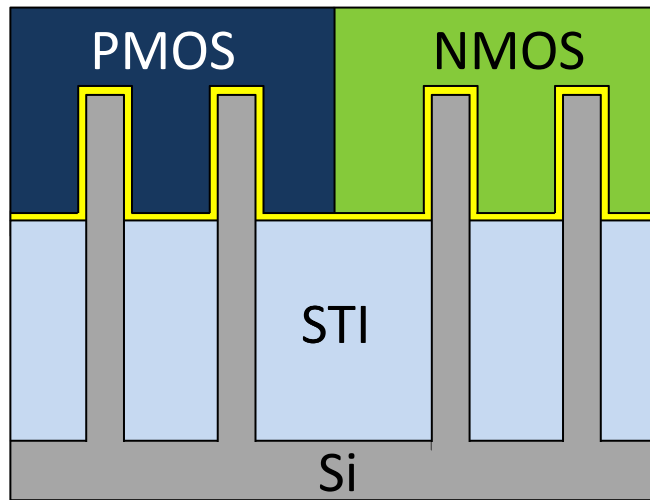


❑ Cell height reduction by decreasing the number of metal tracks is being pursued to compensate for a more modest pitch scaling

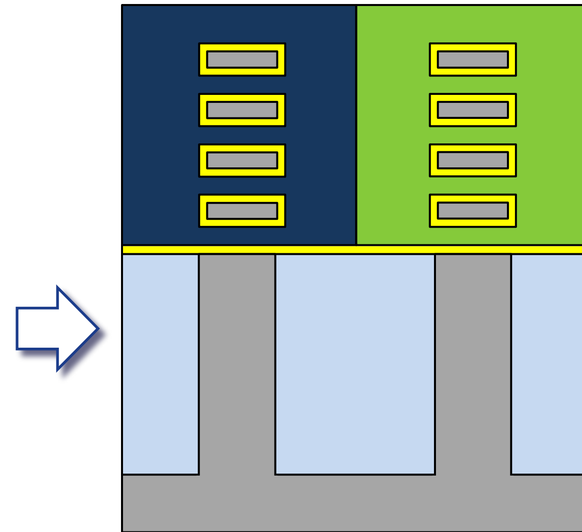
Funded by the European Union

ICOS International Cooperation On Semiconductors

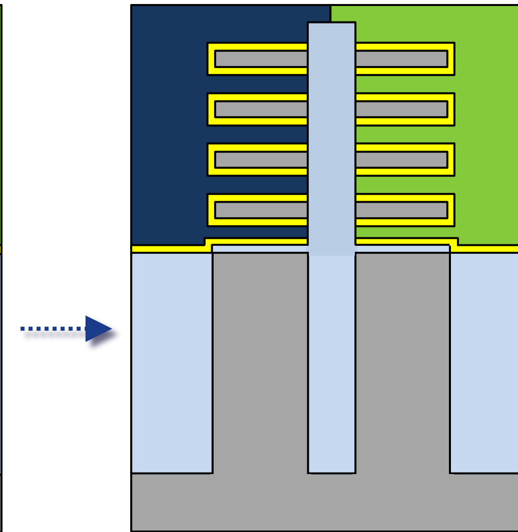
A Possible Transistor's Evolution Path to Help Support the Logic Scaling Roadmap



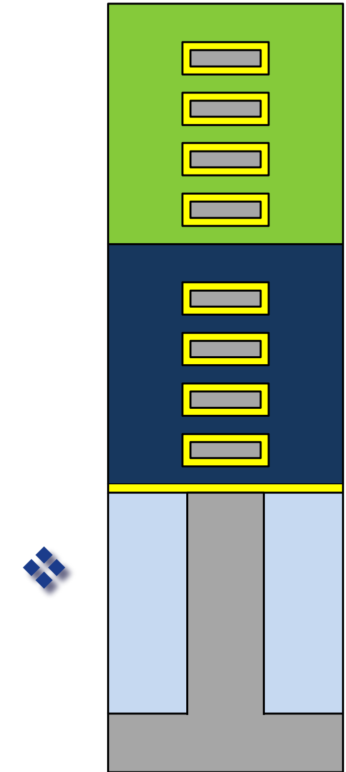
Triple-gate finFETs



Gate-all-around (GAA) vertically stacked lateral nanosheet (NS) FETs

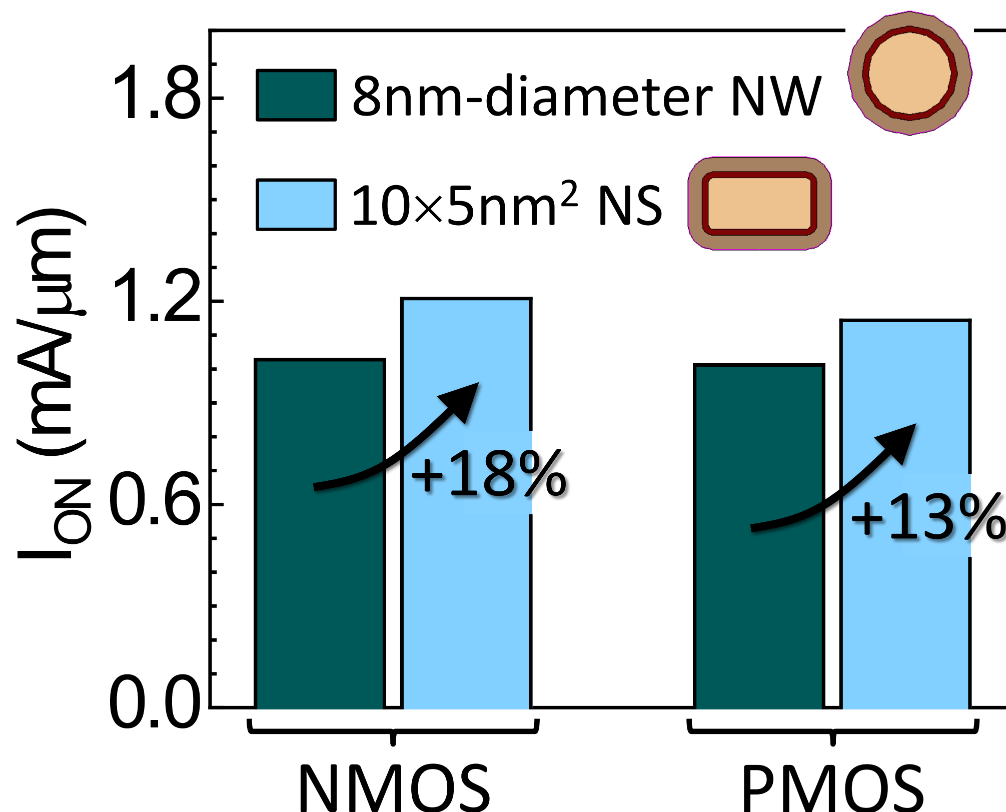


Forksheet device configuration



N/PMOS devices stacked on top of each other (CFET)

Higher Drivability for GAA Nanosheets *vs.* Nanowires FETs



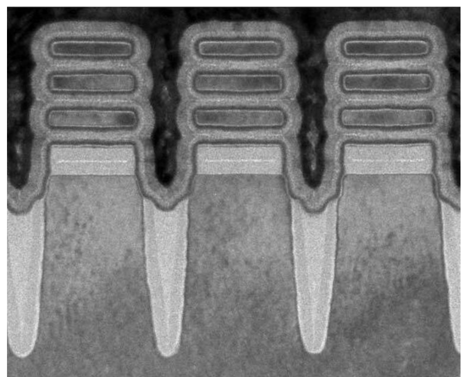
Ballistic current simulations

I_{ON} values normalized by 35nm fin pitch

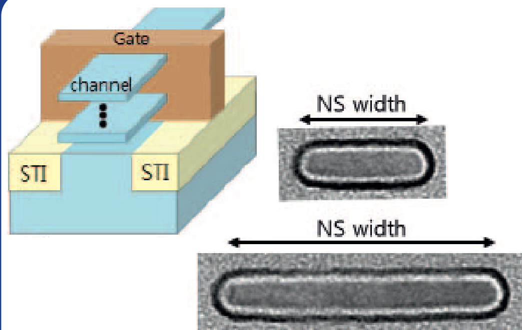
$V_G = V_{G,OFF} \pm 0.75V$
$I_{OFF} = 100nA/\mu m$

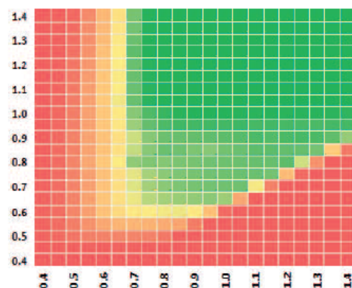
- Significantly higher current drivability, for both NMOS and PMOS, with nanosheets *vs.* nanowires (w/ rectangular *vs.* circular cross-sections, respectively)

Nanosheet FETs in Industry

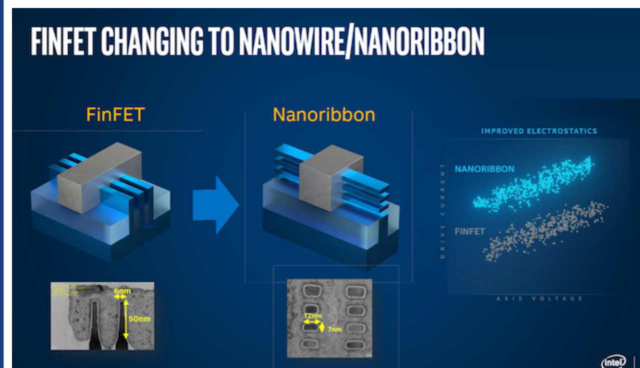


IBM, VLSI 2017, press release 2021

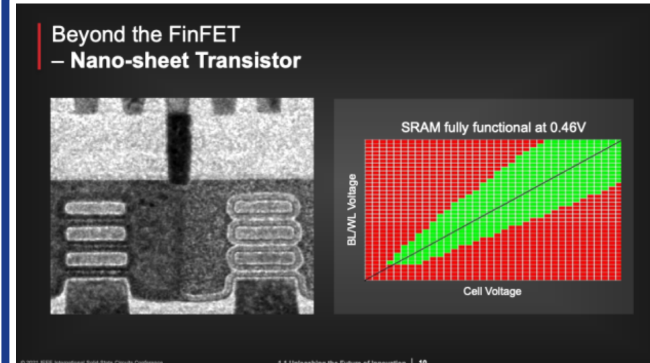




Samsung, IEDM 2018, Foundry Forum 2019



Intel, VLSI 2020

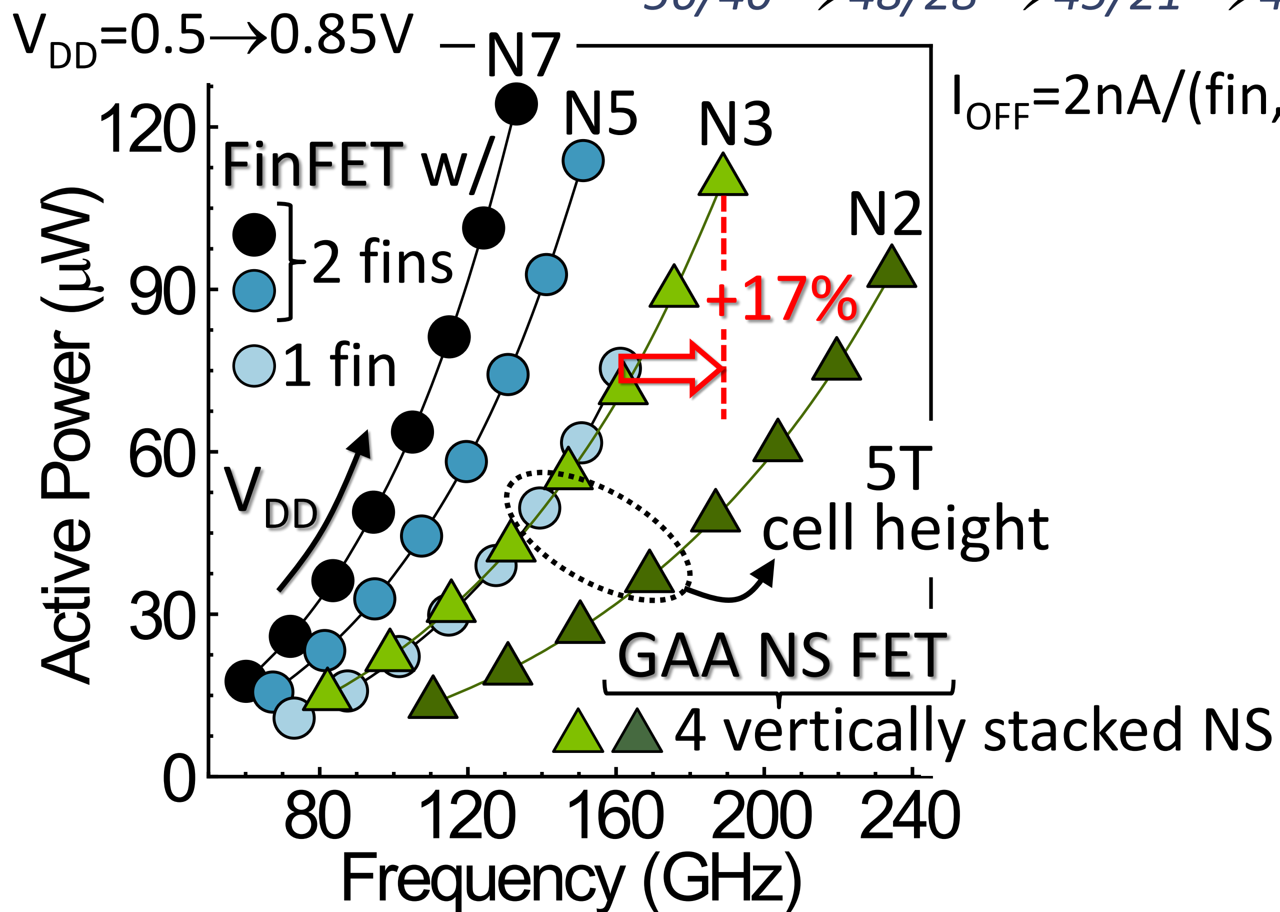


TSMC, 2nm announcement 2020 ISSCC 2021

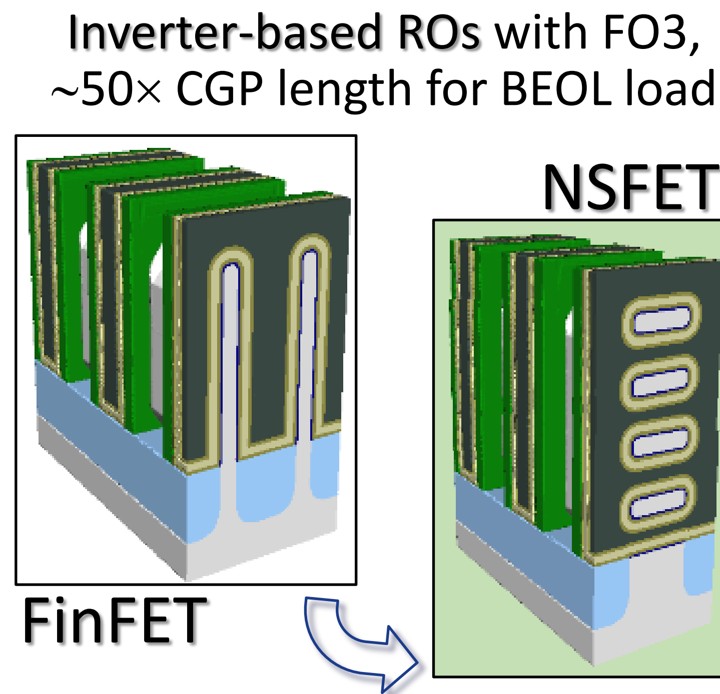
- Nanosheet FETs widely accepted by industry for next transistor generation(s)

Power-Performance: FinFETs *vs.* NSFETs

Assumptions for CGP/MP pitches (dimensions in nanometers):
56/40 → 48/28 → 45/21 → 42/16 for N7 → N5 → N3 → N2, respectively



Inverter-based ROs with FO3,
~50× CGP length for BEOL load

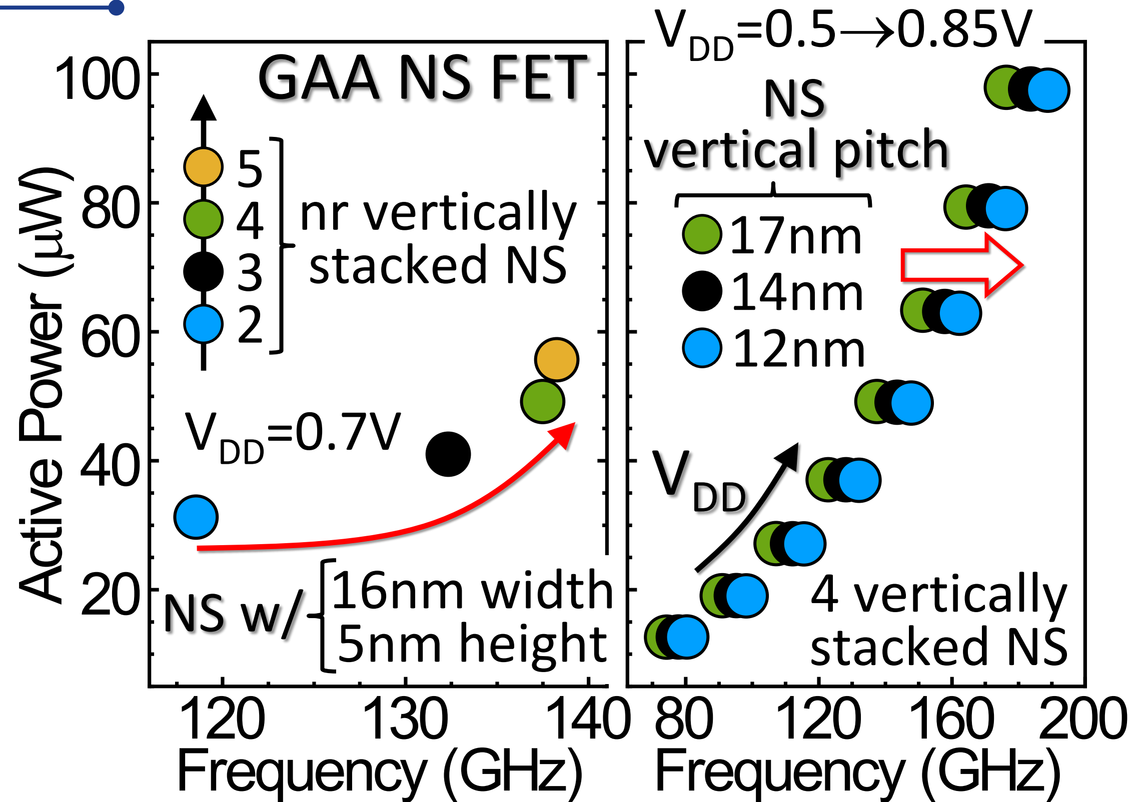


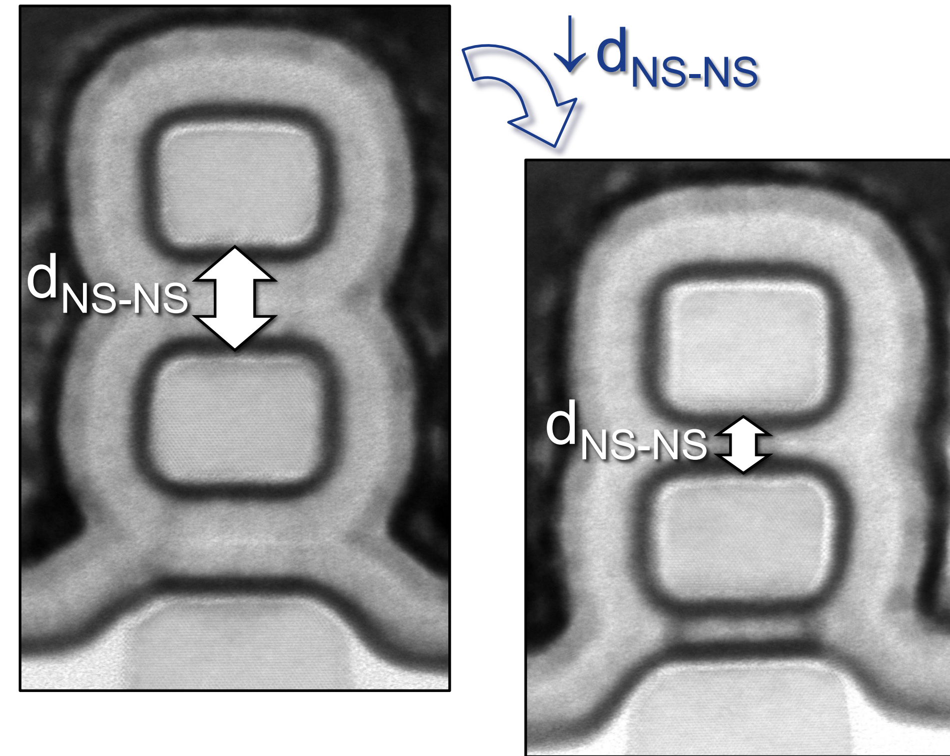
- GAA nanosheet FETs predicted to outperform finFETs at the 3nm node[1]

[1] A. Veloso *et al.*, EDTM 2021

International Cooperation On Semiconductors

Performance Boosting in GAA NSFETs





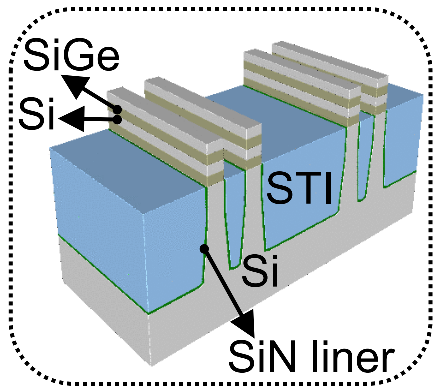
- Increased nr of vertically stacked NS per device ⇒ higher I_{ON} and faster ROs at the expense of increased parasitics and higher power consumption
  - control of parasitics is key, with faster ROs at a given V_{DD} (or power savings at matched performance) enabled by shorter $d_{NS\text{-}NS}$[1]

[1] A. Veloso *et al.*, SSDM 2019

Funded by the European Union

Key Fabrication Steps for GAA NSFETs

fins formation with
Si/SiGe multi-layers



Dummy gate

dummy gate patterning

inner spacers formation

PMOS

NMOS

B-SiGe

P-Si

S/D epi growth

ILD0 oxide

dummy gate removal

Si

SiGe

Si NS release by SiGe removal

EWF metal(s)/W

HfO_2

Si

ILD0

Si

STI

gate stack deposition

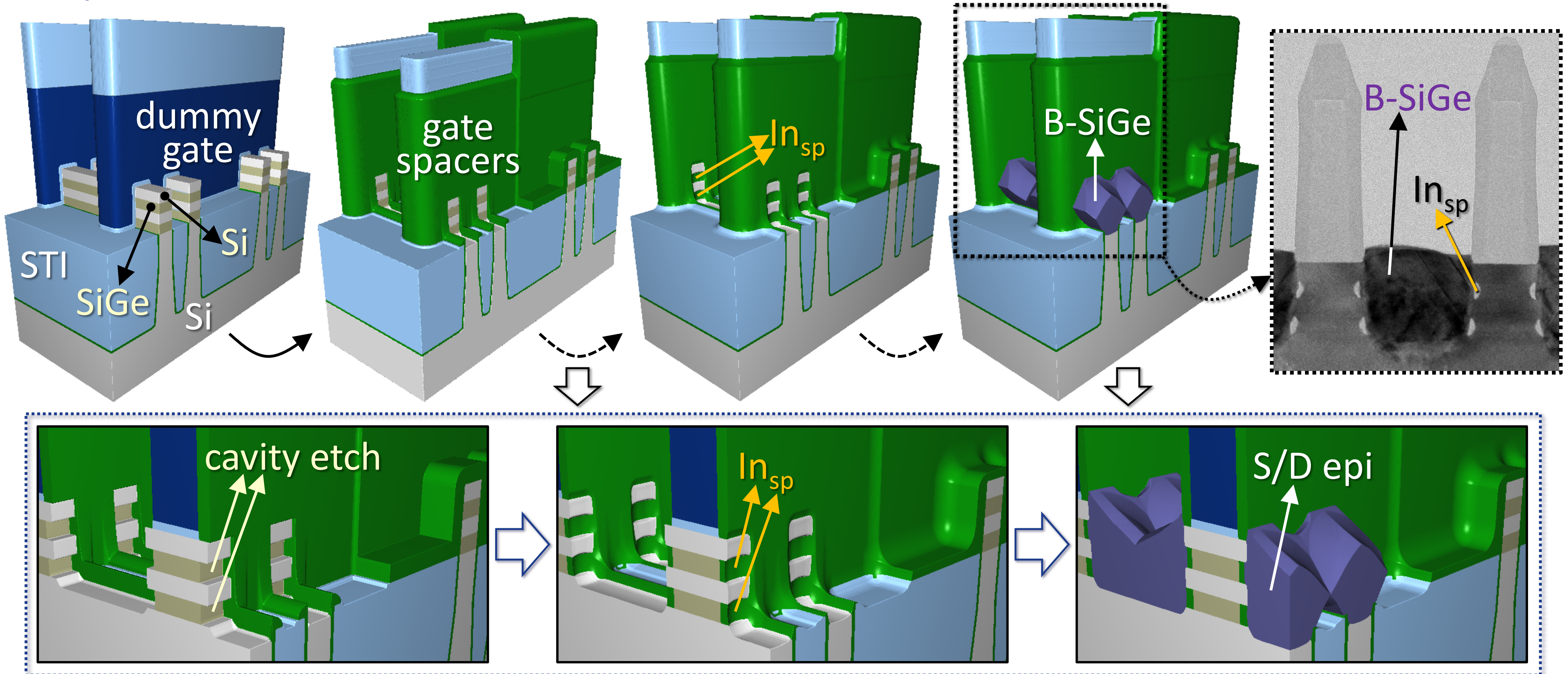
Some critical challenges:

- Si/SiGe multi-layer fins patterning, STI formation, and Si nanosheets release by SiGe selective removal towards Si
- scaled gate stacks for shorter vertical distances between nanosheets
- inner spacers for reduced parasitics
  - junctions & lower $R_{contact}$

Funded by the European Union

ICOS International Cooperation On Semiconductors

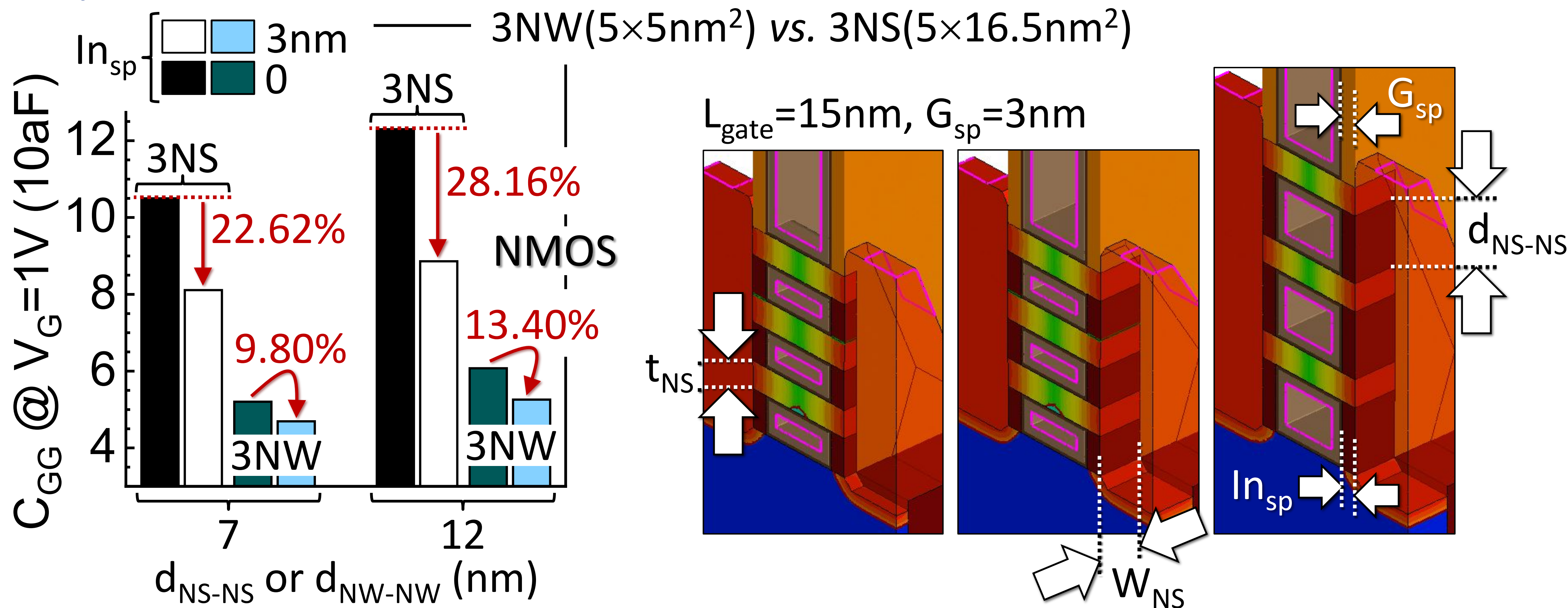
Inner Spacers Implementation in NSFETs



- Inner spacers prior to S/D epi growth: a critical new module in NSFETs

ICOS International Cooperation On Semiconductors

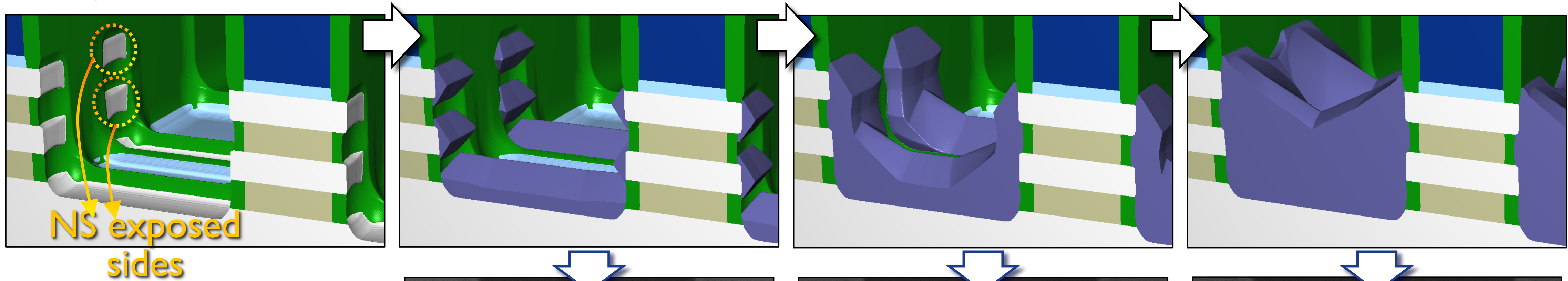
Inner Spacers Impact on Device Parasitics



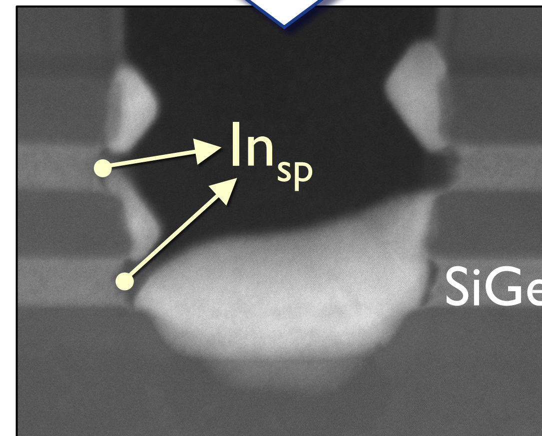
- Inner spacers show higher benefit for wider channels and longer vertical distances between sheets/wires, corresponding to larger In_{sp} volumes[1]

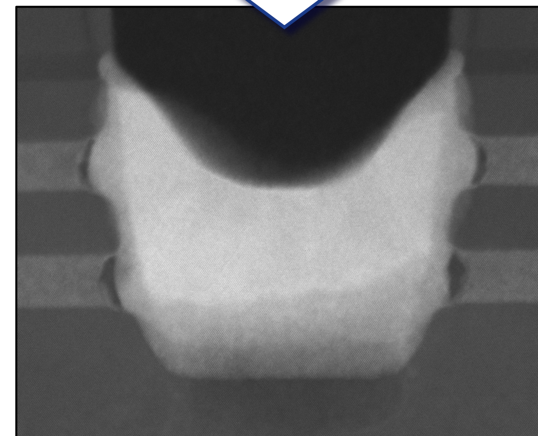
[1] A. Veloso *et al.*, EDTM 2021 and ICICDT 2022

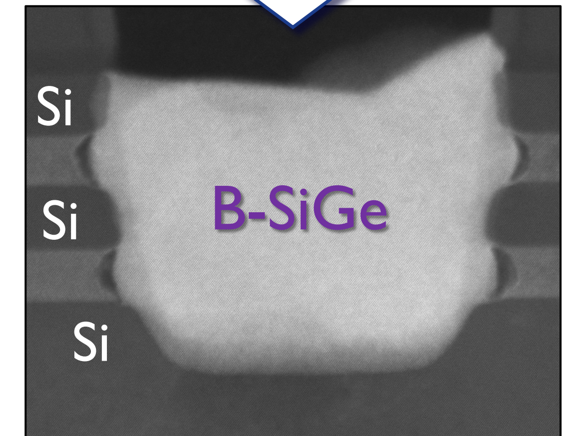
S/D Epitaxial Growth in NSFET Devices



- The profile(s) of the exposed sides of the nanosheets can impact the S/D epi growth



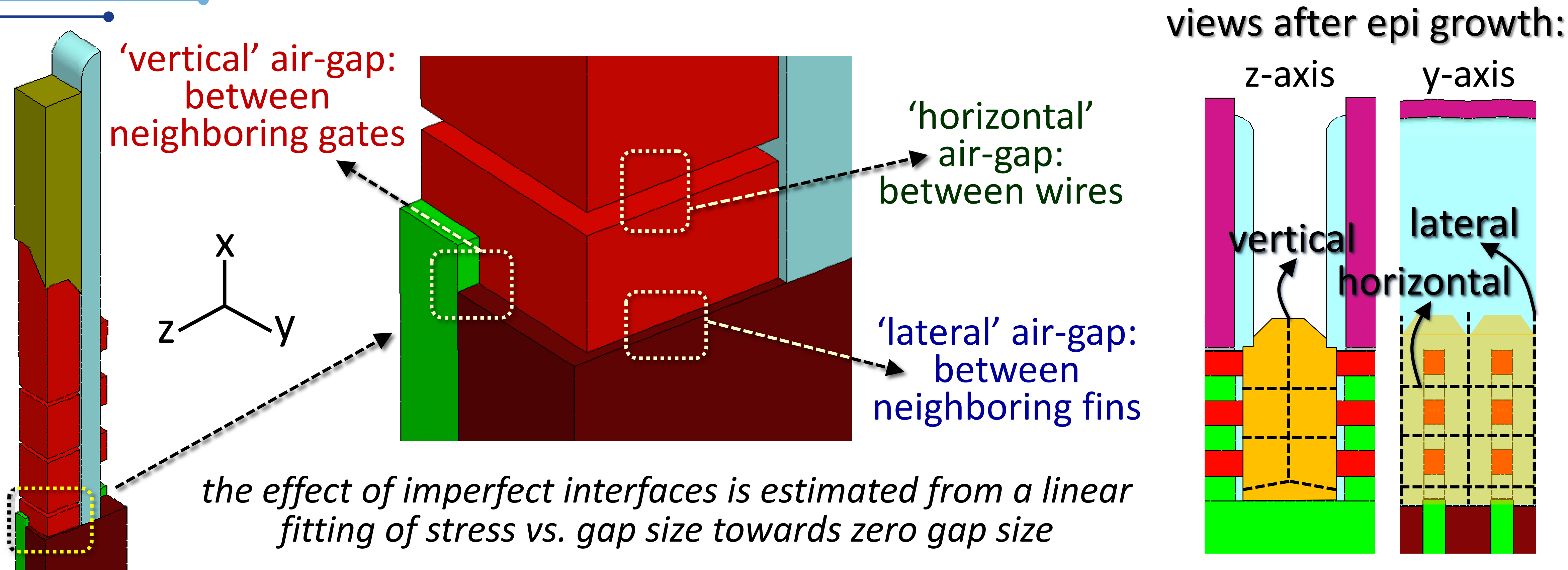




- S/D epi growth in NS FETs with inner spacers ≠ than epi growth in finFETS[1]
  - final epi results from the merger of the epi grown from the bottom Si surface + from the exposed side surfaces of the vertically stacked NS

[1] A. Veloso *et al.*, ICICDT 2022

Assessing S/D Epi Defects Impact on Stress

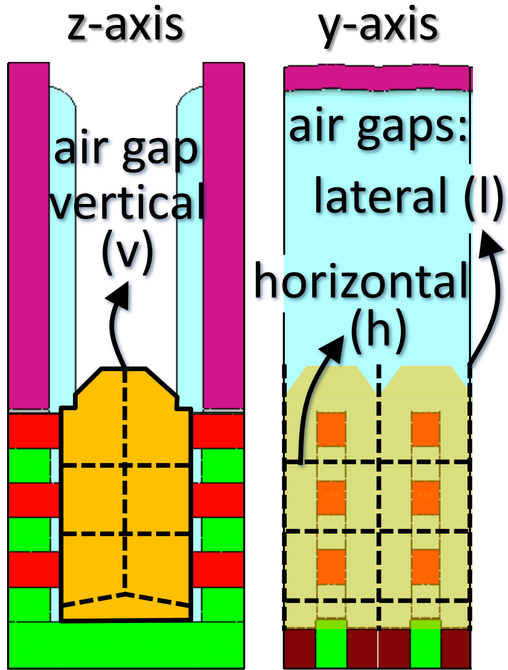


- Epi growth from the NS sides + from the fin's bottom surface, in-between gates, can lead to defective interfaces
  - worst-case assessment done by TCAD assuming air-gaps (=100% defective interfaces): horizontal, vertical, and/or lateral air-gaps[1]

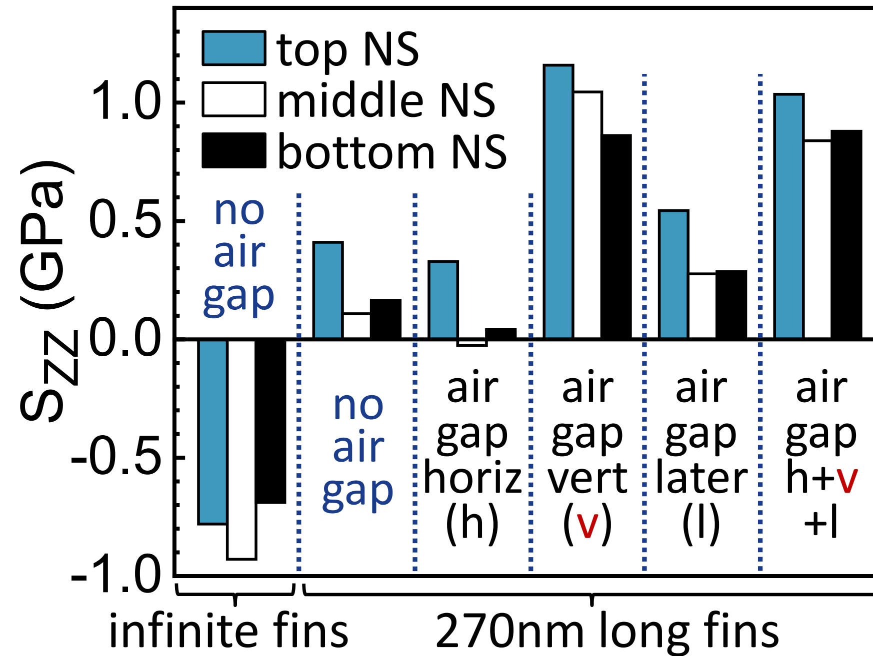
[1] G. Eneman *et al.*, ECST 2020 and TED 2021; A. Veloso *et al.*, EDTM 2021 and ICICDT 2022

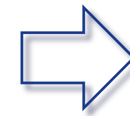
S/D Epi Defects: Stress Impact in NSFETs

views after S/D epi growth:

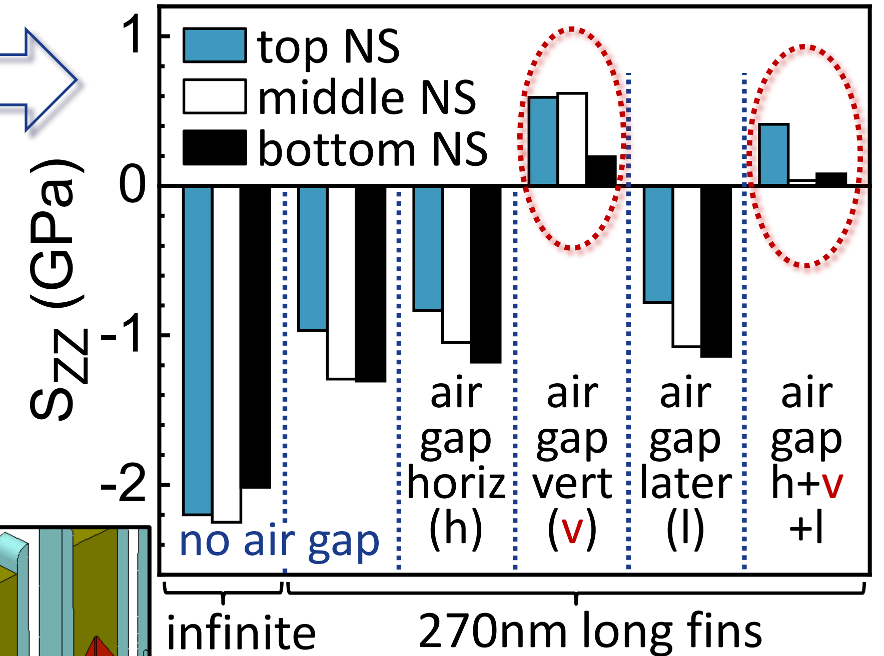


after S/D epi formation

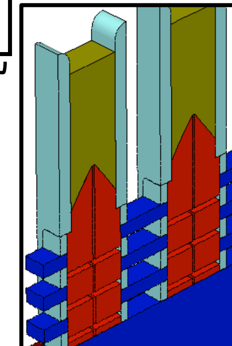




after full process



P-type NSFET with 3 vertically stacked NS:



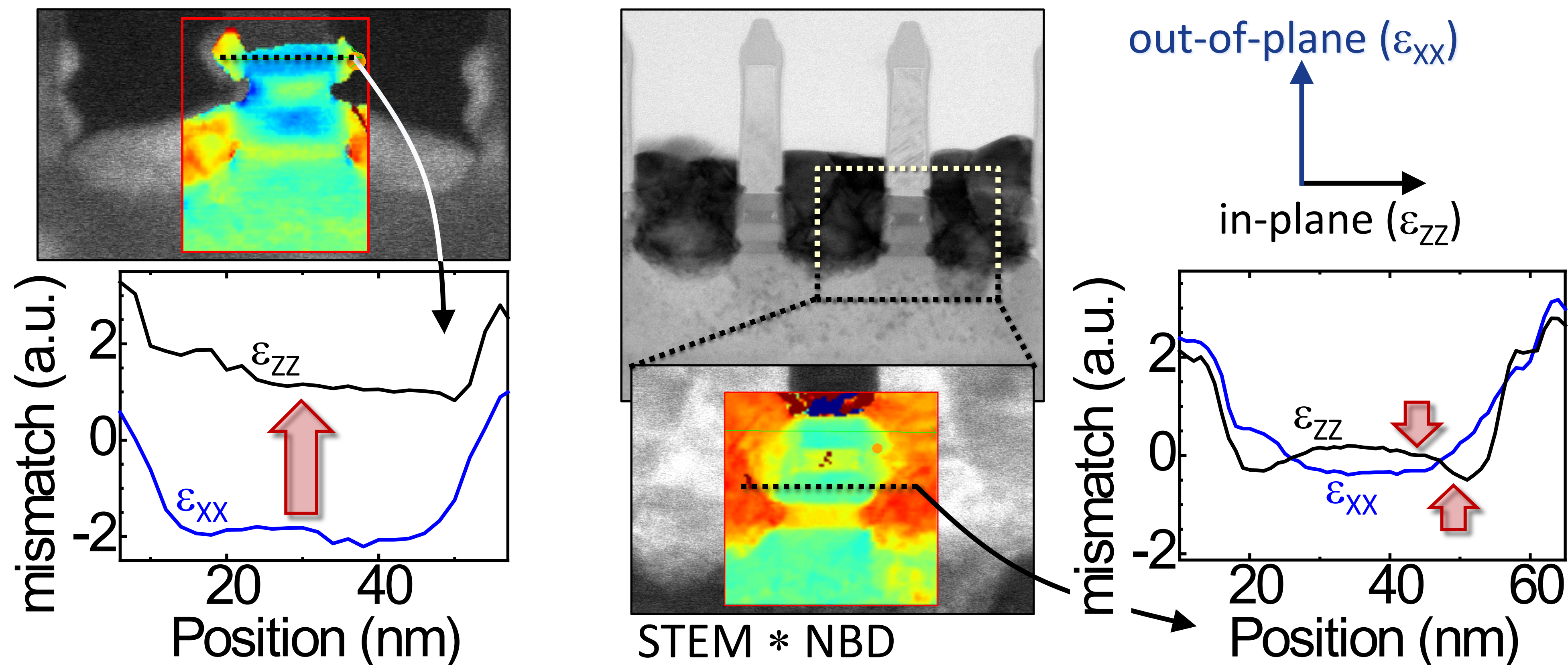
L_{gate}=15nm, CPP=45nm, FP=21nm
W_{NS}=16nm, t_{NS}= 5nm, $d_{NS\text{-}NS}$=9nm

- ‘vertical’ interface the most critical for channel stress: stress lost when epi fronts from neighboring gates don’t join properly[1]
- while minor stress loss due to defective horizontal or lateral interfaces[1]

[1] A. Veloso *et al.*, ICICDT 2022

ICOS International Cooperation On Semiconductors

Channel Strain after S/D Epi Growth in NSFETs with Inner Spacers



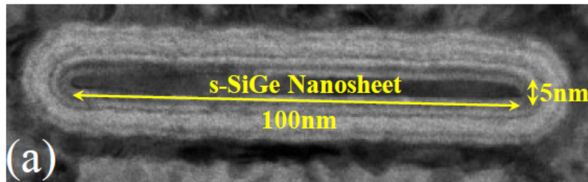
- ❑ Both Si channels are typically tensile strained in the in-plane (<110>) direction
  - ❖ stronger tensile stress for non-merged epi in-between neighboring gates[1]

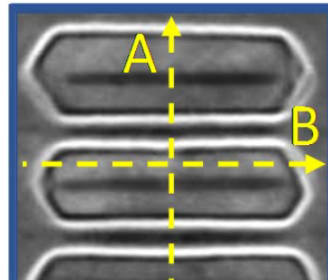
[1] A. Veloso *et al.*, ICICDT 2022

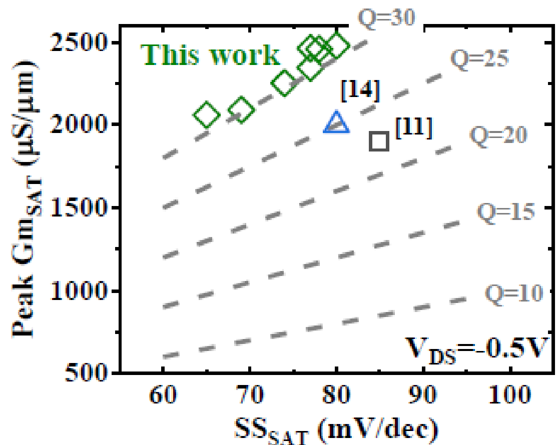
Nanosheet Performance Booster

➢ High mobility channels:

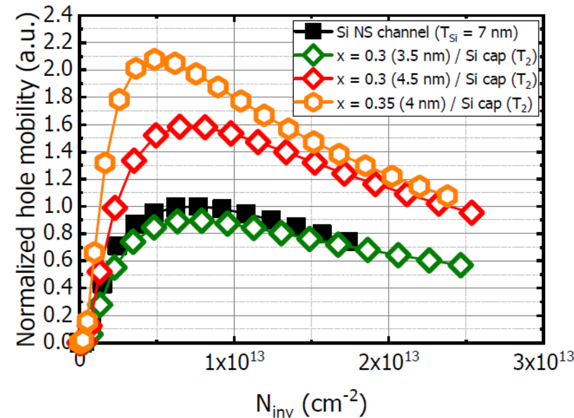
SiGe nanosheet





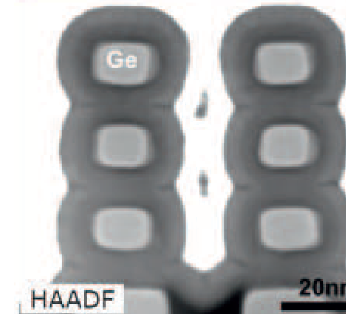


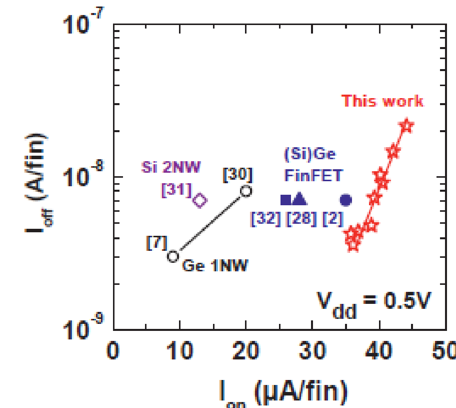
A. Agrawal *et al.*
IEDM 2020



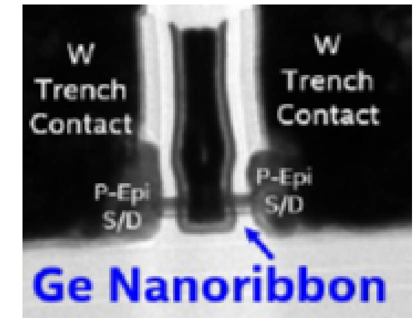
S. Mochizuki *et al.*
IEDM 2020

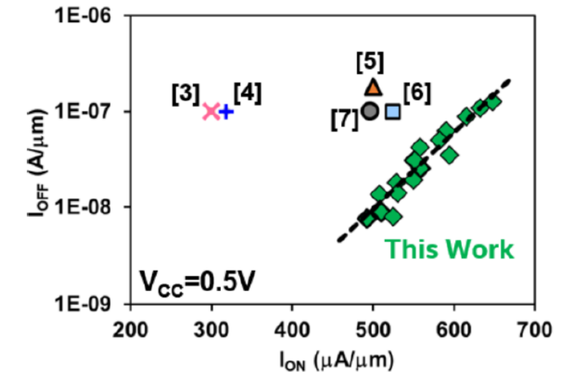
Ge nanosheet





M. Van Dahl *et al.*
IEDM 2018





W. Rachmady *et al.*
IEDM 2019

❑ SiGe and Ge channel promising for nanosheet performance boost

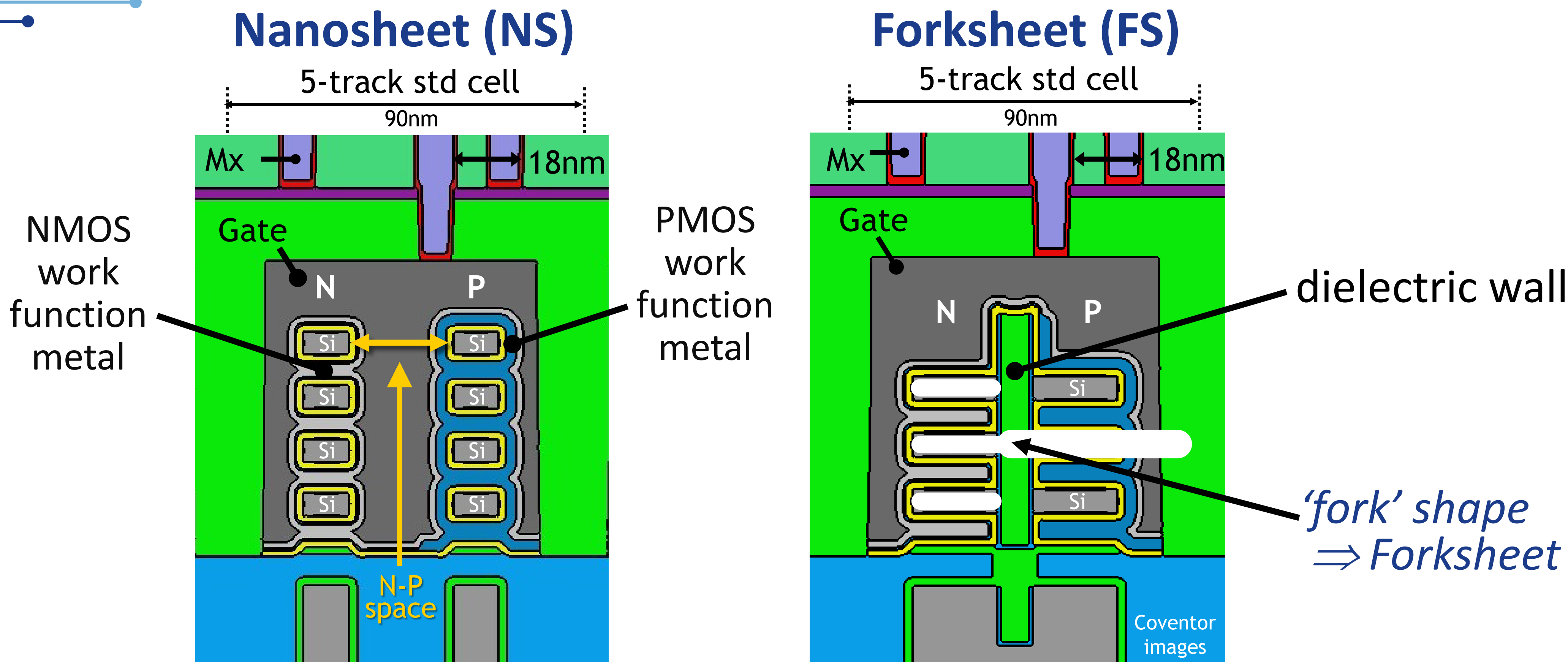
ICOS
International Cooperation
On Semiconductors

Outline

- Introduction – CMOS scaling trends
- Nanosheet FET based device architectures:
  - as enabler of further CMOS logic scaling
  - some key device fabrication aspects
  - extension to further scaling options, e.g.,
    - ✓ forksheet configuration
    - ✓ stacking of different polarity devices (CFET)
- Device connectivity using both wafer sides ⇒ towards CMOS 2.0
- Summary

International Cooperation On Semiconductors

Forksheet FETs: N-P Space Scaling Enablers



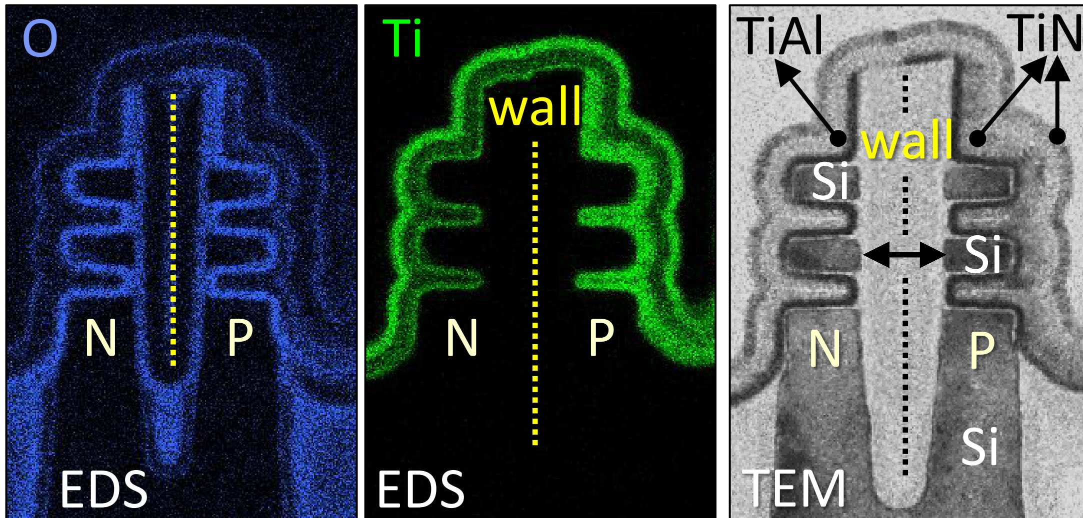
- Forksheet FETs are a particular type of NSFETs enabling aggressive N-P space scaling, hence also maximized active width in lower-track height standard cells

ICOS International Cooperation On Semiconductors

FS-based Circuits with Tighter P-N Spacing

A key feature of FS FETs is a dielectric wall in-between N/PMOS that enables:

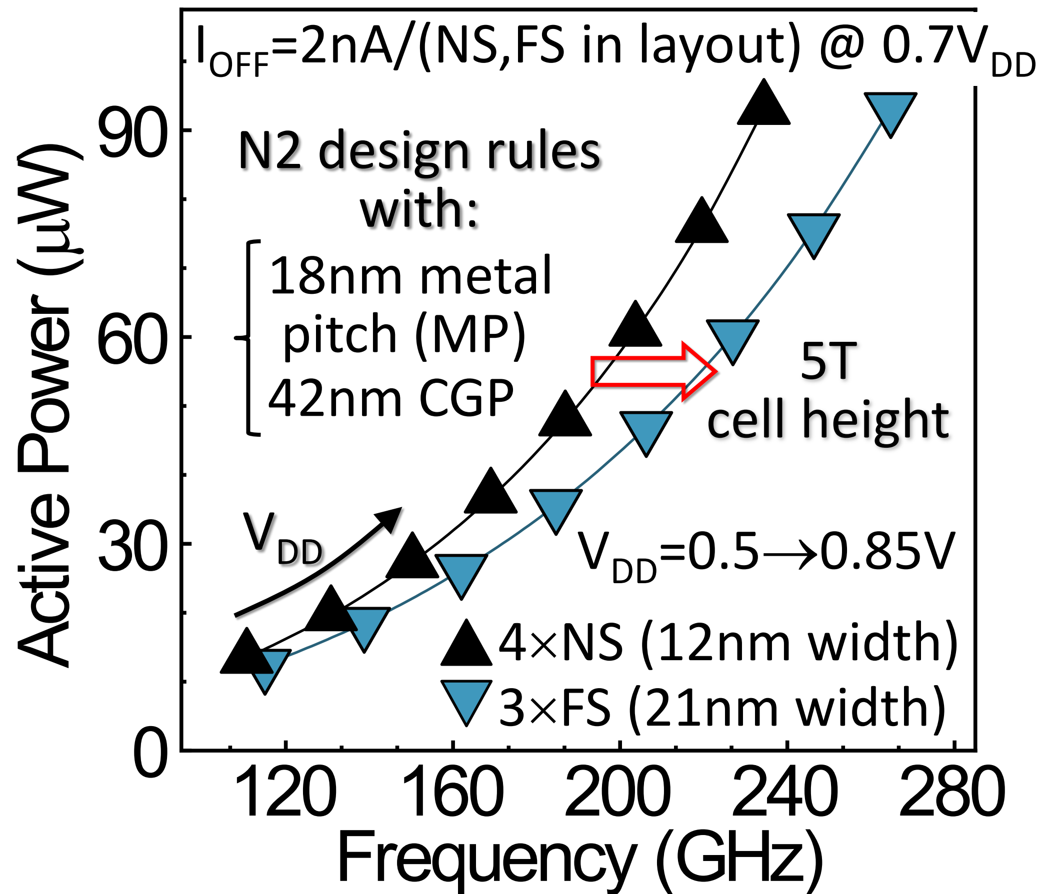
- increased NS width without impacting the footprint of a standard cell
- gate cut placement with enlarged routing flexibility $\Rightarrow$ area reduction
- dual-EWF RMG patterning at tight p-n spacing
- benefits also for self-aligned S/D contacts

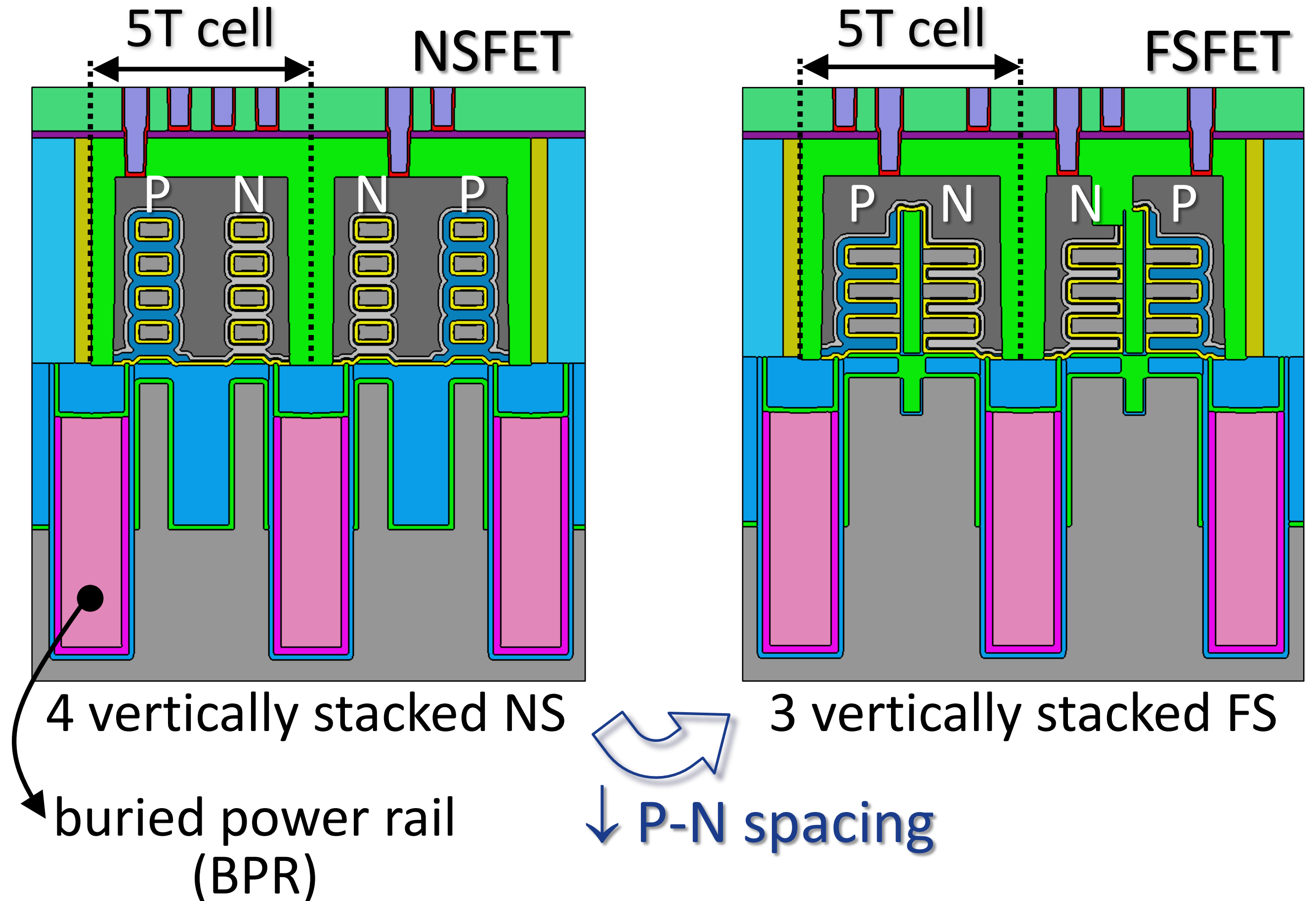


Dual-EWF metal gate patterning at RMG module

ICOS International Cooperation On Semiconductors

Power-Performance Metric: NS *vs.* FSFETs



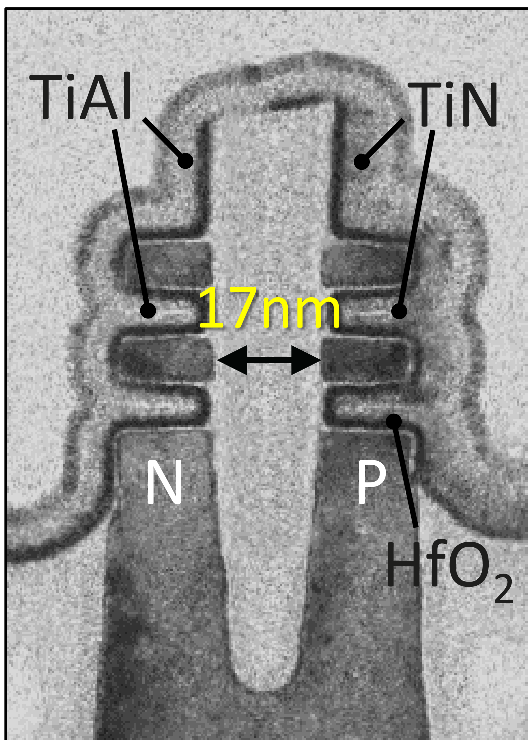


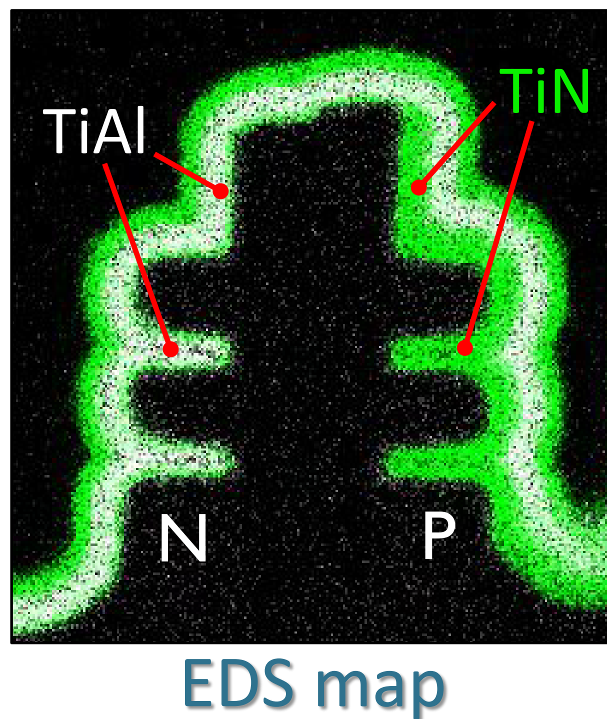
- FS FET based ROs are projected to outperform NS FET based ROs for N2 design rules, showing higher performance and power saving gains[1]

[1] A. Veloso *et al.*, EDTM 2021

FS Dielectric Wall and RMG Demonstration

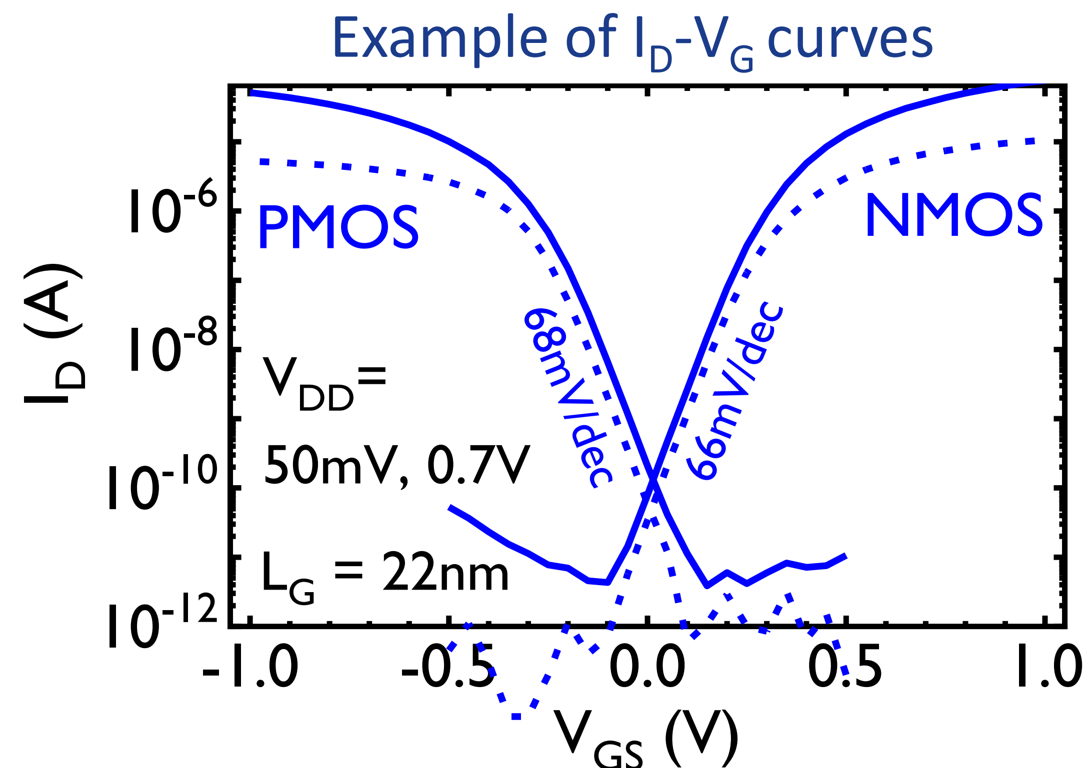
RMG patterning in Forksheet FETs





EDS map

Example of I_D-V_G curves



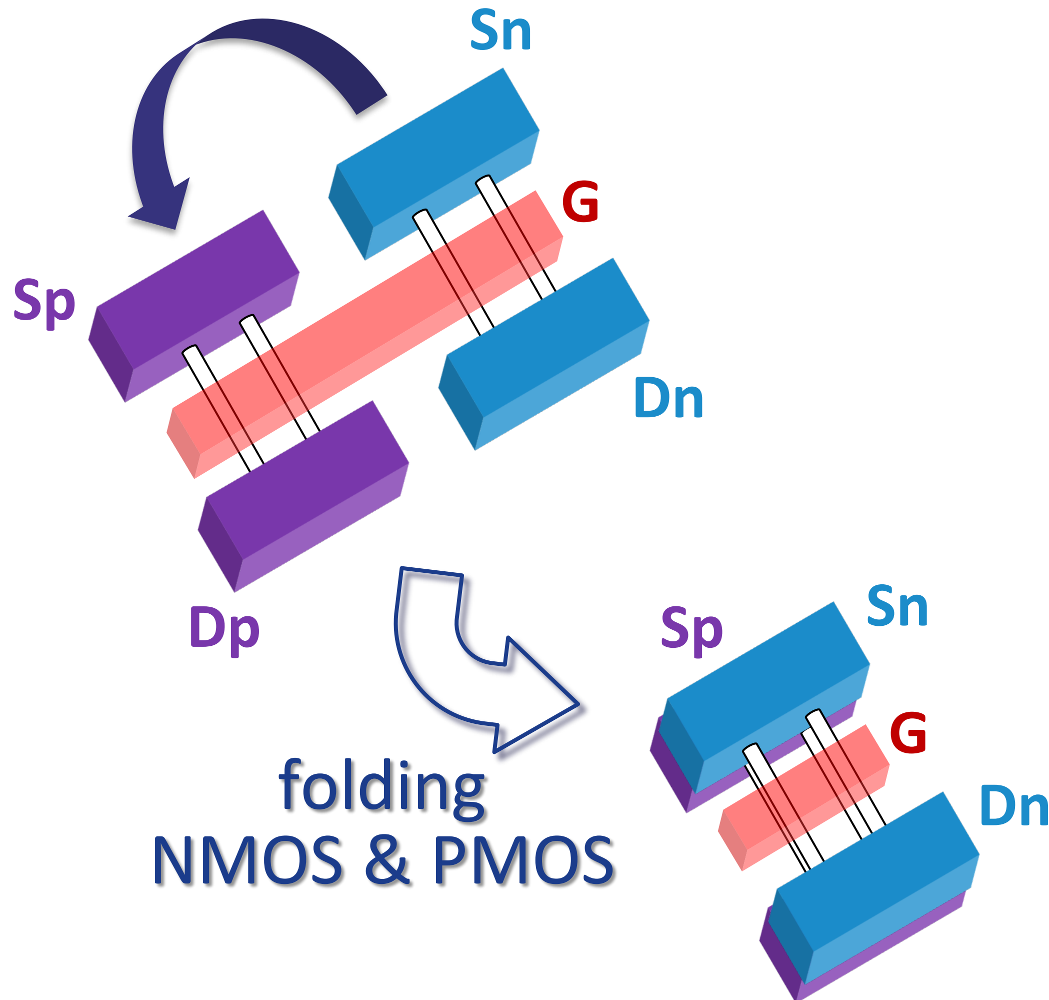
- RMG patterning and Forksheet device demonstrated with 17nm N-P separation[1,2]

[1] S. B. Samavedam *et al.*, IEDM 2020

[2] H. Mertens *et al.*, VLSI 2021

ICOS
International Cooperation On Semiconductors

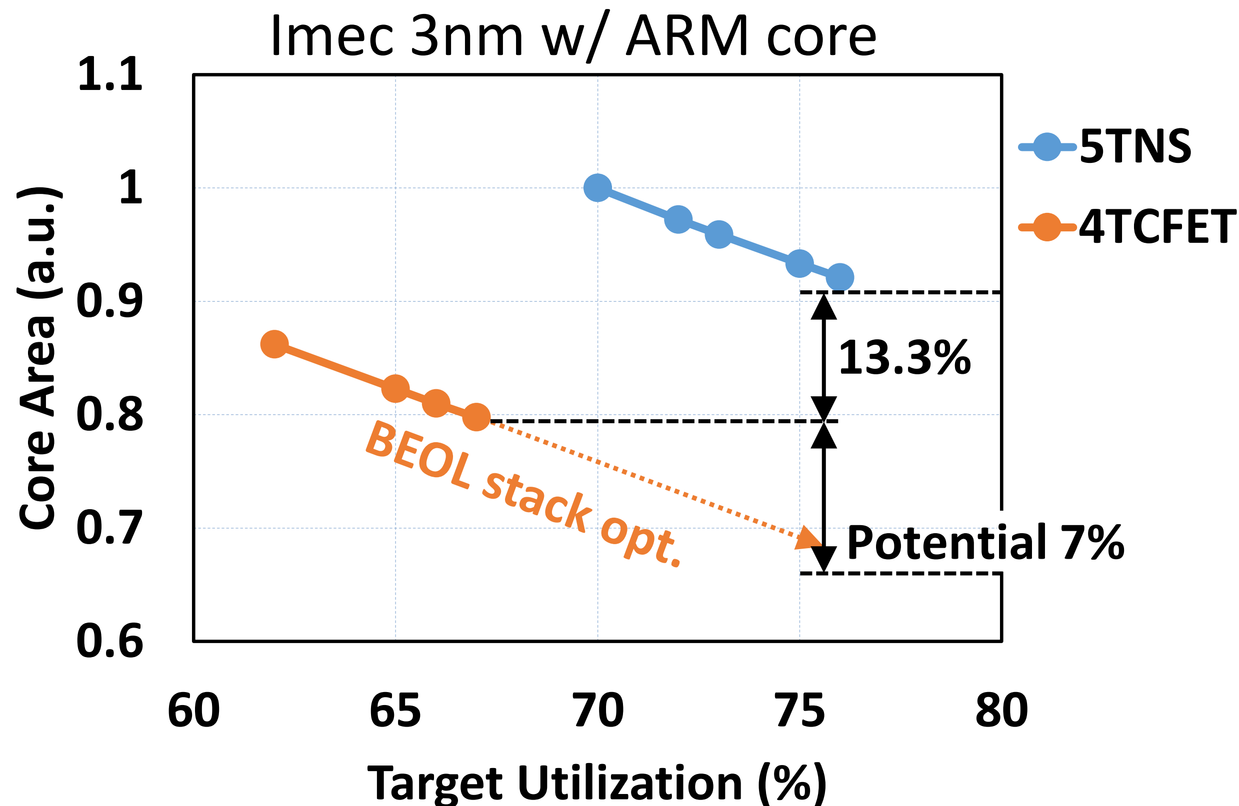
The Complementary FET (CFET)[1]



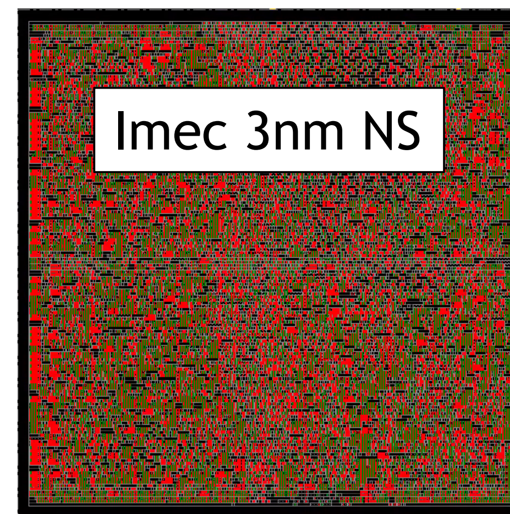
- No area penalty from N-P space due to stacked NMOS & PMOS
- Maximized effective width due to stacked N&PMOS and stacked NS channel in single fin architecture
- Options to integrate optimized channels for N/P independently by sequential integration

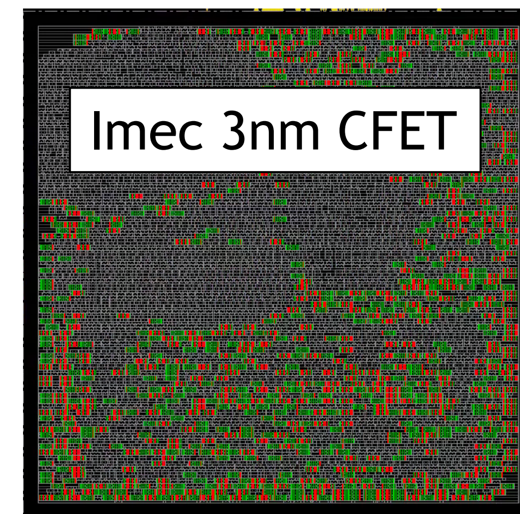
[1] J. Ryckaert *et al.*, VLSI 2018

CFET PnR Demonstrates CFET Logic Area Scaling Potential



M1 after placement





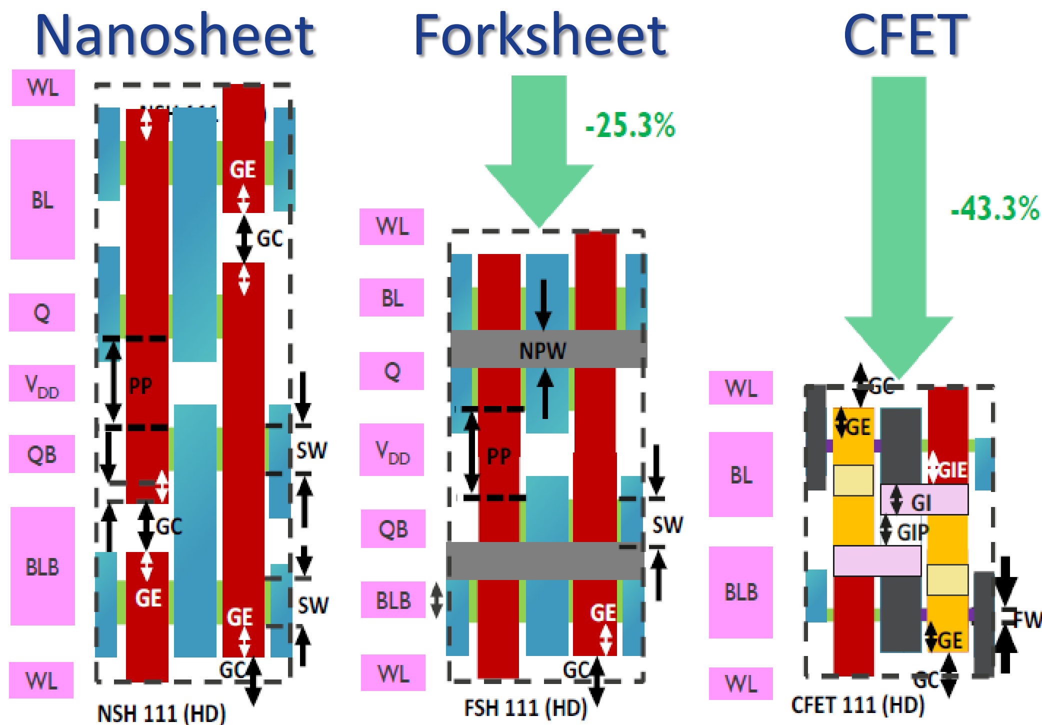
M1 depopulation in CFET standard cell opens M1 for routing

- CFET full PnR loop to compare 5T-NS FET to 4T-CFET based cells[1]
  - >13% area scaling expected

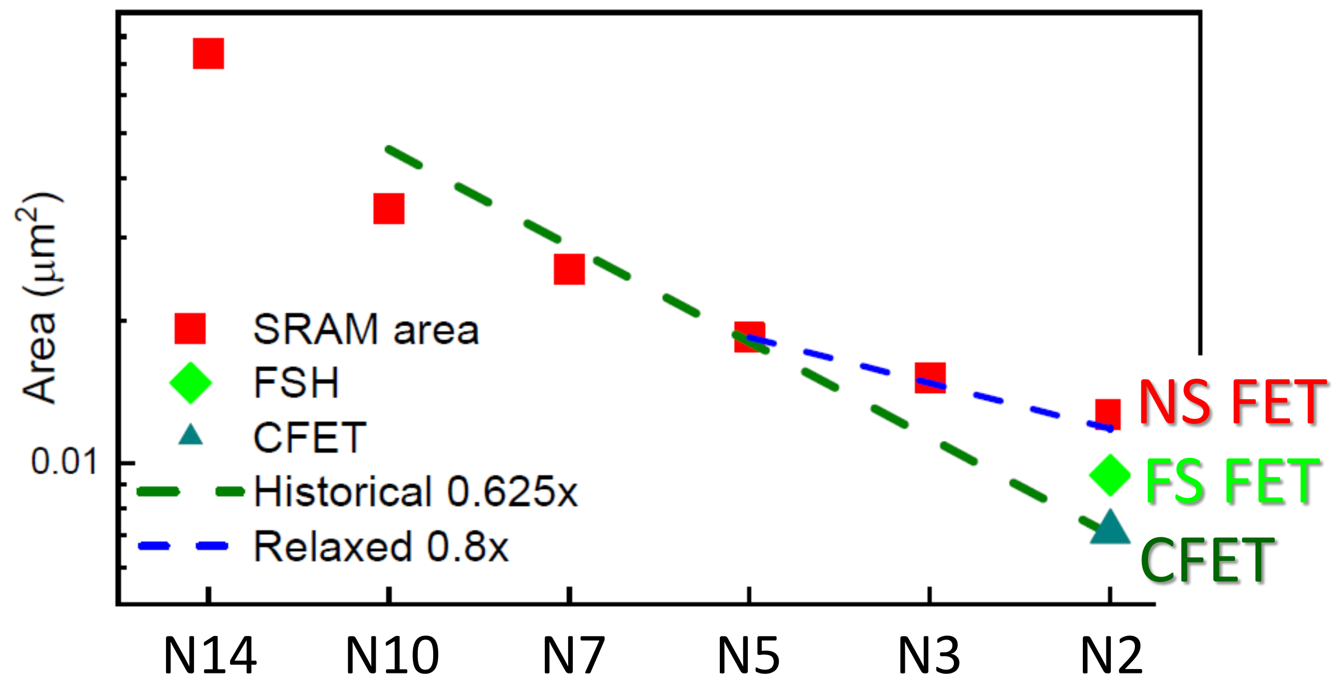
[1] N. Horiguchi, Short Course VLSI 2021

SRAM Area Scaling Projection with Nanosheet FETs, Forksheet FETs, CFET

HD SRAM bitcell design



HD SRAM area scaling



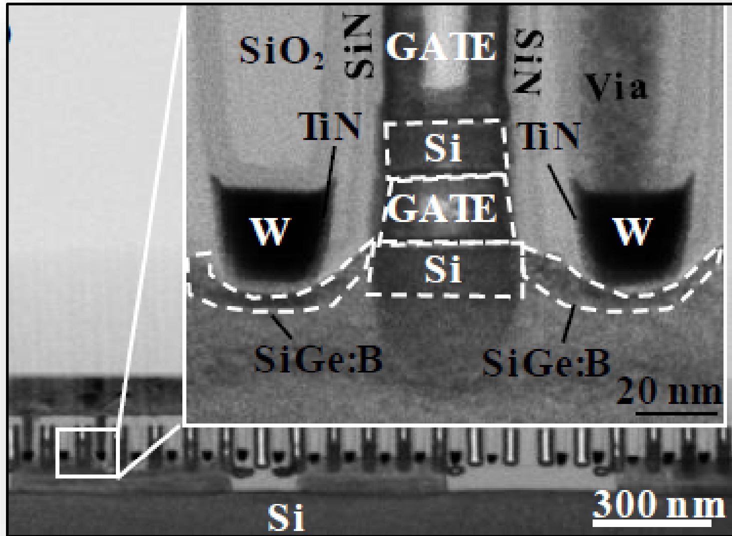
- CFET can bring HD SRAM density scaling on track as compared to cells built with nanosheet FET devices[1]

[1] N. Horiguchi, Short Course VLSI 2021

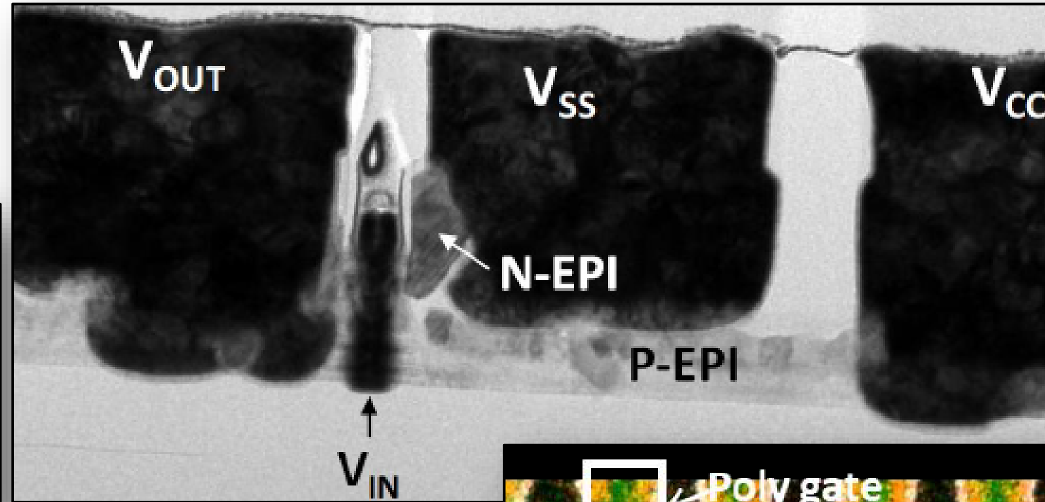
ICOS International Cooperation On Semiconductors

CFET Demonstrations

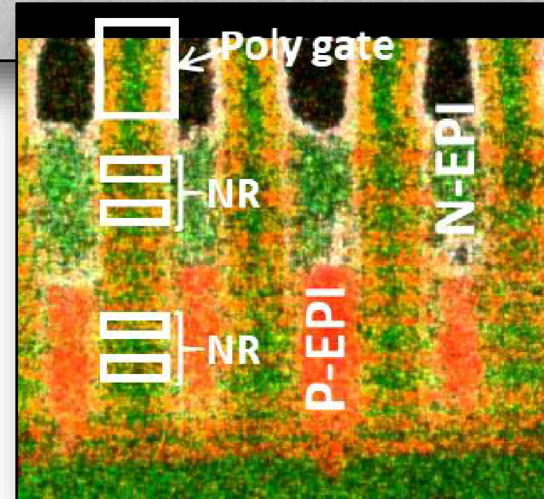
Monolithic Approach



S. Subramanian *et al.*, VLSI 2020



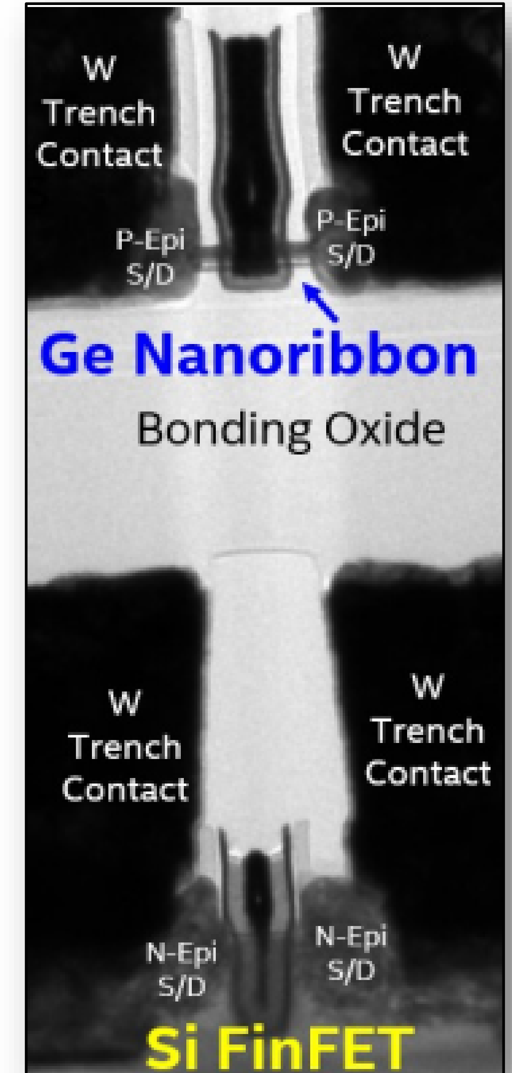
C. Y. Huang *et al.*, IEDM 2020



M. Radosavljevic *et al.*, IEDM 2021

Sequential Approach

W. Rachmady *et al.*, IEDM 2019



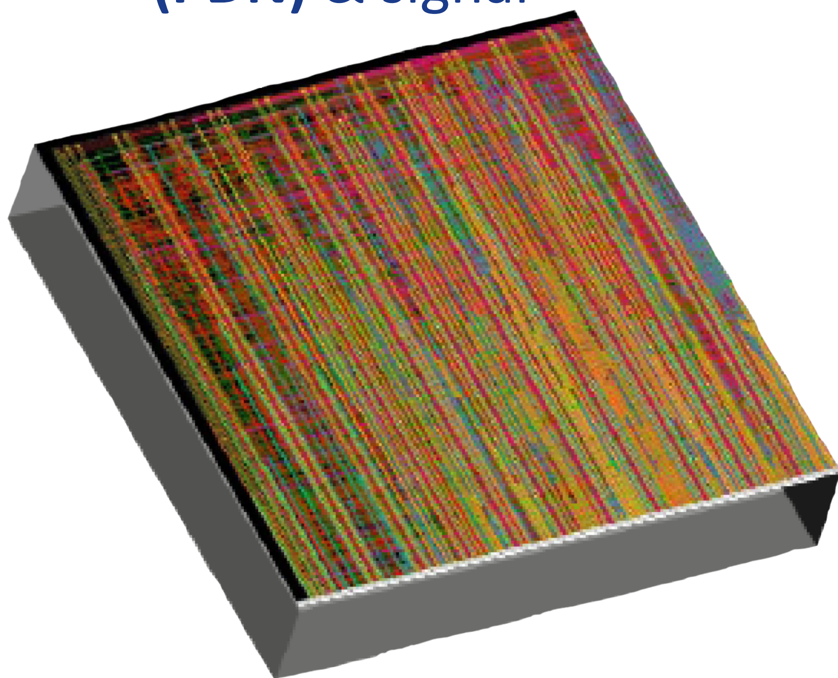
- ❑ Many integration challenges with both approaches
- ❑ Sequential CFETs: different channel materials or orientation

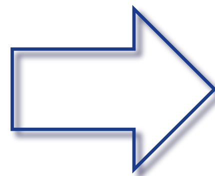
Outline

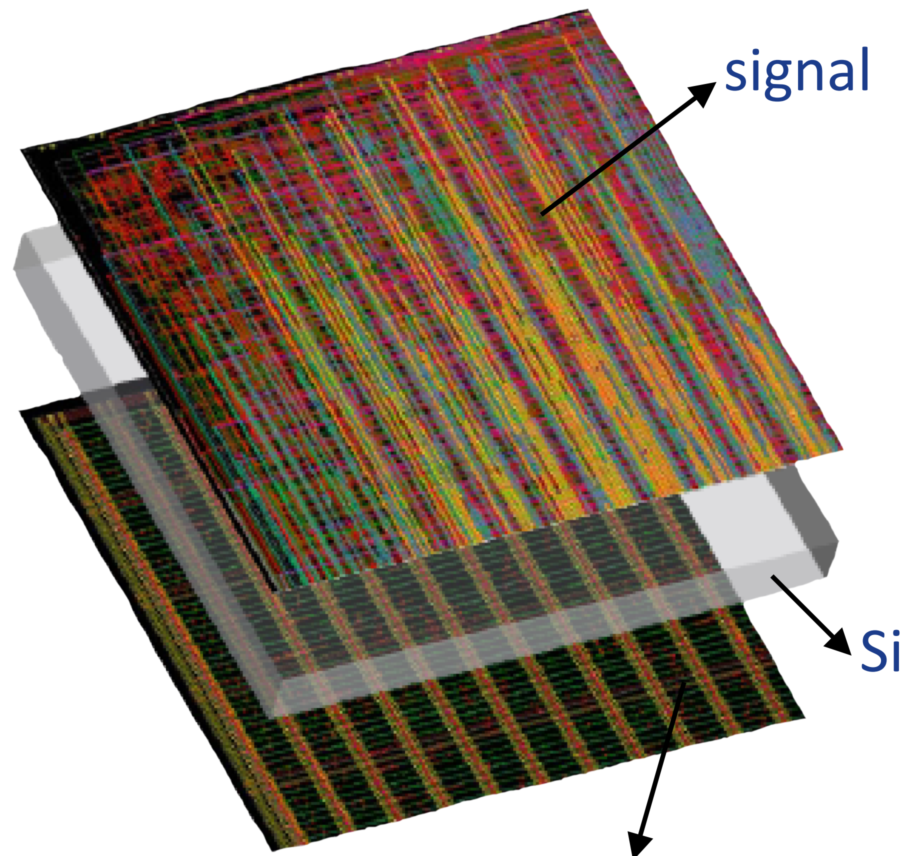
- ❑ Introduction – CMOS scaling trends
- ❑ Nanosheet FET based device architectures:
  - ❖ as enabler of further CMOS logic scaling
  - ❖ some key device fabrication aspects
  - ❖ extension to further scaling options, e.g.,
    - ✓ forksheet configuration
    - ✓ stacking of different polarity devices (CFET)
- ❑ Device connectivity using both wafer sides ⇒ towards CMOS 2.0
- ❑ Summary

Backside PDN: a Game Changer for On-Chip Power Distribution

Frontside (FS)
power delivery network
(PDN) & signal



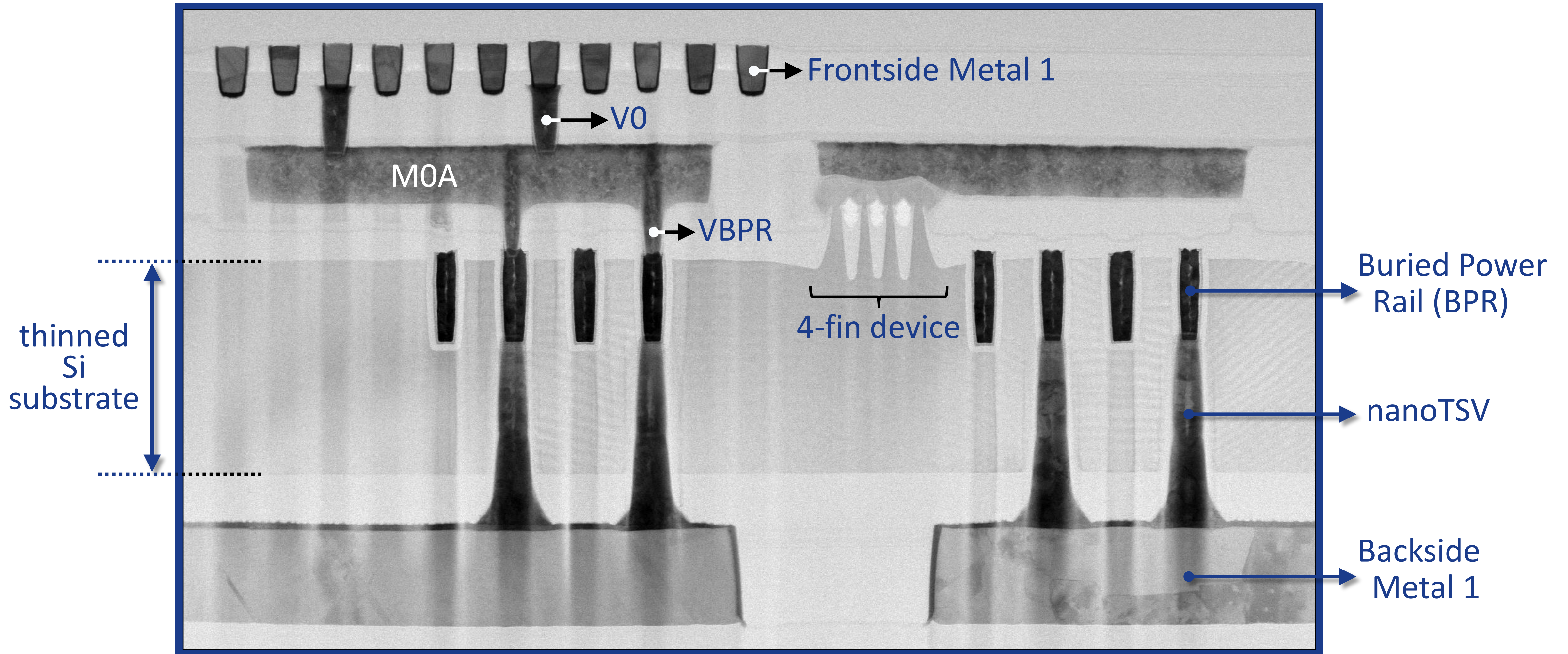




Backside (BS) PDN

ICOS International Cooperation On Semiconductors

Device Demonstration with Frontside & Backside Connectivity

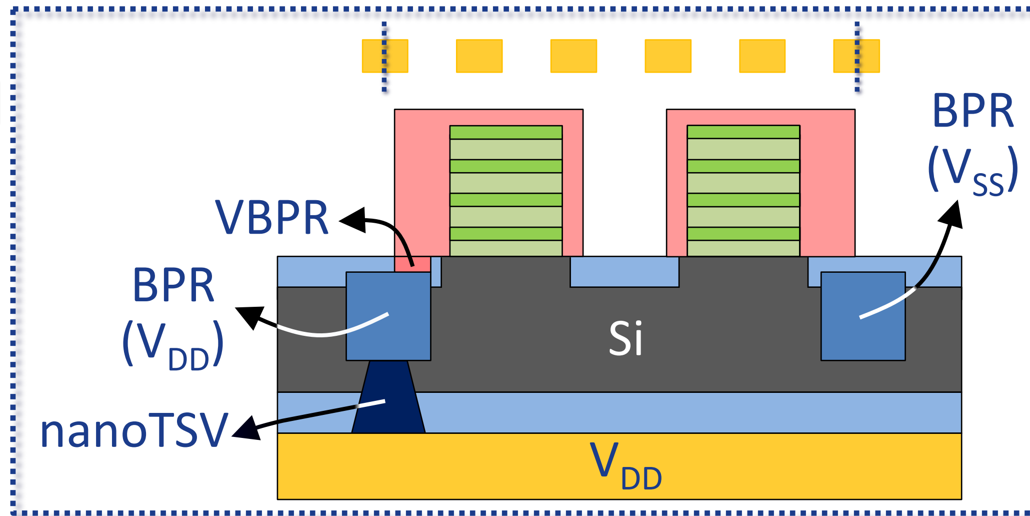


A. Veloso *et al.*, VLSI 2022

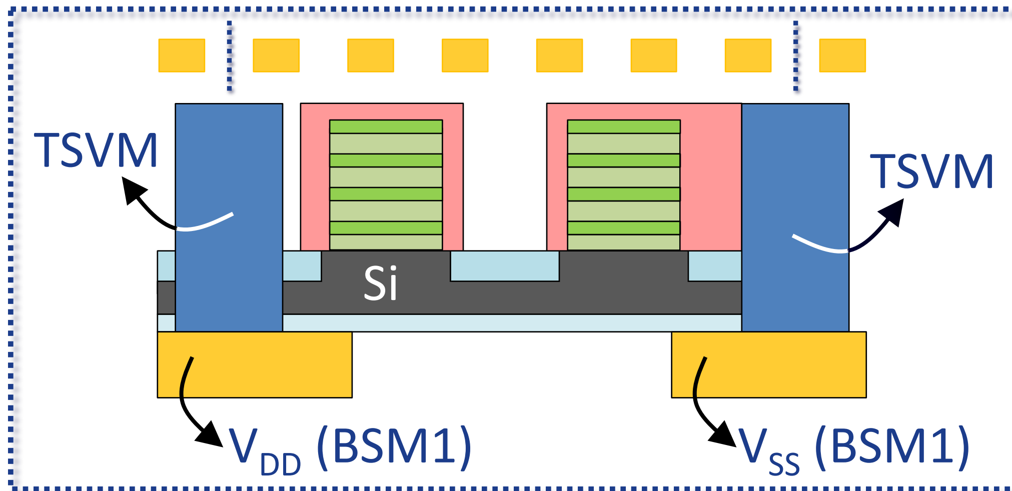
ICOS International Cooperation On Semiconductors

Differentiated BSPDN Process Schemes[1]

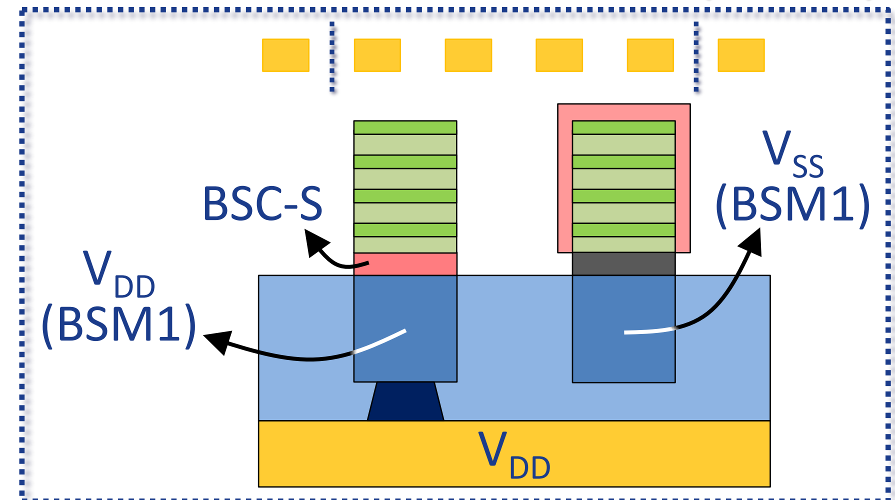
Buried Power Rail (BPR)



TSV Middle (TSVM)



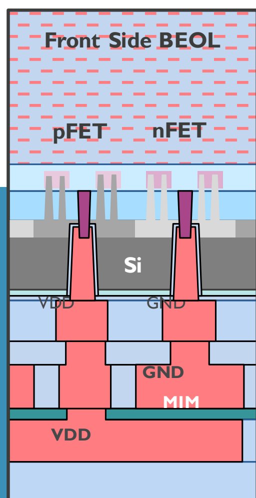
Backside Contact on Source (BSC-S)



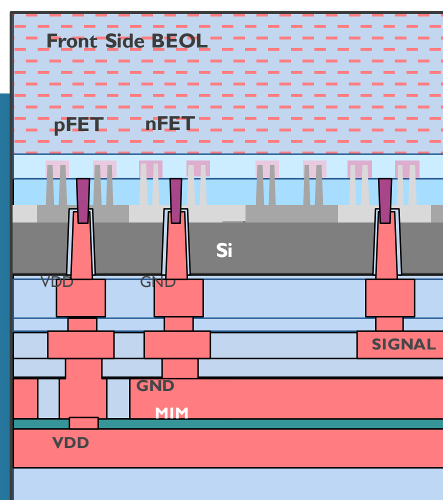
[1] G. Hiblot *et al.*, Short Course IEDM 2022

Backside PDN Paving the Way to a Truly Functional Backside

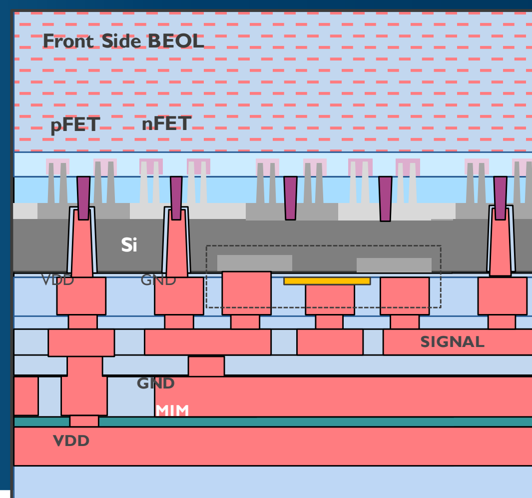
Backside Power Delivery



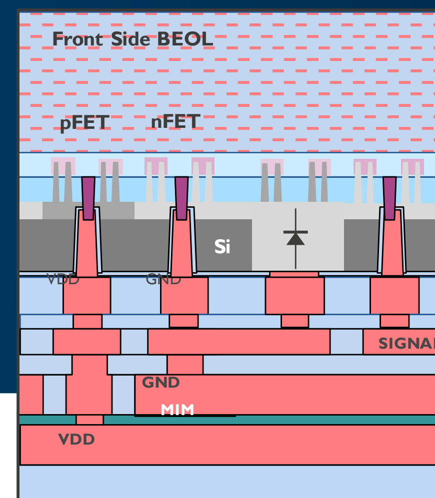
Backside Global Interconnect



Backside Devices

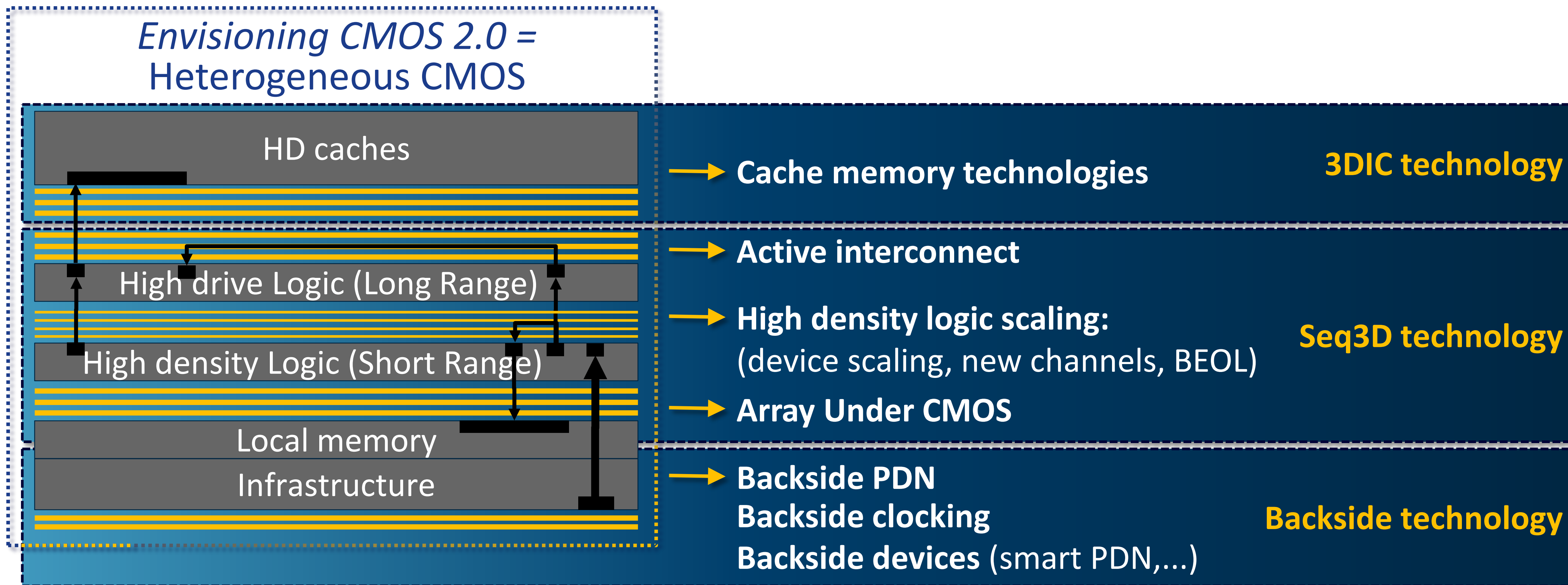


Device Backside Extension



Enhancing system performance by migrating system functions to the backside

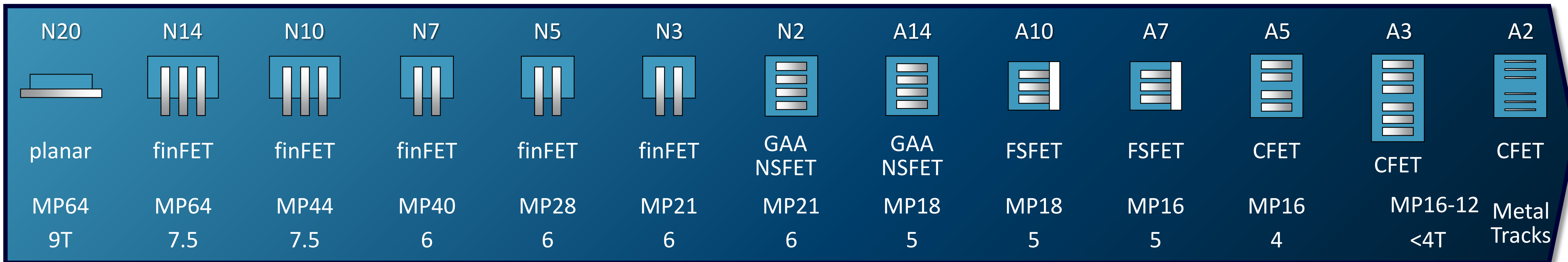
CMOS Platform Leaning Towards Heterogeneity



ICOS
International Cooperation On Semiconductors

Imec's Logic Scaling Roadmap

Transistor density scaling



Std cell: SDB, SAGC, FS wall, VHV?, Common Gate?

Backside: BS-PDN, BPR, BS Interconnect, BS PS

BEOL: Ru DME, Ru SemiD +AG, AR6, Uber via/ New alloy, Act. Interc

CMOS 2.0: AuC

Equivalent density scaling

Funded by the European Union

International Cooperation On Semiconductors

Outline

- ❑ Introduction – CMOS scaling trends
- ❑ Nanosheet FET based device architectures:
  - ❖ as enabler of further CMOS logic scaling
  - ❖ some key device fabrication aspects
  - ❖ extension to further scaling options, e.g.,
    - ✓ forksheet configuration
    - ✓ stacking of different polarity devices (CFET)
- ❑ Device connectivity using both wafer sides ⇒ towards CMOS 2.0
- ❑ Summary

Funded by the European Union

ICOS
International Cooperation On Semiconductors

Summary

- Track height shrinkage has been driving the recent CMOS standard cell scaling
- Introduction of novel transistor device architectures is required to help continue delivering profitable node-to-node scaling gains: nanosheet based FETs (& potential evolution into forksheet FETs, CFETs) are the most promising and mature candidates to replace finFETs
- Structural scaling booster innovations (e.g., buried power rail, backside power delivery network) are also critical to tackle routing bottlenecks and enable obtaining reduced wiring congestion and lower IR drop values
- Material and process innovations overall remain key to enable chip performance enhancement

THANK YOU

This project has received funding from the European Union's Horizon Europe research and innovation programme under GA Nº 101092562