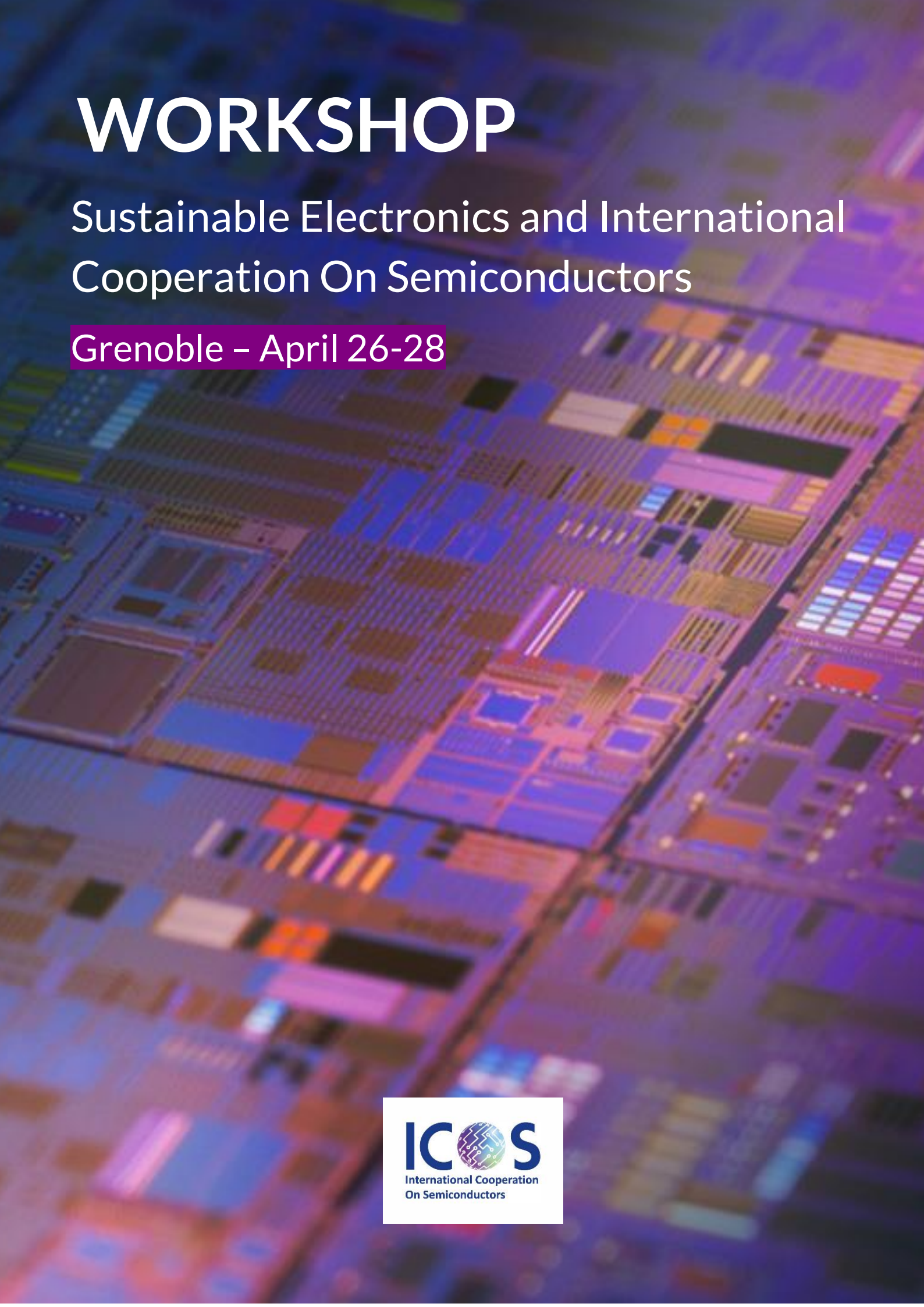
WORKSHOP

Sustainable Electronics and International Cooperation On Semiconductors

Grenoble – April 26-28



Day 1

Day 2

Day 3

PROGRAMME OVERVIEW

1st DAY

Morning

7:30 **Welcome coffee**

8:00 **Welcome & Introduction** – Francis Balestra (Grenoble INP/CNRS - ICOS Coordinator, SiNANO Institute Director)

SESSION 1 – European Innovation Council *(Chair: Francis Balestra)*

8:20 - **EIC Programme** – Eric-Olivier Pallu (European Commission/EISMEA)
8:50 - **EIC Responsible Electronics programme** – Isabel Obieta (European Commission/EISMEA)
9:20 - **How to get help on your way to the EIC Accelerator** – Charlotte Rix Nicolajsen (Bureau Europe - Auvergne Rhône-Alpes Entreprises)
9:35 - **Start-ups success stories:** UPMEM, TiHive, ALEDIA

10:35 - Coffee Break

SESSION 2 – CHIPS ACTS *(Chair: Francis Balestra)*

11:05 - **EU Chips Act** – Marco Ceccarelli (European Commission/DG Connect)
11:35 - **Chips Acts and IRDS building pillars and bridges over valleys of death** – Paolo Gargini (IRDS Chairman & US Chips Act)

Lunch 12:05

Afternoon

SESSION 3 – Sustainable Electronics *(Chair: Thierry Baron)*

13:30 - **IRDS Environment, Safety, Health and Sustainability Chapter Presentation** – Leo Kenny (IRDS ESH/S Team leader)
14:10 - **What future for the semiconductor industry in the age of climate change? Evolution and diversification of semiconductor technologies** – Stephane Monfray (ST)
14:35 - **Key IC data for an accurate life cycle assessment of ICT devices** – Mathilde Billaud (Fraunhofer IZM)
15:00 - **Assessing the environmental impact of integrated circuit chip manufacturing** – Cédric Rolin (IMEC)
15:25 - **Sustainable ICT assessment, adoption and strategy** – Thomas Ernst (CEA-LETI)
15:50 - **Can we cope with the massive production of integrated circuits (ICs) within environmental limits?** – Thibault Pirson (Université Catholique de Louvain)

16:15 - Coffee Break

16:45 - **How innovation leads to a better, safer, more secure and sustainable world?** – Patrick Pype (NXP)
17:10 - **Sustainable printed circuits: a possible path to greener electronics** – Attila Géczy (BME-VIK)
17:35 - **Building Safe-and-Sustainable-by-Design Community in Electronics** – Dmitri Petrovykh (INL)

18:00 - PANEL SESSION 1

Challenges and Solutions for Sustainable Electronics *(Chair: Karine Samuel)*

With **Leo Kenny** (IRDS ESH/S Team leader), **Isabel Obieta** (EC/EISMEA), **Patrick Pype** (NXP), **Markus Pfeffer** (Fraunhofer IISB), **Mustafa Badaroglu** (IRDS More Moore Team leader), **Dominique Thomas** (STMicroelectronics), **Thomas Ernst** (CEA-Leti), **Cédric Rolin** (Imec)

Cocktail Networking Cocktail

2nd DAY

Morning

SESSION 4 – Advanced functionalities *(Chair: Quentin Rafhay)*

8:45 - **The More than More domain in the IRDS: white paper and future perspectives** – Enrico Sangiorgi (Director Emeritus SiNANO Institute – IRDS More than Moore Team leader)

Smart sensors *(Chair: Quentin Rafhay)*

9:25 - **Innovation in MEMS for the IoT and our digital life** – Matthias Illing (Bosch)
9:50 - **Low power transducers for the IoT** – Cosmin Roman (ETHZ)
10:15 - **Sensors for Agriculture & the Environment** – Alan O'Riordan (Tyndall)

10:40 - Coffee Break

Smart energy *(Chair: Irina Ionica)*

11:10 - **SiC VDMOS Technology evolution as an example for sustainable and efficient energy conversion** – Markus Pfeffer (Fraunhofer IISB)
11:35 - **Wide Bandgap Power Devices for a Sustainable Future** – Mikael Östling (KTH)

Lunch 12:00

Afternoon

SESSION 5 – Beyond CMOS *(Chair: Enrico Sangiorgi)*

13:30 - **Ferroelectric memories – Enabler for novel computing architectures** – Konrad Seidel (Fraunhofer IPMS)
13:55 - **On and Beyond CMOS** – Jouni Ahopelto (VTT)
14:20 - **Gate all around nanowire FETs: Operation from RT to Cryogenic temperatures** – Qing-Tai Zhao (FZJ)
14:45 - **Flexible electronics with 2D materials** – Andreas Hemmetter (AMO)
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15:10 - Coffee Break

15:40 - **IRDS Beyond CMOS Presentation** – An Chen (IRDS Beyond CMOS Team leader)

SESSION 6 – Quantum Information Processing *(Chair: Giorgos Fagas)*

16:20 - **IRDS technology roadmap for CEQIP** – Scott Holmes (IRDS Cryogenic Electronic and Quantum Information Processing Team leader)
17:00 - **The path to large scale quantum computing based on CMOS technology** – Maud Vinet (Siquance)
17:25 - **The European Quantum Strategic Industry Roadmap by QUIC**– Johanna Sepulveda (AIRBUS)

18:00 - PANEL SESSION 2

Strategy for International Cooperation - Chips Act *(Chair: Patrick Cogez)*

With **Paolo Gargini** (IRDS Chairman & US Chips Act), **Enrico Sangiorgi** (Director Emeritus SiNANO Institute – IRDS More than Moore Team leader), **Mathias Illing** (Bosch), **Markus Pfeffer** (Fraunhofer IISB), **Abdul Rahim** (EpiXFab), **Giorgos Fagas** (Tyndall), **Holger Schmidt** (Infineon), **Carlo Reita** (CEA-Leti)

Cocktail Networking Cocktail

3rd DAY

Morning

SESSION 7 – Japanese session *(Chair: Julia Kaltschew)*

8:00 - **Japan's Semiconductor Strategy –** Hisashi Kanazashi, Director of IT Industry Division, Commerce and Information Policy Bureau, Ministry of Economy, Trade and Industry

8:20 - **EC presentation –** Colette Maloney, Head of Unit, EC/DG Connect

8:40 - **AI Chip Design Center (AIDC), SoC design platform for small industries and startups in Japan –** Professor Makoto Ikeda, Tokyo University

9:10 - **The EU Test and Experimentation Facility for Hardware Edge AI, PREVAIL, as a platform for development of new solutions** – Carlo Reita (CEA-leti)

9:40 - **Megatrends in the autmotive industry and RENESAS' value proposition –** Takashi Yasumasu, Vice President, Automotive Core Technology Development Division, Automotive Solution Business Unit, Renesas Electronics Corp.

10:10 - **Trends in semiconductors for mobility –** Matthias Illing (Bosch)

10:40 - **ICOS (International Cooperation On Semiconductors) presentation on past and existing cooperation in research between EU-JP –** Francis Balestra, ICOS coordinator

11:00 - **Open table discussion**

Lunch

Afternoon

SESSION 8 – Advanced Computing *(Chair: Thierry Poiroux)*

13:00 - **IRDS More Moore Roadmap for edge and cloud computing** – Mustafa Badaroglu (IRDS More Moore Team leader)

13:40 - **Augmented FDSOI platforms for improved sustainability** – Roberto Gonella (STMicroelectronics)

14:05 - **Nanosheet-based Device Architectures for Enabling Advanced CMOS Logic Scaling** – Anabela Veloso (imec)

14:30 - **FDSOI engineered substrates for advanced computing** – Sébastien Loubriat (SOITEC)

SESSION 9 – Semiconductors-based Photonics *(Chair: Elise Ghibaudo)*

14:55 - **Silicon Photonics: Current state, trends, and future evolution** – Abdul Rahim (EpiXFab)

15:35 - **Neuromorphic Computing - At the intersection between Electronics and Photonics** – Stephan Suckow (AMO)

16:00 - **Silicon photonics and applications** – Frédéric Bœuf (STMicroelectronics)

16:25 - Networking Coffee

ABSTRACTS AND SPEAKERS

Workshop introduction and objectives

Francis BALESTRA – CNRS Research Director at IMEP-LAHC, Director of the European SiNANO Institute

This Workshop will allow to present the EU and International strategies, Roadmaps, activities and challenges dedicated to future important semiconductor technologies for many applications and find possible gaps for developing international cooperation, and present the main challenges of sustainable electronics to be taken into account in future international collaboration, IRDS roadmap and EIC challenges, with possible joint international calls for projects.

Francis Balestra has been Director of several Laboratories. Within FP6, FP7, H2020 and Horizon Europe, he coordinated several European Projects (SiNANO, NANOSIL, NANOFUNCTION, NEREID, ICOS) that have represented unprecedented collaborations in Europe in the field of Nanoelectronics. He is member of several European Scientific Councils, of the Advisory Committees of International Journals, of the IRDS International Roadmap Committee, and founded or organized many international Conferences. He is currently Vice-President of Grenoble INP, in charge of European activities, and Director of the SiNANO Institute he founded 15 years ago.

SESSION 1 – European Innovation Council

EIC Programme

Eric-Olivier PALLU – Policy Adviser in the "EIC Board, Strategy and Feedback to Policy" Unit at the European Innovation Council (EIC) and SME Executive Agency of the European Commission

The EU has established the European Innovation Council (EIC), its most ambitious initiative ever in the field of innovation, to help deep tech startups and SMEs to scale up, and thus get many more unicorns in Europe. Launched only two years ago, the EIC has already become Europe's most active investor into deep tech European startups and SMEs (Sifted, 23 January 2023). The presentation will detail the policy aims, the various EIC instruments and the first results obtained.

Eric-Olivier Pallu is contributing to the development of the European Innovation Council concept since 2018. From 2007 to 2013, he served as Counsellor for Science & Technology within the French permanent representation to the EU, managing the 2008 French Presidency then negotiating Horizon 2020 regulation. Eric-Olivier is « Ancien élève de l'École Nationale d'Administration » (ENA - 2001-2003) and is holding a PhD in public law (international relations and defence).

EIC Responsible Electronics programme

Isabel OBIETA – EIC Programme Manager for Responsible Electronics

The role of the EIC Programme Managers in the identification of potential challenges for emerging technologies and disruptive innovations and in pro-active management of selected portfolios and projects will be described. In my case dealing with non-conventional sustainable electronics, I will present the challenges included in the Workprogramme 2023 and will give some ideas of the future challenges that could be of interest for the Semiconductors community.

Isabel Obieta obtained a Master Degree in Physics (Semiconductor Physics) from the University of the Basque Country (Spain) and, earned a Doctoral Degree in Science (Microelectronics-Materials for Sensors) from the University of Navarra (Spain). All along her career, she has combined her job with activities as expert in innovation by performing Technology Due Diligences, evaluating new business opportunities for Venture capitals and Family offices or as Innovation Radar Expert for EU projects. In September 2022 she joined the European Innovation Council as Programme Manager for Sustainable Electronics.

How to get help on your way to the EIC Accelerator

Charlotte RIX NICOLAJSEN – Head of Bureau Europe - Auvergne Rhône-Alpes Entreprises

As the expert team for European funding of Auvergne-Rhône-Alpes Entreprises, the role of the Bureau Europe is to support the regional companies, in particular the SMEs in their search for funding for their projects and development and to find their way through the jungle of European Funding ending up identifying what is most adapted to their projects. Since several years, the Bureau Europe has developed a range of services specially for EIC Accelerator applicants, in close collaboration with the French EIC National Contact Points, i.e. project diagnosis, individual support, proofreading and pitch training.

Charlotte Rix Nicolajsen is Head of the *Bureau Europe* of the regional economic development agency, Auvergne-Rhône-Alpes Entreprises. She specialized in European funding for innovation and development projects and she is supporting companies, in particular SMEs, in their search for and understanding of the opportunities offered by the European Commission. Her team is member since 2015 of Enterprise Europe Network, a network financed by the EC with 600 consortia spread all over Europe and beyond, helping SMEs internationalize, develop, innovate and finding funding for their projects.

Success stories of a few startups:

UPMEM

Introduced by Gilles Hamou, CEO and Co-founder

UPMEM accelerates 20x big data applications with its Processing In-Memory chips, solving the dominant cost of data movement and the Memory wall, at marginal cost and energy consumption. UPMEM solution readily integrates in-app servers to offer the 1st efficient scalable programmable acceleration solution for data-intensive apps such as genomics, AI, analytics, search... UPMEM is maintaining a sustained effort *en route* to making PIM a dominant architecture in computing nodes, growing his team, customer base, memory, system, server and cloud partners worldwide.

TiHive

Introduced by Hani Sherry, CEO and Co-founder

Green wireless tech ensuring no raw materials are wasted while producing high quality products.

TiHive helps industries become more sustainable by mastering the usage of raw materials and empowers manufacturers using its distributed and inline monitoring systems to build high quality products whilst optimizing their raw materials and reducing waste. Tihive has developed state of the art in-line monitoring systems based on terahertz see-through vision technology allied to deep learning that monitor raw material usage and uncover and process hidden features within products in real time.

ALEDIA

Introduced by Eric Mottin, Program manager

Founded in 2011, Aledia develops 3D micro-light-emitting diode (microLED) chips used in display, based on a unique architecture using gallium nitride (GaN) nanowires on silicon (WireLED™). Aledia technology is currently implemented on 200mm silicon wafers and will scaleup to 300mm silicon wafers for large volume production.

Aledia is a deep tech that is positioned on display market of more than €120 billion/year. Aledia's key asset is to master a growth process on substrates directly compatible with silicon microelectronics (8'' and 12'') and therefore to allow industrial growth compatible with display market volume.

SESSION 2 – Chips Acts

EU Chips Act

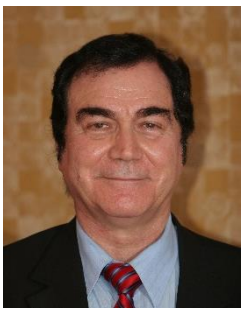
Marco CECCARELLI – European Commission/DG Connect

Marco Ceccarelli is Programme Officer at the European Commission in Brussels where he contributes to the definition of EU policies for the electronics industry. He is one of the main authors of the European "Chips Act", and plays a key role in its implementation. Before joining the Commission in 2017, he held several managerial roles at Philips (Netherlands), where he focused on innovation for electronic systems, as well as several executive positions in high-tech SMEs. He began his career as research scientist in Italy and the Netherlands. Marco holds a Laurea degree in Electronic Engineering from the University of Florence and an Executive MBA from the ESSEC business school in Paris.

Chips Acts and IRDS building pillars and bridges over valleys of death

Paolo A. GARGINI – IEEE Life-Fellow, JSAP Fellow and Chairman IRDS

Personal computers, smart phones, data centers and internet powered by complex semiconductor integrated circuits drove the successes of the electronics industry for the past 30 years. Hardware implementations and software applications have been reaching fundamental limits in the past few years. A new renaissance of the electronics industry powered by multiple cooperative public-private partnerships is in progress around the world to an unprecedented extent and aimed at repeating the successes of the worldwide nanotechnology initiatives that 20 years ago revolutionized the electronics industry and transformed society.



In the 70s, **Dr. Paolo A. Gargini** was a researcher at Stanford University and at Fairchild Camera & Instrument. In 1980 as manager of MPU technology at Intel he transferred into manufacturing the iconic 80286 and 80386. In 1996, he became Director of Technology Strategy and responsible for worldwide consortia research until 2012. He was a member of Sematech, SRC, EUV LLC, EIDEC, ASET, IMEC and SIA Boards, and Chairman of the I300I and NRI. From 1998 to 2015, Dr. Gargini was Chairman of the ITRS sponsored by the WSC. Since 2016 he is the Chairman of the IRDS sponsored by IEEE.

Lunch Break

SESSION 3 – Sustainable Electronics

The IRDS Environmental, Safety, Health and Sustainability (ESH/S) Roadmap: initiative update

Leo T KENNY – IRDS ESH/S IFT Chair and Research Professor at the Center for High Technology Materials at the University of New Mexico

In mid-Q1 of 2022, a half day workshop was held, with the intent to restart the ESH/S International Focus Team (IFT). Given the significant array of ESH/S issues, the consensus was that a return a pre-competitive, forward looking technical approach was critical for industry success. With extensive engagement and participation by key stakeholders (suppliers and manufacturers), the working teams successfully developed a clearly defined scope, drivers, boundary conditions, gap analysis and modelling. These efforts will be contextualized in terms of the value to industry users in standards development and ESHS technology development.

Dr. Leo T Kenny has worked in a broad range of professional roles in science, engineering, and technology. He is the Principal and Founder of PLANET SINGULAR, a technical consulting and advising firm focusing on environmental technology development, materials design, green chemistry... Leo is currently the Chair of the EHS/Sustainability Technical Work group for the IRDS for the Semiconductor Industry and a prior Co-Chair of the Sustainable Electronics Section for INEMI. He has a PhD in Physical Inorganic Chemistry (Tufts University, Boston) with a research focus on thin film batteries and electrochromic smart window devices.

What future for the semiconductor industry in the age of climate change? Evolution and diversification of semiconductor technologies

Stéphane MONFRAY – Senior Principal Engineer, Disruptive Technologies Expert / Technology Development Platform at STMicroelectronics Crolles

Semiconductor technologies are at the heart of the news when it comes to their strategic importance for our connected objects and the automotive market, for example. The purpose of this conference will be to recall the evolution of these CMOS technologies and particularly their diversification (non-volatile memories, microcontrollers, optical, mechanical, photonic sensors, etc.), which has enabled Europe, for example, to maintain and strengthen its competitiveness in these areas. The opportunities related to the care of our environment will be presented, that will make the future of our electronic chips.

Stéphane Monfray graduated as an engineer in 1999 from the National Institute of Applied Sciences (INSA Lyon). He joined STMicroelectronics and received in 2002 his PhD degree in microelectronics from University Aix-Marseille. With more than 20 years of experience, Stéphane has a large portfolio of activities dedicated to advanced technological projects. He co-founded several joint laboratories with academic partners and also co-founded the innovation laboratory (f@STlab) of ST-Crolles where he facilitates the support to innovative projects

Key IC data for an accurate life cycle assessment of ICT devices

Mathilde BILLAUD – Research Fellow, Fraunhofer IZM.

The ICs are the main driver for carbon footprint for small ICT products. That's why the analysis of ICs must be particularly precise to have the most accurate environmental analysis possible to enable the development of greener ICT devices. We will present the key IC data required for an accurate LCA.

Dr. Mathilde Billaud is a Research Fellow at Fraunhofer IZM since 2017. Her main research topics cover critical materials, resource, energy consumption and circular practices in microelectronic manufacturing. She worked from 2013-2016 for CEA-Leti and LTM-CNRS. She received a PhD in 2017 for her thesis on the integration of III-V semiconductors on silicon substrate. She is now involved in the German competence center Green ICT, with 15 research institutes in Germany. She evaluates the potential carbon footprint reduction of new technologies in back-end processes.

Assessing the environmental impact of integrated circuit chip manufacturing

Cédric ROLIN – Manager for the Sustainable Semiconductor Technologies and Systems (SSTS) Program, imec

To help the ICT sector reaching its ambitious sustainability objectives starts with quality and transparent data on the environmental impact of these technologies. In this talk, I will present the methodology developed at imec for the assessment of IC chip manufacturing and will discuss the learnings and possible improvement pathways stemming from this analysis.

Cédric Rolin is Manager for the Sustainable Semiconductor Technologies and Systems (SSTS) Program at imec. After more than 15 years spent both at imec and at University of Michigan holding various positions as researcher and team leader in the fields of flexible and organic electronics and nanoimprint lithography, Cédric has joined in 2021 the sustainability team of imec as Program Manager, focusing on the assessment and improvement of the environmental footprint of the semiconductor manufacturing industry.

Sustainable ICT assessment, adoption and strategy

Thomas ERNST – Scientific Director, CEA-Leti

The impact of digital technology is becoming a topical issue in a context where energy efficiency is a major ecological issue. The dream of a virtual world collides with the materiality of networks, servers, and connected objects demanding for their production and uses rare materials and an increasing amount of energy. The enormous progress in energy efficiency over the past 50 years has been absorbed by spectacular but energy-intensive application developments. Moreover, the miniaturisation and complexity of the circuits will reach physical limits, but also reliability and safety. More generally, there is an urgent need to rethink electronics in order to move towards more sustainable design, from mining to software production and design, and thus take advantage of the enormous potential of digital technology in the many sectors. These include better resource management or knowledge development and

dissemination. A global design, from hardware to software and application, could save several orders of magnitude in energy efficiency.

Thomas Ernst is Scientific Director at CEA-Leti, responsible for long-term research strategy and partnerships. He obtained his diploma in electronics engineering, his doctorate in Grenoble INP and his habilitation to direct research in the field of microelectronics. From 1997-2000, he developed with STMicroelectronics and the CNRS the characterization of the advanced modelling of FD-SOI. He then joined CEA-Leti and led research projects with industry and a startup. He led the development team of the world's first 3D-stacked CMOS nanowires and nanosheets. He received a European Research Council research grant to develop multiphysical integrated intelligent systems.

Can we cope with the massive production of integrated circuits (ICs) within environmental limits?

Thibault PIRSON – PhD researcher in the Electronic Circuits and Systems (ICTEAM/ECS) group at UCLouvain, Belgium

Given the ubiquity of electronic devices and the urgent need to decrease our footprint in the context of global warming and planetary boundaries, it becomes critical to thoroughly consider the environmental impacts of integrated circuit (IC) production. This presentation therefore focuses on the environmental sustainability of IC production by covering three main topics: (i) an extensive review of the data currently available in foundry reports, industry roadmaps, scientific literature, and life-cycle assessment databases; (ii) the analysis of historical trends regarding the environmental footprint of CMOS technology for environmental indicators normalized by area; and (iii) the conflicts between current semiconductor roadmaps and global environmental limits, as outlined in the Paris Agreement for instance.

Thibault Pirson is a PhD researcher since 2019. He holds a master degree in Electrical Engineering and works on life cycle assessment (LCA) applied to electronics, more specifically on LCA applied on the Internet-of-Things (IoT) devices.
In 2020, he co-founded and organized with other researchers the sustainable ICT (SICT) doctoral school, which questions the sustainability of ICT from inter- and transdisciplinary perspectives.

How innovation leads to a better, safer, more secure and sustainable world?

Patrick PYPE – Director of Strategic Partnerships, NXP Semiconductors

The presentation will focus on dedicated steps in designing and manufacturing technologies, that lead to a positive impact on the planet and society and to the achievement of carbon neutrality in operations. Collaboration with stakeholders is key to the continuous improvement of an Environment, Social and Governance program. During the presentation it will be shown how our MSCI ESG rating was upgraded from 'AA' to 'AAA'. This is largely driven by improvements in our corporate governance and conflict mineral management programs, in particular, how we are leading peers in practices to mitigate risks associated with conflict mineral use in chip manufacturing. A number of different initiatives will be

presented, including specific innovation projects which lead to a better, safer, more secure and sustainable world.

Before he worked at Imec, **Patrick Pype** was co-founder of the company CoWare on hardware/software co-design and held different positions at Philips. He is Chairman of the AENEAS Technical Expert Group since 2018 and is member of the INSIDE Steering Board since 2015. He was co-chair of the overall ECSEL Strategic Research Agenda 2019-2021 and he is currently chairing a European Working Group on RISC-V and Open-Source.

Sustainable printed circuits: a possible path to greener electronics

Attila GÉCZY – associate professor, Budapest University of Technology and Economics (BME-VIK)

Aiming for sustainability is an important aspect of both traditional and innovative electronics of the near future. Biodegradable, or bio-based printed circuit boards are a possible solution in the pathfinding process. In the talk, the road to a reinforced, flame retarded bio-based substrate will be presented from the beginnings to the more advanced applications.

Attila Géczy is a habilitated associate professor at the Budapest University of Technology and Economics, Dept. of Electronics Technology. His research field involves heat transfer aspects of surface mounting and reflow technologies, and the advance research of biodegradable substrates in electronics assembly.

Building Safe-and-Sustainable-by-Design Community in Electronics

Dmitri PETROVYKH – Corporate Expert, International Iberian Nanotechnology Laboratory (INL)

The formation by SEMI of the Semiconductor Climate Consortium and the publication of the EC Recommendation on the Safe-and-Sustainable-by-Design (SSbD) assessment framework at the end of 2022 highlighted the need to plan the SSbD transition in the electronics value chain. Guidance and assistance in this process will be provided by dedicated SSbD projects, including IRISS: InteRnatIonal ecosystem for accelerating the transition to Safe-and-Sustainable-by-Design materials, products and processes.

Dr. Dmitri Petrovykh is a Corporate Expert at INL, using his broad expertise in science and technology to promote interdisciplinary research activities as well as productive partnerships with industry.

PANEL SESSION 1

Challenges and Solutions for Sustainable Electronics

Chair

Karine Samuel
Vice-President for International Affairs, Université Grenoble Alpes

Patrick Pype
Director of Strategic Partnerships, NXP Semiconductors

Leo Kenny
IRDS ESH/S Team leader

Isabel Obieta
Programme Manager, EC/EISMEA

Markus Pfeffer
Senior Manager Quality and Process Control, Fraunhofer IISB

Thomas Ernst
Scientific Director, CEA-Leti

Dominique Thomas
Director Funded Programs France, STMicroelectronics

Mustafa Badaroglu
IRDS More Moore Team leader

Cédric Rolin
SSTS Programme Manager, Imec

Networking Cocktail

Panel speakers

Karine Samuel, Vice-President for International Affairs of the Université Grenoble Alpes

Karine is Full Professor of Management at the Grenoble Institute of Technology and Management (Grenoble INP-UGA). Her area of expertise relates to supply risks and the resilience of organizations, with a specific focus on risks linked to the lack of visibility in supply chains. She is also President of the International Association for Research in Logistics and Supply Chain Management (AIRL-SCM).

Patrick Pype, Director of Strategic Partnerships, NXP Semiconductors

Patrick is Chairman of the AENEAS Technical Expert Group since 2018 and is member of the INSIDE Steering Board since 2015. He was co-chair of the overall ECSEL Strategic Research Agenda 2019-2021 and he is currently chairing a European Working Group on RISC-V and Open-Source.

Leo Kenny, IRDS ESH/S Team leader

Leo is currently the Chair of the EHS/Sustainability Technical Work group for the IRDS for the Semiconductor Industry and a prior Co-Chair of the Sustainable Electronics Section for INEMI. He has a PhD in Physical Inorganic Chemistry (Tufts University, Boston) with a research focus on thin film batteries and electrochromic smart window devices.

Isabel Obieta, Programme manager for Sustainable Electronics, European Innovation Council

Isabel earned a Doctoral Degree in Science (Microelectronics-Materials for Sensors) from the University of Navarra (Spain). All along her career, she has combined her job with activities as expert in innovation by performing Technology Due Diligences, evaluating new business opportunities for Venture capitals and Family offices or as Innovation Radar Expert for EU projects.

Markus Pfeffer, Senior Manager Quality & Process Control / Funded R&D, Fraunhofer IISB

Markus works at Fraunhofer IISB in the Business Department Semiconductor Technology, where he is the deputy fab manager of the Fraunhofer IISB Pi-Fab (SiC Processing and Prototype Fabrication) and he is in charge of quality and process control as well as founded research.

Thomas Ernst, Scientific Director, CEA-Leti

Thomas, Scientific Director at CEA-Leti, is responsible for long-term research strategy and partnerships. From 1997-2000, he developed with STMicroelectronics and the CNRS the characterization of the advanced modelling of FD-SOI. He then joined CEA-Leti and led the development team of the world's first 3D-stacked CMOS nanowires and nanosheets.

Dominique Thomas, Director Funded Programs France, STMicroelectronics

After a PhD in Solid State Physics from Paris-Orsay University, Dr. Thomas held several R&D management positions in the industry, both in semiconductor and application fields such as Optronics (Thales) or environmental sensing (Envea). He joined ST in 1999. From 2009-2018, he was the Director of the "Centre Commun de Microelectronique de Crolles". He is now with the Europe and France Public Affairs team.

Mustafa Badaroglu, IRDS More Moore Team leader

Mustafa works at Qualcomm with focus on technology ramp and architecture enhancements of AI chipsets, ultra-low voltage process and design methods and stacked memory technologies. Before joining Qualcomm, he previously worked at Huawei, imec, ON Semiconductor, and Tubitak Space.

Cédric Rolin, Manager for the Sustainable Semiconductor Technologies and Systems Program, imec

After more than 15 years spent both at imec and at University of Michigan holding various positions as researcher and team leader in the fields of flexible and organic electronics and nanoimprint lithography, Cédric has joined in 2021 the sustainability team of imec as Program Manager, focusing on the assessment and improvement of the environmental footprint of the semiconductor manufacturing industry.

SESSION 4 – Advanced functionalities

The More than More domain in the IRDS: white paper & future perspectives

Enrico SANGIORGI – Director Emeritus SiNANO Institute – IRDS More than Moore Team leader

The objective of More than Moore is to extend the use of the silicon-based technology developed in the microelectronics industry to provide new, non-digital functionalities.
The concept of "More than Moore" was introduced in the 2005 edition of the ITRS. Since then, the perspective of the roadmap shifted from being mostly technology driven to being increasingly determined by application requirements. In line with this, the ITRS evolved into the International Roadmap for Devices and Systems, including the More than More domain.

Enrico Sangiorgi is professor of Electronics the University of Bologna and Director Emeritus of the Sinano Institute. He is a member of the Aeneas Supervisory Board and Chairman of the Aeneas Scientific Council. He is coordinator of the Italian Government Task Force on Semiconductors Expert Group and Editor-in-Chief of the IEEE Journal of the Electron Device Society, Distinguished Lecturer of the Electron Device Society, and Fellow of the IEEE. His research covers the physics, characterization, modelling, and fabrication of solid-state devices and integrated circuits. He has been working on device scaling, its technological, physical, functional limits, and reliability.

Smart sensors

Innovation in MEMS for the IoT and our digital life

Matthias ILLING – Program Manager Collaborative R&D, Bosch

Microelectromechanical systems (MEMS) are made with specialized semiconductor technologies that are particularly suited for sensors and actors. They connect the physical life with our digital life. Innovation and technology advances broaden their application scope every year. The presentation will provide examples of recent developments of this exciting technology with a strong European presence.

Matthias Illing studied physics in Würzburg, Germany and Buffalo, NY. He received a PhD in applied physics for work on quantum structures and lasers based on III-V and II-VI semiconductors. He joined Bosch in 1996 as project lead for MEMS process and product development. He also held various leadership positions in development, product management as well as research and product innovation. Since 2018 he is responsible for the program management of cooperative R&D projects at Bosch's Automotive Electronics division.

Low power transducers for the IoT

Dr. Cosmin ROMAN – Senior Assistant at ETH Zürich

This presentation focuses on the role of sensors, and tangentially on energy harvesters, in achieving autonomous operation of wireless sensor nodes. We derive energy consumption bounds based on energy storage solutions and wireless communication, and give guidelines to select or develop sensing technologies. Zero-powered, self-powered sensors and other emerging energy-oriented approaches will be reviewed.

Dr. Cosmin Roman is with the Micro and Nanosystems group at Swiss Federal Institute of Technology Zürich (ETHZ) since 2006.

His research interests encompass the science and technology of solid-state micro and nanotransducers, from traditional Silicon micromachining to Carbon nanotubes, with a special emphasis on energy efficient transducer concepts.

Sensors for Agriculture & the Environment

Alan O'RIORDAN – Senior Research Fellow Tyndall

With the global population expected to grow to over 9.6 billion by 2050 it is a projected that a 50-60 % increase in food production will be required. A key challenge then, going forward, will be to sustainably close the food gap. This must be achieved against the backdrop of climate change & desertification, labour shortages and competition for energy, land & resources. It is clear then, that addressing this challenge will require the development of more efficient and sustainable food production techniques and processes. To this end, new technologies, that are fit for purpose, are urgently required to digitise the entire food chain. This convergence between the Internet of Things (IoT) and the agri-food industry requires sensor systems and technologies that provide real time data to producers and processers; required for rapid, but informed, decision making. This presentation will provide an overview on current problems in agriculture and demonstrate how digital technologies can address the sustainability issues currently being experienced in this sector.

Dr. Alan O'Riordan received a PhD in Chemistry (Nanotechnology) in 2005. He leads a team focused on developing smart sensors and systems for Sustainable Agri-food and Environmental applications. He has led the European team's contribution on Smart Sensor Systems for the recent IEEE International roadmap on Devices and Systems - More than Moore white paper. He won the Enterprise Ireland Gold Medal for Most Innovative Technology Emerging from Third Level (National Ploughing Contest 2016/2022). He is Core steering committee member of EPoSS SSI conferences 2021 & 2022, and a H2020 Technical evaluator for ICT photonics call.

Smart energy

SiC VDMOS Technology evolution as an example for sustainable and efficient energy conversion

Dr. Markus PFEFFER – Senior Manager Quality and Process Control / Funded R&D at Fraunhofer Institute for Integrated Systems and Device Technology IISB

The commercialization of 4H-SiC power devices for industrial and automotive applications is in full progress. Cost pressure and technology innovation are pushing device performance to the next level. Conversely, further progress is become more challenging in modern manufacturing technologies due to the increasing effort towards device optimization. In order to visualize the progress revolving around SiC power device evolution, the technology and design innovation history for VDMOS transistors is reviewed first. This includes wafer quality and diameter, design improvements using JFET implantation and cell shrink. Then, device optimization strategies are discussed. This includes trade-offs between on-state resistance, blocking voltage (performance), surge current and avalanche capability (ruggedness) as well as gate oxide reliability and yield. Finally, a basic roadmap is presented to project further optimization strategies like overlay accuracy, wafer grinding, alternative wafer materials and yield optimization (e.g. for thermal oxidation, wafer substrates).

Dr. Markus Pfeffer holds a diploma in Electrical Engineering and a PhD (Dr.-Ing.) with specialization in manufacturing optimization both from the University of Erlangen-Nuremberg. Since 2002 he has been working at Fraunhofer IISB in the Business Department Semiconductor Technology, where he is the deputy fab manager of the Fraunhofer IISB Pi-Fab (SiC Processing and Prototype Fabrication) and he is in charge of quality and process control as well as founded research. He was and is involved in several national and international cooperative R&D projects in different functions.

Wide Bandgap Power Devices for a Sustainable Future

Mikael ÖSTLING – Professor, solid state electronics, KTH Royal Institute of Technology (Sweden)

The world is in a frantic pace towards electrification. The annual total electrical energy consumption is around 26000 TWh and will double in 15-20 years. We are in urgent need of improved energy efficiency in many technology fields. In energy generation, in energy distribution and in energy storage. More than 50% of the electrical energy in the world is passing through semiconductor power devices. Semiconductor devices made in wide bandgap materials such as silicon carbide SiC and gallium nitride GaN will contribute significantly to the needed energy efficiency. If only a 1% efficiency improvement in the whole value chain is achieved, 100 average fossil-based power plants can be saved. This paper will discuss recent power device trends and accomplishments in SiC and GaN technology and illustrated what typical improvements that we already can see and what to expect.

Mikael Östling received his MSc and the PhD degrees from Uppsala University, Sweden. He was deputy president of KTH between 2017-2022. His research interests are nanoscaled Si and Ge device technologies and emerging 2D materials, as well as device technology for wide bandgap semiconductors for high power/high temperature applications. He has supervised 47 PhD theses work and co-authored 500+ scientific papers published in international journals and conferences. Östling was an editor of the IEEE Electron Device Letters 2005-2014 and editor in chief of the IEEE J-EDS 2016-19. Östling is a Fellow of the IEEE.

SESSION 5 – Beyond CMOS

Ferroelectric memories – Enabler for novel computing architectures

Konrad SEIDEL – Manager of the "Emerging Memories" group, Fraunhofer IPMS, Center Nanoelectronic Technologies

After introduction of concept for ferroelectric hafnium oxide based devices we will present typical implementation examples and discuss advantages and challenges for applications. As one aspect typical reliability are discussed and compared with other solutions. In the second part concepts with ferroelectric devices in novel computing architectures will be presented.

After receiving his diploma degree in Information Technology at TU Dresden in 2004, **Konrad Seidel** joined the Flash memory development group of Infineon Flash and accompanied different positions in the field of Reliability and Qualification of different memory concepts. In 2008, he joined the Fraunhofer Society and worked on various integration and characterization activities as well as new device concepts. He has about ten years of experience in managing industrial and public funded applied research projects bringing new device concepts and integration approaches to demonstration level.

On and Beyond CMOS

Jouni AHOPELTO – Chair of Nanoelectronics, VTT Technical Research Centre of Finland

In this presentation we will discuss some of the promising candidates for back-end integration of extra functionalities on CMOS platform to enhance the performance of the current circuits. In addition, we will briefly cover the potential of ultra-low power IT based on optoelectromechanics.

Professor **Jouni Ahopelto** is holding the chair of Nanoelectronics at VTT Technical Research Centre of Finland.
His research interests include various aspects of nanotechnology, arching from electronics to photonics to phononics with the main emphasis currently on nanophononics and nano-optoelectromechanics.

Gate all around nanowire FETs: Operation from RT to Cryogenic temperatures

Qing-tai ZHAO – Forschungszentrum Jülich (FZJ)

Gate-all-around (GAA) nanowire (NW) FETs have emerged as highly promising candidates for ultra-short channel FETs, owing to their superior electrostatics. In this presentation, we will discuss our research on Si and GeSn nanowire GAA FETs, with a particular emphasis on their steep slope switching at cryogenic temperatures. Our study has significant implications for the development of cryogenic computing applications.

Qing-Tai Zhao completed his PhD in Physics at Peking University, China, in 1994, and subsequently joined the Institute of Microelectronics at the same university, where he focused on research of SOI materials and devices. In 1997, he was awarded as a Humboldt Research Fellow and started his research in Forschungszentrum Juelich, Germany, where he currently leads a group on the research of nanoelectronic devices. His primary research focuses on Si-Ge-Sn based devices and technology, FDSOI and nanowire devices, neuromorphic devices and cryogenic electronics.

Flexible electronics with 2D materials

Andreas HEMMETTER – Ph. D, AMO/ RWTH Aachen University

2D materials excel in terms of flexibility and frequency response, and are therefore prime candidates for enabling a new generation of flexible, wearable electronic devices. This presentation highlights the recent advances in 2D materials-based electronics fabrication achieved at AMO with a special focus on devices on flexible substrates.

Andreas Hemmetter received his B.Sc. degree in physics from TU Dresden (Germany) in 2016, and his M.Sc. degree in metamaterials and nanophotonics from ITMO University in St. Petersburg in 2018, where he was involved in research on perovskite optoelectronics.

He is currently with AMO GmbH in Aachen, Germany and is pursuing a Ph.D. degree at RWTH Aachen University, where he focuses on graphene diodes for high-frequency applications and energy harvesting.

IRDS Beyond CMOS Presentation

An CHEN – IRDS Beyond CMOS Team leader

This presentation will provide an overview of the IRDS Beyond-CMOS roadmap, including Emerging Materials Integration. The BC roadmap covers emerging memory and logic devices, as well as their applications in novel computing paradigms. The co-optimization of beyond-CMOS devices and architectures has become a key driver of this roadmap.

An Chen is a Research Staff Member at IBM Research, Almaden Center. He has worked on emerging memory devices, beyond-CMOS technologies, and analog AI hardware. He received his Ph.D. degree from Yale University.

SESSION 6 – Quantum Information Processing

IRDS technology roadmaps for Cryogenic Electronics and Quantum Information Processing (CEQIP)

Dr. Scott HOLMES – IRDS Cryogenic Electronic and Quantum Information Processing Team leader

CEQIP covers superconductor electronics (SCE), cryogenic semiconductor electronics, and quantum information processing. After a status summary for these areas, the talk will focus on current efforts to develop a roadmap for superconducting quantum computing. Important needs in the roadmap include cryogenic electronics for control and readout of the superconducting qubits.

Dr. D. Scott Holmes chairs the Cryogenic Electronics and Quantum Information Processing (CEQIP) International Focus Team (IFT) for the International Roadmap for Devices and Systems (IRDS). He is a member of the IEEE Council on Superconductivity as a representative of the Electron Device Society. Work experience includes IARPA, DARPA, Talsico, and Lake Shore Cryotronics. He received a BSME from MIT and graduate degrees from the University of Wisconsin–Madison.

The path to large scale quantum computing based on CMOS technology

Maud VINET – Physicist, Co-founder of Siquance

Quantum computing when available will tackle life changing applications, like in energy or chemistry. Silicon has the ability to enable this full quantum advantage leveraging Very-Large-Scale Integration (VLSI) fabrication and design techniques. First scientific demonstrations have been made, it's now up to electrical engineers in collaboration with physicist to turn these demonstrations into practical machines.

After starting her career as a research physicist, **Maud Vinet** spent 20 years in development and technology transfer in the semiconductor industry at CEA-Leti. She spent 5 years in Albany (NY) working with STMicroelectronics, IBM and Globalfoundries to develop FDSOI technology.
In 2022, she stepped in entrepreneurship by co-founding Siquance, which aims to develop and commercialize a quantum computer based on microelectronics technologies.

The European Quantum Strategic Industry Roadmap by QuIC

Dr. Johanna SEPÚLVEDA – Chief Engineer, Airbus

The European Quantum Industry Consortium (QuIC) has a mission to boost European industry competitiveness in quantum technologies, to foster economic growth and value creation for business and

citizens. QuIC brings together 170 members, including large companies, SMEs, investors, academic and research organisations, and associations. QuIC members discuss a wide variety of strategic topics for the quantum uptake in Europe, all compiled in the Strategic Industry Roadmap (SIR). In this talk, the SIR will be presented highlighting the current state of quantum technologies in Europe, trends and needs for a strong pan-European quantum position.

Johanna Sepúlveda received her M.Sc. and Ph.D. degrees in Electrical Engineering – Microelectronics by the University of São Paulo, Brazil. She was a Senior Researcher in the area of security and emerging technologies at the University of South Brittany (France), INRIA (France) and at the Technical University of Munich (Germany). Currently she holds a position as the Airbus Expert on Quantum-Secure Technologies, being Chief Engineer of different European quantum initiatives such as EuroQCI. She is a member of the Strategic Advisory Board of Quantum Technologies for the European Commission and leader of the Strategic Industry Roadmap at the Quantum Industry Consortium (QuIC).

PANEL SESSION 2
Strategy for International Cooperation - Chips Act

Chair

Patrick Cogez
Technical Director, AENEAS

Paolo Gargini
IRDS Chairman & US Chips Act

Mathias Illing
Bosch

Carlo Reita
Director, Strategic Partnerships and Planning at CEA-Leti

Enrico Sangiorgi
Director Emeritus SiNANO Institute – IRDS More than Moore Team leader

Holger Schmidt
Senior Director Funding Projects & Coordination, Infineon Technologies AG

Markus Pfeffer
Senior Manager Quality and Process Control / Funded R&D, Fraunhofer IISB

Giorgos Fagas
Head of CMOS++ and EU Programmes, Tyndall

Abdul Rahim
Program manager, ePIXfab

Networking Cocktail

Panel speakers

Patrick Cogez, Technical Director, AENEAS and Chair of the ECS Strategic Research & Innovation agenda

Patrick graduated from Ecole Polytechnique and Ecole des Ponts et Chaussées (France). He holds a PhD in Industrial Engineering from UC Berkeley (US). He completed an Executive MBA at NEOMA Business School, Paris. He joined STMicroelectronics in 1988, where he designed and implemented the Information Systems of the Crolles site, and was later appointed Director for Innovation and External Research.

Paolo Gargini, IRDS Chairman & US Chips Act

In 1980 as manager of MPU technology at Intel, Paolo transferred into manufacturing the iconic 80286 and 80386. Later he became Director of Technology Strategy and responsible for worldwide consortia research until 2012. From 1998 to 2015, he was Chairman of the ITRS sponsored by the WSC. Since 2016 he is the Chairman of the IRDS sponsored by IEEE.

Mathias Illing, Program Manager Collaborative R&D BOSCH

Mathias received a PhD in applied physics for work on quantum structures and lasers based on III-V and II-VI semiconductors. He joined Bosch in 1996 as project lead for MEMS process and product development. Since 2018 he is responsible for the program management of cooperative R&D projects at Bosch's Automotive Electronics division.

Carlo Reita, Director, Strategic Partnerships and Planning at CEA-Leti

Carlo is in charge of the relations with major RTOs and of the actions for the support of nanoelectronics in the future EU R&D plans. In the last years he has been acting as "Sherpa" of the Leti Director for EU documents, discussions…and representing Leti to Int. Public Authorities/Private Companies as well as constructing the overall materials, devices, integration & design enablement roadmap for computing.

Enrico Sangiorgi, Director Emeritus SiNANO Institute – IRDS More than Moore Team leader

Enrico is professor of Electronics at the University of Bologna and Director Emeritus of the Sinano Institute. His research covers the physics, characterization, modelling, and fabrication of solid-state devices and integrated circuits. He has been working on device scaling, its technological, physical, functional limits, and reliability.

Holger Schmidt, Senior Director Funding Projects & Coordination, Infineon Technologies AG

Holger has been working for Infineon Technologies AG (formerly Siemens Semiconductors) since 1995 in different positions related to design automation, project management in the area of wireline communication and since 2012 he is responsible for collaborative projects on European and national level.

Markus Pfeffer, Senior Manager Quality & Process Control / Funded R&D, Fraunhofer IISB

Markus works at Fraunhofer IISB in the Business Department Semiconductor Technology, where he is the deputy fab manager of the Fraunhofer IISB Pi-Fab (SiC Processing and Prototype Fabrication) and he is in charge of quality and process control as well as founded research.

Giorgos Fagas, Head of CMOS++ and EU Programmes, Tyndall

Giorgos has been contributing to key int. strategic R&I agendas incl. the ECS-SRIA and IRDS and has initiated several EU projects. He leads the ASCENT+ Programme (Access to European Infrastructure for Nanoelectronics) and the ICOS workpackage Technology Scanning & Foresight. Giorgos research focuses on quantum devices and energy-efficient nanoelectronics.

Abdul Rahim, Program manager, ePIXfab

In his ePIXfab role, Abdul orchestrates activities for the advocacy of silicon photonics, designs educational and training activities for silicon photonics, provides matchmaking and consultancy to the adopters of silicon photonics technology, and tracks the evolution of the latest trends followed by the field.

SESSION 7 – Japanese session

Japan's Semiconductor Strategy

Hisashi KANAZASHI, Director of IT Industry Division, Commerce and Information Policy Bureau, Ministry of Economy, Trade and Industry

The environment surrounding the digital industry, digital infrastructure and the semiconductors they are based on is facing significant changes. These include the advance of digitalization due to COVID-19 responses, the moves toward carbon neutrality by 2050, tight supply/demand conditions of semiconductors worldwide, trade issues surrounding cutting-edge semiconductors and digital technologies, and economic security. In this presentation, the strategy of Japan's semiconductor industry recognizing these changes, including enhancement of basic semiconductor production capacity, technology development for beyond 2nm next generation semiconductor and so forth.

Hisashi Kanazashi entered to the Ministry of International Trade and Industry in 1998. He was a visiting fellow at Stanford University and received his MBA from EDHEC Business School.

He has successively hold the positions at Industrial Revitalization Division, Economic and Industrial Policy Bereau and at Policy Planning and Coordination Division, Minister's Secretariat since 2009.

He also has experienced the positions of Director of Japan's Economic Revitalization Secretariat, Cabinet Sectetariat, as well as Deputy Commissioner of Los Angeles Office, Japan External Trade Organization, and Director of Industry Creation Policy Division, Economic and Industrial Policy Bureau, etc., since 2014. He has been on his current position since July 2022.

EC presentation- Colette Maloney, Head of Unit, EC/DG Connect

AI Chip Design Center (AIDC), SoC design platform for small industries and startups in Japan

Professor Makoto IKEDA, Tokyo University

AIDC has jointly established with AIST and the University of Tokyo, in 2018, founded by Ministry of Economy, Trade and Industry (METI) and New Energy and Industrial Technology Development Organization (NEDO), aiming encouraging AI hardware implementation by small industries and startups in Japan. This talk covers overall activities of AIDC, including details of design platform, and especially our exampled designs, AI-One, and AI-Two, which are SoCs with multi-core AI-IPs from different companies. Based on these designs, we provide not only complete design flow of such SoCs, but also education program & materials.

Makoto Ikeda received the B.S., M.S., and Ph.D. degrees in Electronic Engineering from the University of Tokyo, Tokyo, Japan, in 1991,1993, and 1996, respectively. He joined the Electronic Engineering Department, University of Tokyo, as a Faculty Member in 1996, and he is currently a full Professor with the Systems Design Lab, at the University of Tokyo.

His research interests include the hardware security, including cryptographic engine design, asynchronous system design and smart image sensor designs. Along with this he has been involved in VDEC (VLSI Design and Education Center, the University of Tokyo) activities since 1996, from the beginning, for VLSI chip design platform for entire Japanese Academia.

He served numerous positions in conferences including ISSCC 2021 ITPC Chair, Symposium on VLSI Circuits 2017 Program Chair and 2019 Symposium Chair, and A-SSCC 2025 Program Chair. Also he served IEEE SSCS Distinguished Lecturer in 2015 and 2016, and is now an IEEE SSCS/EDS Commemorative Lecturer for Transistor 75th Anniversary. He is a senior member of IEEE, IEICE Japan, and a member of IPSJ and ACM.

The EU Test and Experimentation Facility for Hardware Edge AI, PREVAIL, as a platform for development of new solutions

Carlo REITA, Director of Strategic Partnerships and Planning in the CTO Office, CEA-Leti

Under the Digital Europe Initiative, the EU has launched the Test and Experimentation Facilities initiative for the development of AI. Within this frame, since December 2022 the PREVAIL project has started preparing an infrastructure to fabricate advanced chip demonstrator from the design community and aiming at lowering the power demands of distributed AI. The presentation will describe the project and how it can serve the EU stakeholders, starting from the results of other AI projects funded by the EU.

Carlo Reita is currently Director of Strategic Partnerships and Planning in the CTO Office of CEA-Leti, (Grenoble, France), in charge of the relations with major RTOs and of the actions for the support of nanoelectronics in the future EU R&D plans. In the last few years he has been acting as “Sherpa” of the LETI Director for EU documents, discussions, events preparation, and representing LETI representative to International Public Authorities and Private Companies as well as constructing the overall materials, devices, integration and design enablement roadmap for computing.

Between 2016 and 2019 he has been the initiator and coordinator of the EU H2020 project NeuRAM3 aiming at using novel technologies like FDSOI, Resistive RAMs, 3D integration and TFT to fabricate bioinspired circuits for embedded artificial intelligence applications. In 2022 he has coordinated the successful bid to the EU for a creation of a joint Test and Experimentation Facility for Hardware AI among CEA-Leti, imec, FhG and VTT (PREVAIL Project).

Megatrends in the autmotive industry and RENESAS' value proposition

Takashi YASUMASU, Vice President, Automotive Core Technology Development Division, Automotive Solution Business Unit, Renesas Electronics Corp.

Megatrends in the automotive industry such as CASE, softwarization and semiconductor market growth, as well as evolutions inside vehicles including E/E architecture change towards software-defined car will be introduced. Renesas' solutions for E/E architecture, EV and AD/ADAS will also be presented.

Takashi Yasumasu started for Hitachi /semi-conductor, Renesas technology and then Renesas electronics corp. He had experience mainly technical marketing and automotive core technology development. Currently, as division head, he is responsible for the core technology development of semi-conductor product and driver software in the Area of Functional Safety, Security and Network. Moreover, he has been involved in ISO26262 functional safety standard creation for more than 12 years. He is now providing support in the Japanese national delegation to the ISO/TC22/SC32/WG8.

Trends in semiconductors for mobility

Matthias ILLING, Program Manager Collaborative R&D BOSCH

Matthias Illing studied physics in Würzburg, Germany and Buffalo, NY. He received a PhD in applied physics for work on quantum structures and lasers based on III-V and II-VI semiconductors. He joined Bosch in 1996 as project lead for MEMS process and product development. He also held various leadership positions in development, product management as well as research and product innovation. Since 2018 he is responsible for the program management of cooperative R&D projects at Bosch's Automotive Electronics division.

ICOS (International Cooperation On Semiconductors) presentation on past and existing cooperation in research between EU-JP

Francis Balestra, ICOS coordinator

Lunch Break

SESSION 8 – Advanced Computing

IRDS More Moore Roadmap for edge and cloud computing

Mustafa BADAROGLU – IRDS More Moore Team leader

More Moore technologies bring promising venues for enabling native interfaces between human and data. Those venues require a global consensus and alignment across the various stakeholders such as industry, academia, consortiums, and national labs. For this motive IRDS More Moore roadmap introduces a 15-year horizon of high-volume-manufacturable More Moore devices to sustain power, performance, area, and cost (PPAC) scaling to enable energy-area-efficient performance for edge and cloud applications. In this talk we will describe the opportunities, challenges, and mitigation paths for the scaling enablement not only by new device structures but also through holistic system integration maximizing the gains from those devices.

Mustafa Badaroglu works at Qualcomm with focus on technology ramp and architecture enhancements of AI chipsets, ultra-low voltage process and design methods and stacked memory technologies. Before joining Qualcomm, he previously worked at Huawei, imec, ON Semiconductor, and Tubitak Space. During his career he had various assignments for the execution and management of mobile and automotive chipset design from concept to initial ramp, process technology pathfinding, and system-technology co-optimization. He holds a PhD in electrical engineering from the Catholic University of Leuven in Belgium

Augmented FDSOI platforms for improved sustainability

Roberto GONELLA – R&D Director, Digital/ NonVolatile/Analog RF Technologies Development at STMicroelectronics

After a brief reminder of the main characteristics of the FDSOI technology, a review of the multiple features implemented in ST platforms to keep leading positions in several domains like the automotive and general-purpose microcontrollers, the IoT, connectivity, the RF communications will be given. This technology, energy-aware by construction, continues being an instrumental enabler in applications where economic and ecological sustainability are relevant performance indicators and few illustrations of it will be shared during the presentation.

Roberto Gonella received his Engineer Degree and the M.S. in Electronic Engineering from both the Politecnico of Turin (Italy) and the INPG (Institut National Polytechnique de Grenoble - France) in 1996.

He is currently Director of the R&D Digital, Non-volatile and Analog RF technologies development in STMicroelectronics Central R&D where he held different technical and managerial positions in domains like the reliability, the electrical characterization, the process integration, the technology modelling, the yield and manufacturability improvement.

Nanosheet-based Device Architectures for Enabling Advanced CMOS Logic Scaling

Anabela VELOSO – Imec

As finFET-based CMOS logic scaling is coming to an end, new device architectures are required to help continue delivering profitable node-to-node scaling gains. In this presentation, the currently expected evolution to vertically stacked nanosheet FETs is discussed, highlighting some of their key aspects, opportunities, and challenges. An extension of this technology could be feasible by strongly reducing the p-n separation with a transition into forksheet devices, beyond which 3D stacked CMOS, also called CFET, where NMOS and PMOS are folded on top of each other by a monolithic or 3D sequential approach appear as its ultimate scaling limit. In parallel, to take full advantage of multiple innovations at transistor level, de-coupling signal and power wiring by using both wafer sides for routing is a new concept that has been gaining traction enabling further device engineering options and cells scalability.

Anabela Veloso received a Ph.D. from INESC-IST-Lisbon University, Portugal in 2002. Since 2001, she has been working at Imec, in Leuven, Belgium, where she is a principal member of technical staff. Currently, her main research interests are in the areas of advanced CMOS device physics, integration, characterization, and technology, with recent focus on the exploration of scaled nanowires/nanosheets based FETs (with lateral or vertical transport), logic with functional backside, buried power rails, nTSVs, and overall novel device schemes considering also possible options for transistor engineering and connections from front/backside. She has authored or co-authored more than 200 papers published in peer-reviewed international conference proceedings and technical journals, presented 18 invited conference talks, and has been (co-)inventor of more than 23 filed/granted patents. She has also been serving on several conference committees including IEDM, SSDM, ECS Meeting, and the Symposium on VLSI Technology and Circuits.

FDSOI engineered substrates for advanced computing

Sébastien LOUBRIAT – Technology Leader of FDSOI products, SOITEC

FDSOI technology provides an optimal balance of digital performance, mixed-signal compatibility, power consumption, and cost. It is now strongly positioned in megatrends such as the connectivity, automotive and smart device markets. To follow the "More than Moore" roadmap and meet the requirements of the advanced CMOS technologies, Soitec develops and offers innovative FDSOI substrates.

Sebastien Loubriat has received an Engineering Master's Degree (Master 2 Micro & Nano structures) and a Technological Research Diploma (DRT) from University Joseph Fourier (Grenoble). He led his DRT at CEA-Leti (in collaboration with STM) on both elaboration of materials and interfaces study within a PCRAM cell. He joined Soitec as Prototyping engineer, then became Product Industrialization engineer. He led the industrialization of SOI substrates for FinFet transistors and 2D Fully Depleted SOI substrates to address 28nm & 22nm technology nodes. Since 2019, he is in charge as Technology Leader of FDSOI products (from 28 nm to advanced nodes below 12nm), leading the technology from R&D to pre-industrialization phase.

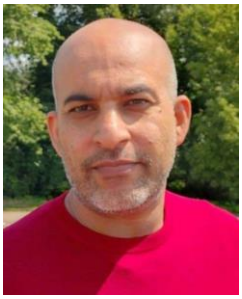
SESSION 9 – Semiconductors-based Photonics

Silicon Photonics: Current state, trends, and future evolution

Dr. Abdul RAHIM – Program manager, ePIXfab – the European silicon photonics alliance

Silicon photonics is a technology that offers compact, energy-efficient, and cost-effective photonic ICs by leveraging the existing CMOS infrastructure. Silicon photonics made a transition from lab to fab in the last decade. Today several industrial fabs offer silicon photonics as a technology option for the next generation of telecom and datacom applications. The versatility of this technology makes it an interesting choice for several other applications, such as high-performance computing, AI acceleration, medical diagnostics, industrial sensing, LiDAR, etc.

In this talk, I will discuss the current state of the silicon photonics ecosystem, the latest trends followed by the field, and how the field is expected to evolve in the years ahead. The talk will also position the European silicon photonics ecosystem with respect to the rest of the world.



Dr. Abdul Rahim is a silicon photonics evangelist with a comprehensive grasp of the global silicon photonics ecosystem. In his ePIXfab role, he orchestrates activities for the advocacy of silicon photonics, designs educational and training activities for silicon photonics, provides matchmaking and consultancy to the adopters of silicon photonics technology, and tracks the evolution of the latest trends followed by the field. He holds a Ph.D. in silicon photonics from the Technical University of Berlin and a degree in innovation management from HEC Paris.

Neuromorphic Computing - At the intersection between Electronics and Photonics

Stephan SUCKOW – Nanophotonics group leader, AMO GmbH

The talk gives an overview of the main semiconductor based photonic platforms and compares them to dielectric platforms, including the perspective of integration with CMOS electronics. Some recent more niche developments will be presented.

Stephan Suckow obtained his B.Sc. and M.Sc. in Physics of Semiconductor Technology from the BTU Cottbus, Germany, and his PhD in Physics from RWTH Aachen University in 2012 on the simulation of photonic silicon nanostructures. He joined AMO in 2015, became the vice head of the Nanophotonics group in 2018 and is leading the group since 2022. He coordinates the H2020 project POSEIDON, is the technical manager of the H2020 Project GRACED and coordinates the work at AMO for several other national and European funded projects

Silicon photonics and applications

Frédéric BŒUF – STMicroelectronics

Silicon photonics attracted a lot of interest in the last decade, due to its potential in addressing low cost and large volume optical applications. STMicroelectronics developed Silicon Photonics technologies for

datacom applications from 100G to 400G, but also R&D on sensing applications. We will detail these platforms and some example of applications addressed in R&D.

Frédéric Boeuf joined STMicroelectronics in Crolles working on Advanced Devices Physics and Integration in 2000. He led the 65nm and 45nm research program as well as the UTBB and FDSOI research program between 2006 and 2012. He also led the development of MASTAR road-mapping tool used by the ITRS for more than 10 years.

Since 2011 he's leading the Silicon Photonics program in STMicroelectronics Crolles, especially the development of 100G and 400G Silicon Photonics platforms.

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