Assessing the environmental impact of integrated circuit chip manufacturing

Cédric Rolin

Program Manager, Sustainable Semiconductor Technologies & Systems

ICOS Workshop, April 26, 2023, 15:00

Session 3: Sustainable Electronics

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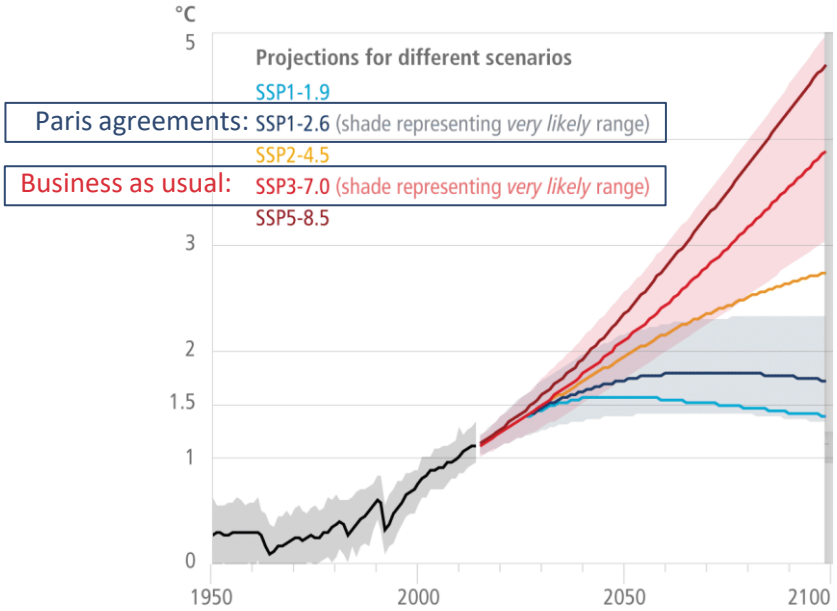
Risks for increasing levels of global warming

IPCC AR6 Synthesis report: Summary for Policy Makers Figure 4, March 2023, https://www.ipcc.ch/report/ar6/syr/downloads/report/IPCC_AR6_SYR_SPM.pdf

Global surface temperature change



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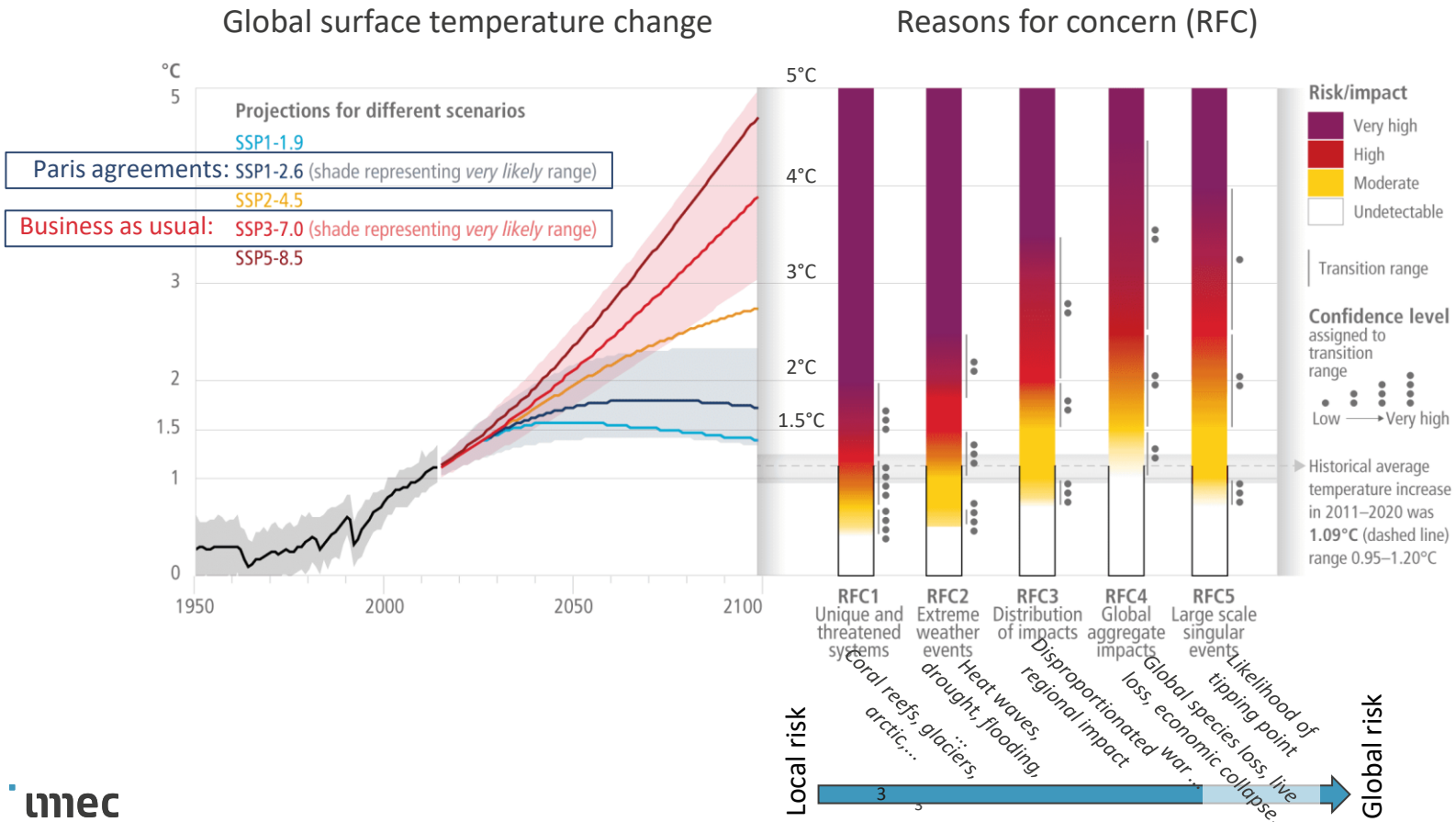
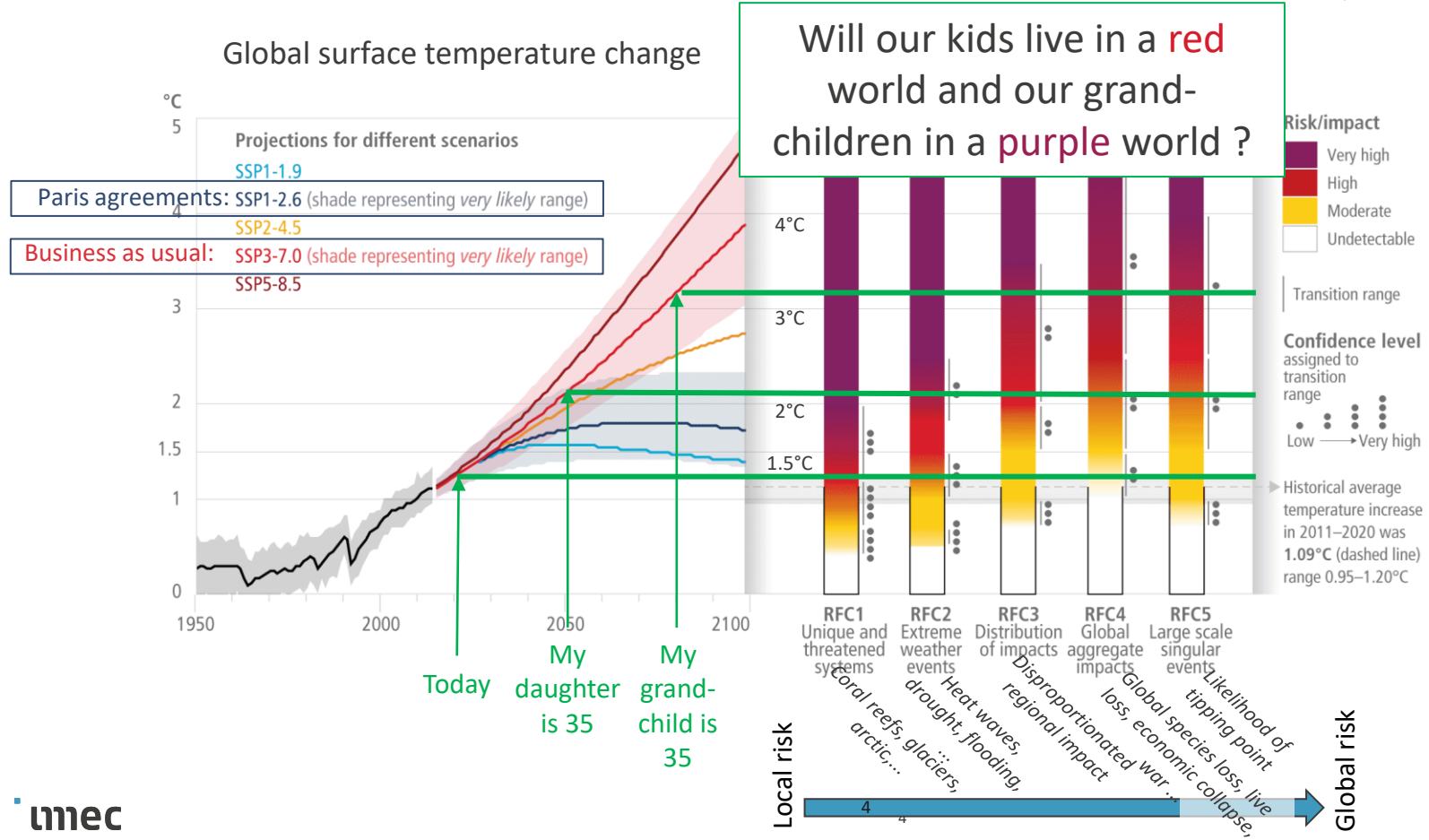


Risks for increasing levels of global warming

IPCC AR6 Synthesis report: Summary for Policy Makers **Figure 4**, March 2023, https://www.ipcc.ch/report/ar6/syr/downloads/report/IPCC_AR6_SYR_SPM.pdf

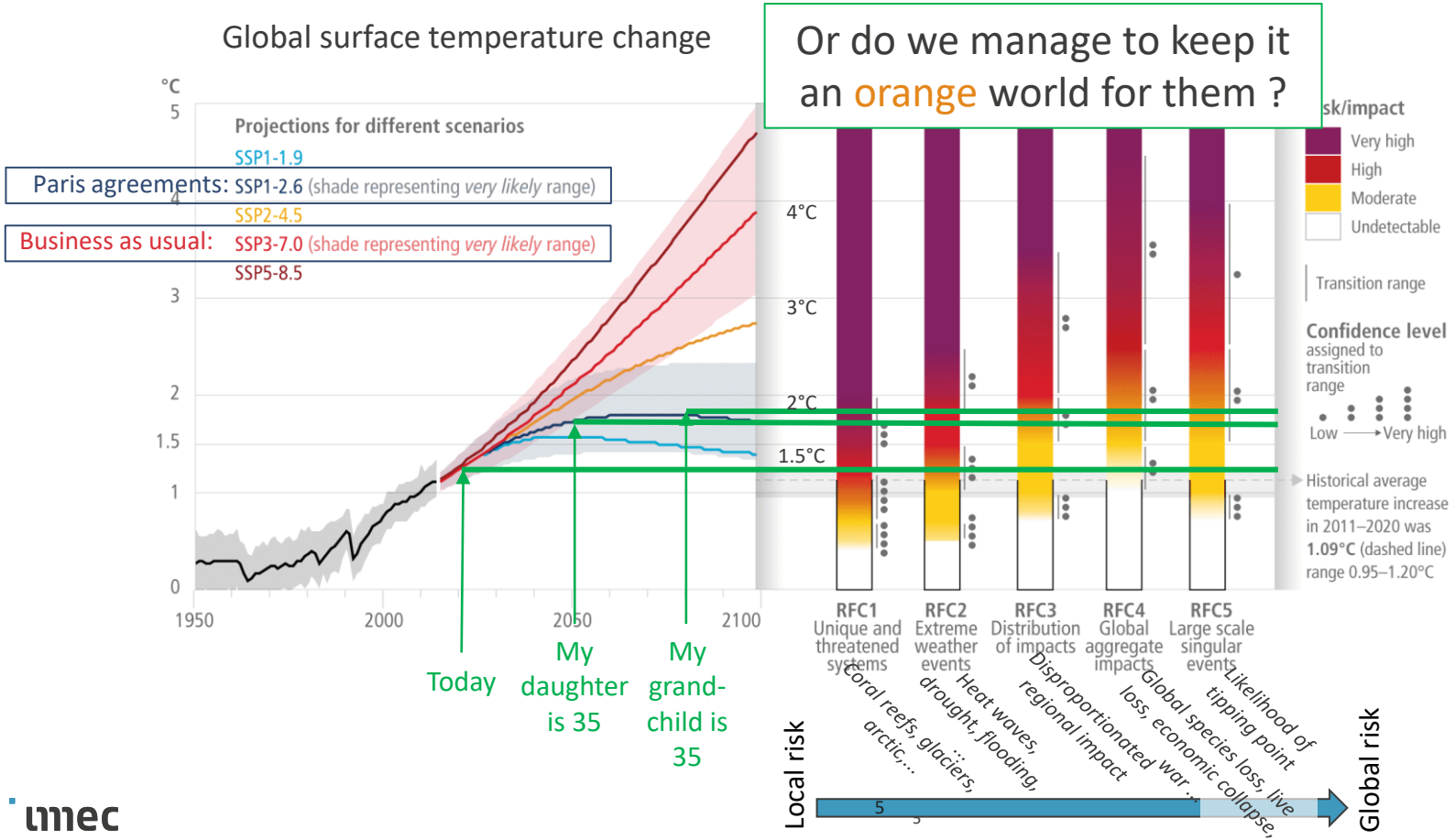
Will our kids live in a red world and our grand-children in a purple world ?



Risks for increasing levels of global warming

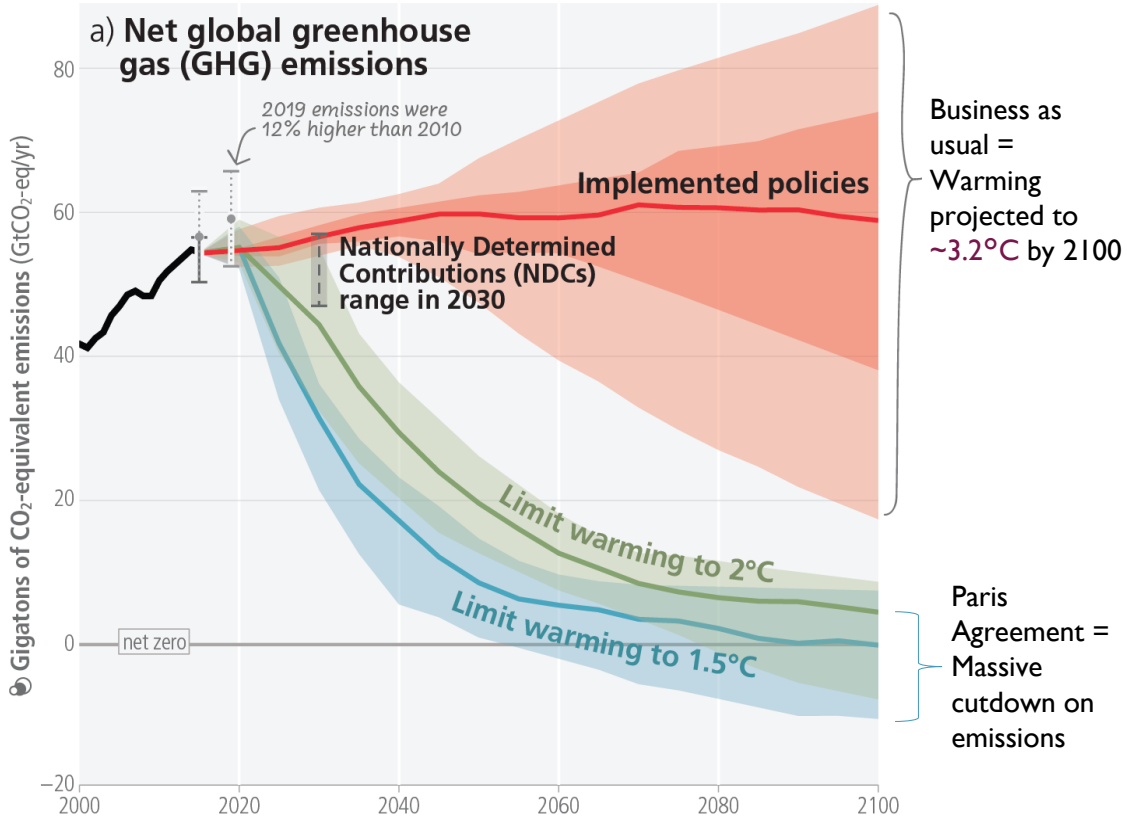
IPCC AR6 Synthesis report: Summary for Policy Makers **Figure 4**, March 2023, https://www.ipcc.ch/report/ar6/syr/downloads/report/IPCC_AR6_SYR_SPM.pdf

Or do we manage to keep it an orange world for them ?



Carbon emission projections in IPCC AR6 Synthesis

IPCC AR6 Synthesis report: Summary for Policy Makers **Figure 5**, March 2023, https://www.ipcc.ch/report/ar6/syr/downloads/report/IPCC_AR6_SYR_SPM.pdf



We are on the road to a purple world...

We need to do much better, not only for future generations, but even for ourselves...

Risk for industry is very high. Semiconductor industry to align on the global efforts.

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Opportunities for scaling on climate action in semicon industry

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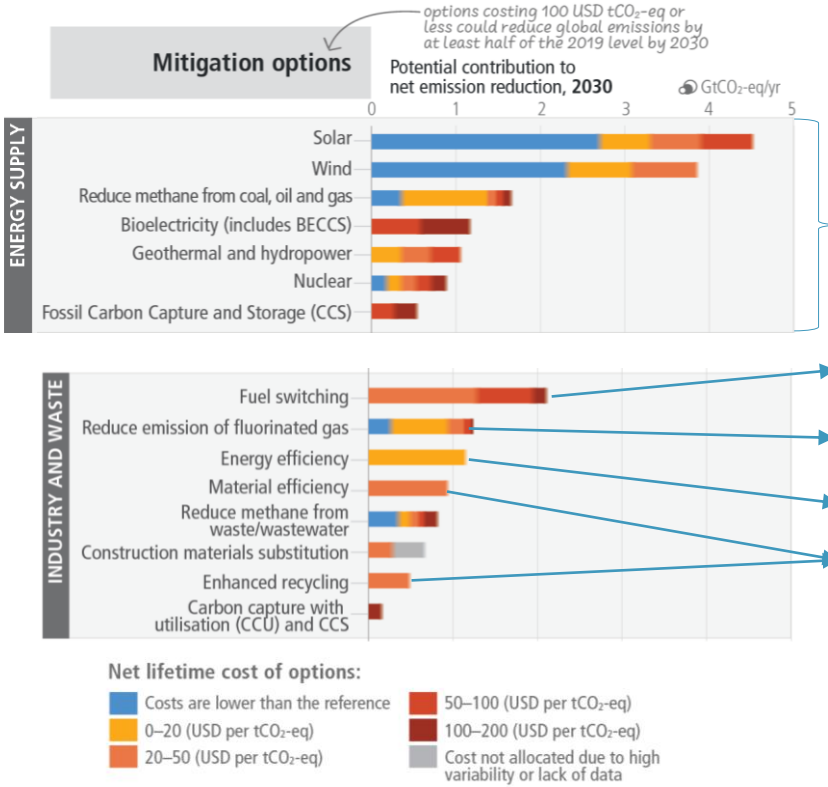
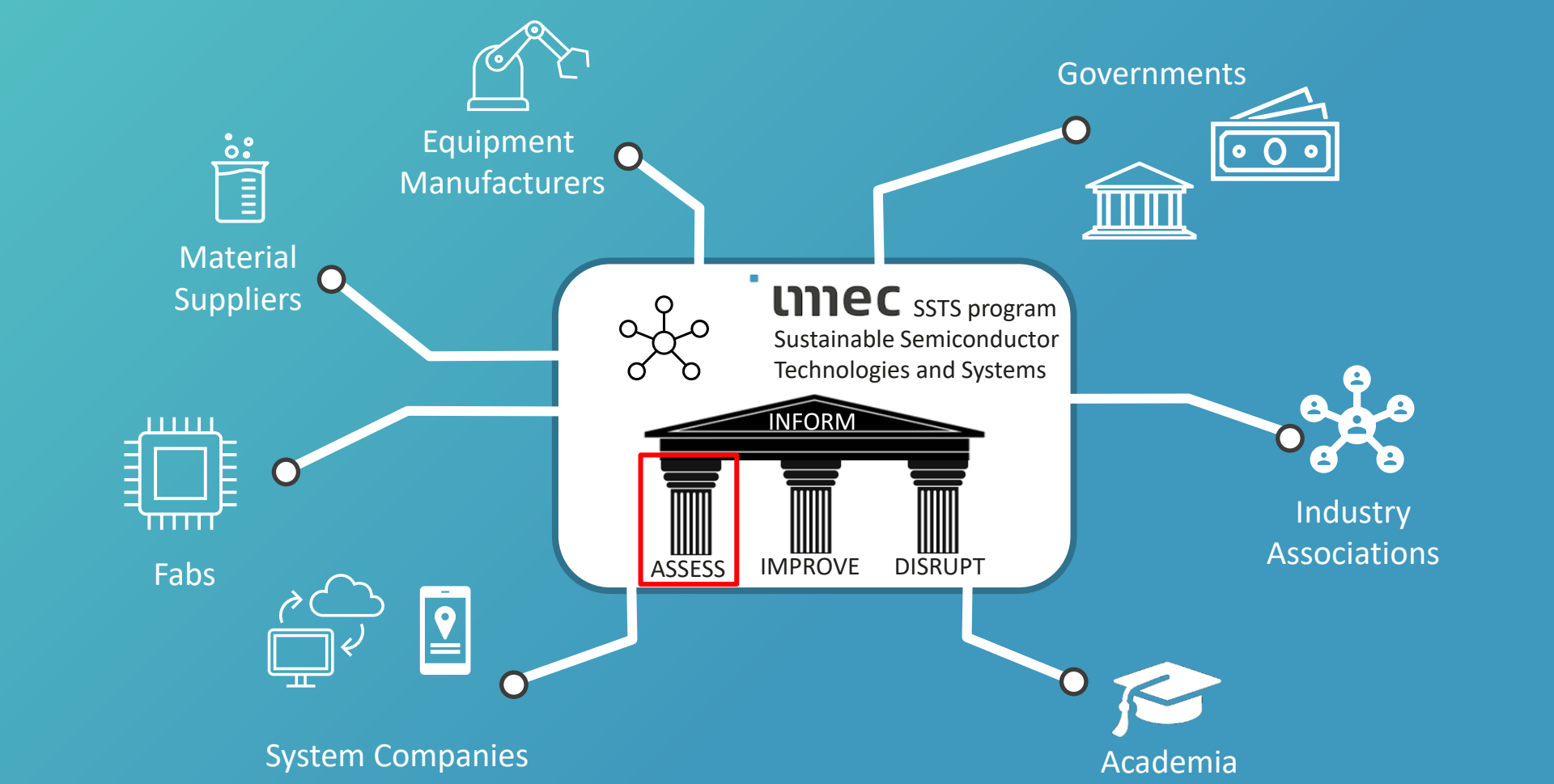


More renewable electricity !!!

- Reduce natural gas consumption
- Replace / Reduce / Abate F-Gasses
- Energy efficiency & Industry 4.0
- Material circularity

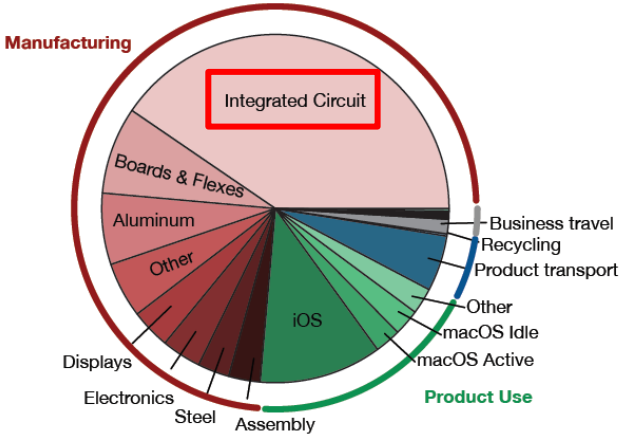
Main levers for change

Changes take time.
Need to accelerate on R&D of more sustainable solutions and their implementation in Fabs.

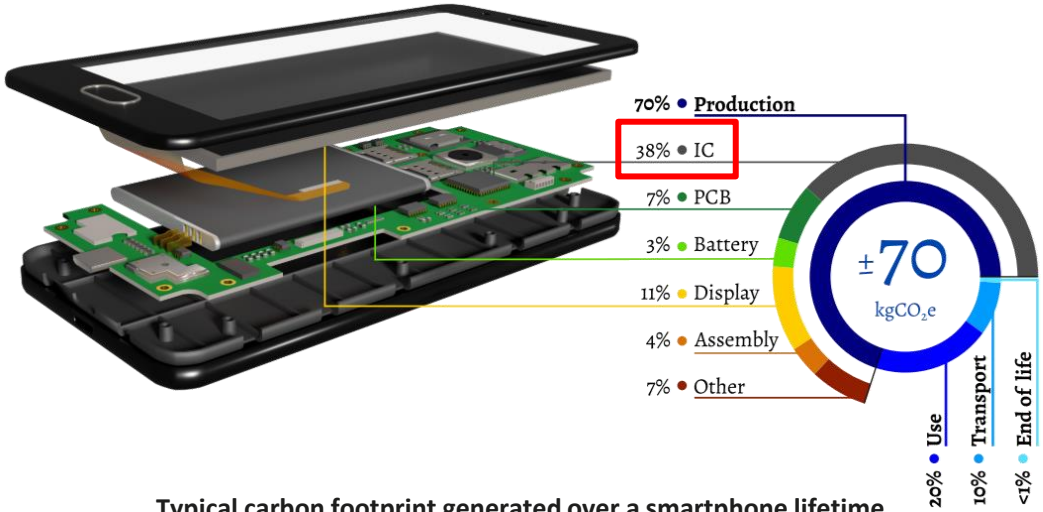


Our mission: Help the semiconductor industry achieve its targets in carbon footprint reduction

The climate impact of Consumer Electronics manufacturing



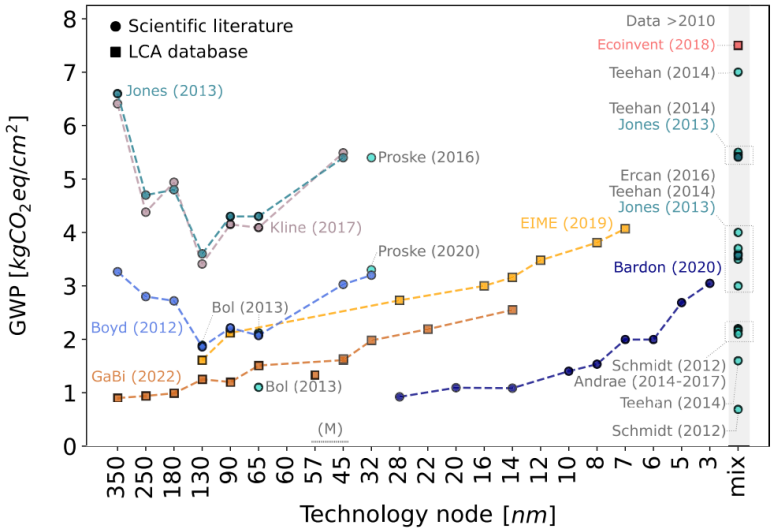
Apple's Carbon-Emission Breakdown
Source: Gupta et al., 2021 –The elusive environmental footprint of computing

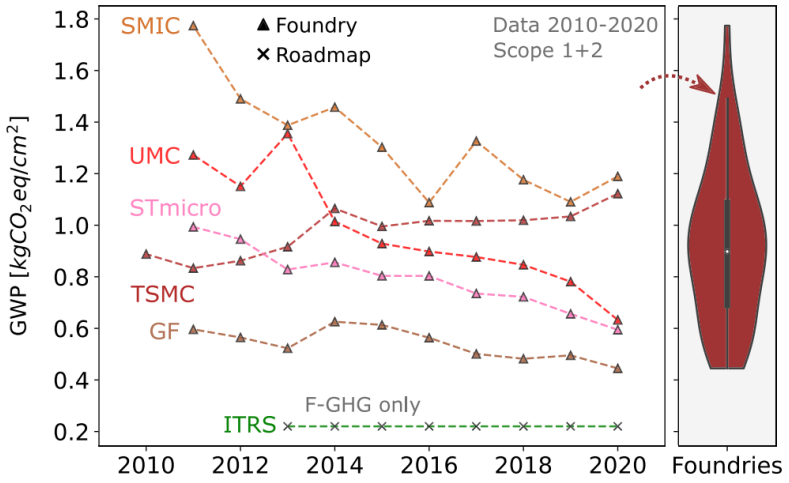


Typical carbon footprint generated over a smartphone lifetime
Source: Moreau et al., 2021 –Could Unsustainable Electronics Support Sustainability?

IC chip manufacturing accounts for the largest share of the climate impact, dominating over product use phase

Scattered data over IC chip manufacturing environmental impact





Literature and LCA database data:

- Variable Scope
- Variable sources (Primary vs. Secondary)
- Variable approaches (e.g. Bottom-up vs Top-down)
- Data gaps require “creative” plugging methods

Industry data from public CSR reports:

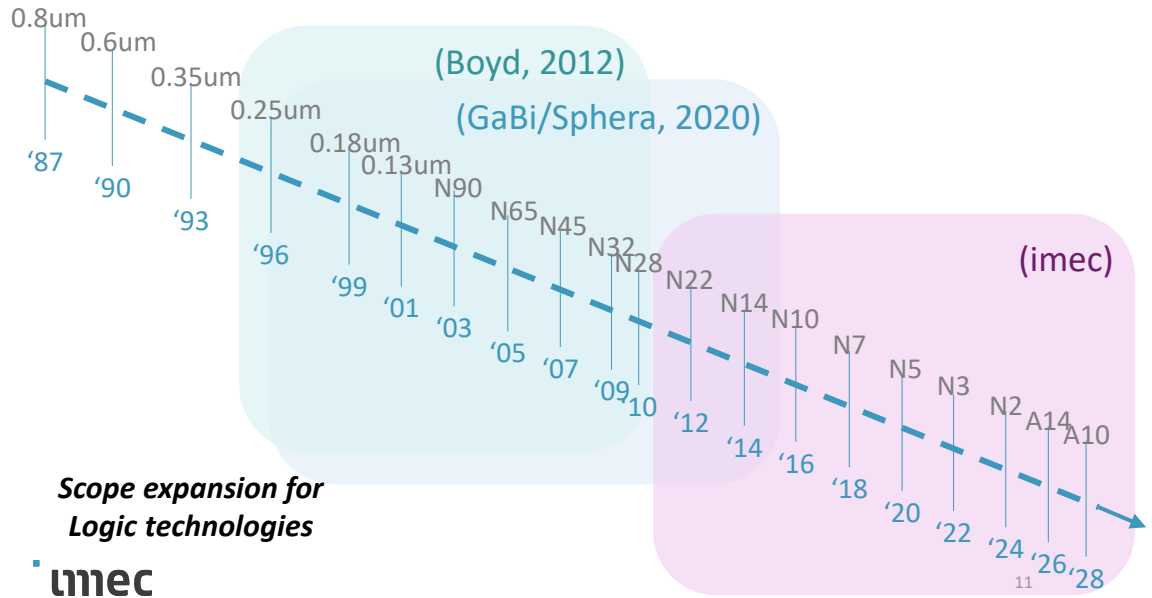
- Top-down, primary sourced data
- Aggregated over entire company operation, not “per chip” or “per-node”
- Limited scope
- Non-transparent methodology

Source: Pirson et al., 2023 – The Environmental Footprint of IC Production: Review, Analysis, and Lessons From Historical Trends

GWP: Global Warming Potential

Imec ambition for the SSTS Assess pillar

Close the data gap by providing **quality, transparent** data on environmental impact of IC chip fabrication in a **generic high volume manufacturing plant**



Scope expansion for Logic technologies

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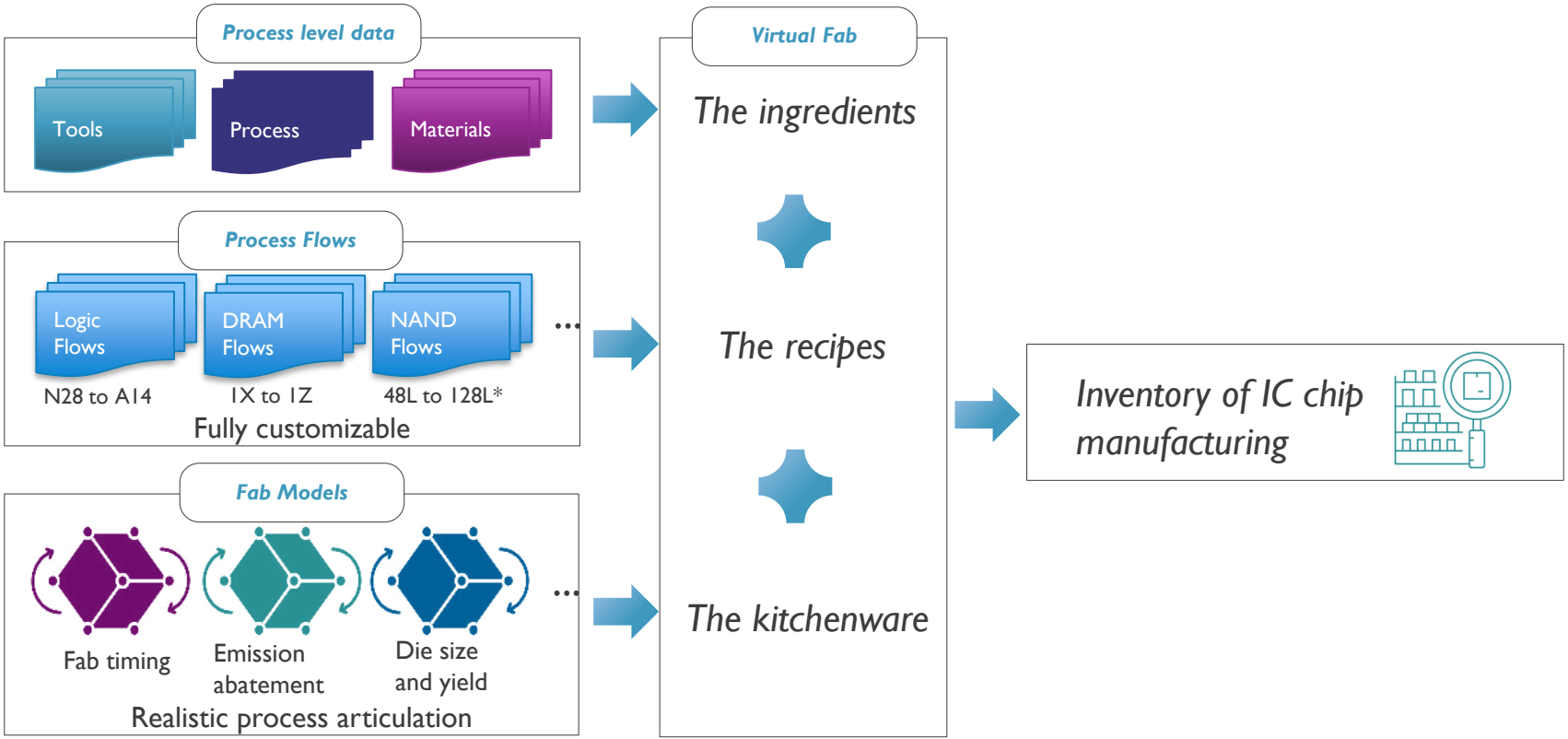
a *Virtual Fab* model for environmental impact assessment

Expand the analysis to:

- Identify **high impact** problems to focus Improve efforts
- Project **the future impact of IC chip manufacturing**

SSTS Assess - Virtual Fab Model

Quantify the footprint of a chip



SSTS Assess - Virtual Fab Model

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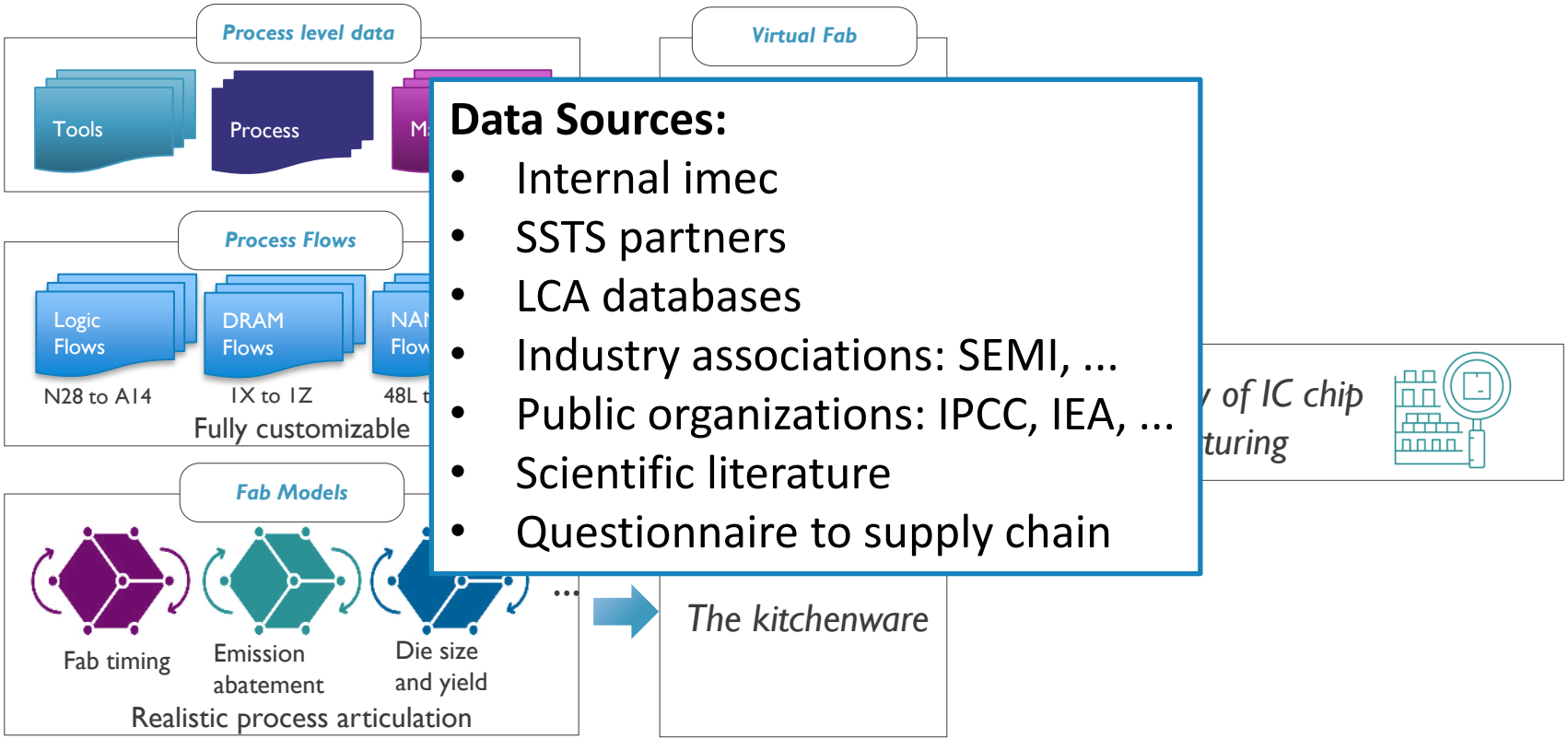
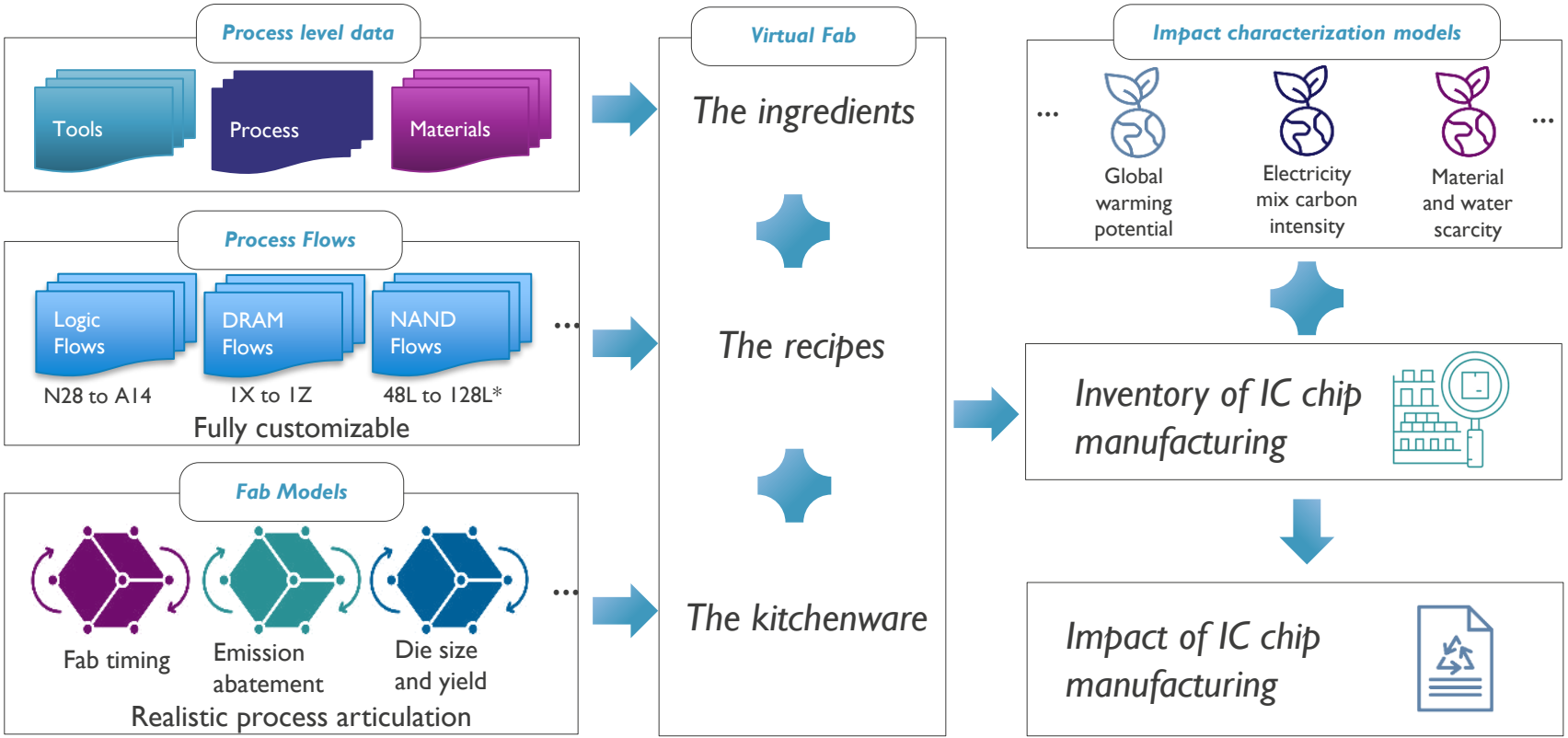


Data Sources:

- Internal imec
- SSTS partners
- LCA databases
- Industry associations: SEMI, ...
- Public organizations: IPCC, IEA, ...
- Scientific literature
- Questionnaire to supply chain

SSTS Assess - Virtual Fab Model

Quantify the footprint of a chip



SSTS Assess - Virtual Fab Model

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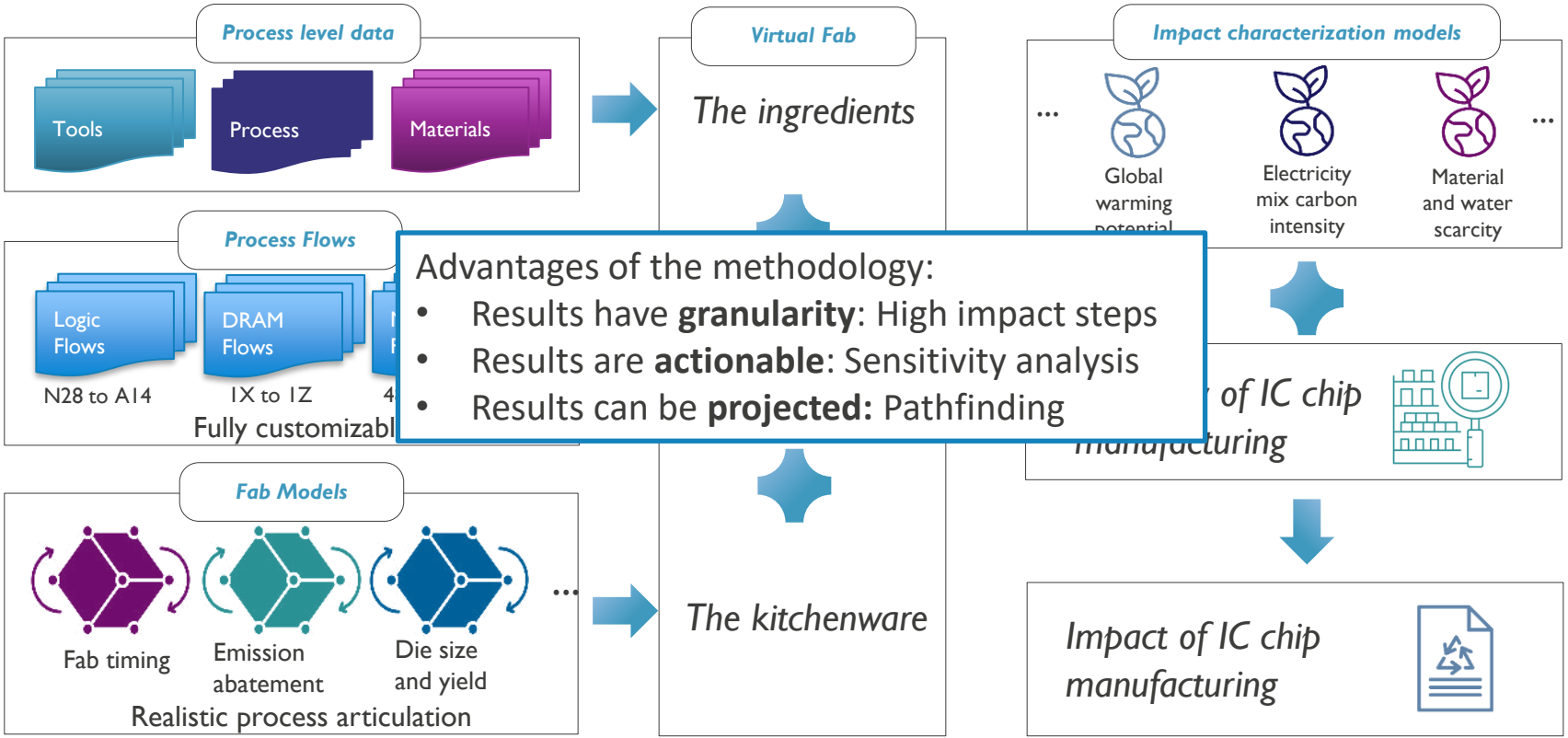


Advantages of the methodology:

- Results have **granularity**: High impact steps
- Results are **actionable**: Sensitivity analysis
- Results can be **projected:** Pathfinding

Bottom-up vs top-down approach in LCA

Top-down

Benefits:

- Representative of real fabs

Drawbacks:

- Scope 1 depends on declaration protocol
- Scope 3 estimates very difficult
- Highly aggregated data

Complementarity through benchmarking

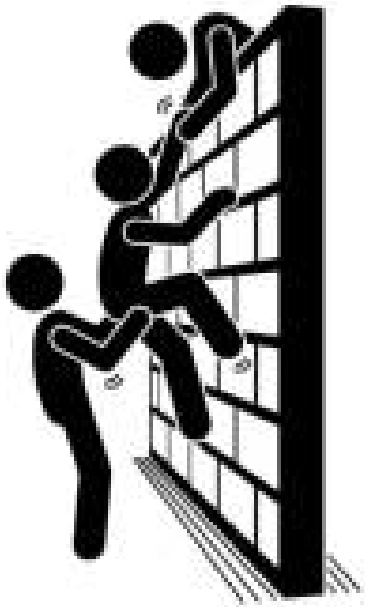
Bottom-up

Benefits:

- Results are Granular, Actionable and Projectable

Drawbacks:

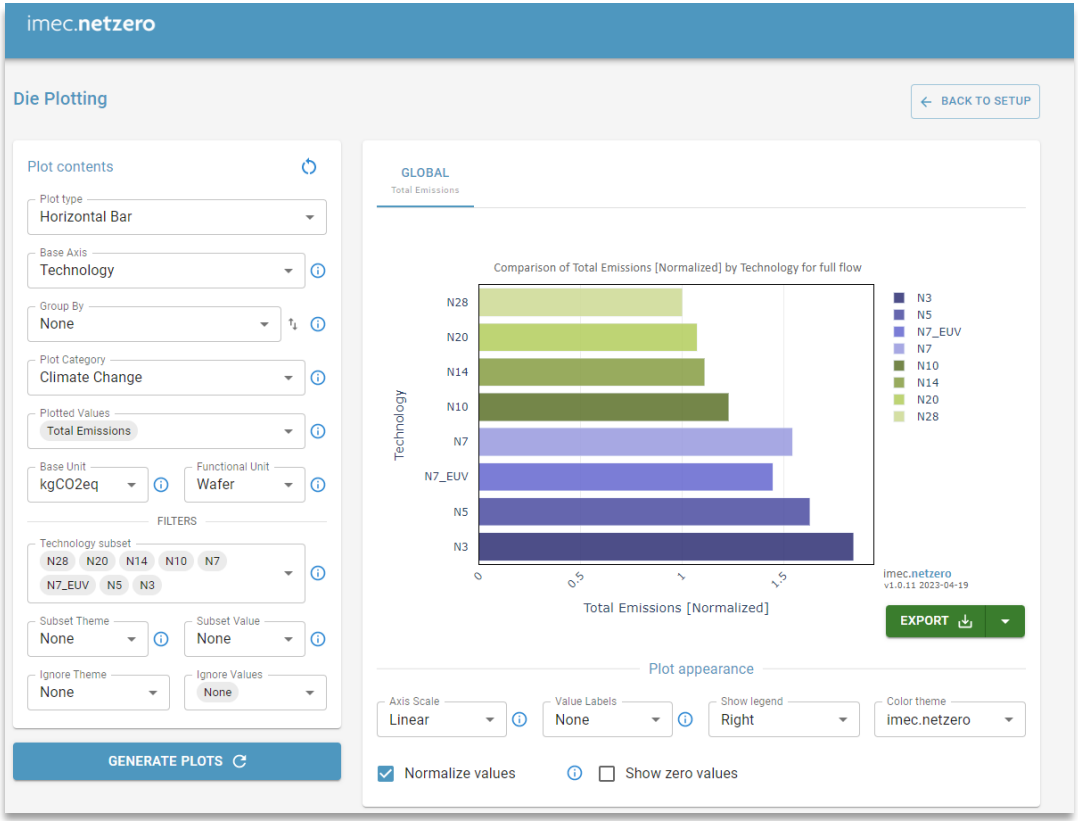
- Accounting never 100% complete
- Highly specialized expertise required



imec

imec.**netzero** Web Application

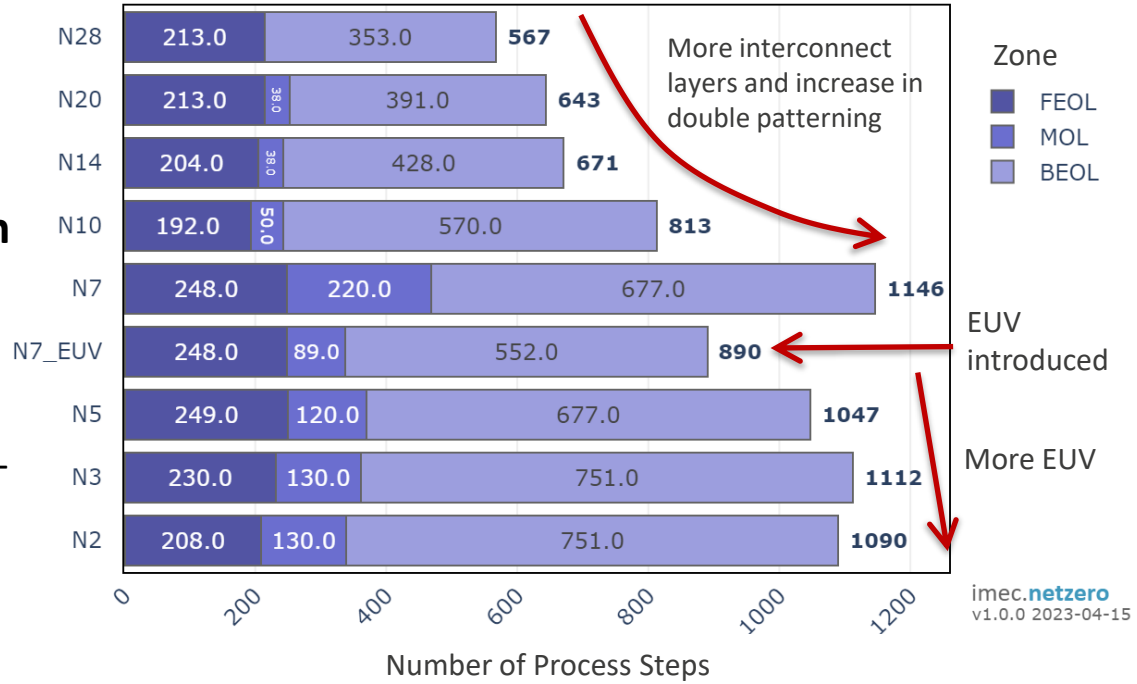
Public version release: June 30th 2023



Complexity Increase of a Mobile SoC

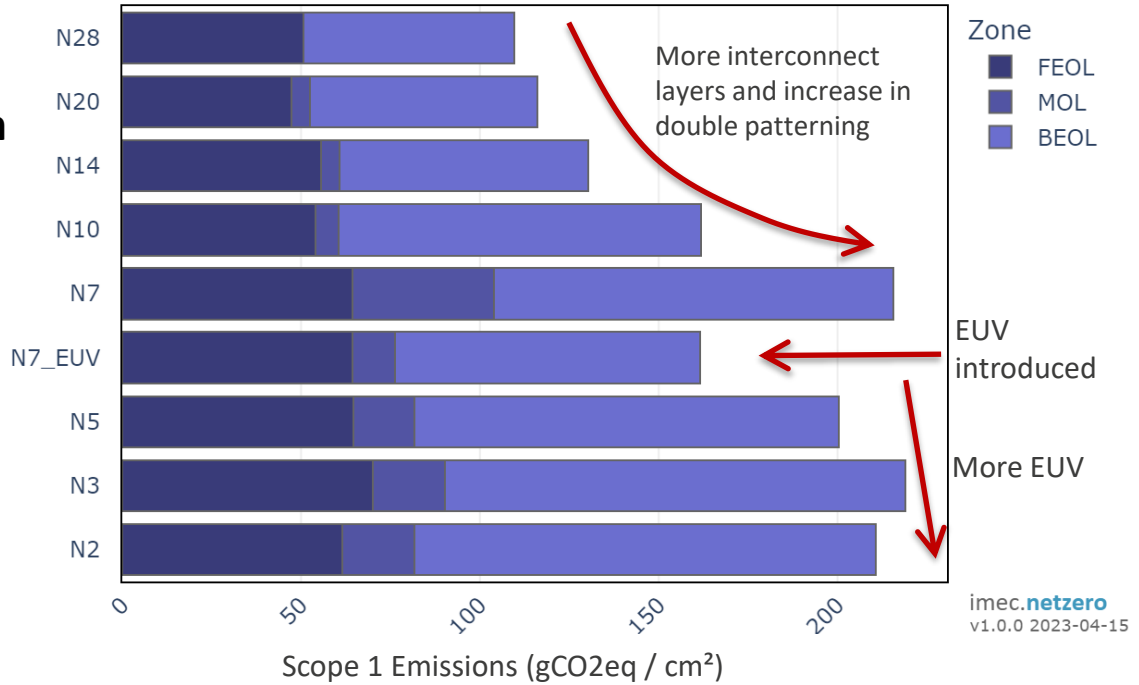
Number of process step evolution per node

- Increase in Complexity node to node where BEOL interconnects dominate
- Introduction of **EUV slows down the increase in complexity**:
  - Less multi-patterning DUV immersion steps
  - Less deposition, Dry-Etch, Wet-Clean, Metrology steps



Direct Emissions (Scope 1)

- Process gases are potent Greenhouse gases => **Deposition and Etch** contribute strongly to direct emissions
- Multi patterning use many repeats of deposition and etch ⇔ **By reducing complexity, EUV keeps direct emissions under check**

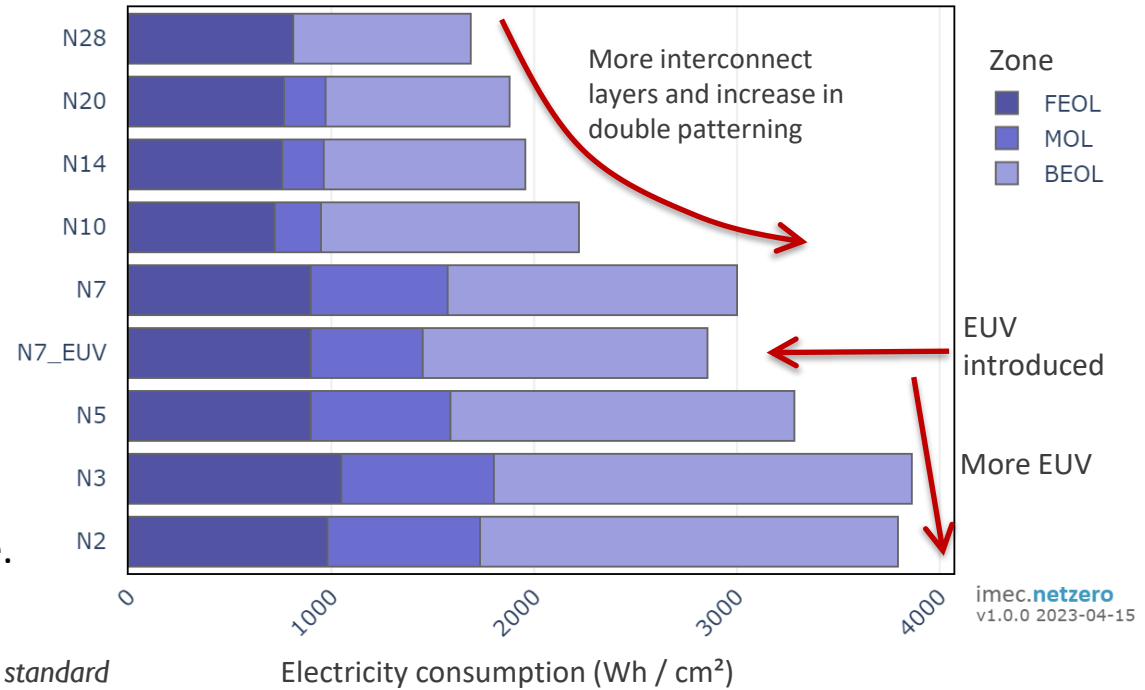


- *10x10mm² die, Murphy yield with 0,15 defect/cm²*
- *Tier 2C Abatement model (2019 Refinement to the 2006 IPCC Guidelines for National Greenhouse Gas Inventories)*
- *GHG global warming potential from IPCC AR6*

Electricity consumption

- Increase in process complexity directly leads to **increased electricity consumption**
- Introduction of EUV leads to:
  - **Reduce in process complexity**
  - **Increased electricity consumption** of the litho process area

These two effect counteract each other leading to a continued increase.



- *10x10mm² die, Murphy yield with 0,15 defect/cm²*
- *Utility electricity consumption modelled using SEMI S23 standard*
- *Tool Utilization assumed using SEMI S23 standard*

Carbon Emissions for Semiconductor Manufacturing are Increasing

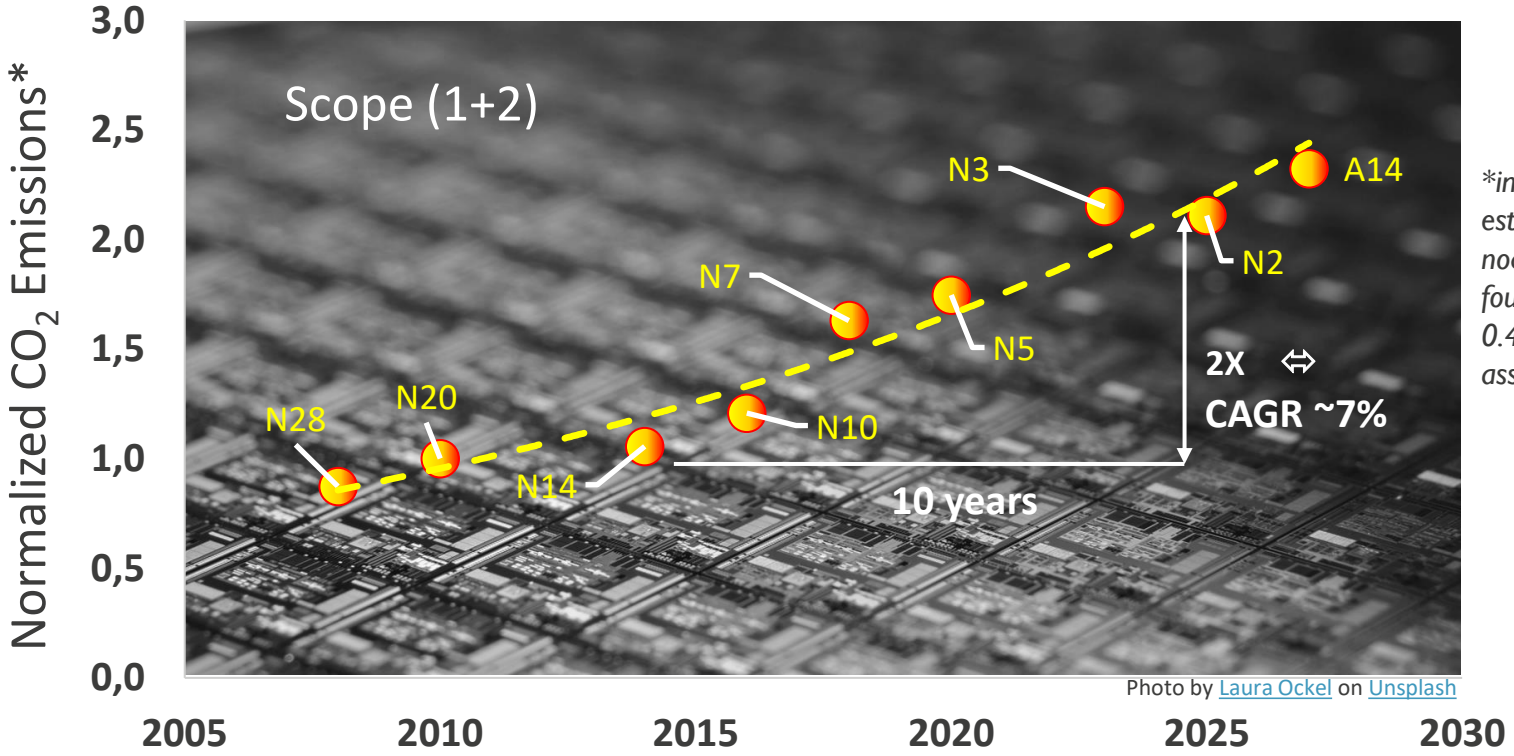
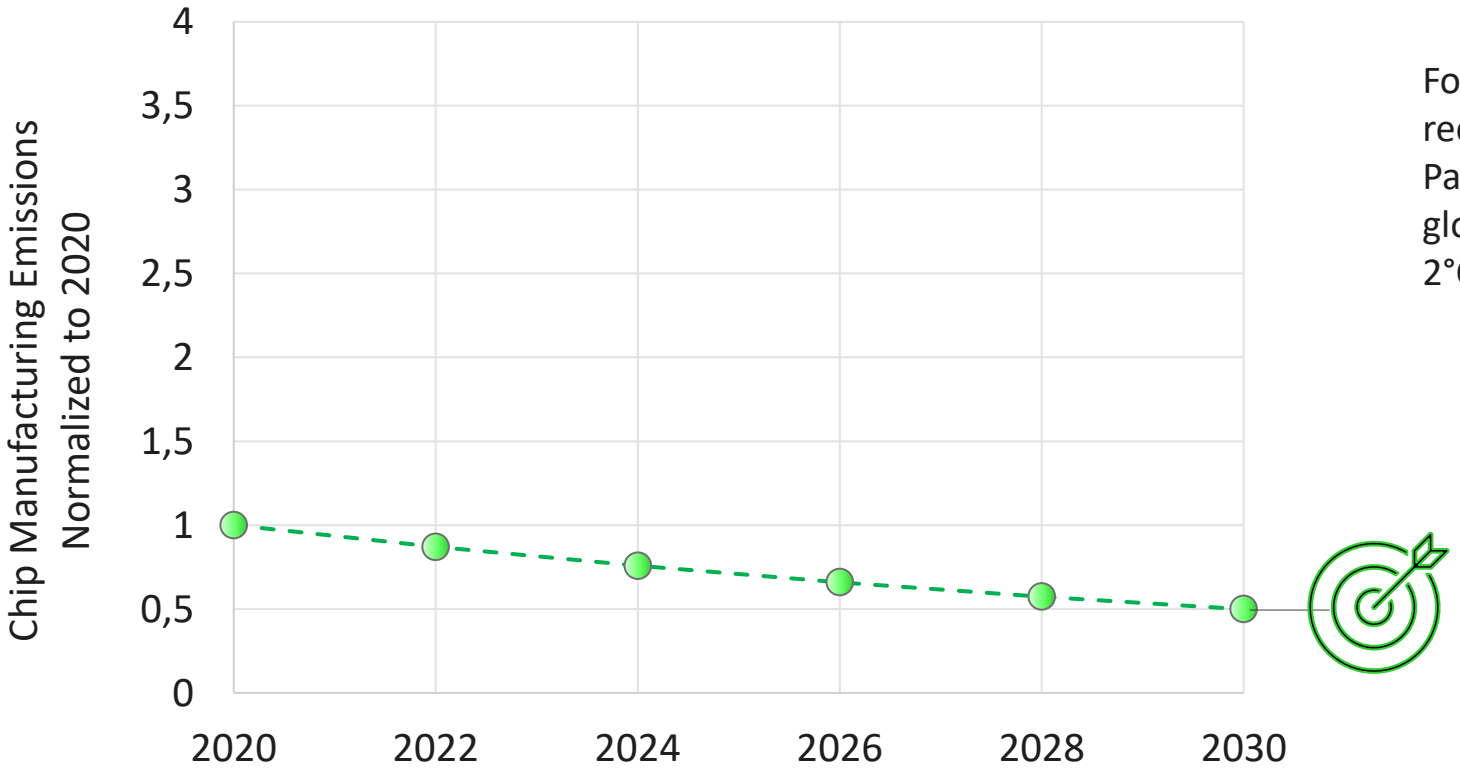


Photo by Laura Ockel on Unsplash

**imec.netzero: emissions estimate of imec process nodes representative of foundry nodes. 0.49kgCO_2eq/kWh assumption for electricity*

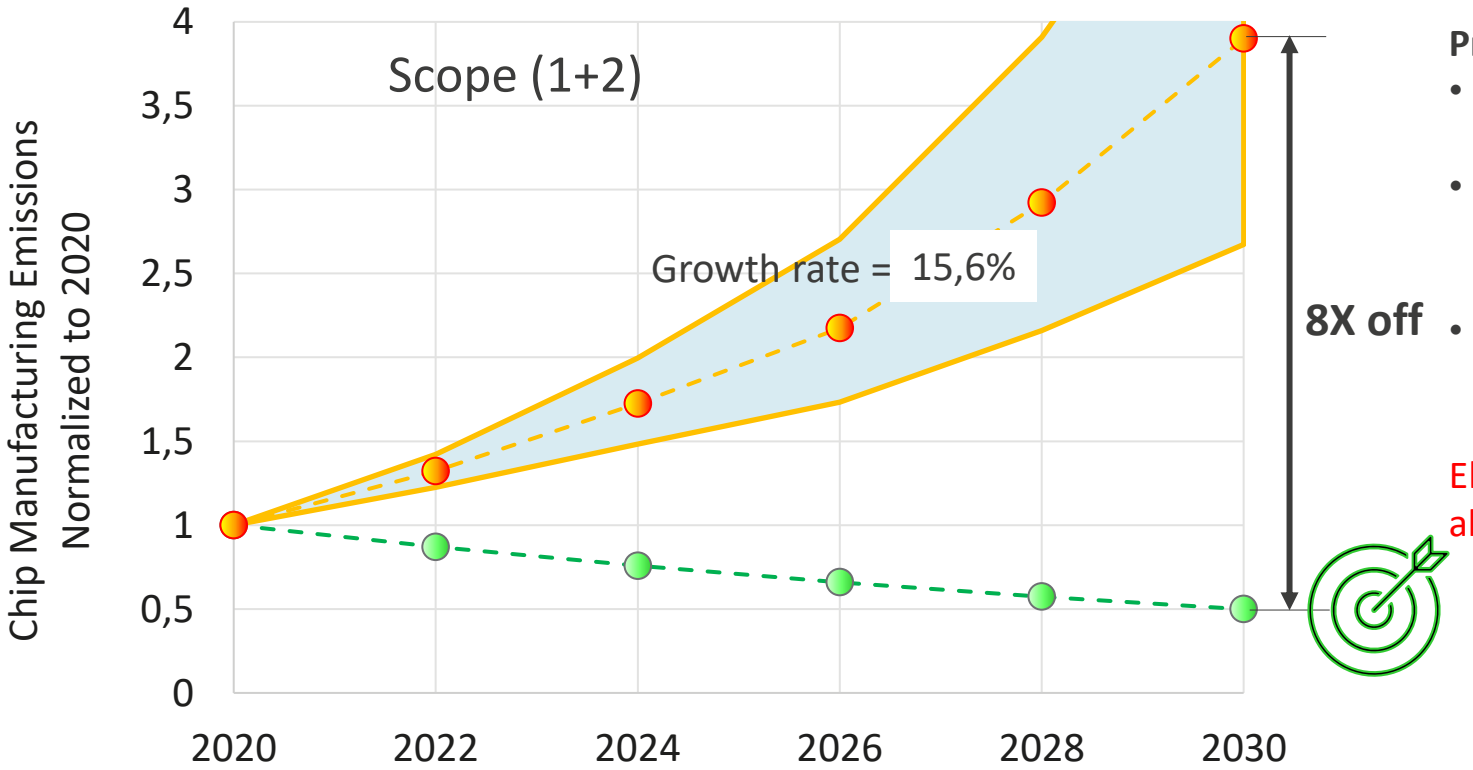
CAGR = Compound Annual Growth

Ideal climate impact scenario for Semiconductor Manufacturing



Following the path recommended by the Paris Agreement to keep global warming under 2°C

“Do Nothing” Scenario for Semiconductor Manufacturing



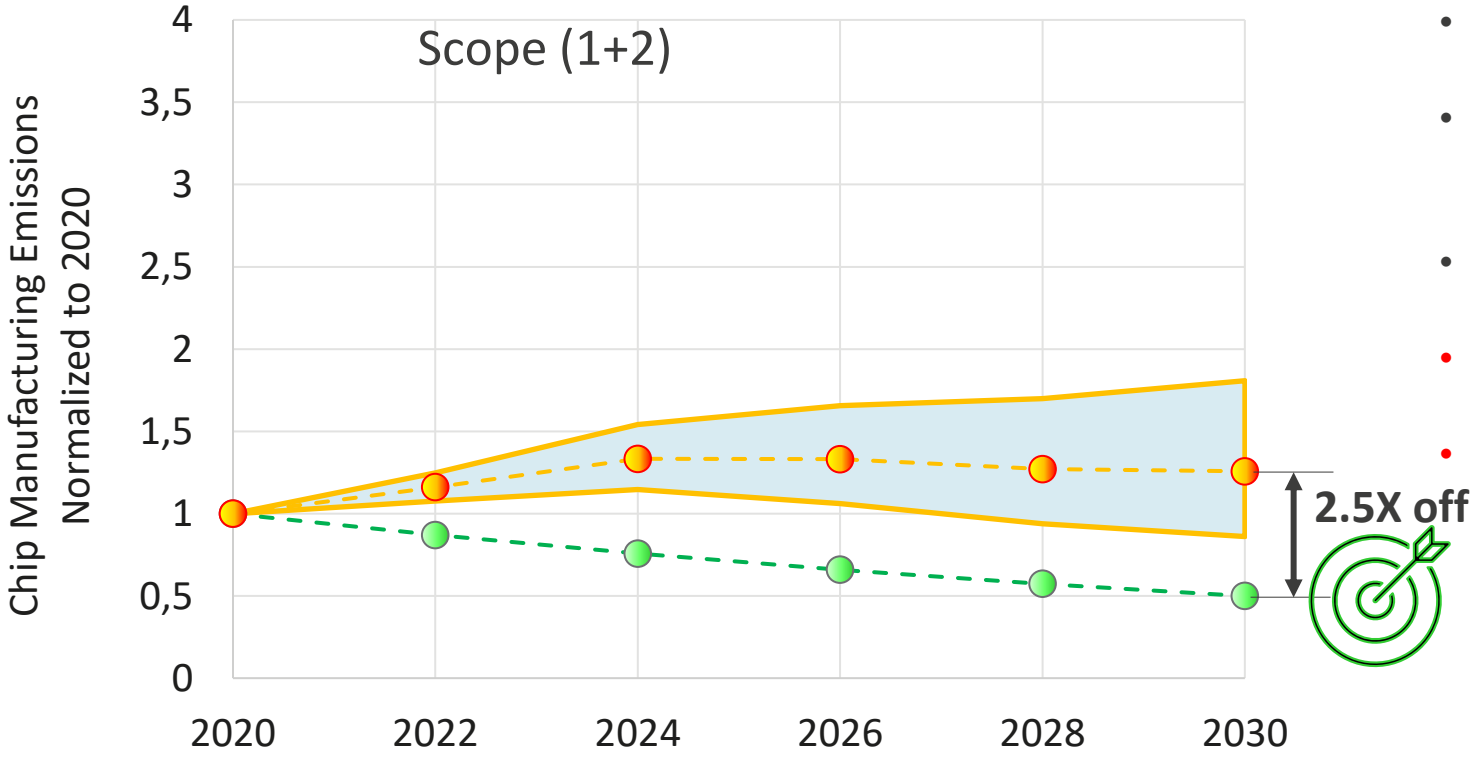
Projection includes:

- Evolution of technology mix
- Increase in technology complexity with CAGR ~7%
- ICT Market growth with CAGR 8% ± 4%

Electricity mix and abatement not evolving.

Constant electricity mix (0.49 kCO2eq/kWh), Tier 2C Abatement (2019 Refinement to the 2006 IPCC Guidelines for National Greenhouse Gas Inventories) and GHG global warming potential (IPCC AR6). Volume technology mix from IBS “Foundry Market Trends and Strategic Implications” Vol 30, N 12 , Dec 2021. Logic nodes only.

With Renewable Energy and State-of-the-Art GHG Abatement



Projection includes:

- Evolution of technology mix
- Increase in technology complexity with CAGR ~7%
- ICT Market growth with CAGR 8% ± 4%
- Renewable energy deployment
- State-of-art abatement from 2026 onwards

Adding to previous slide: Renewable Energy deployment according to IEA and abatement according to IPCC assumed for the years 2020-2024, State-of-the art Abatement from 2026.

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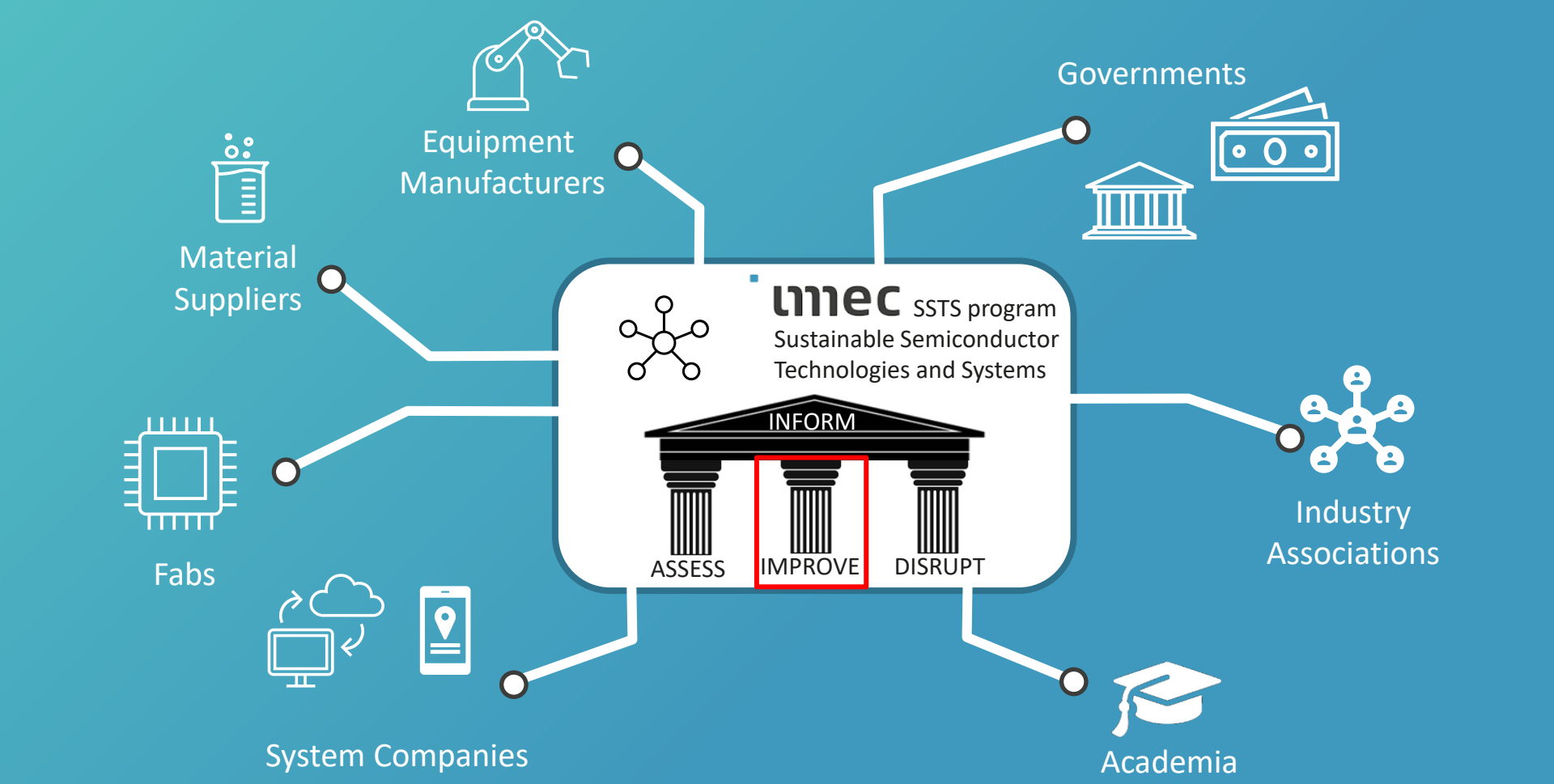

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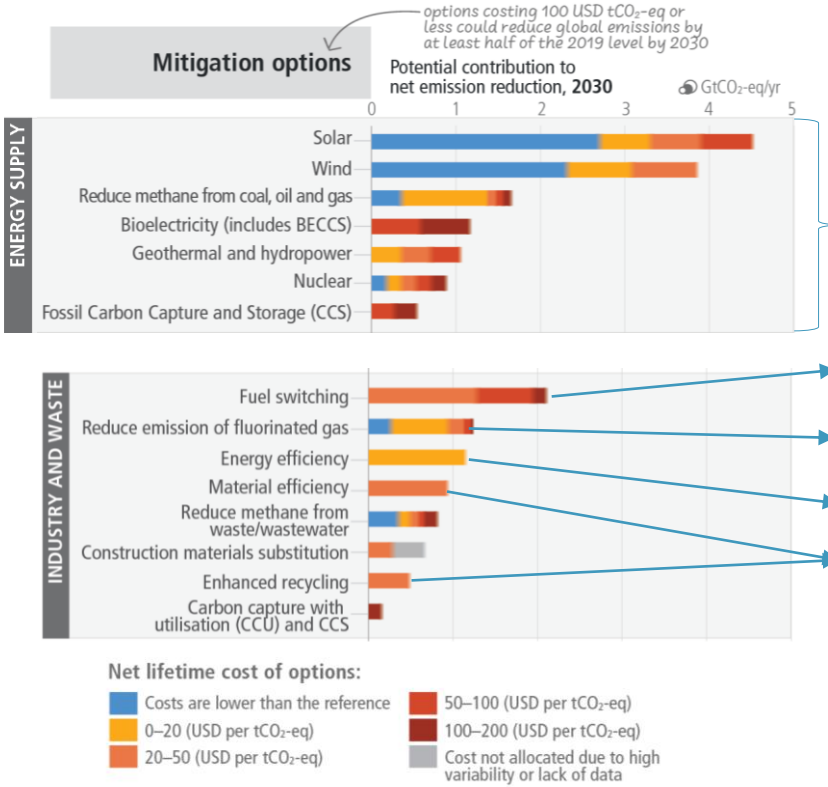


More renewable electricity !!!

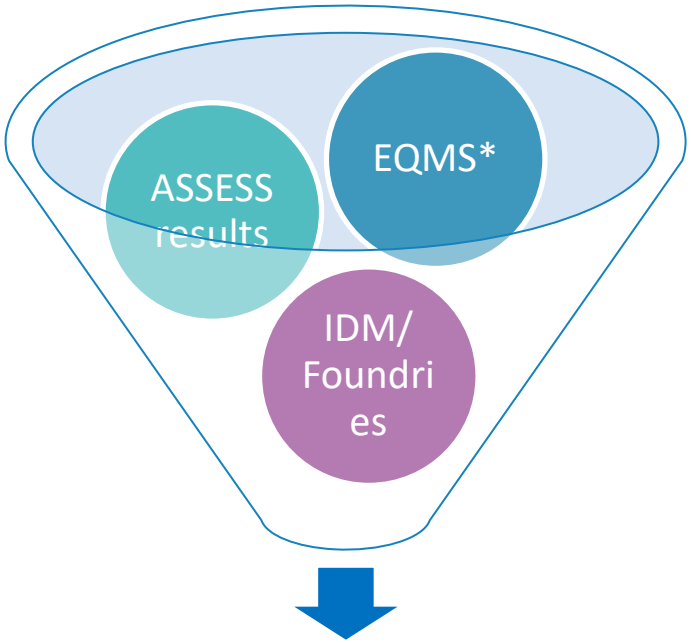
- Reduce natural gas consumption
- Replace / Reduce / Abate F-Gasses
- Energy efficiency & Industry 4.0
- Material circularity

Main levers for change = **IMPROVE Projects**

Changes take time.
Need to accelerate on R&D of more sustainable solutions and their implementation in Fabs.

SSTS – *Improve* projects

Focusing on **high-impact**



Defining high impact IMPROVE projects

- imec.**netzero** & ASSESS pillar offer in depth analysis for high impact problems.

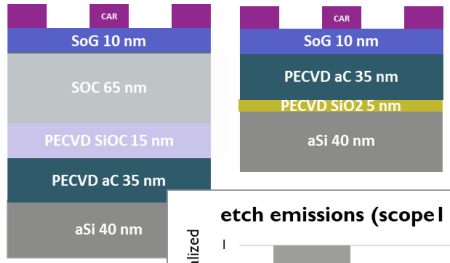
  Key topics for major improvements:
  - **Energy Efficiency**
  - **GHG emission reduction**
- SSTS & partners indicate also work needed in various supplies to the fab, in particular:
  - **Water Management**
  - **Material Circularity**

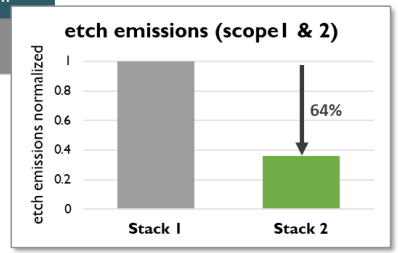
Without compromising continuous improvement of device performance.

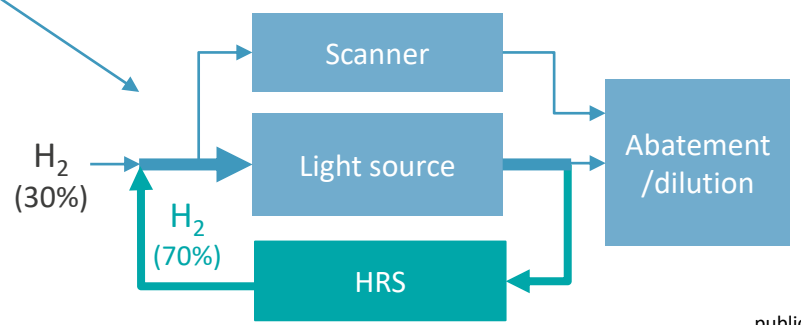
** EQMS = Equipment and Material Suppliers*

SSTS – Selection of *Improve* projects

Topic	Scope
Sustainable wet strip solution	Resource efficiency
GHG monitoring	GHG emission
Ge Recovery at epi tool	Material circularity
Reduction of emission with etch optimization	GHG emission
H2 recovery for EUV Scanner	Material circularity
Power consumption reduction for baking steps	Energy saving
Dose reduction on litho resist patterning	Energy saving





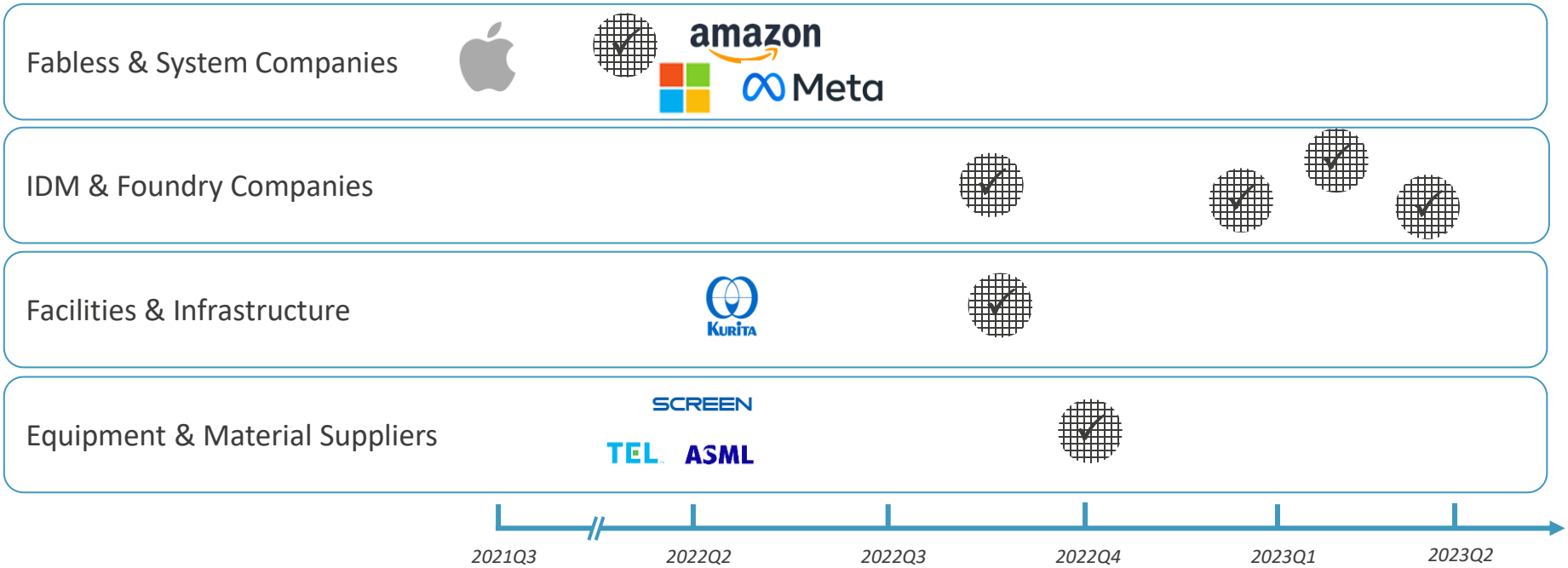


E. Gallagher et al. SPIE Litho & Patterning 2023

Conclusion

Imec building a strong program ecosystem for sustainability

SSTS partnerships



ICOS project: An opportunity to promote sustainability

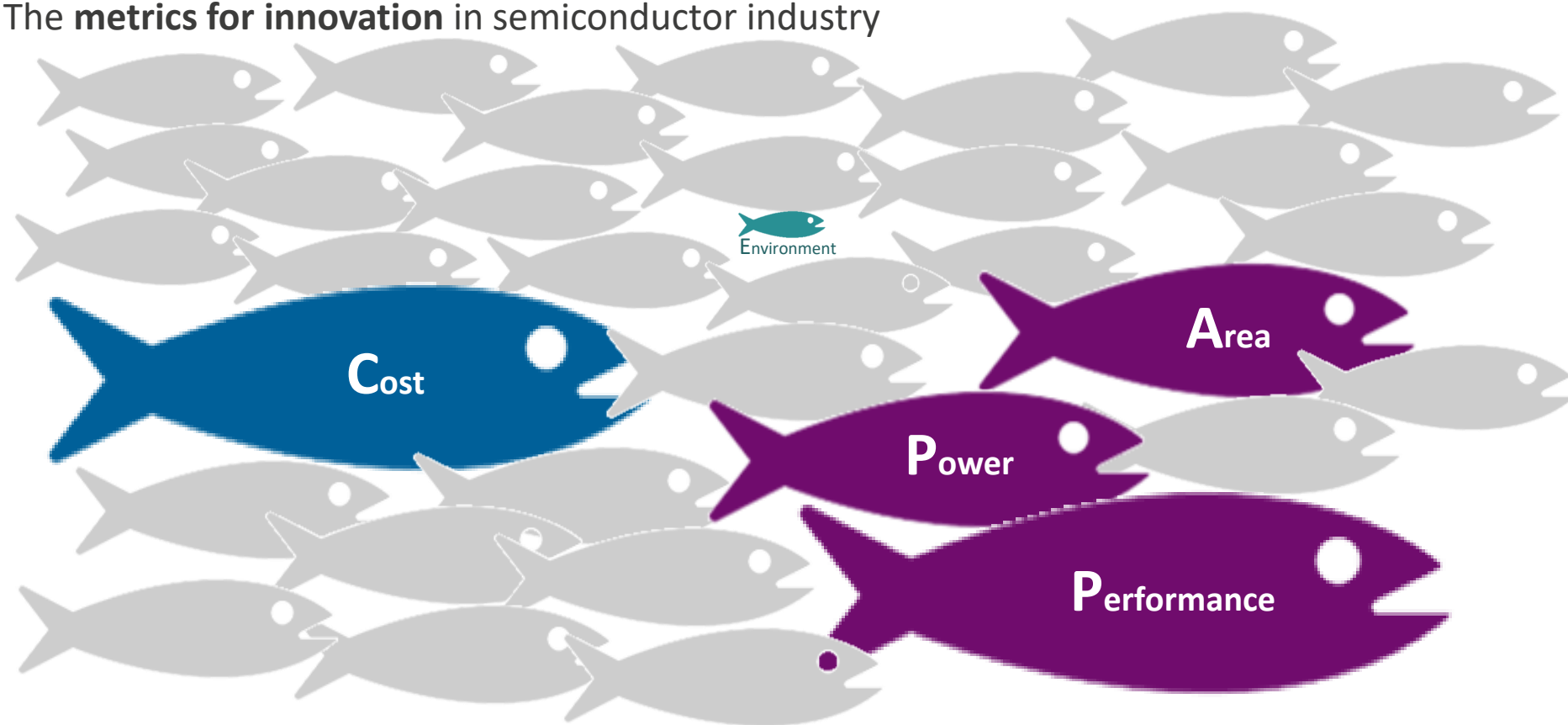
- Drive European semiconductor industry towards:
  - More **resilient supply chain**
  - More **robust products**
- Adopt **Life-Cycle Thinking** early in Innovation pipelines
- Drive R&D with **Environmental metrics** included in the scorecard:

  Power – Performance – Area – Cost - **Environment**

https://www.icos-cp.eu/
Research infrastructure for standardized GHG measurement throughout Europe

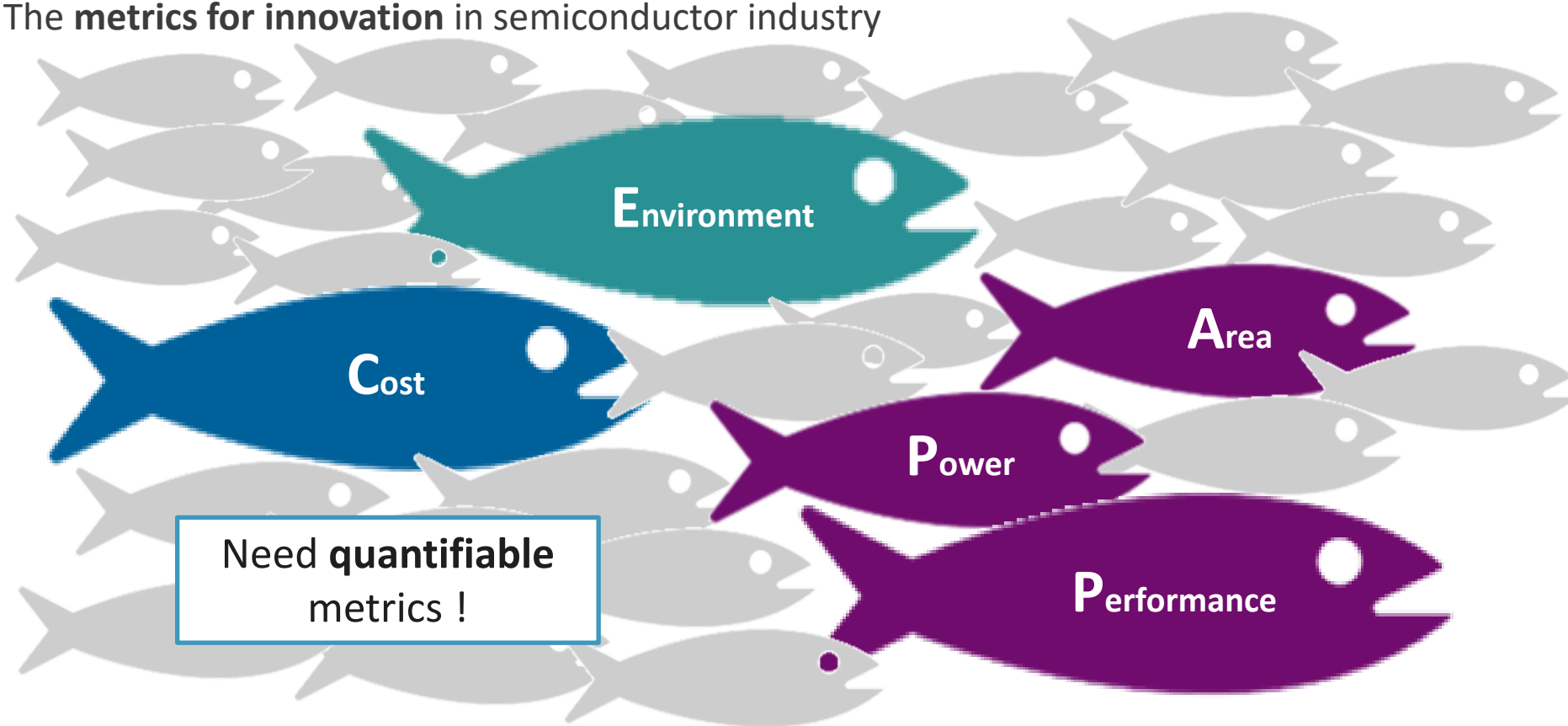
How can innovation drive to more sustainability ?

The **metrics for innovation** in semiconductor industry



How can innovation drive to more sustainability ?

The **metrics for innovation** in semiconductor industry



Acknowledgments

The SSTS team,
our partners and our supporters

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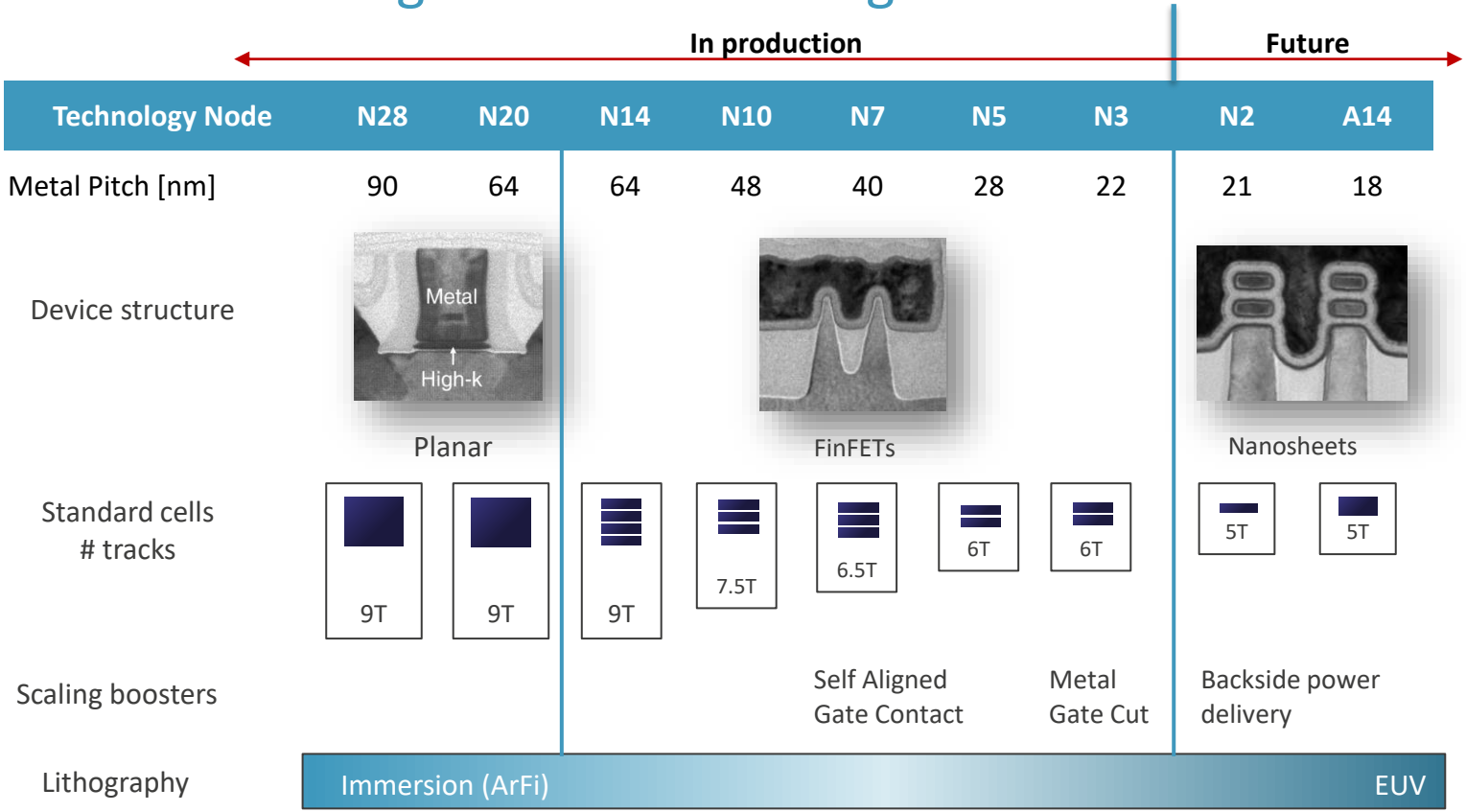
cedric.rolin@imec.be

embracing a better life

Appendix: Studied Logic CMOS technologies and nodes



Nodes based on imec process flow are generic but representative of foundry nodes.