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Can we cope with the massive production of integrated circuits (ICs) within environmental limits ?

Thibault Pirson, Jean-Pierre Raskin, and David Bol

UCLouvain, ICTEAM institute

thibault.pirson@uclouvain.be









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Integrated circuits (ICs) are the **building blocks** of ICTs supporting digital products and services.



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ICs represent a high share of the production impacts in existing LCA



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Source : [Malmodin, 2018; Belkhir, 2018; GreenIT, 2019, GeSI, 2020]

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Huge challenge:

very few trials to get it right and short period of time (<30 years)

→ today's actions are critical



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ICOS S Chip manufacturing and 1.5°C trajectory



Implementing all known decarbonization measures will not get the semiconductor industry on a 1.5°C trajectory by 2030.





¹Public announcement of 20 key players; assume base year 2020 if not specified. ²Install gas-abatement system (90% destruction efficiency) on 90% of tools with greenhouse-gas emission is NF3, 50% is CF4 (average of industry reports), 374 place 70% HTF with low GWP alternative; reduce chiller leakage by 30%. ³Replace 80% fuel supply in EU and US with hydrogen/biomass. ⁴Reduce energy consumption per wafer by 10% from 2020 level. ⁴Renewable energy adoption: Europe, 56%; US, 46%; Malaysia, 100%; Taiwan, 15%; China 42% (Asia average); Japan, 100%; South Korea, 60%; Singapore, 15%; rest of world, 53% (industry average 2020). ³The 2030 goal of 54 million tons of CO₂e is based on a cross-sector pathway calculation method offered by Science Based Targets initiative (SBTI): it assumes emissions reduction at a linear annual rate of 4.2% from 2020 base year; the long-term goal, which is based on the International Energy Agency's Net-Zero Emissions scenario, requires energy and industrial-process CO₂emissions to fall 95% between 2020–50, resulting in emissions of 4.7 million tons CO₂e. Source: CDP Worldwide reports; expert interviews; SBTI guidelines; SENI World Fab Forecast; McKinsey wafer capacity mode; McKinsey analysis

McKinsey & Company



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Source : [imec, 2022; McKinsey&Company, 2022] 6



Insights from the academia ...





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Source : [Roussilhe, 2022; Wang, 2023]

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- Represent a sage operating space for Humanity
- 3 boundaries are FULLY exceeded in the high-risk zone
- 2 boundaries are in the increasingrisk zone: **climate change** and land change (deforestation)



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Can we **cope** with the **massive production** of integrated circuits (ICs) within environmental limits?

- 1. Clear conflicting trends are already identified for GHG emissions (Paris Agreement)
- 2. The minimization of the environmental impacts per cm² will not be sufficient
- 3. Roadmaps currently fail in defining environmental targets
- 4. Issue with the choice of environmental efficiency metrics
- 5. The EU Chips Act adds difficulty for reaching the climate targets at the EU scale





Outline

• Context

- The Impact of Pursuing Advanced Scaling for Foundries
- The Issue with Environmental Targets in Industrial Roadmaps
- Environmental perspectives for the European Chips Act
- Take-aways
- Suggestions





Our previous work on ...

... the environmental footprint of IC production $TOD\Delta$

IEEE TRANSACTIONS ON SEMICONDUCTOR MANUFACTURING, VOL. 36, NO. 1, FEBRUARY 2023

The Environmental Footprint of IC Production: Review, Analysis, and Lessons From Historical Trends

Thibault Pirson[©], *Graduate Student Member, IEEE*, Thibault P. Delhaye[®], Alex G. Pip, Grégoire Le Brun, Jean-Pierre Raskin[®], *Fellow, IEEE*, and David Bol[®], *Senior Member, IEEE*



Embedded Tutorial Paper

Moore's Law and ICT Innovation in the Anthropocene

David Bol, Thibault Pirson and Rémi Dekimpe Electronic Circuits and Systems group, ICTEAM Institute Université catholique de Louvain, Louvain-Ia-Neuve, Belgium david.bol@uclouvain.be

From Silicon Shield to Carbon Lock-in? The Environmental Footprint of Electronic Components Manufacturing in Taiwan (2015-2020)

Gauthier Roussilhe[‡], Thibault Pirson[†], Mathieu Xhonneux[†], David Bol[†] [†]*RMIT*, Royal Melbourne Institute of Technology, Australia [†]*ICTEAM*, Université catholique de Louvain, Belgium Email: gauthierroussilhe@protonmail.com



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... the environmental footprint of IoT and 5G







Assessing the embodied carbon footprint of IoT edge devices with a bottom-up life-cycle approach Thibault Pirson *, David Bol Université cabaligue de Lourain, ICTEAMLECS, Lourain le Neure, Régium

Technical and Ecological Limits of 2.45-GHz Wireless Power Transfer for Battery-Less Sensors

Marco Gonzalez, Student Member, IEEE, Pengcheng Xu, Member, IEEE, Rémi Dekimpe, Student Member, IEEE, Maxime Schramme, Student Member, IEEE, Ivan Stupia, Member, IEEE, Thibault Pirson, and David Bol, Senior Member, IEEE



Annals of Telecommunications

https://doi.org/10.1007/s12243-022-00932-9

Check for updates



Evaluation and projection of 4G and 5G RAN energy footprints: the case of Belgium for 2020–2025

Louis Golard¹ 💿 • Jérôme Louveaux¹ • David Bol¹

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Pol Maistriaux, Thibault Pirson, Maxime Schramme, Jérôme Louveaux and David Bol ICTEAM, UCLouvain, Belgium {pol.maistriaux,thibault.pirson,maxime.schramme,jerome.louveaux,david.bol}@uclouvain.be



The Impact of Pursuing Advanced Scaling for Foundries



The environmental footprint of IC production

	56 T Thiba	The Environmental Footprint of IC Pro- Review, Analysis, and Lessons Fro Historical Trends ault Pirson [©] , <i>Graduate Student Member, IEEE</i> , Thibault P. Delhaye [®] , Alex G. Pip, Jean-Pierre Raskin [®] , <i>Fellow, IEEE</i> , and David Bol [®] , <i>Senior Member, II</i>	duction: Dm Grégoire Le Brun, ZEE
	$\begin{array}{llllllllllllllllllllllllllllllllllll$	$\begin{array}{ll} \text{In-depth analysis} & \rightarrow \\ (\text{Section III}) & \end{array}$	Historical trends (Section IV)
Goals Methodology (Section II) Outputs	 (1) Identify key sources (2) Identify LCA data (1) Review 4 literature categories[⊲] (2) Focus on 3 indicators[▷] (1-2) 27 key sources identified[◊] (+ 9 historical sources) 	 (1) Identify the scope of the sources[†] (2) Identify variation in LCA data^{†,*} (1) Define 10 objective features[†] (2) Normalize impacts per area[*] (1) Scope mismatch identified[†] (2) Environmental impacts per area[*] 	 (1) Put results in a long-term perspective^{†,*} (2) Foster systemic thinking (1) Define 10 objective features[†] (2) Normalize impacts per area[*] (1) Lack of roadmaps and environmental targets^{†,*} (2) Limits of environmental improvements per area[*]

† : qualitative \star : quantitative \triangleright : energy consumption, carbon footprint and water consumption \diamond : 27 = 5+1+18+3, see Table III for more details \triangleleft : foundry reports, industry roadmaps, scientific literature, and commercial state-of-the-art LCA databases

Focus on **3 environmental indicators**: energy, **GWP (this talk)**, water All metrics are **normalized** by silicon area (cm²)





The environmental footprint of IC production







The Impact of Pursuing Advanced Scaling for Foundries



 The impacts per area either (slightly) decrease over the period 2010-2020 for most of the foundries, while they increase for TSMC

This is not due to a lack of effort from the foundry to pursue efficiency but rather to the introduction of more demanding processes such as extreme ultraviolet (EUV) lithography for scaling purpose



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Historical trends





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Rebound effect



- □ The average die area is roughly constant for Apple's A-processors although technology node shifted from 45 to 5 nm → ever increasing functionality
- □ The total silicon area produced over time keeps increasing, faster than the reduction in environmental impacts per area → rebound effect





Conflicting trends







About -1%/year ... (if 2015-1995=20 years)



■ Rebound effect are observed at the hardware level
 → The minimization of the environmental impacts per cm²
 will not be sufficient

→ Clear conflicting trends between massive production of ICs and GHG reduction pathways (Paris Agreement)



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The Issue with Environmental Targets in Industrial Roadmaps



Long-term analysis of ITRS roadmaps

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS 2001 Edition

ENVIRONMENT, SAFETY, AND HEALTH

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS 2003 Edition

ENVIRONMENT, SAFETY, AND HEALTH

THE ITRS IS DEVISED AND INTENDED FOR TECHNOLOGY ASSESSMENT ONLY AND IS WITHOUT REGARD TO ANY COMMERCIAL CONSIDERATIONS PERTAINING TO INDIVIDUAL PRODUCTS OR EQUIPMENT. INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

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ENVIRONMENT, SAFETY, AND HEALTH

THE ITRS IS DEVISED AND INTENDED FOR TECHNOLOGY ASSESSMENT ONLY AND IS WITHOUT REGARD TO AN COMMERCIAL CONSIDERATIONS PERTAINING TO INDIVIDUAL PRODUCTS OR EQUIPMENT.



Table ESH5 Facilities Technology Requirements



IMPORTANT:

- No target for GHG emissions/cm² (only for F-GHG)
- 2. No quantitative data after 2015



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Environmental targets are at best reaching the targets from the ESH 2001 roadmap

(in the meantime, more transistors are fitted on a given square cm.

Yet, the total area produced keeps on increasing)

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Need for a fundamental reset

INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS

EXECUTIVE SUMMARY

THE IRDST^M IS DEVISED AND INTENDED FOR TECHNOLOGY ASSESSMENT ONLY AND IS WITHOUT REGARD TO ANY COMMERCIAL CONSIDERATIONS PERTAINING TO INDIVIDUAL PRODUCTS OR EQUIPMENT.

THE INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS: 2022 COPYRIGHT © 2022 IEEE. ALL RIGHTS RESERVED 40 Roadmap Process and Structure

The IRDS International Focus Team on More than Moore, as listed in the acknowledgments section has generated the content of this chapter. Extensive use has been made of the NEREID NanoElectronics Roadmap for Europe.⁴

2.2.12. Environment, SAFETY, HEALTH AND SUSTAINABILITY (ESH/S)

The Environmental, Safety, Health, and Sustainability (ESH/S) chapter was not updated for 2021 IRDS given the many changes that have occurred within the industry and externally, which require a fundamental reset in how ESH/S emerging challenges are addressed from a technology roadmap perspective. However, a white paper will be published in the 2022 IRDS as a result of reenergizing the IFT effort. To effectively define critical issues and gaps, a broader approach to comprehend the overarching risks, upstream from the supply chain, within the semicondum manufacturers and downstream to key customers in microelectronics will require a systems integration approach to ensure state of a linkage and alignment with key stakeholders.

2021 & 2022 IRDS executive summary:

"the ESH chapter has not been updated for 2021 IRDS given the many changes that have occurred within the industry and externally, **which require a fundamental reset** in how ESH/S emerging challenges are addressed from a technology roadmap perspective."

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- Systematic relaxation of the environmental targets (aposteriori)
- Lack a standardization across the ITRS/IRDS roadmaps

 → Roadmaps currently fail in defining environmental targets as manufacturing processes become more and more complex for advanced technologies.

Environmental perspectives for the European Chips Act

The European Chips Act

Green deal

- "No net emissions of greenhouse gases by 2050,
- economic growth decoupled from resource use,
- no person and no place left behind."

Green growth

Is "green growth" possible?

- Green growth = the absolute decoupling of GDP growth from the ecological footprint
- Can only be studied at the global world scale because of [Parrique, 2019]:
 - rebound effects,
 - problem & cost shifting issues.

- Absolute decoupling has never been observed so far at global scale [Jackson, 2009][Parrique, 2019][Hyckel and Kallis, 2020]
- Betting on green growth for carbon neutrality is a risky strategy

Cost shifting issue

* * * * * * * * * *

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Citizen protest

WORKSHOP - Sustainable Electronics & International Cooperation On Semiconductors T. Pirson, **UCLouvain**

Environmental concerns ...

Europe Technology Policy Committee

COMMENTS OF THE ACM EUROPE TECHNOLOGY POLICY COMMITTEE ON THE PROPOSAL FOR A REGULATION ESTABLISHING A FRAMEWORK OF MEASURES FOR STRENGTHENING EUROPE'S SEMICONDUCTOR ECOSYSTEM

9 May 2022

Capsule Conclusion

Europe TPC supports the Commission's intention to promote European digital sovereignty, but also see its Proposal for a Regulation Establishing a Framework of Measures for Strengthening Europe's Semiconductor Ecosystem as an important opportunity to improve the sustainability of semiconductor technologies and applications. With this goal in mind, we raise a number of environmental considerations that would need to be accounted for, noting that at present the Chips Act fails to address the substantial probability that it will produce "rebound" effects potentially significant enough to wholly negate efficiency savings or even induce net energy and emissions increases (aka "backfire"). The Framework should thus be amended to expressly identify, quantify, and mitigate such impacts, with a view to aligning semiconductor innovation with the technological and environmental objectives of the Green Deal.

Prospective GHG emissions for EU chips

Assumptions:

- In 2020: 10% of 100 MtCO2e (SEMI data) with 1.5× uncertainty
- Global market: CAGR +8% +/-4%
- Complexity: CAGR +5% +/-2%
- Fixed abatement schemes
- Carbon intensity of electricity mix: CAGR -2%/year
- Chip production: 5-33% of the total EU carbon budget !

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- The European Chips Act targets the supply chain sovereignty (increase resilience) ...
- ... at the cost of 3-10× higher GHG emissions for the EU semiconductor fabrication sector (BaU scenario targeting 20% market share in 2030)
- \rightarrow At the EU scale: one more difficulty for reaching the climate targets

Let's focus on the world scale ...

Substitution

Replacing existing products EU Chips Act = opportunity for climate (depends on electricity mix)

Deploying new products EU Chips Act = threat for climate

What would be the additional chip production capacity fostered by the European Chips Act for ?

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Current initiatives (megafabs only)

Company	Location	Market	Tech. node
Intel	Magdeburg, DE	?	7-5nm
TSMC	Dresden, DE	?	28/22nm ?
ST & GF	Crolles, FR	Automotive & 6G	22-18nm
European Chips Act plan		Automotive, 6G, Quantum, Al	12/10nm + 3/2nm ?

Substitution or accumulation ?

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• At the world scale, two options:

- opportunity: replacement of carbon-intensive capacity somewhere else in the world (substitution)
- threat: additional capacity for new markets (accumulation)
- At the EU scale, one more difficulty for reaching the climate targets

Take-aways

Can we **cope** with the **massive production** of integrated circuits (ICs) within environmental limits?

- 1. Clear conflicting trends are already identified for GHG emissions (Paris Agreement)
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Suggestions

- ➤ Develop a clear and transparent methodology for reporting environmental targets → insights and suggestions provided in [Pirson, 2022] and [Roussilhe, 2022]
- Foster coherency between CSR reports and ITRS roadmaps terminology
- > Evolution of relative efficiency metrics through time should be (better) monitored and reported
- Carbon tuneling should be (systematically) avoided (already partially the case is ESH ITRS reports)
- > Include explicit environmental regulations in te Chips Act, together with in-depth reporting of environmental indicators
- Investigate the potential of low-throughput resilient and economically viable production lines in Europe -> important change in current semiconductor business models
- ➤ Using backcasting instead of forecasting for designing roadmaps for European IC manufacturing → focusing on absolute cumulative GHG emissions rather than relative environmental efficiency improvements

Suggestions

> Levers for aligning the sector emissions on climate targets:

- ✓ savings in other sectors (caution: requires proper science-based evaluation including negative enabling effects
 + political quidance to arbitrate the targets between sectors)
 - + political guidance to arbitrate the targets between sectors),
- efficiency #1: sourcing low-carbon electricity (location matters, beware of preemption mechanism !),
- efficiency #2: lower energy intensity of the fabs + GHG abatement,
- efficiency #3 + sobriety #1: reduce die size,
- ✓ sobriety #2: planned <u>degrowth</u> of production volumes through: longer service lifetime, circular economy and sober innovation!
 → deep changes for the semiconductor industry business models

THANK YOU

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