

# Key IC data for an accurate life cycle assessment of ICT devices

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# Fraunhofer IZM

## Technology Development

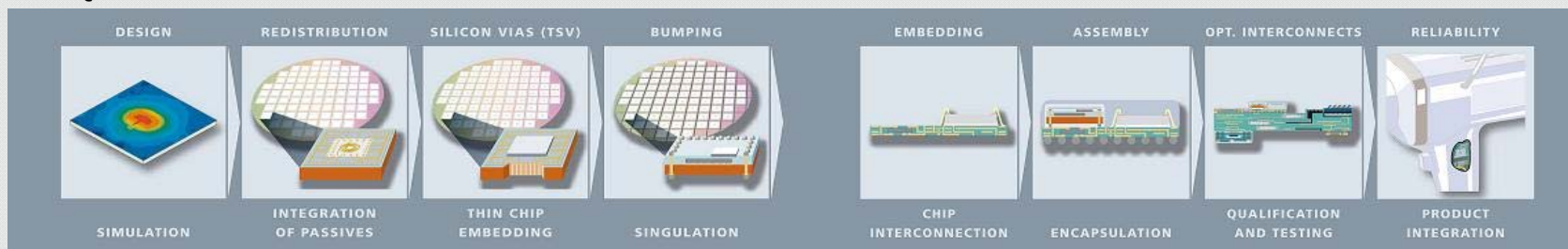
## From Lab to Fab

Material and  
Technology  
Development

Module design,  
hetero-system  
integration

System design,  
manufacturing  
& testing

Smart system,  
function / product  
integration



Wafer-Level  
& Panel-Level  
Packaging

Embedding of  
active & passive  
components

**Reliability  
assessment  
and Testing**

**Sustainability  
assessment and  
Ecodesign**

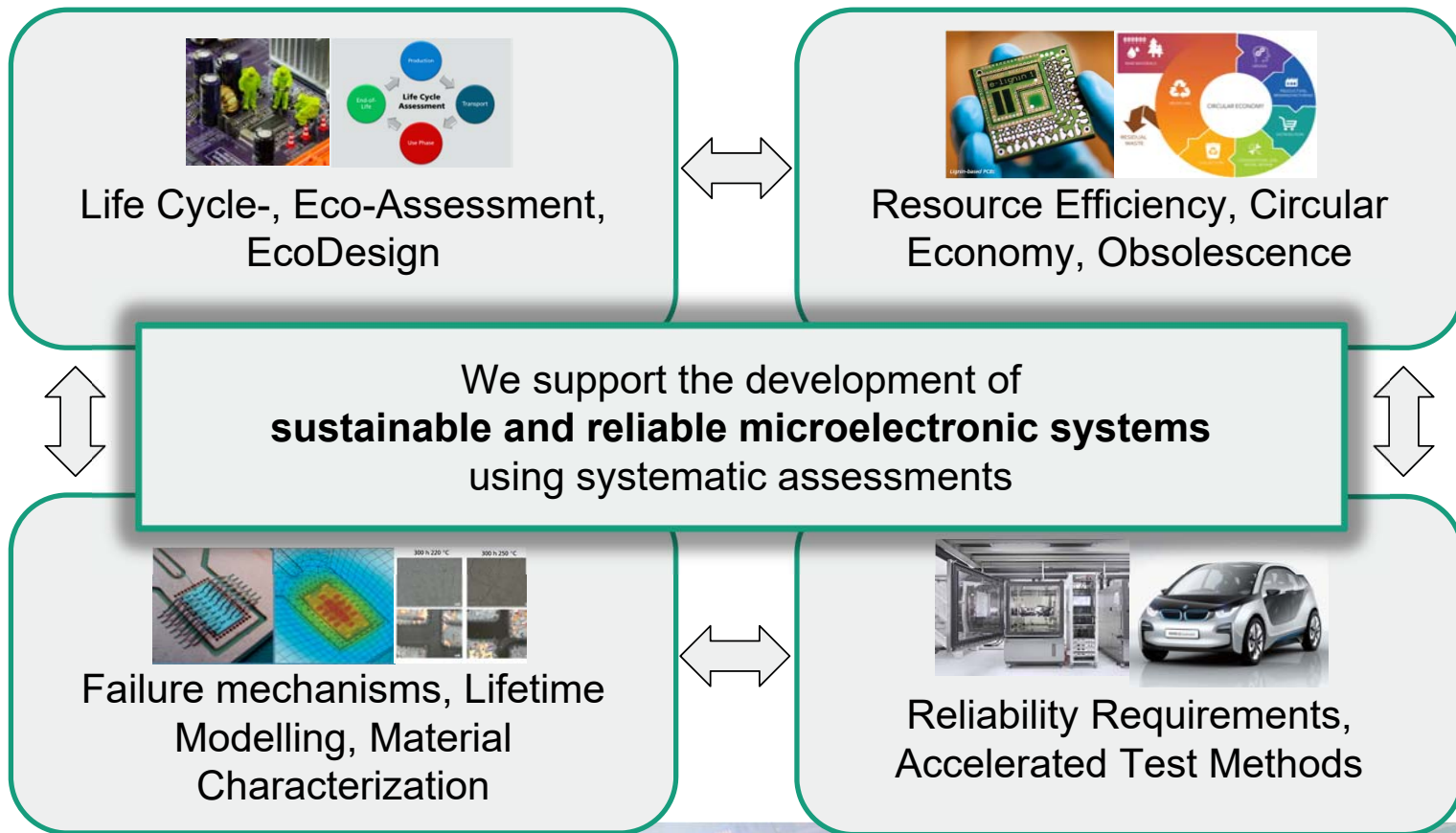


## Module & System Design

## Assessment & Testing

**Dept. Environmental and Reliability Engineering  
ERE**

**Our Mission**





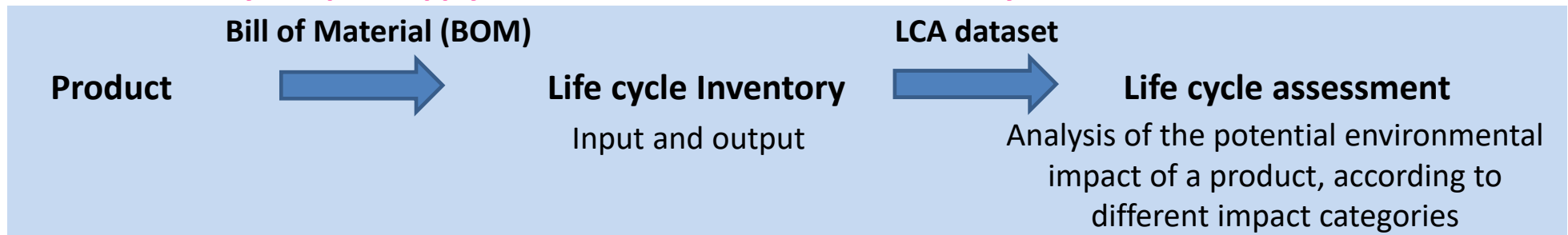
# Main phases of an LCA

## Specificity of ICT

ICT devices:

Very complex supply chain

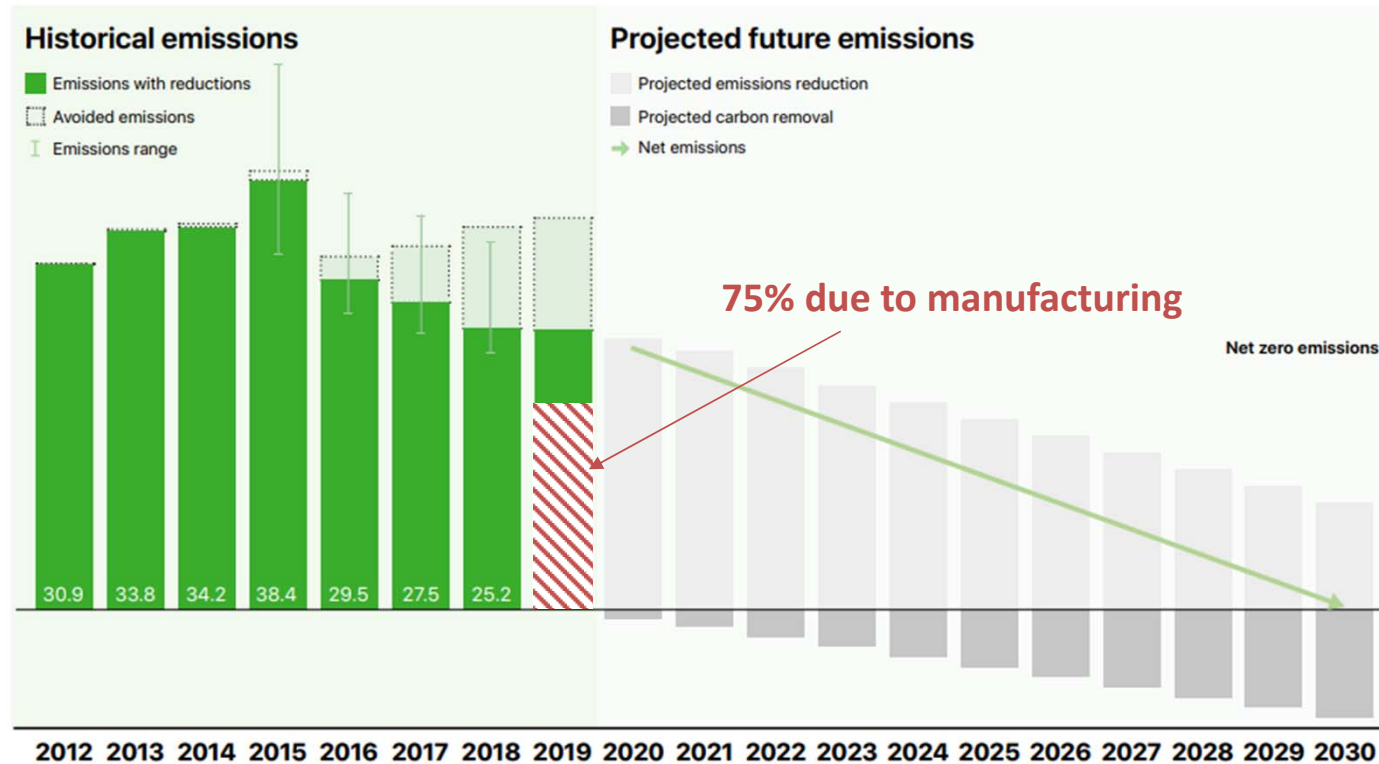
Datasets are currently insufficient



**For ICT devices: Manufacturing phase usually causes the highest environmental impact (short lifetime, low power consumption)**

# Net Zero Targets: driver towards low-emission manufacturing process and high-quality LCA data

Apple historical and projected emissions (Scope 1,2,3 ) from 2012 to 2030



Source: Apple environmental progress report 2020

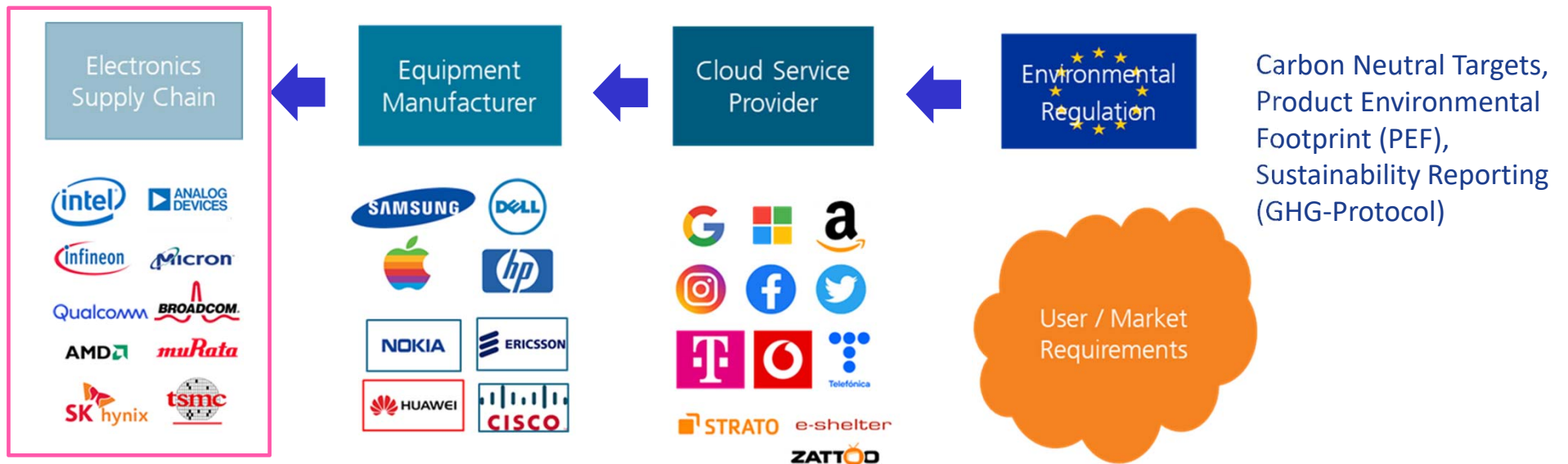
# Net Zero Targets: driver towards low-emission manufacturing process and high-quality LCA data

The production of the core PCB causes the highest impact: 71%



Source: Life cycle assessment of Fairphone 3 (Fraunhofer IZM)

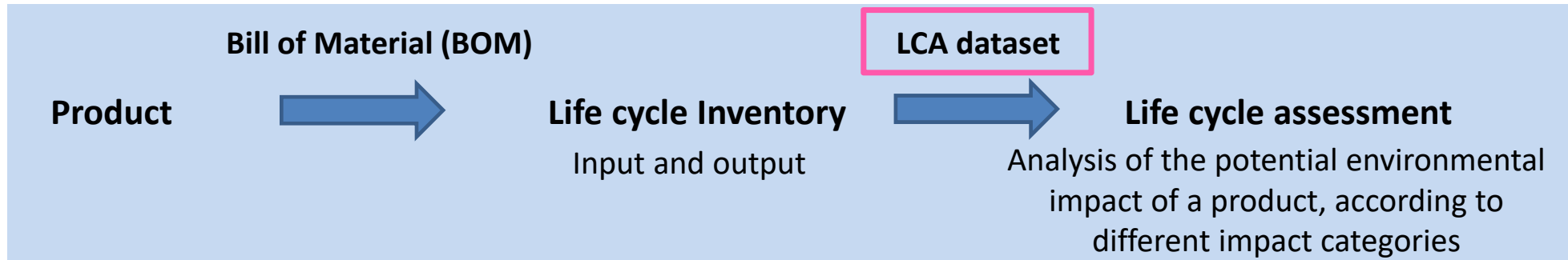
# Equipment & component manufacturers must provide accurate data



## Pressure on the electronics supply chain

# Main phases of an LCA

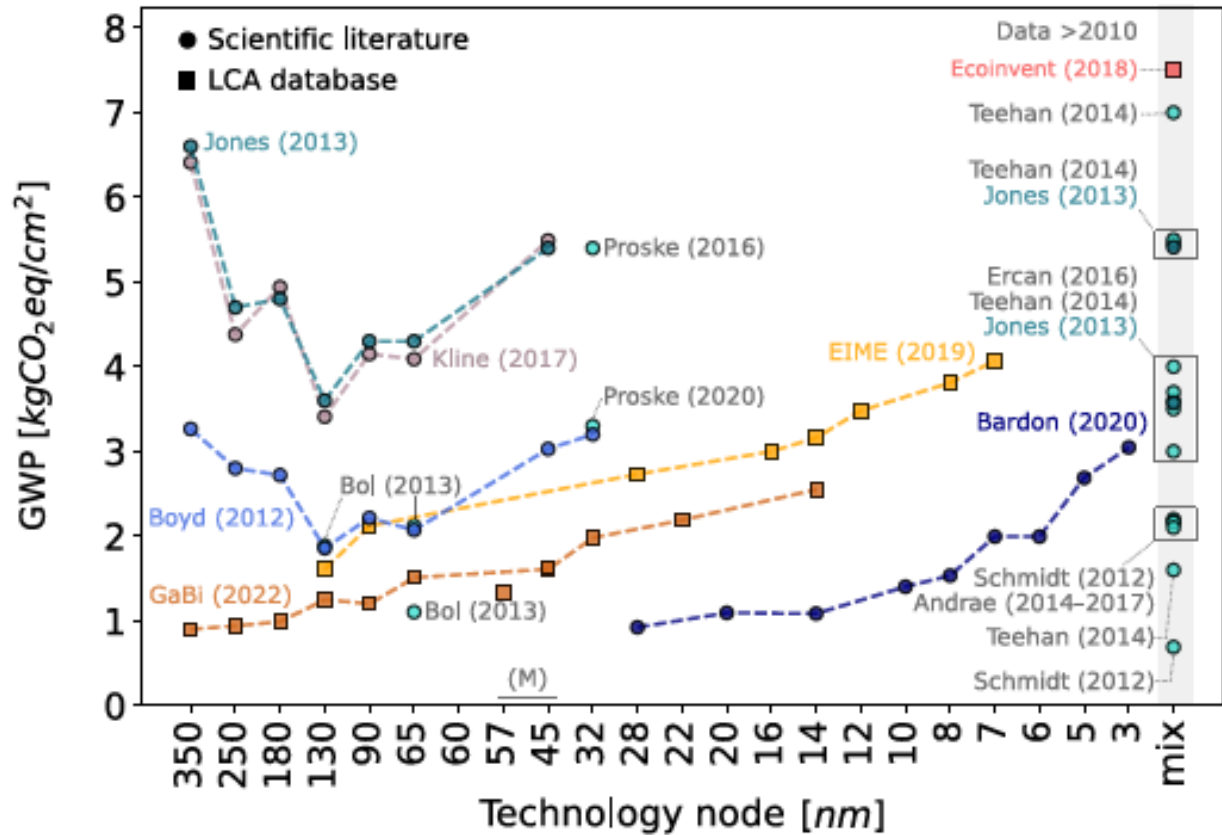
What kind of data are needed for an LCA?





# Actual LCA dataset

Comparison of GWP per die area between the data sets

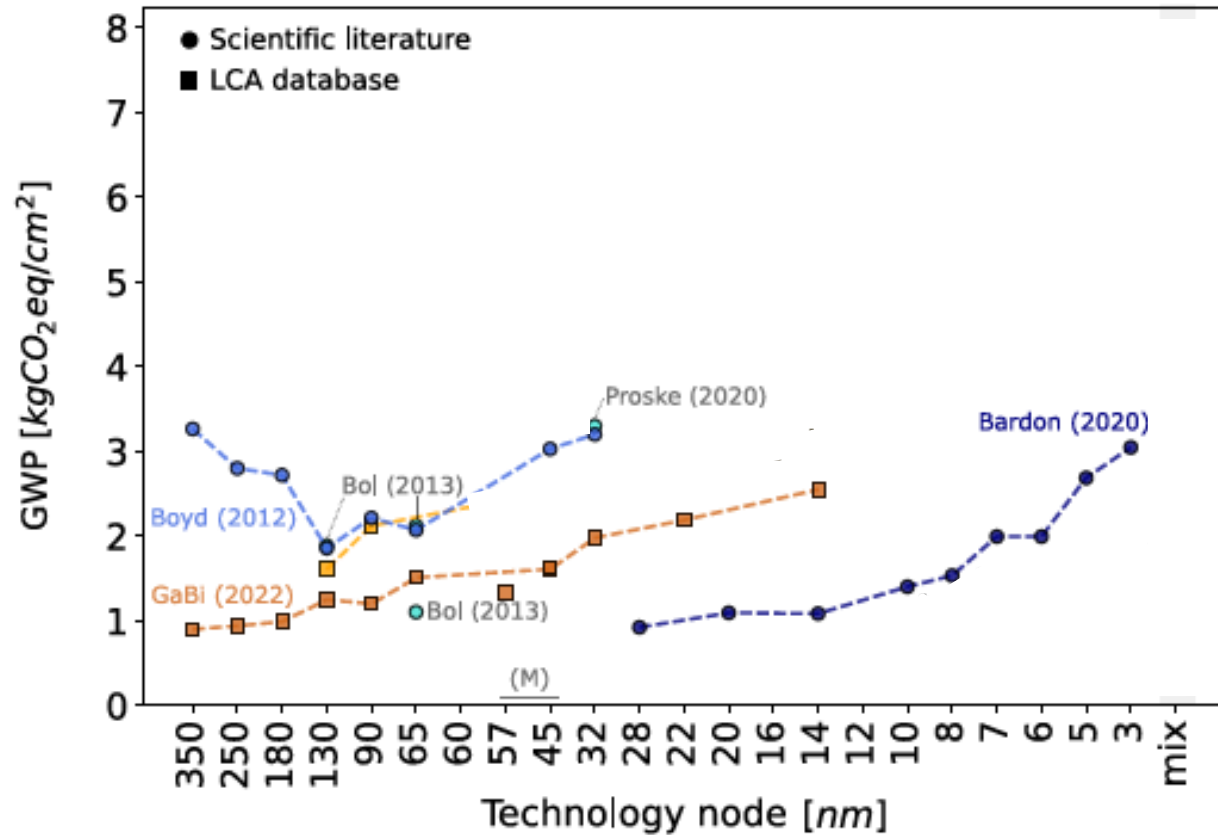


Source: Pirson et al. (2022) "The Environmental Footprint of IC Production: Review, Analysis and Lessons from Historical Trends"



# Actual LCA dataset

Large discrepancy  
between the data sets



Source: Pirson et al. (2022) "The Environmental Footprint of IC Production: Review, Analysis and Lessons from Historical Trends"



# Evaluation of parameters recorded in the IC data sets

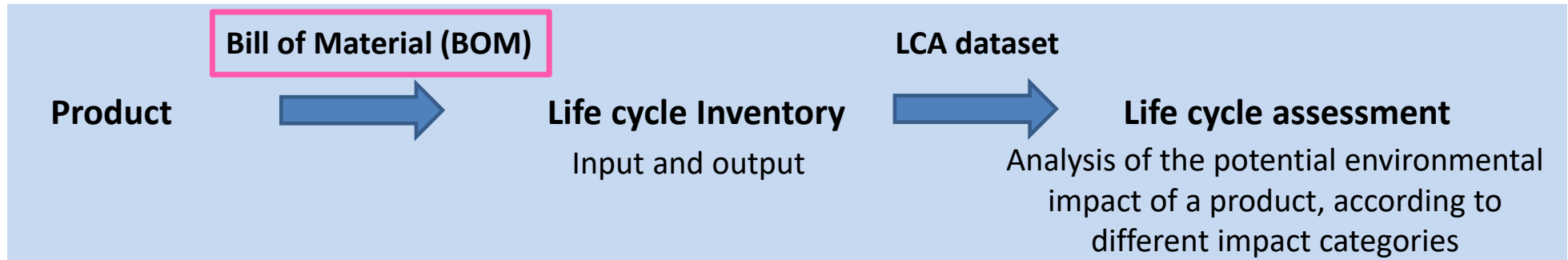
	Boyd (2012)	Bardon et al. (2020)	GaBi LCA database (2022)
Energy demand of raw wafer production	✓ (2002)	✗	✓ (unknown)
Process energy FEOL & BEOL	✓	✓	✓
Process Energy Packaging & (Testing)	✗	✗	✓
Production yield	✓	✗	✓
Direct emissions of chemicals & gases	✓	✓	✓
Energy for the operation of the clean room & sub-fab infrastructure (proportionate)	✓ (Part of process energy)	✓ (percentage surcharge)	✓ (unclear)
Chemical Manufacturing (proportionate)	✓ (tw. 1997)	✗	✓
Machine manufacturing (proportionate)	✓ (1997)	✗	?
Infrastructure production (proportionate)	✓ (1997)	✗	?
	<b>Detailed but old</b>	<b>New, but incomplete</b>	<b>Intransparent</b>

Source: Pirson et al. (2022) "The Environmental Footprint of IC Production: Review, Analysis and Lessons from Historical Trends"



# Main phases of an LCA

## Specificity of ICT





# LCA of a populated PCB

## Example of BOM for a populated PCB

IC,SDRAM,1GBIT,64MX16BIT,1.35V,DDR3L-1600,11-11-11,SM,FBGA-96,NT5CC64M16GP-DII,INDUSTRIAL

IC,SW,WLAN,802.11A/B/G/N/AC,1.9-5V,INSERTION LOSS=0.5DB,H ISOLATION=30DB,SM,DFN-8-64,NJG1804K64

IC,MPU,VIDEO,1.1V,380MW,1080P@30FPS,SM,BGA-256,OV00798-B56G-1C

IC,SENSOR,IMAGE,1080P,2688X1520P,4MP,10BIT RAW,1.1-3.0V,SM,CSP5-67,OV04686-H67A

IC,WLAN/BT,802.11A/B/G/N,BT 5,802.15.4,SM,QCA-4020-1-217MSP,I-TEMP

IC,SW,RF,SPDT,5V,0.03-6GHZ,33DBM,SM,QFN-6,RTC6608OSP

IC,SW,DPDT,DUAL BAND,4.5V,2.4-2.5GHZ,4.9-6GHZ,PIN=30DBM,SM,QFN-6,RTC6615H

IC,REG,LDO,LINEAR,2.5-5.5V,350MA,VOUT=3.3V,SM,SOT-23-5,G2259-330T11U

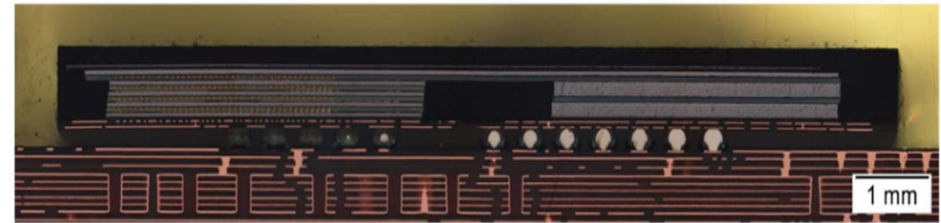
IC,CNVT,2.5-6V,1.2A,2000KHZ,SM,WSON-8,TLV62080DSG

IC,MCU,24MHZ,16BIT RISC,32KB FRAM,4KB SRAM,12BIT ADC,1.8-3.6V,SM,LQFP-48,MSP430FR2155TPTR

# Accurate assessment of semiconductor die in package



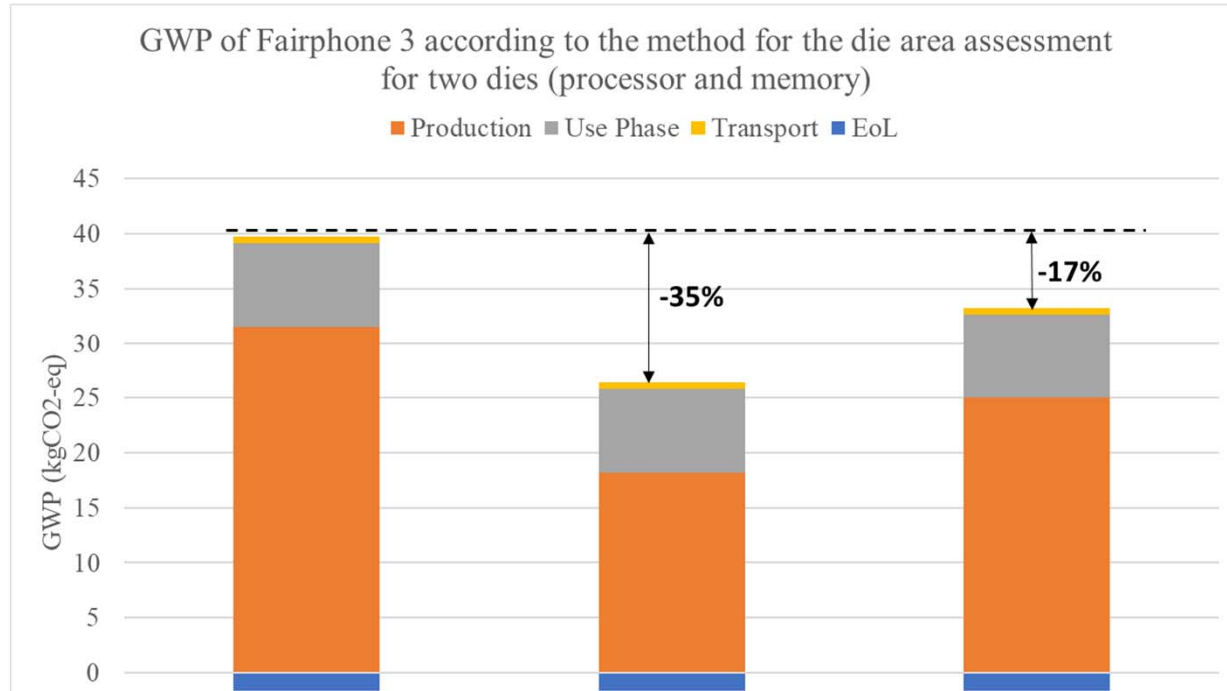
Destructive analysis to assess the number of dies and total semiconductor area in package



Memory chip

Source: Billaud et al. CARE INNOVATION conference paper "ICs as drivers of ICT carbon footprint: an approach to more accurate die size assessment"

# Accurate assessment of semiconductor die in package



chip	Destructive analysis	Assumption 1 DPR* = 8%	Assumption 2 DPR* = 80%
Memory chip	508 mm <sup>2</sup>	12 mm <sup>2</sup>	120 mm <sup>2</sup>
SoC	47 mm <sup>2</sup>	13 mm <sup>3</sup>	134 mm <sup>2</sup>

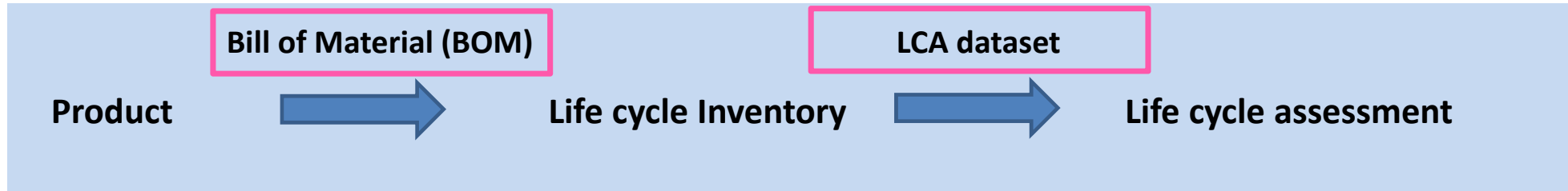
**Variation in semiconductor content has a high impact on the LCA results**

This assumption is usually not mentioned in LCA !!

\*DPR= die-to-package ratio

Source: Billaud et al. CARE INNOVATION conference paper "ICs as drivers of ICT carbon footprint: an approach to more accurate die size assessment"

# Wish list for an accurate LCA of ICT



- Key IC data from a product

- Number and size of dies in package
- Type of semiconductor
- Type of package
- Technology node or memory technology

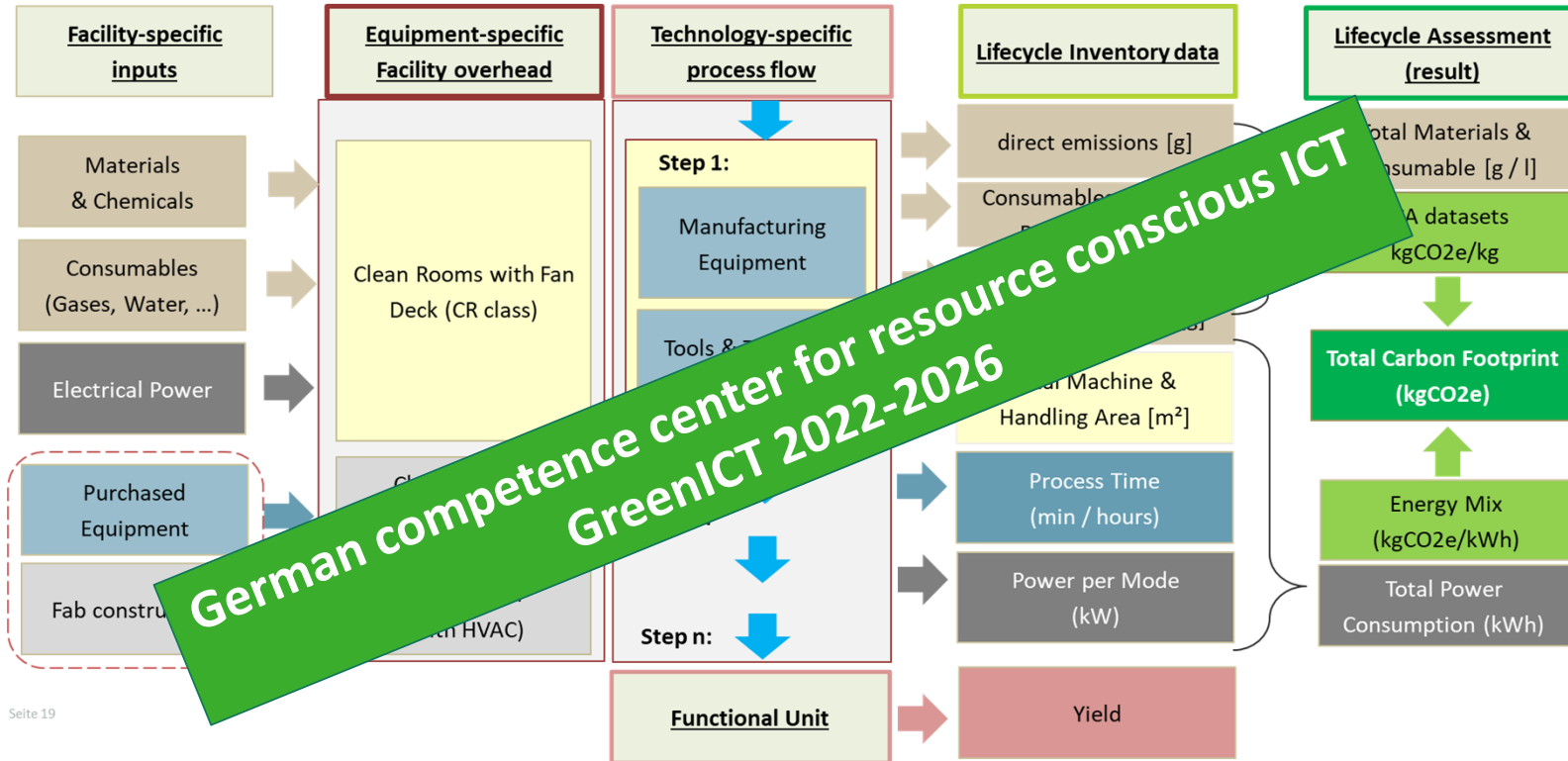
- Key IC data in LCA dataset

- Transparent methodology
- At least two impact categories ADP and GWP
- Impact per chip type, technology node, and package type

**Not exhaustive!**



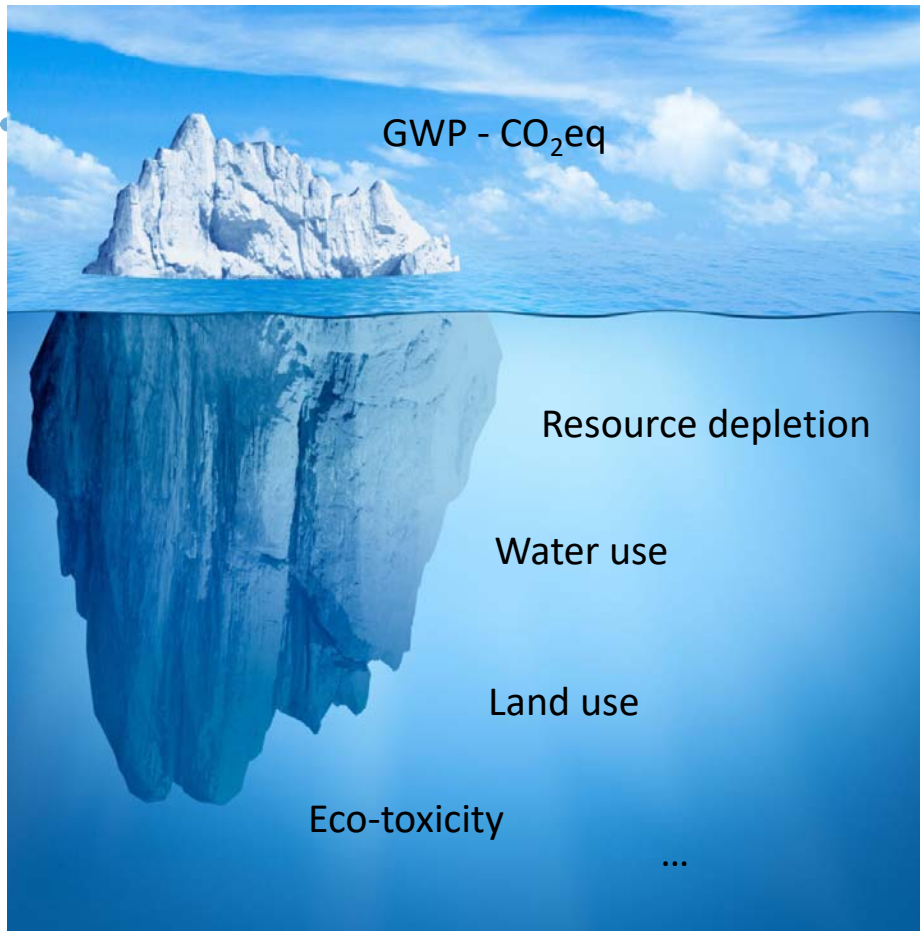
# Data requirements for life cycle assessment of IC production (process step-specific) Equipment-specific carbon footprint and overall process



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<https://greenict.de/ueber-fmd/>





For gold, silver and palladium in IC packages for the core module of Fairphone 3

**3 mg of Au, Ag, Pd → ~ 4 kg of rock extracted**

For WW smartphone production in 2021  
**More than 5 million tonnes rock extracted**

Source: USGS 2022 "Rock-to-Metal Ratio: A Foundational Metric for Understanding Mine Wastes"

Source: LCA of Fairphone 3



THANK YOU

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WORKSHOP - Sustainable Electronics & International Cooperation On Semiconductors

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