Augmented FDSOI platforms for improved sustainability

Roberto GONELLA

R&D Executive Director

STMicroelectronics

We are creators and makers of technology

One of the world's largest semiconductor companies

48,000 employees of which **8,400** in R&D

$16.1 billion revenues in 2022

Over **80** sales & marketing offices serving over **200,000** customers across the globe

14 manufacturing sites

Signatory of the United Nations Global Compact (UNGC)
Member of the Responsible Business Alliance (RBA)

Where you find us

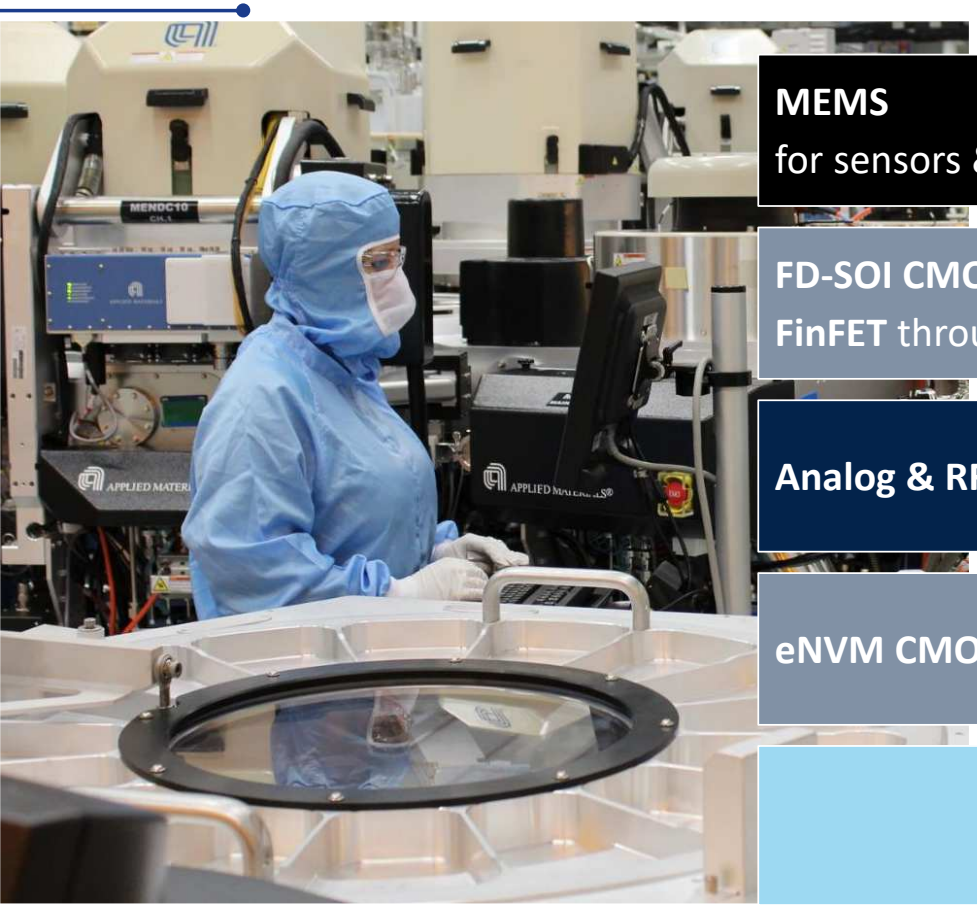
Making **driving** safer, greener, and more connected

Enabling the evolution of **industry** towards smarter, safer, and more efficient factories & workplaces

Making **homes & cities** smarter, for better living, higher security, and to get more from available resources

Making everyday **things** smarter, connected, and more aware of their surroundings

Differentiated technologies are our foundation



MEMS
for sensors & micro-actuators

Smart Power: BCD
(Bipolar - CMOS - Power DMOS)

FD-SOI CMOS
FinFET through Foundry

Discrete, Power MOSFET, IGBT
Silicon Carbide, Gallium Nitride

Analog & RF CMOS

Vertical Intelligent Power

eNVM CMOS

Optical sensing solutions

Packaging technologies
Leadframe – Laminate – Sensor module – wafer level

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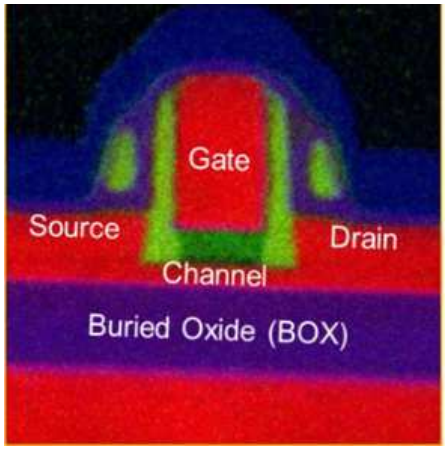
Our strategy stems from key long-term enablers

Smart Mobility	Power & Energy	Internet of Things & Connectivity
		
Helping car manufacturers make driving safer, greener, and more connected for everyone	Enabling industries to increase energy efficiency everywhere and the use of renewable energy	Supporting the proliferation of smart, connected IoT devices with products, solutions & ecosystems

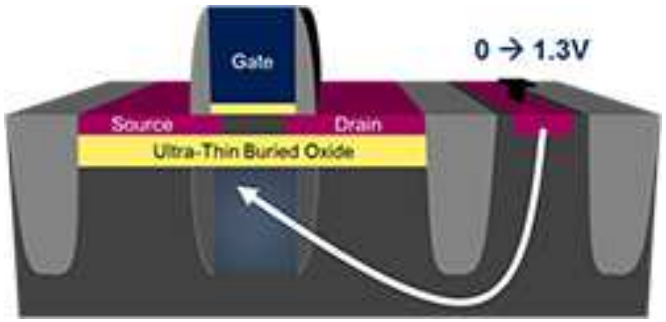
What's FDSOI?



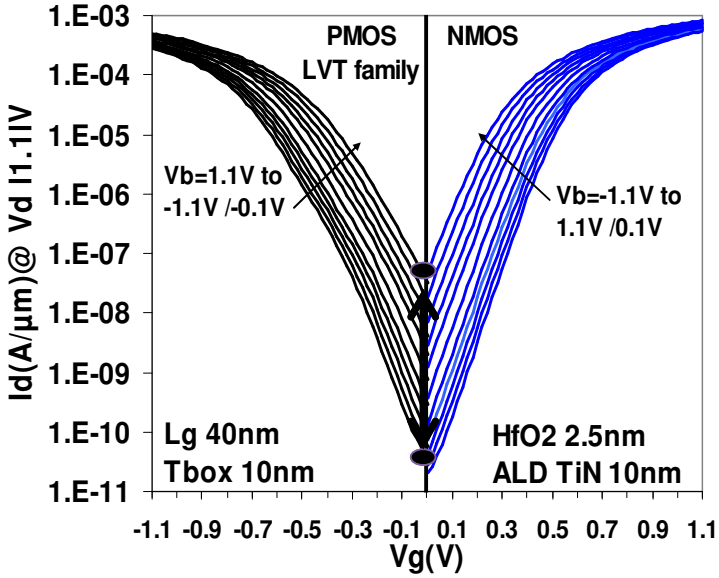
FDSOI is a cost-effective planar technology that relies on

- sub-threshold slope reduction
- DIBL lowering
- FBB techniques

To boost performances especially at low and ultra low voltage



- The presence of the buried oxide allows the application of back-biasing voltages, resulting in breakthrough **dynamic control of the transistor**

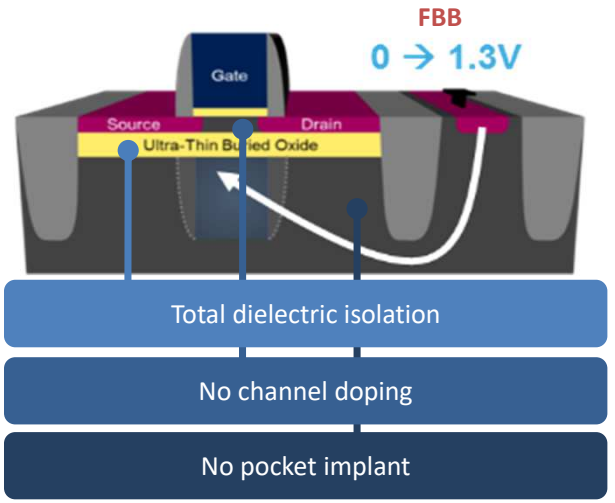


FD-SOI - the body bias advantage

- Forward Body Biasing is a unique and effective knob available in FD-SOI for getting **maximum leverage on the device operating range**

Forward **B**ody **B**iasing: An **extremely powerful** and flexible concept in FD-SOI

- Performance boost
- Reduce power consumption at a given performance requirement
- Process compensation reducing the margins to be taken at design
- Seamless inclusion in the EDA flow



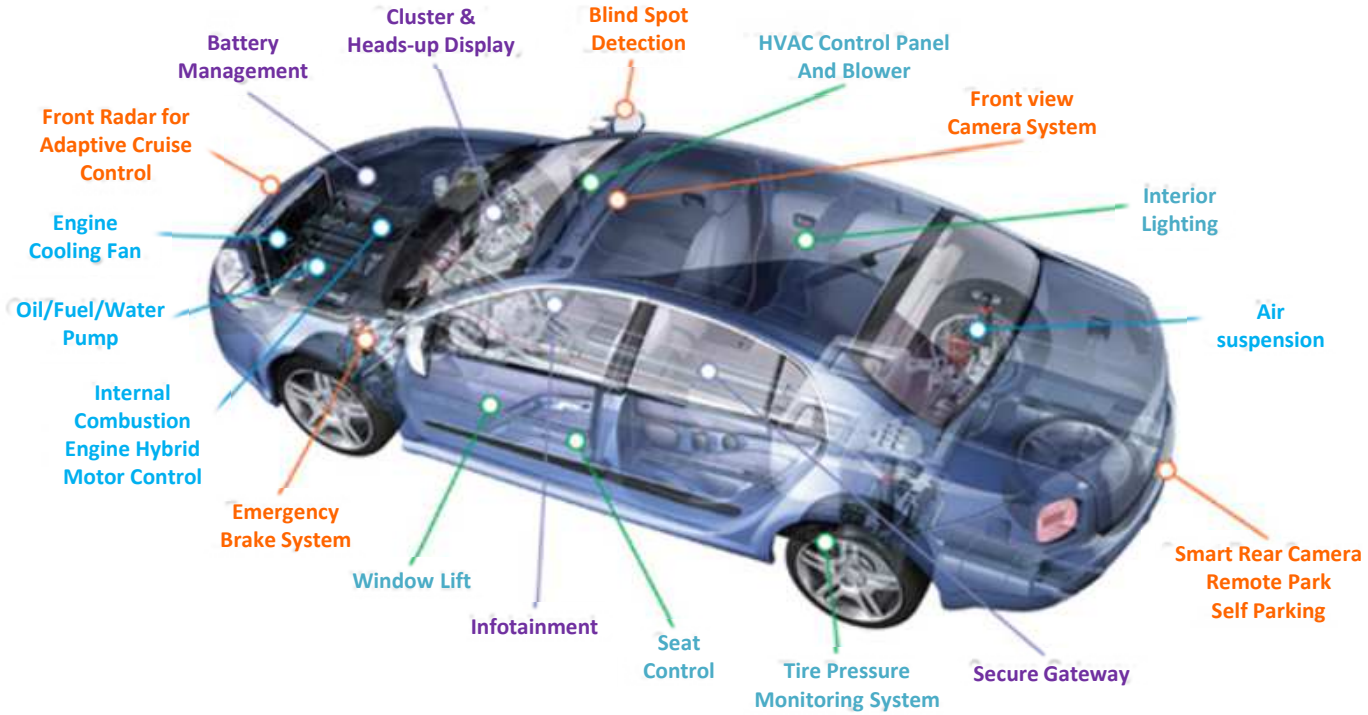
A very reasonable effort for extremely worthwhile benefits

Smart Mobility – FDSOI Inside

Smart Mobility

Helping car manufacturers make driving safer, greener, and more connected for everyone

Automotive MCUs & eNVM Usages



Advanced Drivers Assist System (ADAS)

→ Ultimate speed digital / eNVM

Power Train & Chassis

→ eNVM / high performance analog / full reliability

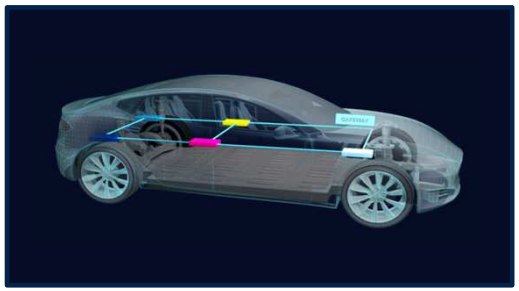
Body & Comfort

→ eNVM / high speed digital / high perf. analog

Driver information & Connectivity

→ RF features / eNVM / dense digital

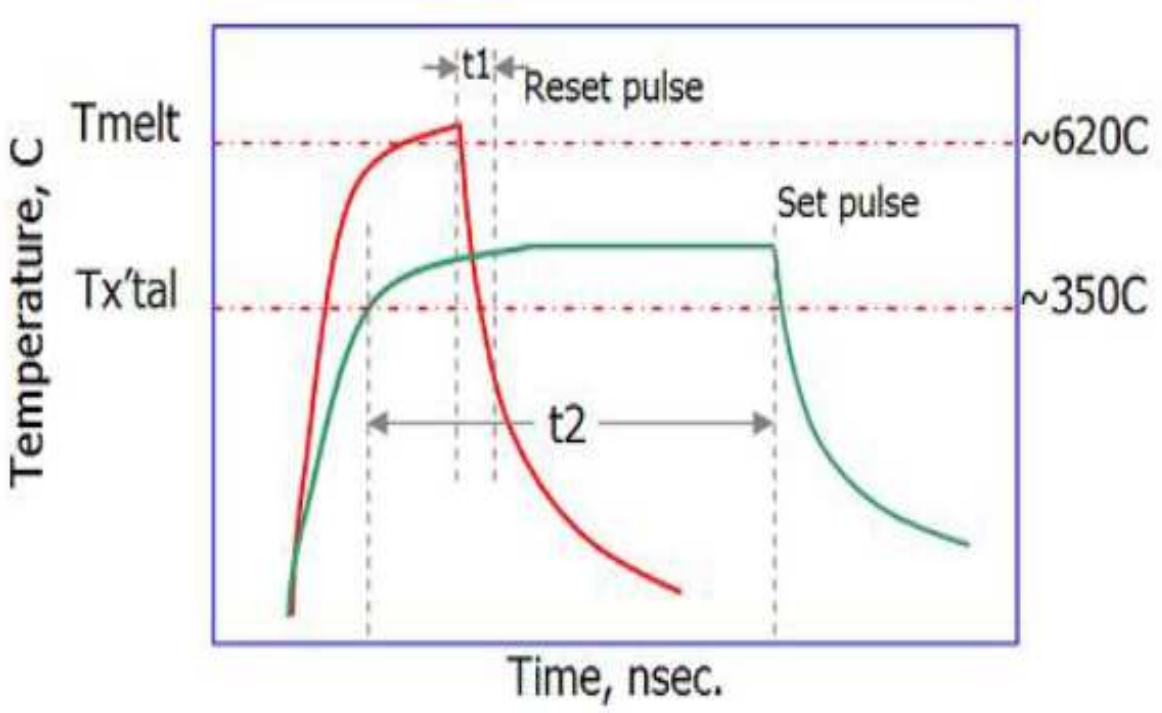
MCUs Dissemination in Automotive

Advanced safety L2++	Connectivity	Domain/zone car architectures	Electrification
			
Radar & Sensor fusion **V2X , Driver Monitoring**	**Telematics, Connected GW,** HD **Precise Positioning**	**System integration** & **SW reconfigurable vehicles**	**Digital power conversion**

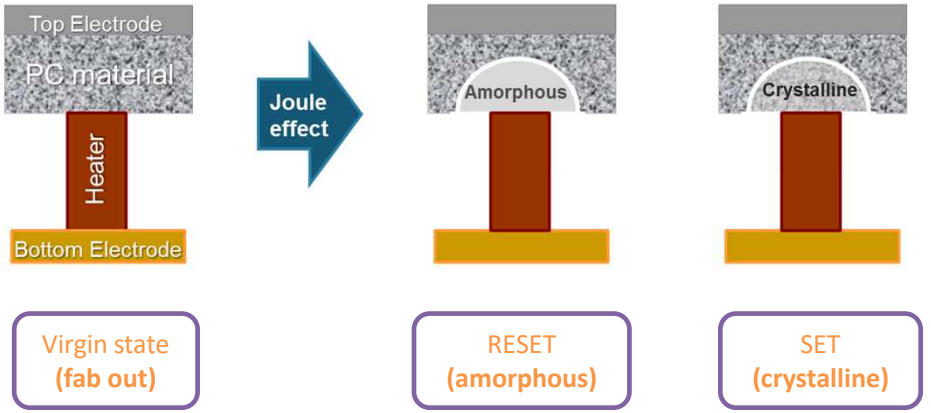
Technology innovation
ST's key to drive Digital transformation

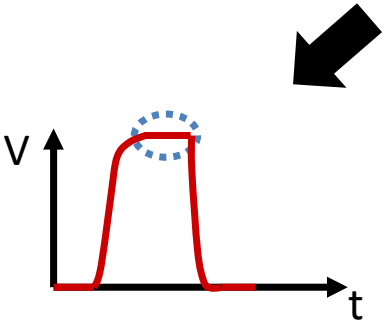
Technology	**FD-SOI and PCM**
Energy	**Wide bandgap materials**
Design	**Smart architectures**

Phase-Change-Material working principle

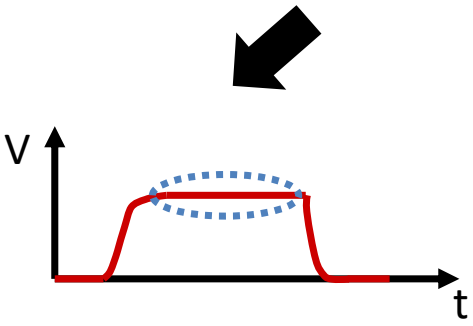


[Arnaud et al., IEDM 2018]



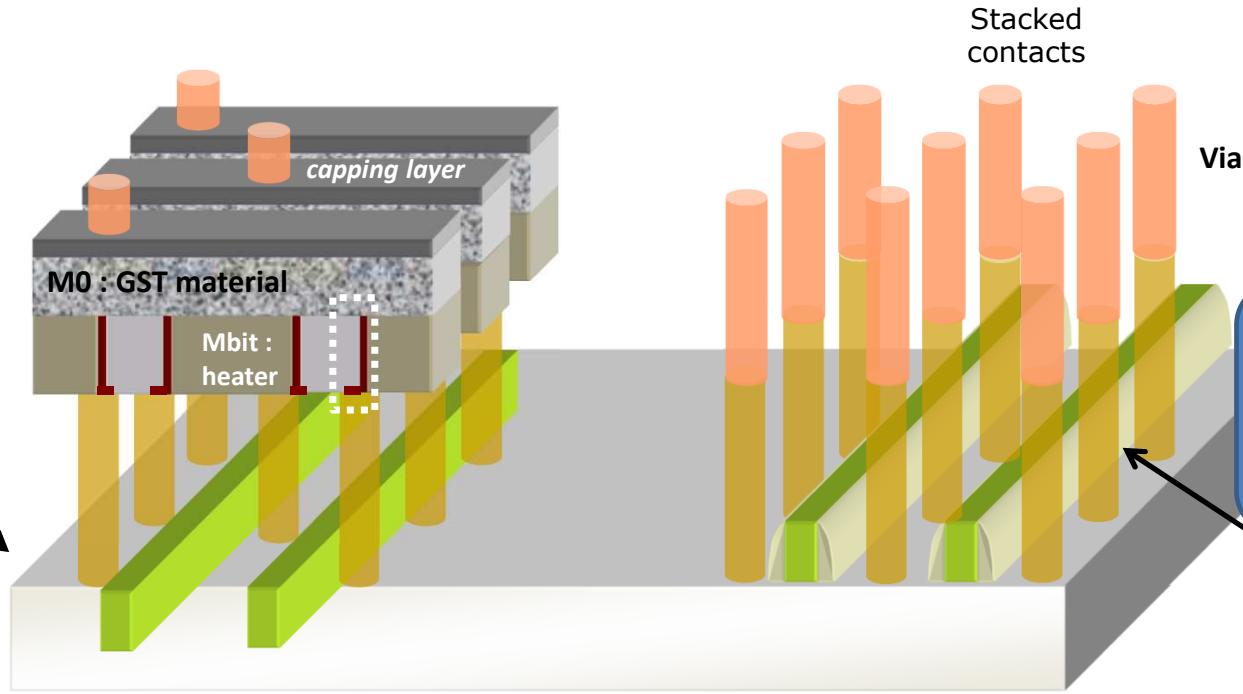


- Rapid falling edge
- $T > T_{melting}$



- $t_{pulse} > t_{crystallization}$
- $T_{crystallization} < T < T_{melting}$

ePCM-FDSOI Co-Integration



BJT Selector

ENABLED BY FDSOI

WELL ESTABLISHED 28nm FDSOI

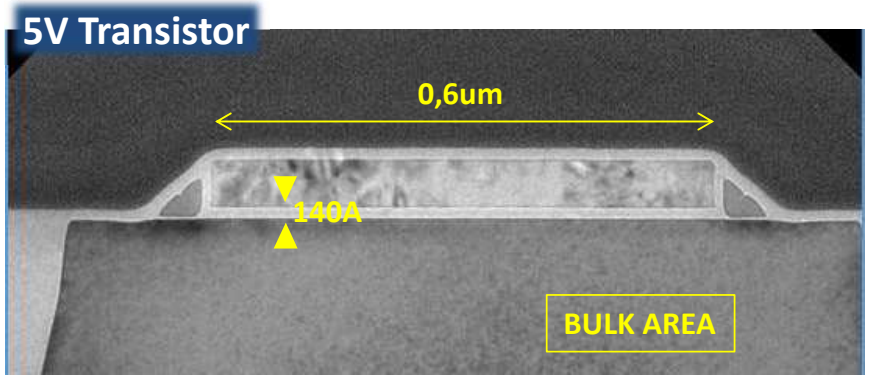
FDSOI & HYBRID devices

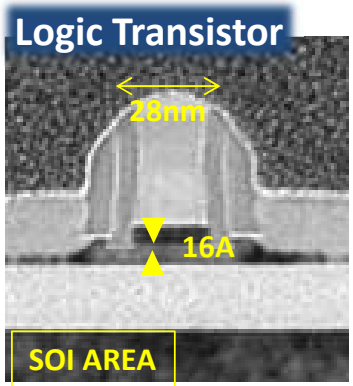
PCM array

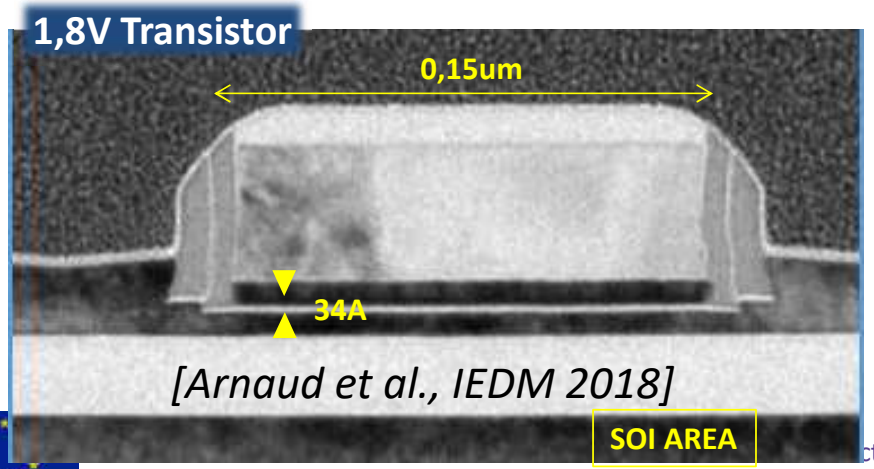
Logic SRAM

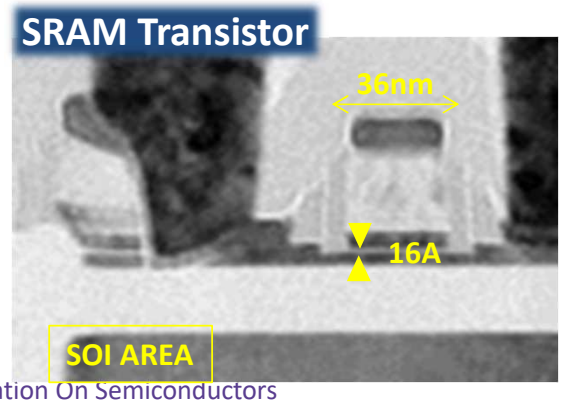
[Arnaud et al., IEDM 2018]

Triple Gate Oxide Device Integration



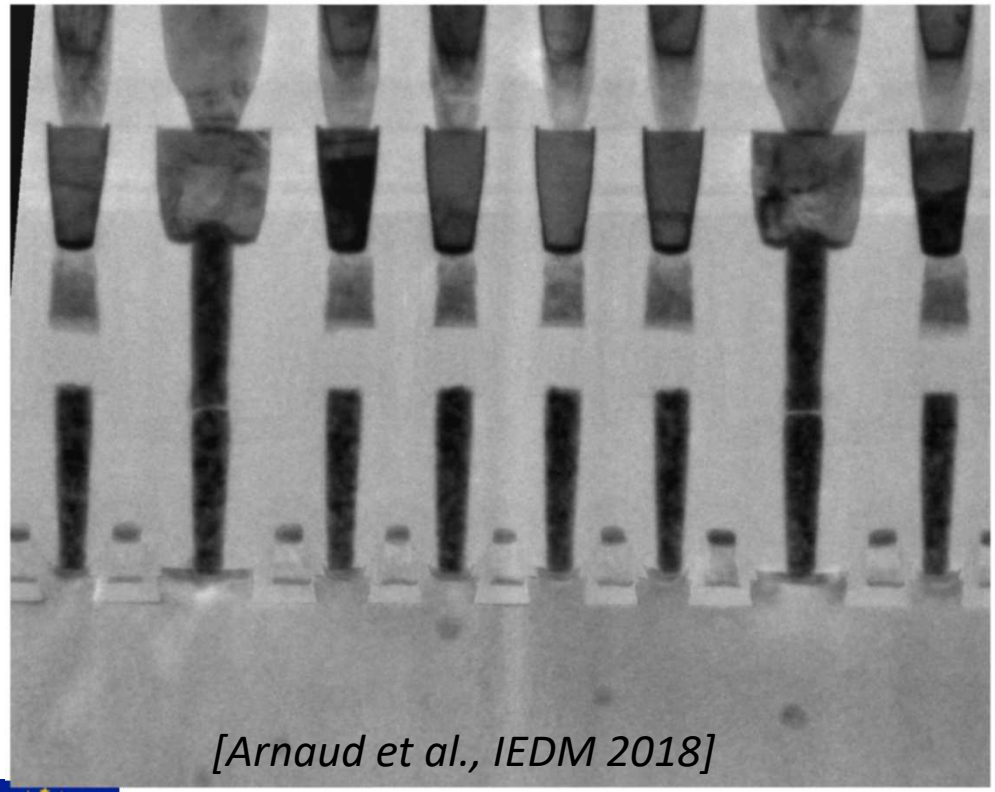


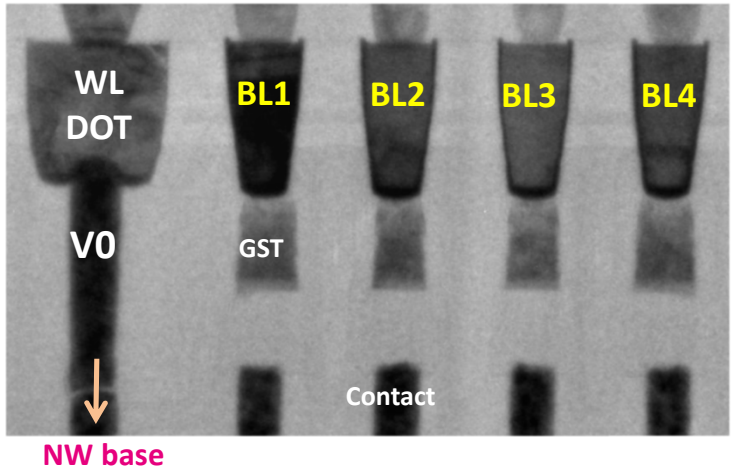




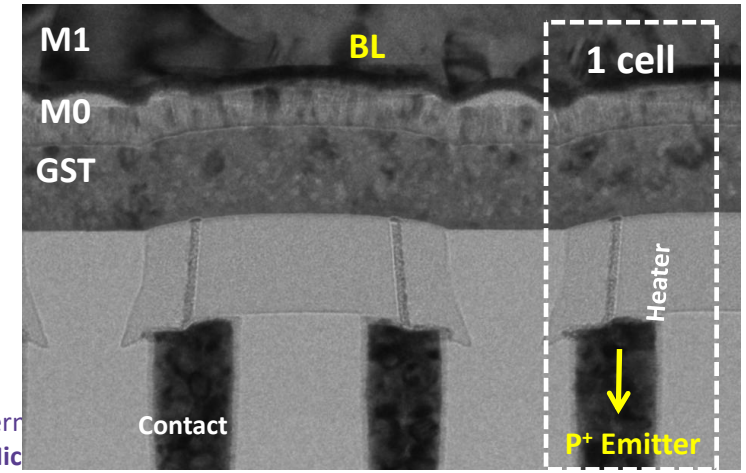
PCM Morphology (Storage element & heater)

General view of the structure



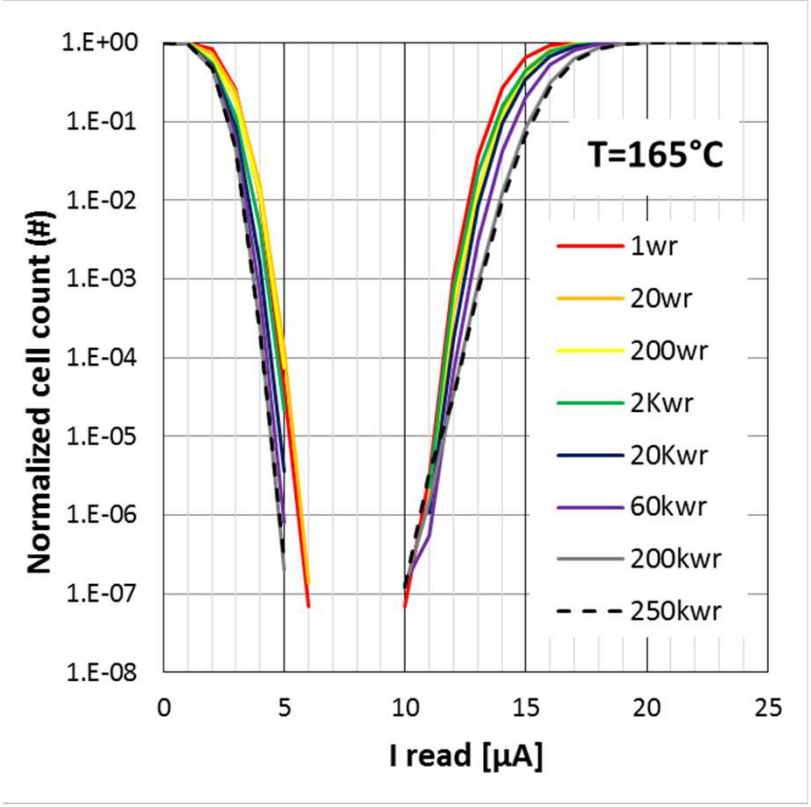


Section along WL

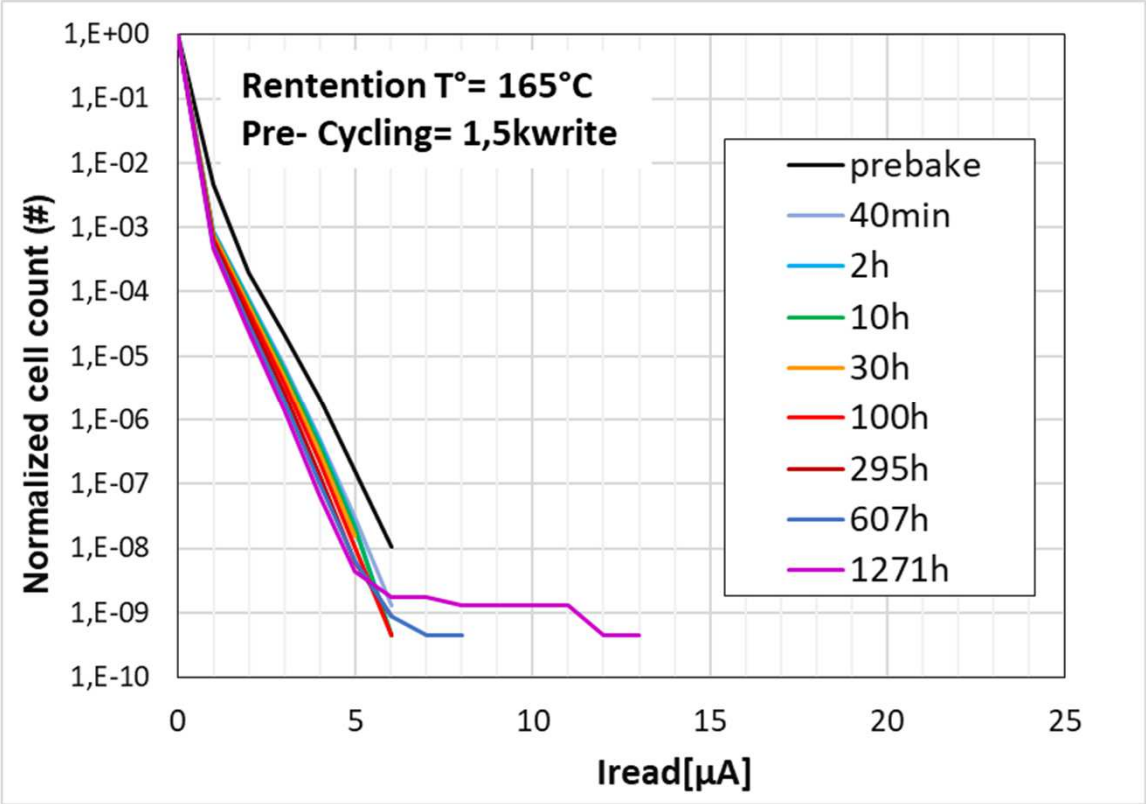


Section along BL

16MB ePCM Reliability for Grade-0 Automotive MCUs



Reading Window

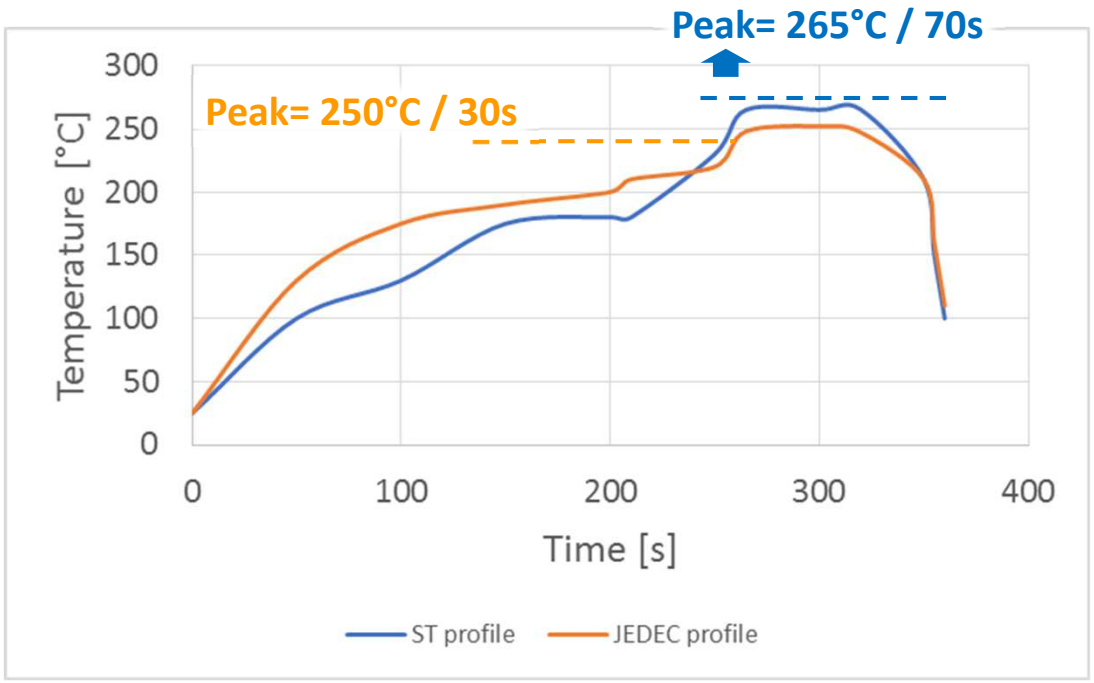


RESET data retention

[Arnaud et al., IEDM 2018]

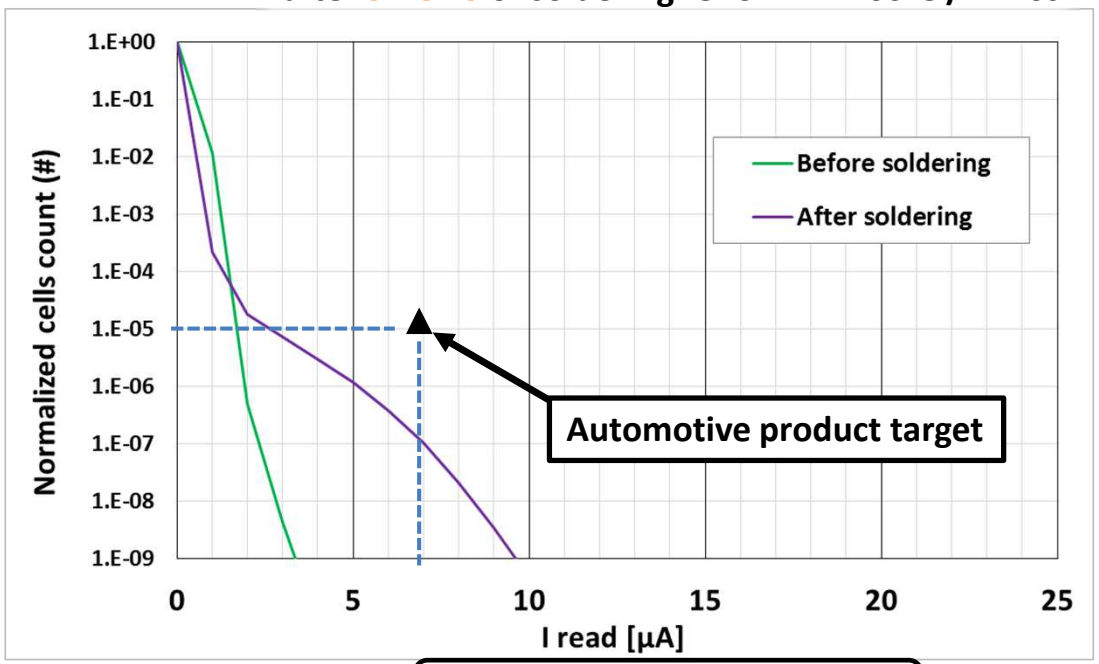
16MB ePCM - Post Soldering Reflow RESET

UNIQUE AND KEY ADVANTAGE OF PCM



Soldering reflow thermal profile

16MB PCM array cell distributions after 3 RUNS of soldering reflow - T>260°C / ~210s



RESET current distributions

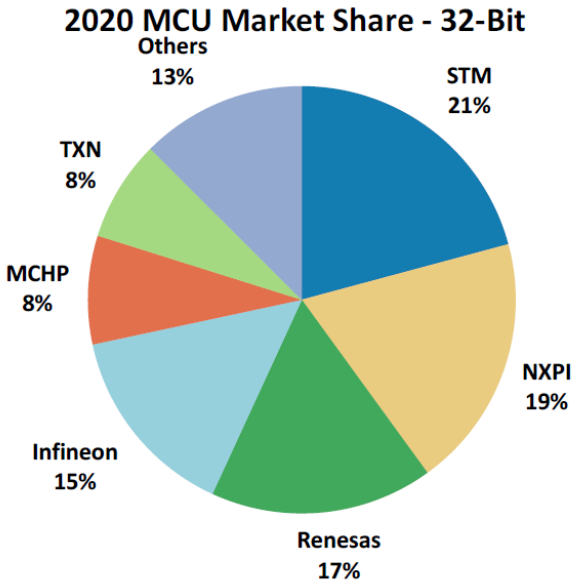
[Arnaud et al., IEDM 2018]

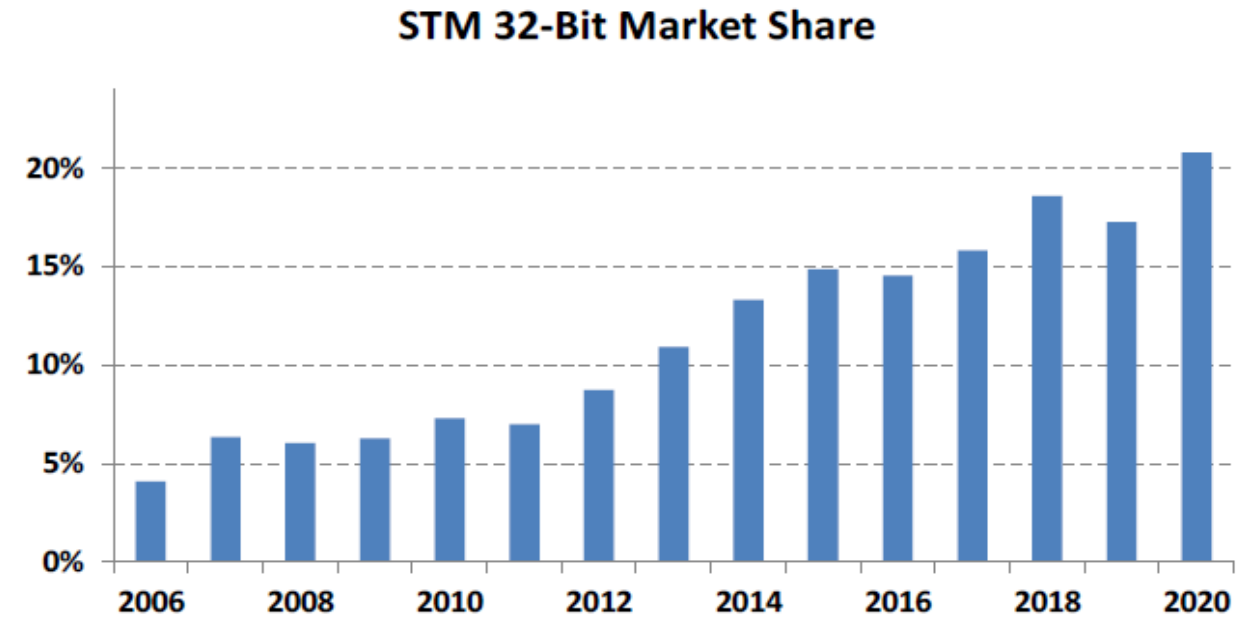
Power & Energy – FDSOI Inside

Power & Energy

Enabling industries to increase energy efficiency everywhere and the use of renewable energy

STMicroelectronics 32-bit MCUs growth

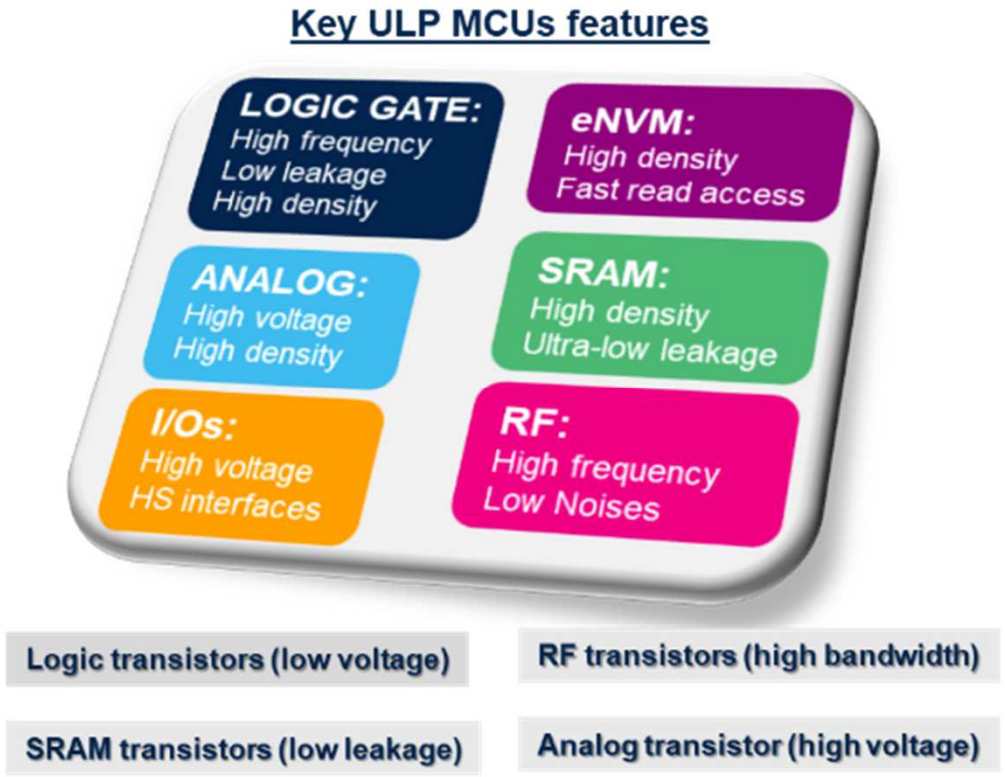




Source: Gartner, Morgan Stanley Research

- Continuous growth of market share in MCUs, especially 32-bit
- Main business for ST is about general purpose and ULP MCUs

ULP MCUs wide range needs : birth of 18nm FDSOI



+ cost

18nm FDSOI

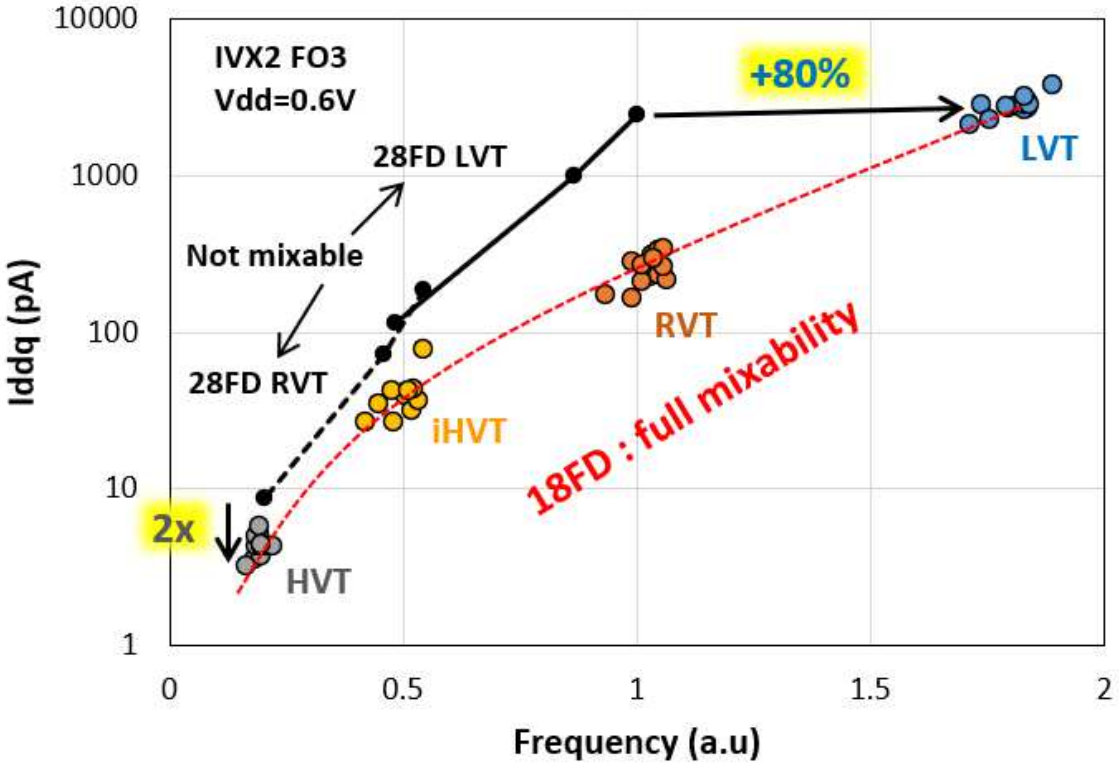
Need performance at low voltage, low leakage, density and low process cost

18nm FDSOI: global features

- Triple gate oxide: SG (0.9V), EG (1.8V), eZG (3.3V)
- 4 VTs, full flipwell
- Mx pitch: 64nm
- CPP: 100/108nm
- SRAM: 0.102µm^2
- cSiGe continuous active (CNRX) standard cells scheme
- RF dedicated offer
- ePCM for eNVM

[Doohong Min et al., IEDM 2021]

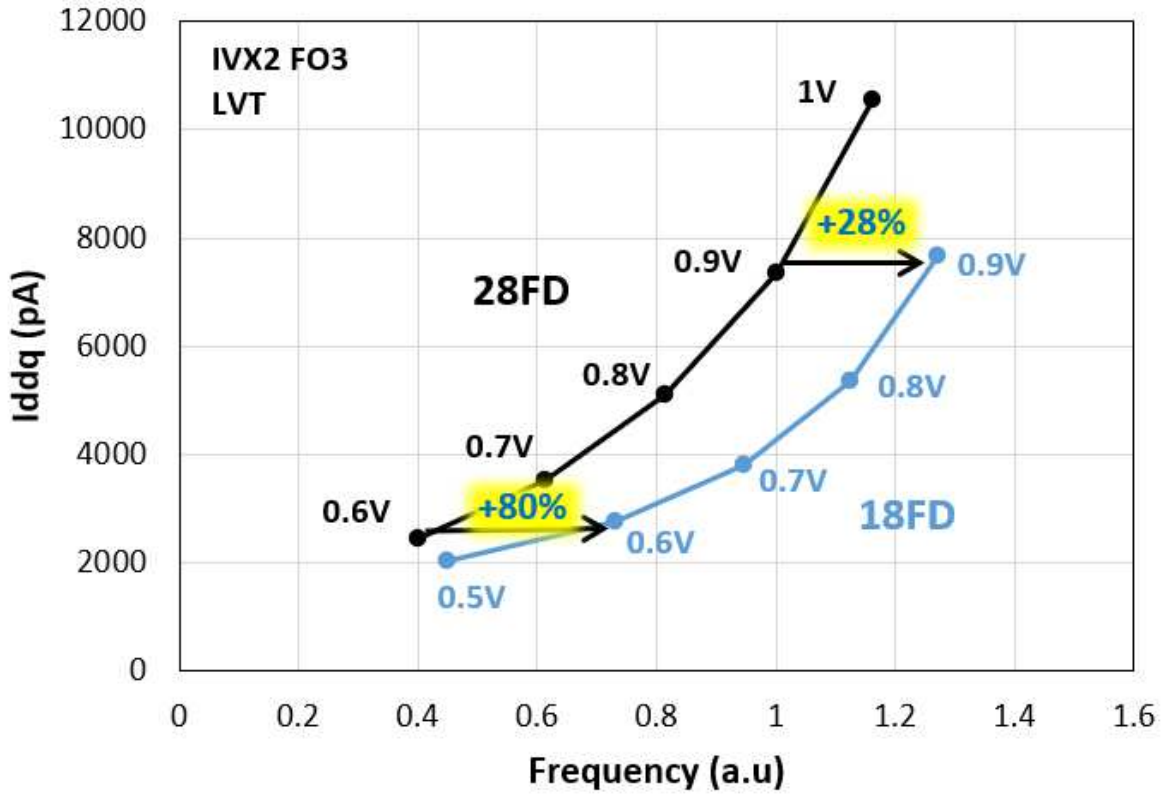
Wide range of speed/leakage



- 4 VTs mixability
- +80% perf. at 0.6V wrt 28FDSOI, 2X leakage reduction

[Weber et al., IEDM 2022]

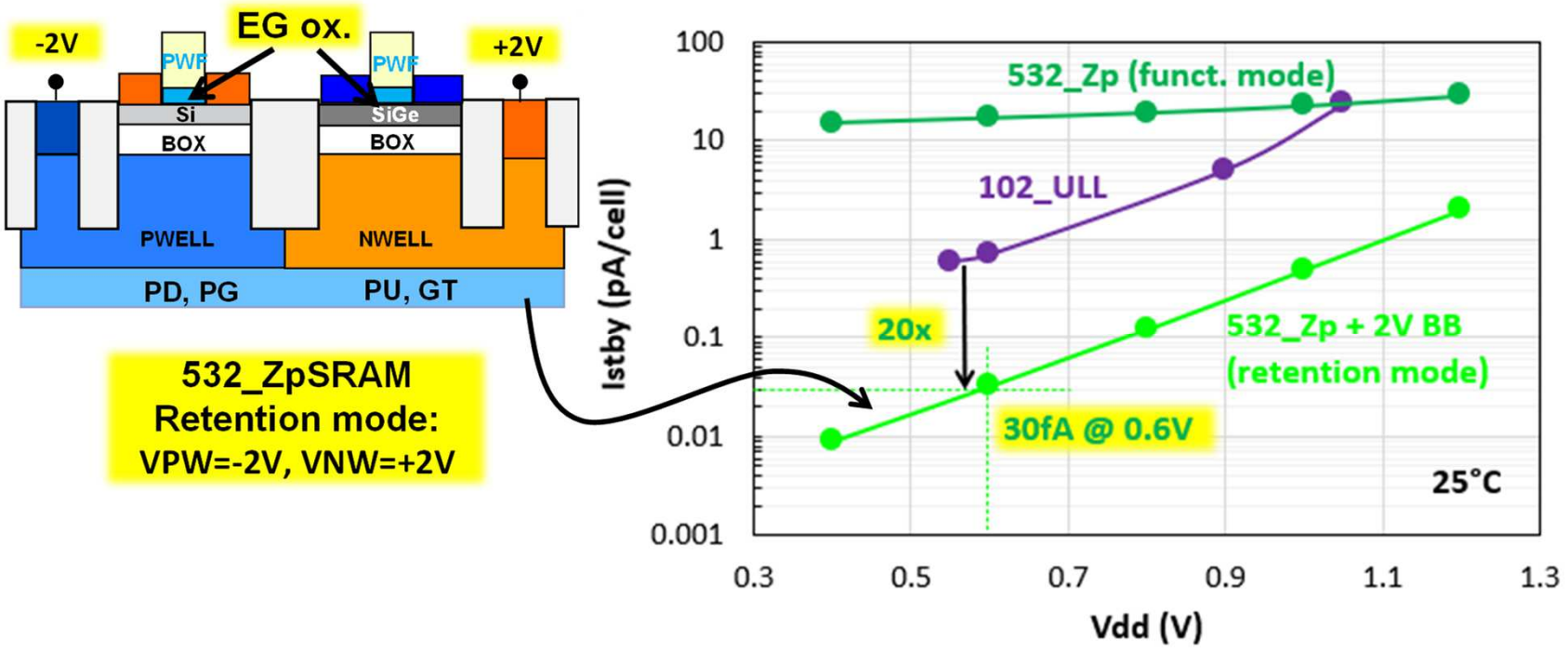
High performance at low voltage



[Weber et al., IEDM 2022]

- From +28% speed at 0.9V up to +80% at 0.6V wrt 28FDSOI

ZpSRAM retention leakage



[Weber et al., IEDM 2022]

- Extremely low retention leakage of 30fA/cell at 0.6V, 25°C is demonstrated, 20x lower than for the 102ULL bitcell !

IoT & Connectivity – FDSOI Inside

Internet of Things & Connectivity

Supporting the proliferation of smart, connected IoT devices with products, solutions & ecosystems

IoT Devices Requirements

	Processing & Security	Sensing & Actuating	Connectivity	Signal Conditioning & Protection	Power & Energy Management
Smart Things	Ultra-Low Power to High Performance Scalable Security solutions	Full range of sensors and actuators	10 cm to 10 km	Nano Amps to Kilo Amps	Nano Watt to Mega Watt
Smart Home					
Smart City					
Smart Industry					

IoT Devices Requirements

Processing & Security	Sensing & Actuating	Connectivity	Signal Conditioning & Protection	Power & Energy Management
Smart Things				
Smart Home				
Smart City				
Smart Industry				

FD-SOI enabling Integration Path

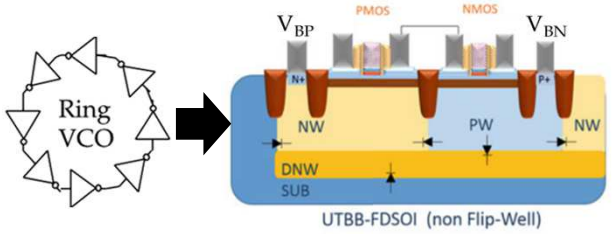
solutions

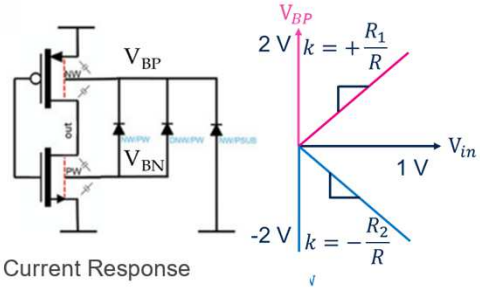
Nano Watt to Mega Watt

Highly Linear Large Signal Compact Voltage-to-Current Converter in 28 nm FD-SOI Technology

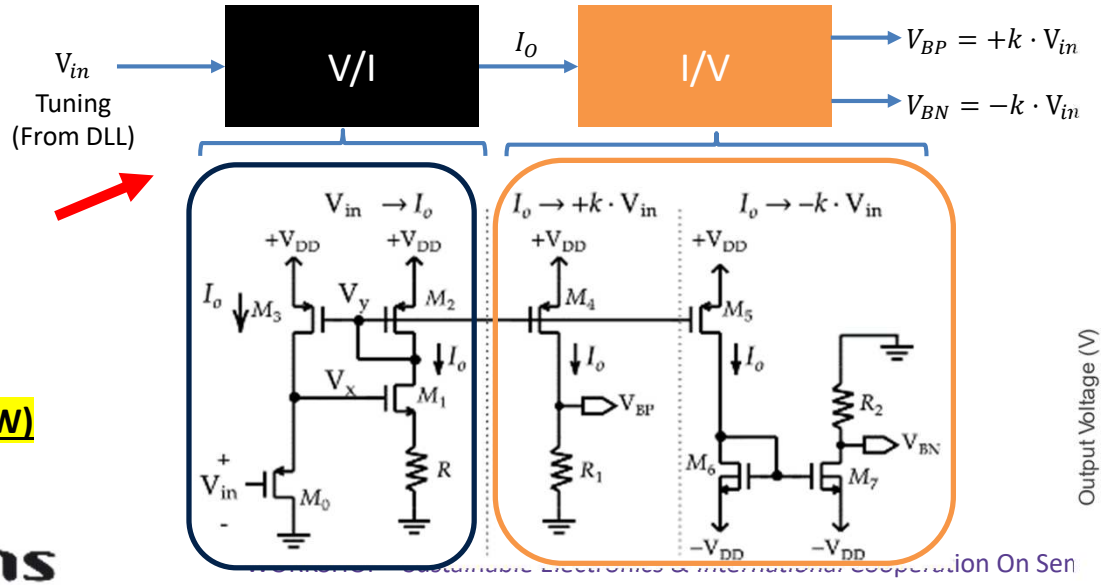
Novel and compact voltage generator design with high linearity and output range

- Used for providing complementary body voltages in 28 nm FDSOI circuits
- Applied in the frequency tune of a **body-biased ring VCO**
  - ✓ Keeping symmetrical rise and fall times ($t_{rise} \approx t_{fall}$)
  - ✓ Increasing tuning range
  - ✓ Improving the PVT Robustness
- Extended range of applications covered



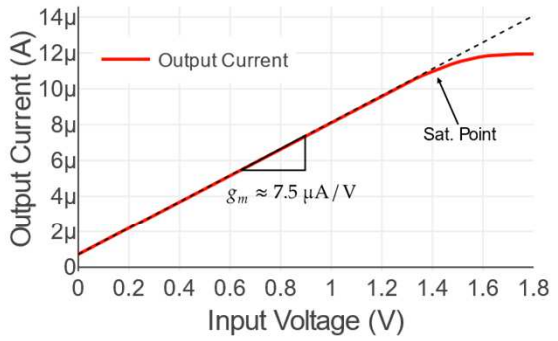


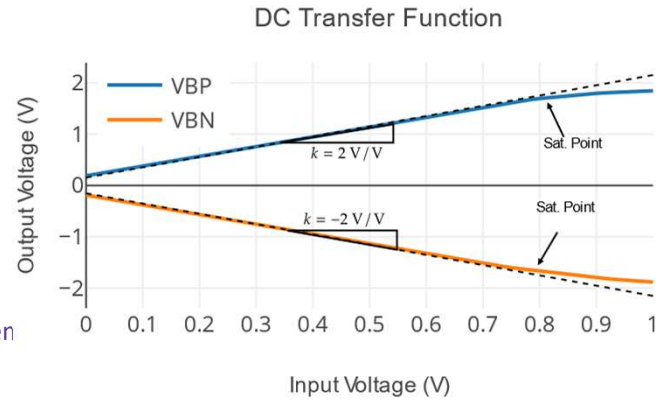
ULP RF for IoT enabler



Convert the input voltage to current, and then to voltage again

- ✓ Positive feedback (keeping stability)
- ✓ **Low power (34 µW)**

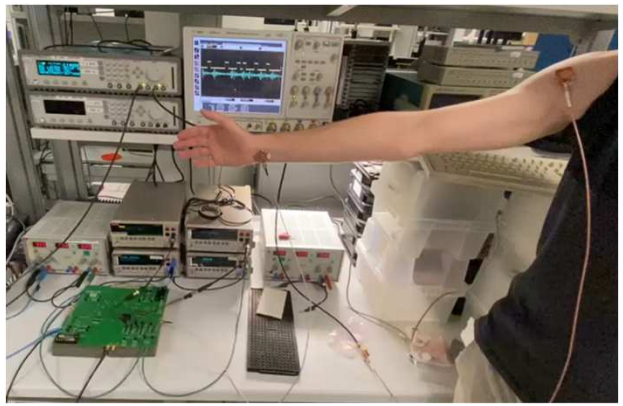


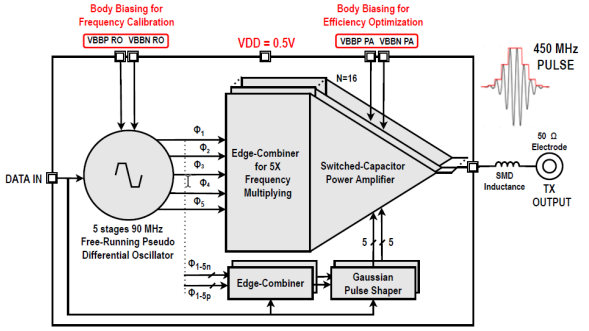


[A. Asprilla et al., LASCAS2022]

Ultra-Low Power Transmitter for The Human Intranet in 28 nm FD-SOI

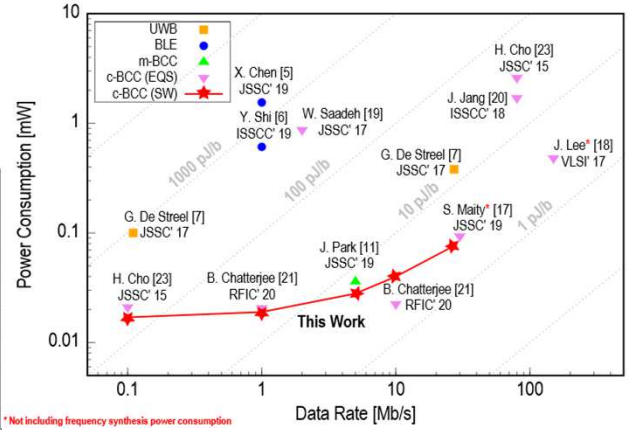
- Energy efficient transmitter to interconnect sensors and actuators on the human body. Medical and wellness IoT applications
- Capacitive **Body-Coupled Communication** in the 400-500 MHz band with dominant surface wave propagation
- **Highly duty-cycled** transmitter with pulse-based communication in 28 nm FD-SOI
  - Body-biasing optimization and calibration
    - FBB on power amplifier (+/- 2.2) V for improved power efficiency
    - FBB on ring oscillator for frequency tuning
  - Ultra-low voltage operation (0.5V)
  - Unlocked frequency reference
- **Energy efficient** TX at the state of the art
  - Flexible data rate (100kb/s to 27 Mb/s) with 17 to 76 µW power consumption (**170 to 2.8 pJ/b**)





	This Work		H. Cho [23] JSSC'15		J. Lee [18] VLSI' 17	W. Saadeh [19] JSSC' 17	J. Jang [20] JSSC' 19	S. Maity [17] JSSC'19	B. Chatterjee [21] RFIC' 20		J. Park [11] JSSC'19	G. De Streel [7] JSSC'17		X. Chen [5] JSSC' 19	Y. Shi [6] ISSCC' 19
Radio Technology	C-BCC (SW)		C-BCC (EQS)		C-BCC (EQS)	C-BCC (EQS)	C-BCC (EQS)	C-BCC (EQS)	C-BCC (EQS) IEEE 802.15.6		M-BCC	UWB IEEE 802.15.4a		BLE	BLE
Process Technology	28nm FD-SOI		65nm		65nm	65nm	65nm	65nm	65nm		65nm	28nm FD-SOI		40nm	65nm
Carrier Frequency [MHz]	350 - 550		13.56	20 - 60 140 - 180	Baseband <100MHz	20 - 120	20 - 60 100 - 180	Baseband <100MHz	22.27		40	3500 - 4500		2400	2400
Supply Voltage [V]	0.5		1.2	1	Not Reported	1.1	1	1	0.7		0.6	0.55		0.6	1.2
Data rate [Mb/s]	0.1	27	0.1	80	100	2	80	30	1	10	5	0.11	27	1	1
Modulation	OOK		OOK	BPSK	Decision Feedback Equalization	P-OFDM BPSK	QPSK BPSK	NRZ	OOK		OOK	BPM/BPSK		GFSK	GFSK
TX Power Consumption [µW]	17	76	21	2600	0.35*	870	1700	93*	20.6	22.4	37	100	380	490	610
TX Energy per bit [pJ/b]	170	2.8	210	32.5	3.5	435	22	3.1	20.6	2.24	7.2	950	14	490	610
Output Power [dBm]	-33.8	-19.7	Not Reported		Not Reported	Not Reported	Not Reported	Not Reported	Not Reported		-24.8	-20		-19	-8.4
TX System Efficiency [%]	2.44	14	Not Reported		Not Reported	Not Reported	Not Reported	Not Reported	Not Reported		17.8	2.6		2.6	23.6
Area [mm²]	0.0418		0.1672	5.76	0.00348	0.54	1.3	0.02	0.117		0.0204	0.095		0.0166	0.494

* Note : Not including frequency synthesis power consumption

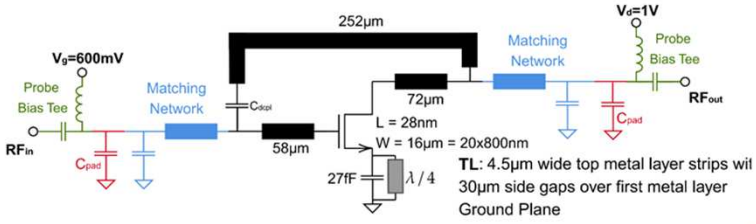


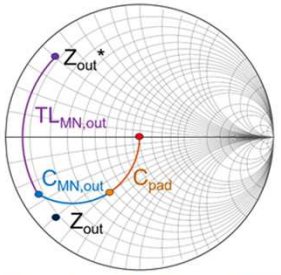
[G. Tochou et al., RFIC 2021 and JSSC, May 2022]

One stage gain boosted power driver at 184 GHz in 28 nm FD-SOI CMOS

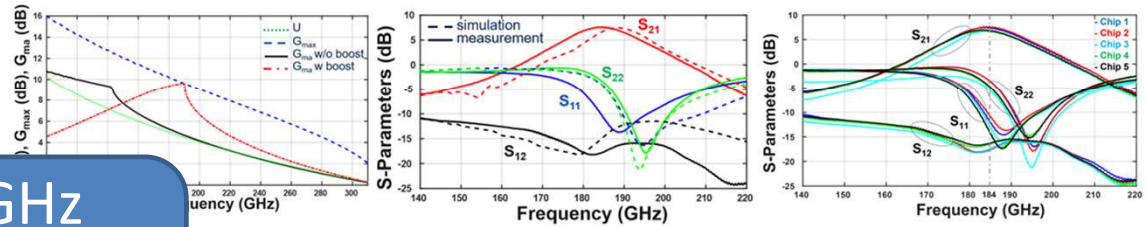
- Investigation for 28nm FD-SOI potential for next generations of standards (6G)
  - Carrier frequencies above 100GHz; High data rates
  - Power amplifier with positive feedback to enhance the limited available gain
- One stage amplifier with gain boosting embedding
  - Analytical methodology to design the required embedding
  - Meticulous layout and electromagnetic simulations of passive elements
- State of the art performances:
  - Best in class trade-off for gain/power consumption
  - For the same technology
    - 3.6dB extra gain
    - Power consumption reduced by 35%
  - Demonstration of mm-Wave/THz potentialities for 28nm FD-SOI technology

Towards 200GHz integration in FD-SOI





Output Impedance Matching at 190GHz



		f_{max} (GHz)	Operation Freq. (GHz)	Gain Boosting	Structure	Gain (dB)	Gain/Stage (dB)	P_{sat} (dBm)	BW (GHz)	peak PAE (%)	P_{DC}/Stage (mW)	FOM	Area (mm^2)
I		**390**	**184**	**Yes**	**1 CS**	**7.6**	**7.6**	**-3.7**	**20**	**4.2**	**5.1**	**1.30**	**0.12**
		280	173	Yes	3 CE	18.5	6.2	0.9	8.2	-	**14**	**1.65**	0.40
		280	183	Yes	1 Casc.	9.5	9.5	-2.8	8.5	-	**30**	**1.27**	0.16
		395	242	Yes	4 CS	13.9	3.48	-3.3	29.7	1.6	**6**	**0.85**	0.142
		352	257	Yes	4 CS	9.2	2.3	-3.9	12.2	0.8	**6.9**	**0.91**	0.14
	OS	395	247/272	Yes	2 CS	18/15	9/7.5	0.09/-2.36	5	4.4/2.4	**10.8**	**3.11/2.64**	0.28
[12]	65nm CMOS	395	280/300	Yes	3 CS	12/9	4/3	-4.7/-5.3	-	1.6/1.4	**6**	**1.26/1.15**	-
[13]	40nm CMOS	275	213	No	9 CS	10.5	1.17	-3.2	13	0.75	**4.7**	**0.79**	0.12
[14]	130nm SiGe	450	200	No	2 Casc.	17	8.5	-3.5	44	-	**9**	**1.40**	0.24
[4]	28nm FD-SOI	390	160	No	4 CS	15.7	3.93	1.3	23	-	**8**	**0.42**	0.34

*$FOM = \frac{\sqrt[n]{Gain}}{U(f)}$: where n is the number of stages and $U(f)$ is the unilateral power gain of the device at the frequency of operation.

[S. Sadlo et al., RFIC 2021]

AI – FDSOI
(and we did not ask ChatGPT!)

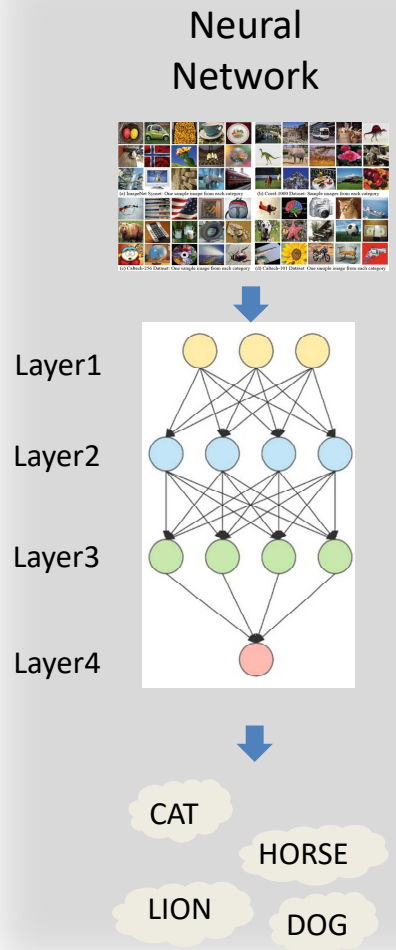
AI computing at the edge

Edge AI poses significant restrictions:

- Amount of on-chip storage (for activations, and weights)
- Die size (cost)
- Energy consumption (e.g. for battery operation)

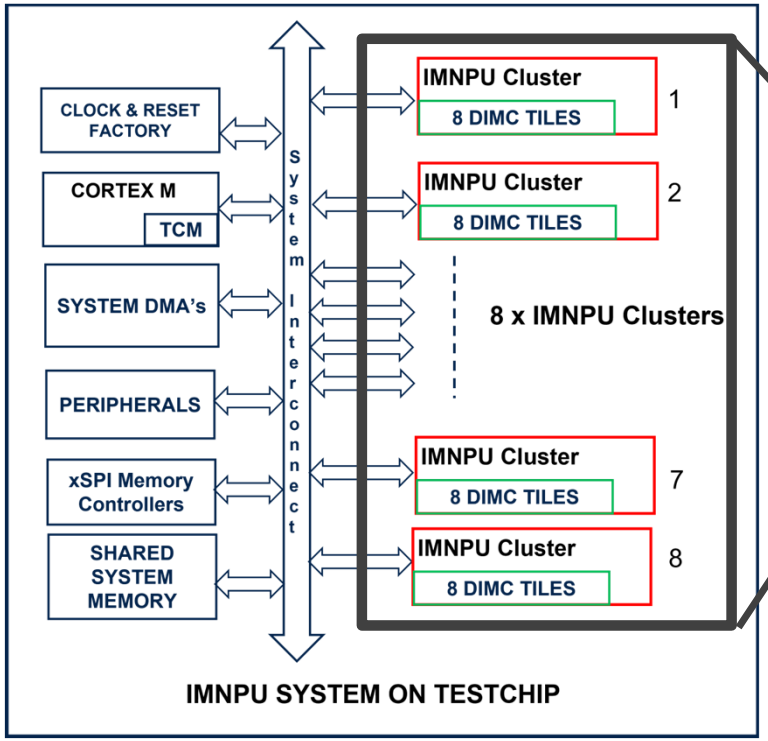
What we are looking for:

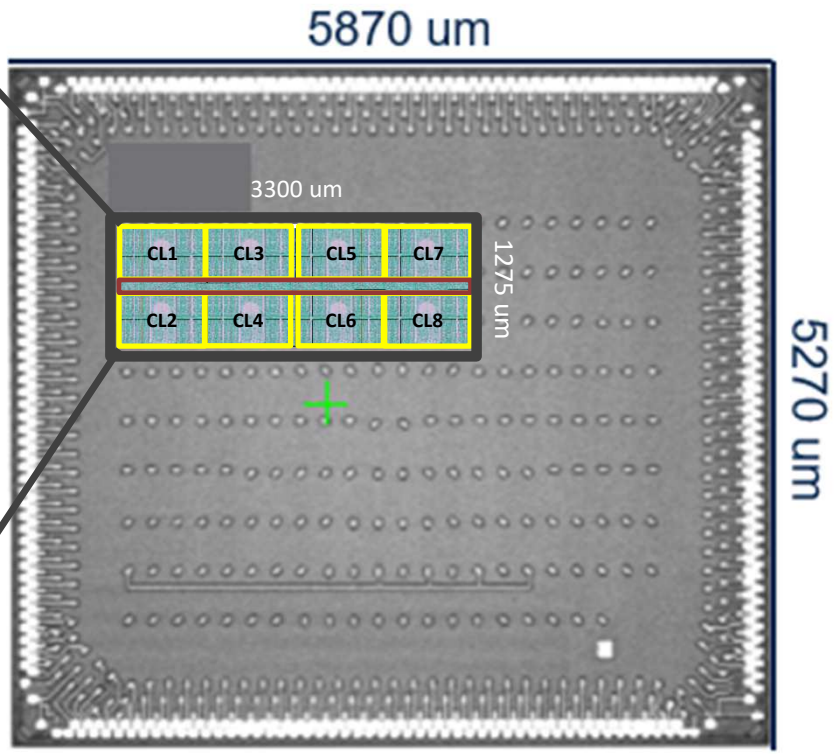
- Ease of reconfigurability/programmability
  (to support for different types of networks and products)
- Computation at reduced precision to save cost and power
  (neural networks often work well with reduced)
- Processing performance in the TOPs range.
- High efficiency in terms of TOPs/Watt and TOPs/mm2



Desoli et al., ISSCC 2023

IMNPU integration in 18nm FDSOI





CL : IMNPU Cluster

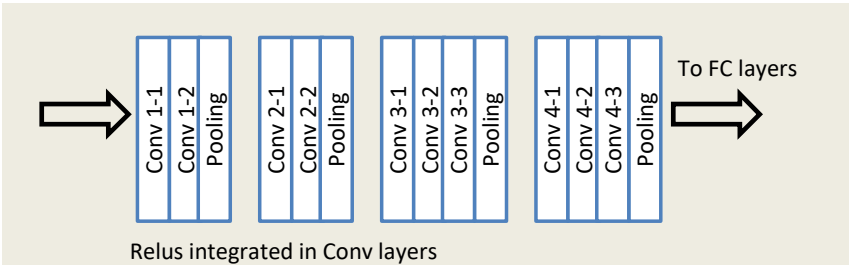
Technology 18nm FDSOI
Multi-Cluster NPU along with system interconnect: **4.2 mm2**
Voltage range: 0.525-1.0V, FBB 0-1.5V
Precision Mode:1-4 bits
229 TOPS(Peak Performance) 1bit Weight-1bit Feature **57 TOPS(Peak Performance)** 4bit Weight-4bit Feature
310 TOPS/W(1 bit) **77 TOPS/W(4 bit)**
54 TOPS/mm2(1 bit) **13.6 TOPS/mm2(4 bit)**

Desoli et al., ISSCC 2023

Real world performance evaluation

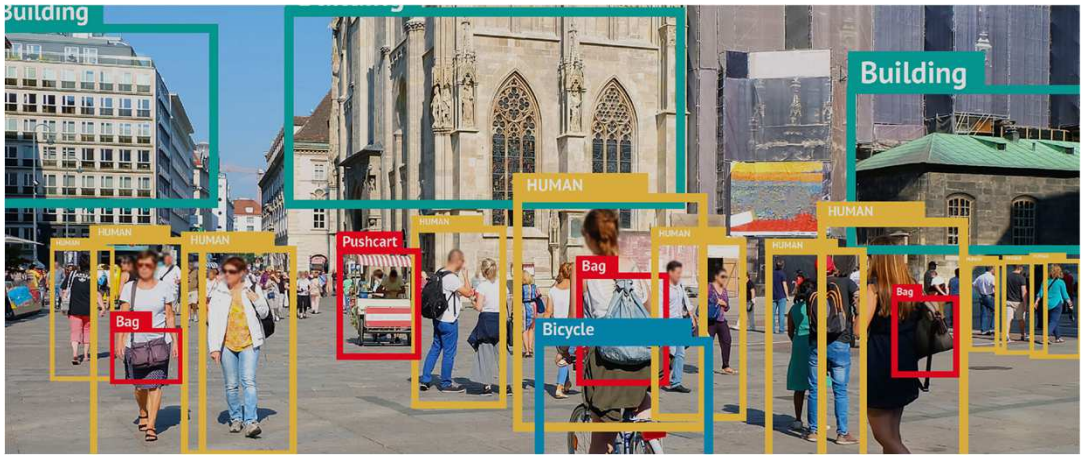
Object detection with VGG16

(scaled down version @ 112x112 pixel resolution)



Measured at 0.525V and 600MHz with 1.5v FBB

configuration	# of MACS	# of cycles/inf	Inf/sec	TOPS/W
1 cluster	8.15E+08	602513	996	46.8
max clusters		87719	6840	



Example: always on inference running on a dynamic partition**

Very slow system frequency for battery powered always-on applications

~1.6 GOPs/inf image object detection @ 10FPS -> 300-350uW @ 6 MHz + I/O power + Camera sensor (e.g. Sensor consumption: 200-300uW*) -> 1-1.5 years on 2 AA batteries

Desoli et al., ISSCC 2023

* e.g. https://www.himax.com.tw/products/cmos-image-sensor/always-on-vision-sensors/hm01b0/

** Assumption: with embedded ePCM for weights

AI in FDSOI – Take-away

- **AI applications in edge devices require a specific focus on cost and energy efficiency.**
- A dataflow orient architecture has been used to integrate DIMC tiles into a Neural processing Unit (NPU).
- Our 18nm FDSOI SoC integration demonstrates the potential of in-memory computing tiles integrated in a NPU architecture for AI processing in edge devices.

System	NVIDEA Titan X	ST ORLANDO	ST STM32N6	This work 4-bit mode	This work 1-bit mode
Technology	16FF	28nm FDSOI	16FF	18nm FDSOI	18nm FDSOI
Calc precision	floating point single precision	16-bit signed fixed point	8-bit signed fixed point/ integer scale offset	4-bit signed, fixed point	1-bit
Power efficiency	0.0439 FLOPS/W	2.9 TOPS/W	up to 5 TOPS/W	**77 TOPS/W**	**310 TOPS/W**
Peak calculation density	0.023 FLOPS/mm^2	0.188 TOPS/mm^2	0.72 TOPS/mm^2	**13.6 TOPS/mm^2**	**54 TOPS/mm^2**

Desoli et al., ISSCC 2023

FDSOI Augmented platform – take aways

- Augmented FDSOI platform enable ST and his partner to address multiple domain of today semiconductor applications
- Versatile, with the extra knob brought by the *fourth terminal*, enable extremely low-power application, to implement **sustainable and eco-friendly devices**
- Simple, hence highly manufacturable technologies, enabling a wide range of scalable applications
- FDSOI derivative embedded-non-volatile and RF evolutions offers ST and his partners an **economically sustainable** roadmap

Aknowledgements

- The authors would like to warmly thanks all ST colleagues who contributed to the development of FDSOI, his derivative technologies solutions and the numerous R&D and commercial implementations from Crolles, Agrate, Grenoble, Rousset, Greater Noida,… ST premises without whom many of these foils wouldn’t have been materialized
- Special thanks to ST Fellows Franck Arnaud, Andreia Cathelin, Andrea Redaelli, Nitin Chawla, Giuseppe Desoli
- A last word for our partners from CEA-LETI in Grenoble for their instrumental contribution to the FDSOI birth and growth

ICOS International Cooperation On Semiconductors

SiNANO Institute

IRDS International Roadmap for Devices and Systems

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