The path to large scale quantum computing based on CMOS technology

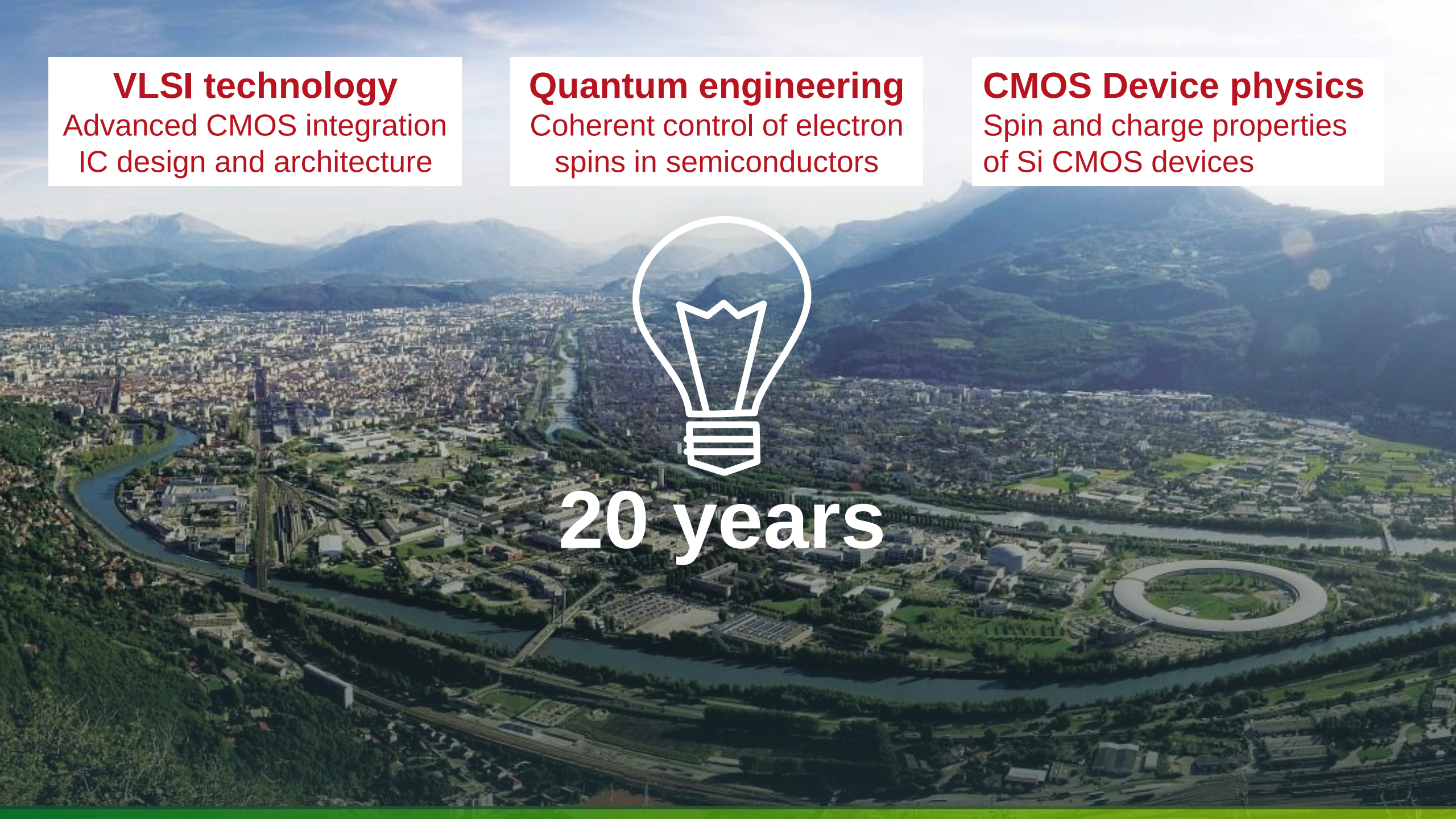
Maud Vinet, CEO

Siquance

VLSI technology
Advanced CMOS integration
IC design and architecture

Quantum engineering
Coherent control of electron spins in semiconductors

CMOS Device physics
Spin and charge properties of Si CMOS devices



20 years

Quantum computing value creation is huge

> US$ 800B in more than 10 years [1]

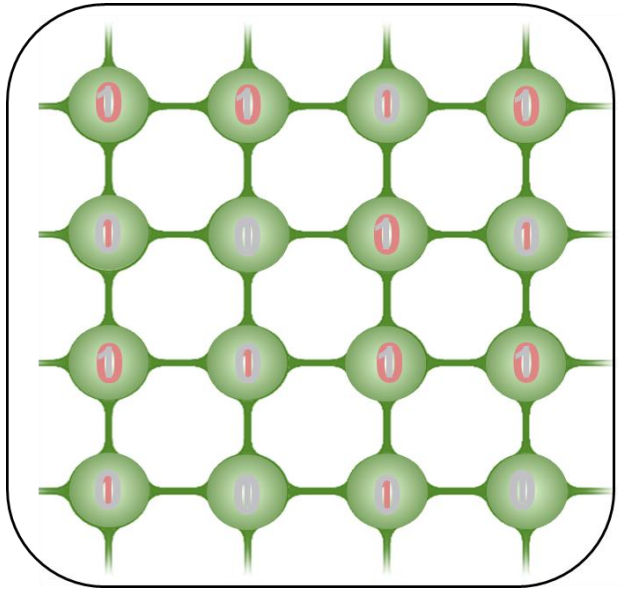
1 Based on data taken from Langione et al., "Where Will Quantum computers Create Value and When?" Boston Consulting Group, May 2019. 2 Hazan et al., "The Next Tech Revolution: Quantum Computing." McKinsey & Company, March 2020. What Happens When 'If' Turns to 'When' in Quantum Computing? Jean-François Bobier, Matt Langione, Edward Tao, and Antoine Gourévitch, July 2021

Living with errors

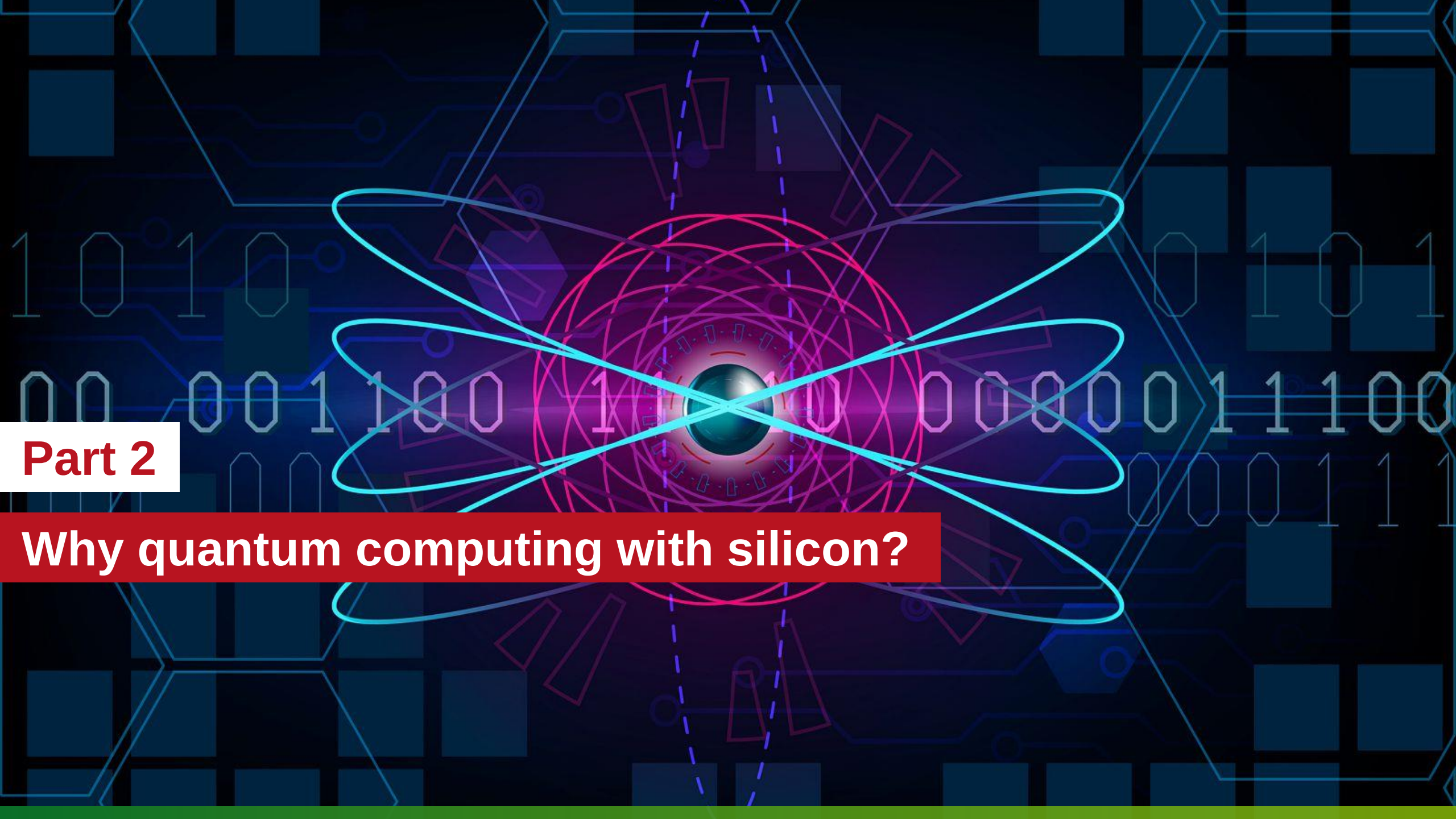
› **Millions of errorless operations**

Quantum Error Correction protocols

› More than **100 000** of physical qubits in 2D arrays



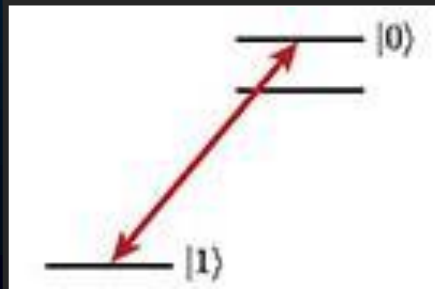
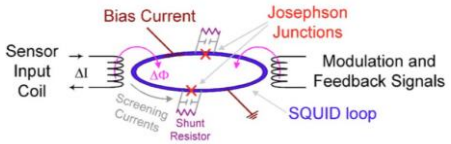
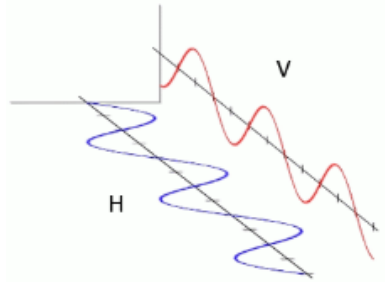
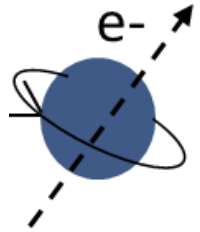
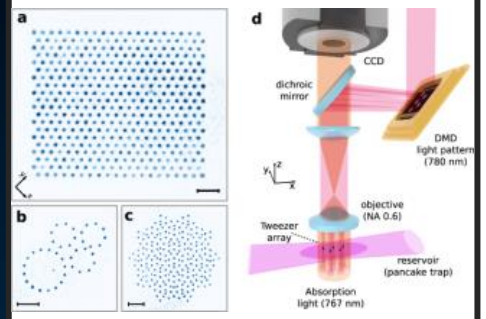
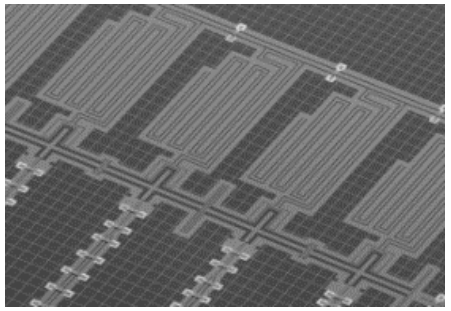
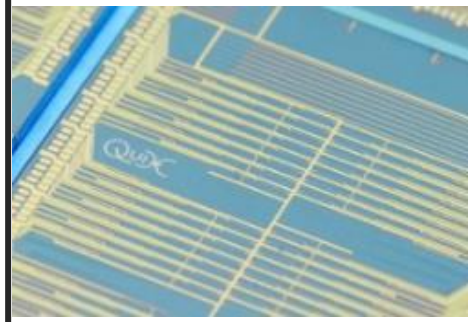
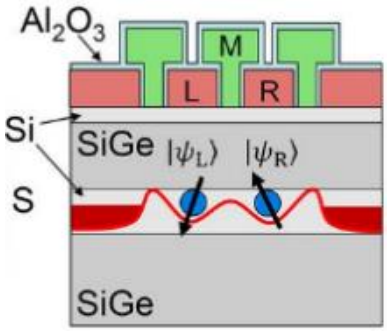
1 errorless logical qubit
> 1000 physical qubits



Part 2

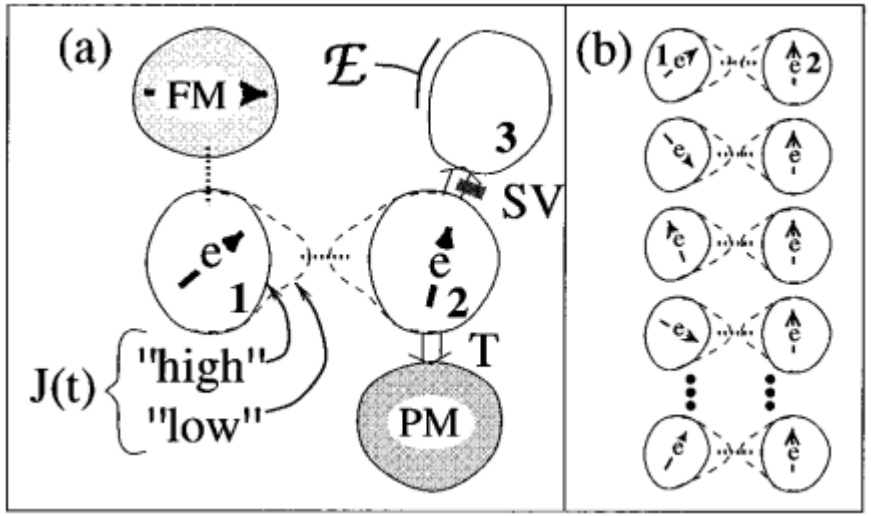
Why quantum computing with silicon?

Many qubits experimental platforms

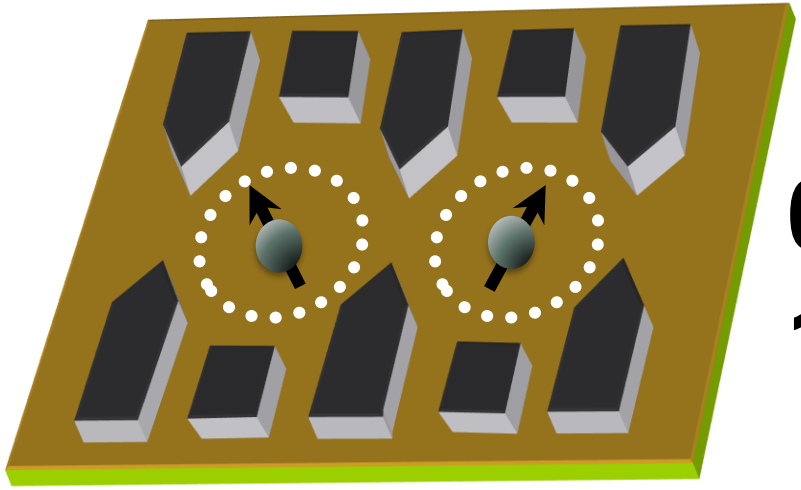
	atom	superconductors	photons	Si qubits
				
Quantum information	Atomic energy level	Phase or energy in a current loop	Photon polarisation (or other properties)	Spin degree of freedom of a charge
Physical aspect				

Silicon spin qubits

› **1998 theoritical concept**



Loss, D. and DiVincenzo, D. Quantum computation with quantum dots, Phys. Rev. A 57, 120 (1998)



$0 \rightarrow |\uparrow\rangle$

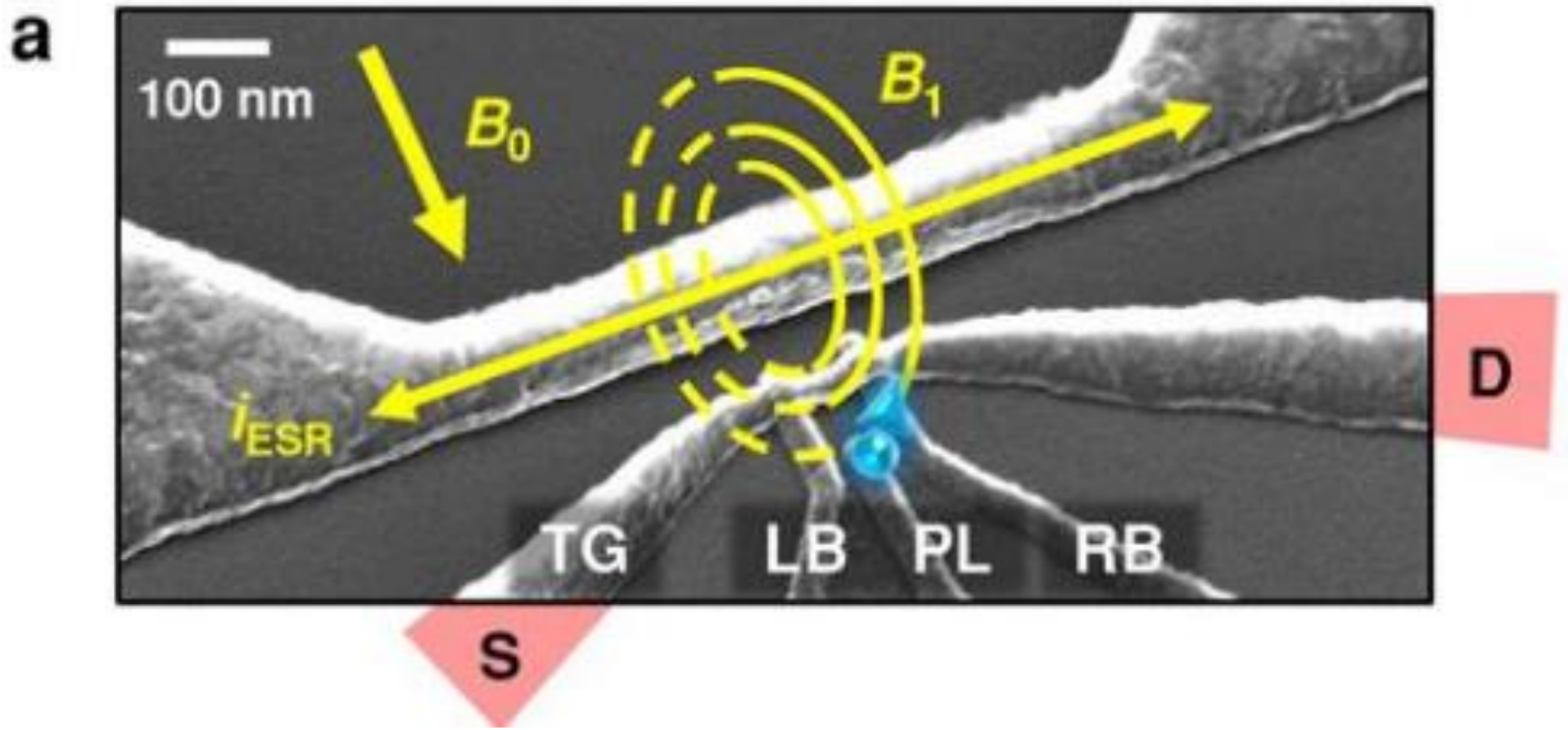
$1 \rightarrow |\downarrow\rangle$

Spin degree of freedom of an electron

Gate defined quantum dots

Silicon spin qubits

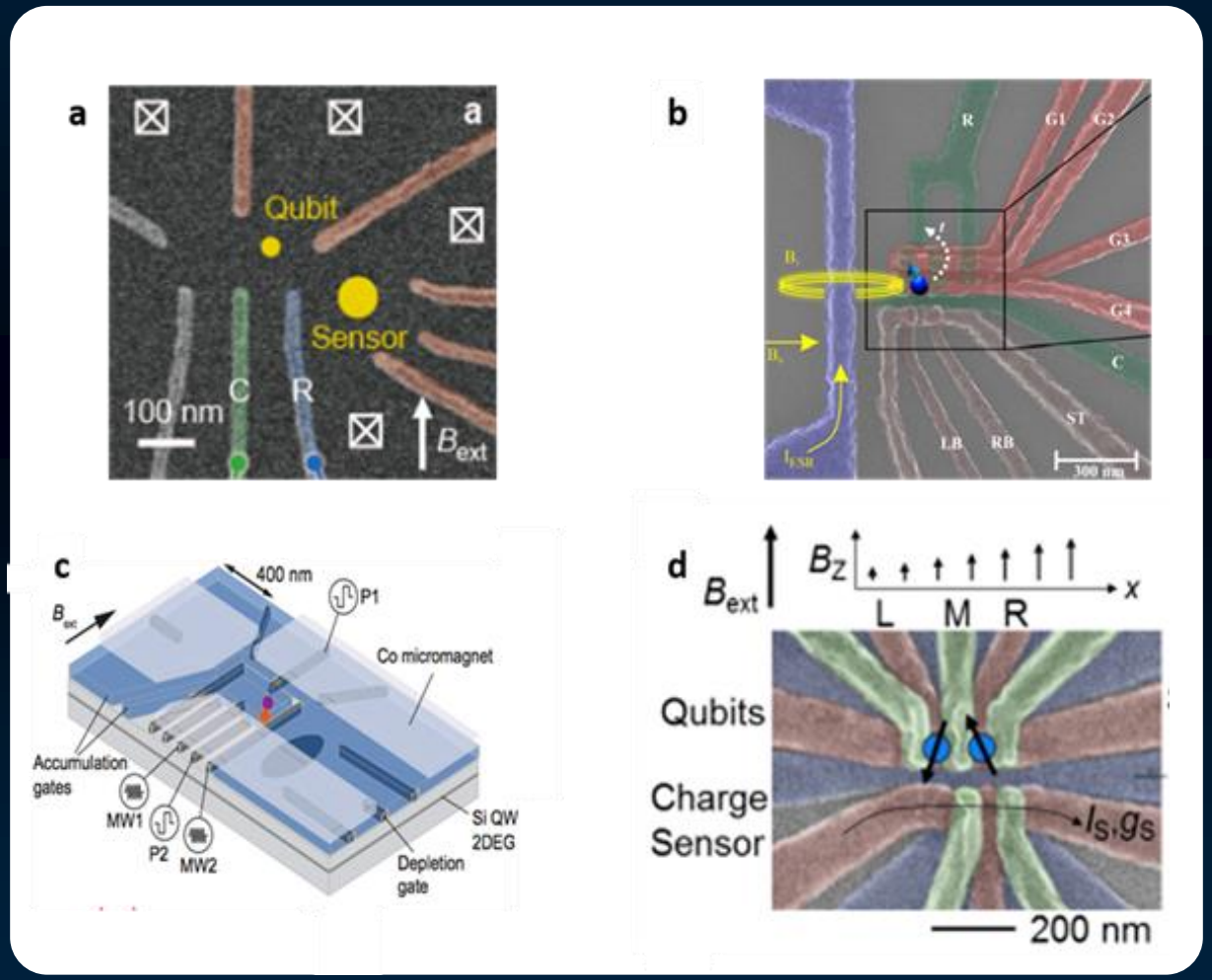
› **2012: first experimental demonstration**



Pla, J., Tan, K., Dehollain, J. et al. A single-atom electron spin qubit in([silicon. Nature 489, 541–545 (2012).

Early academics demonstrations

› **Many gates planar designs**



Si MOS
SiGe/Se

› *RIKEN (a) UNSW (b) Delft (c) and Princetown (d)*

Figures of merit – State of the art

Size*
1qubit fidelity
2qubit fidelity
Speed**
Variability
T° of operation
Entangled qubits

* Estimation taking into account all the quantum functionalities (read out, control and initialization)
** Speed of the limiting operation between read out and measurement

Figures of merit – State of the art

	Superconductor	Si spin qubit	Trapped ion	Photon
Size*	(100μm)²	(100nm)²	(1mm)²	~(100μm)²
1qubit fidelity	99.96%	99.93%	99.98%	
2qubit fidelity	~99.3%	>99%	99.9%	50% (measurement) 98% (gates)
Speed**	12-400 ns	~1 μs	100 μs	1 ms
Variability	3%	0.1%-0.5%	0.01%	0.5%
T° of operation	15mK	1K	10K	4K/10K
Entangled qubits	433 (IBM)	3 (TU) (6 - QuTech)	32 (IonQ)	70 (Pan-China)

* Estimation taking into account all the quantum functionalities (read out, control and initialization)
** Speed of the limiting operation between read out and measurement

Figures of merit – State of the art

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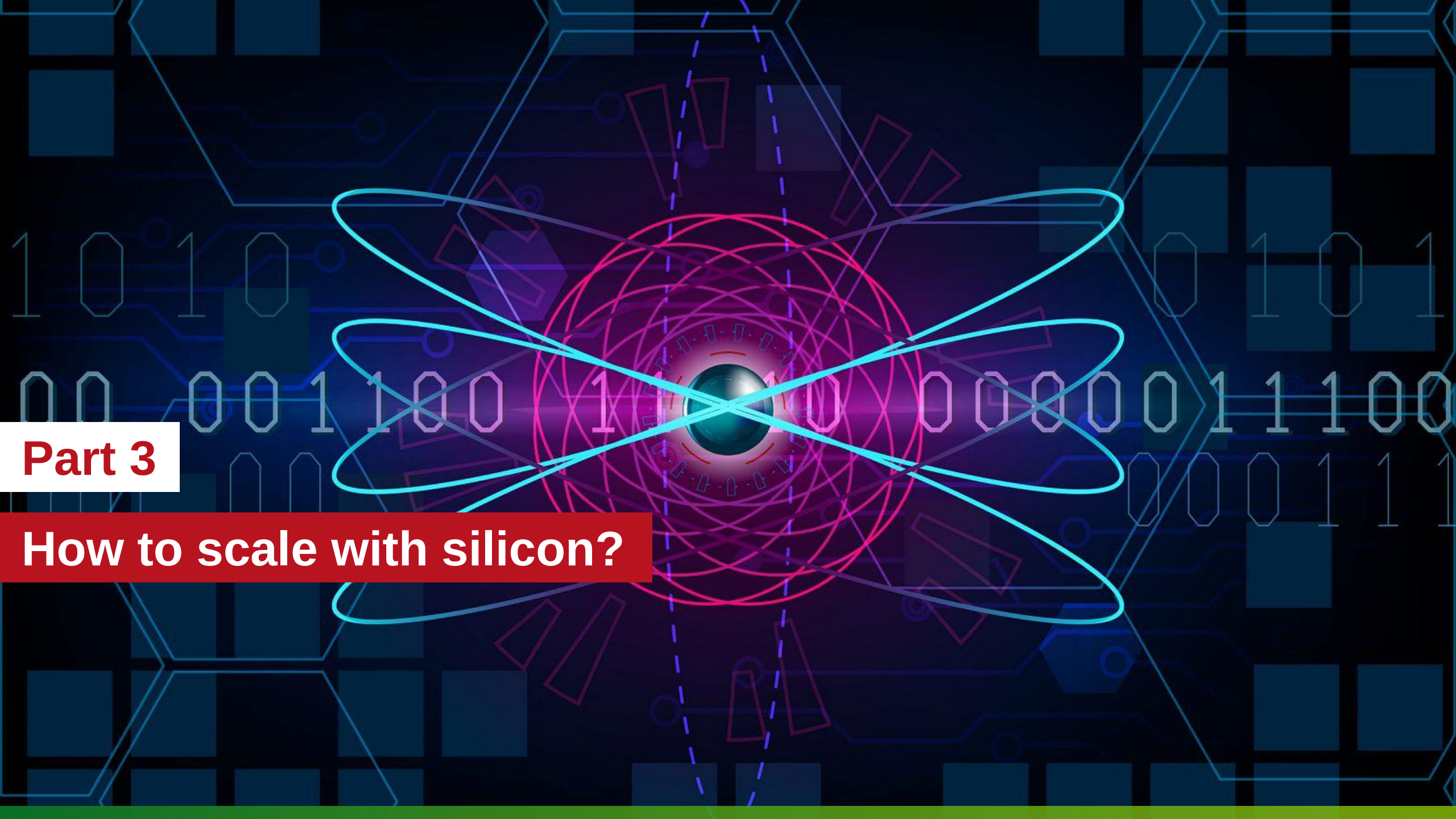
✓**Size**
up to 100 000 per mm²

✓**Quality**
above error correction threshold

✓**Speed**
1s for millions of operations - compatible with competitive run time

Silicon is a very promising candidate for scaling

* Estimation taking into account all the quantum functionalities (read out, control and initialization)
** Speed of the limiting operation between read out and measurement



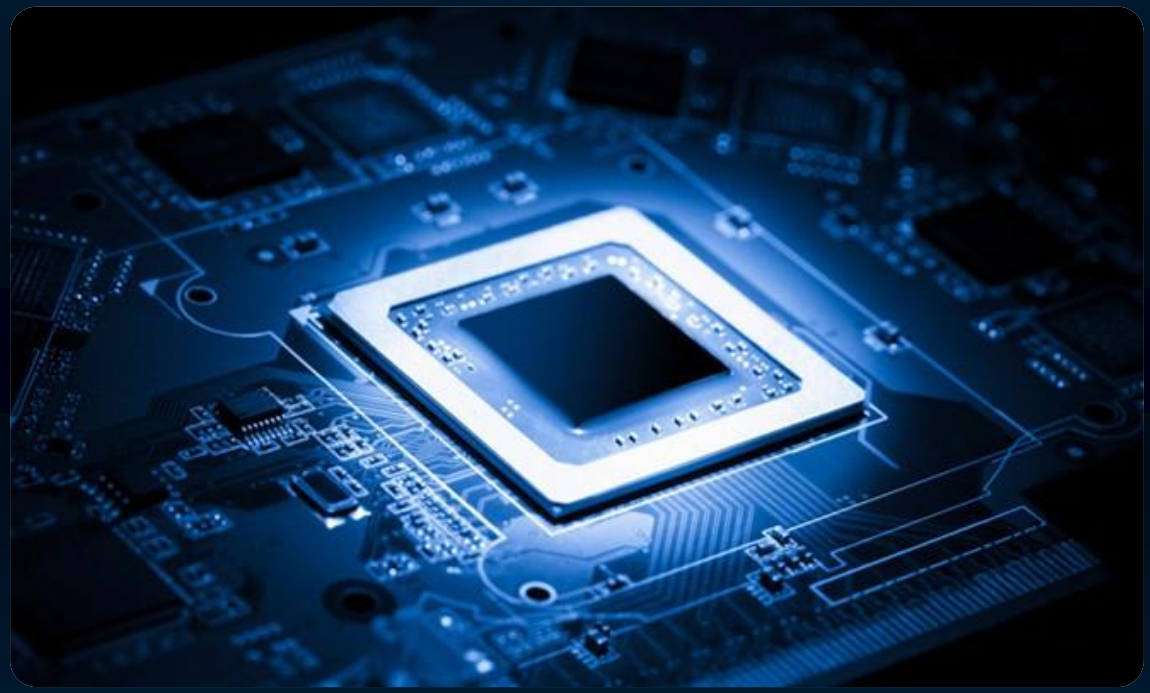
Part 3

How to scale with silicon?

Semiconductor industry power

Potential to fabricate billions of devices

Integrated circuits



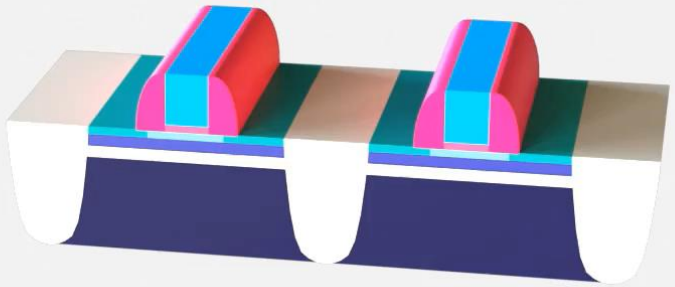
Potential to efficiently control and program millions of qubits

Fastest path to leverage semiconductor industry potential

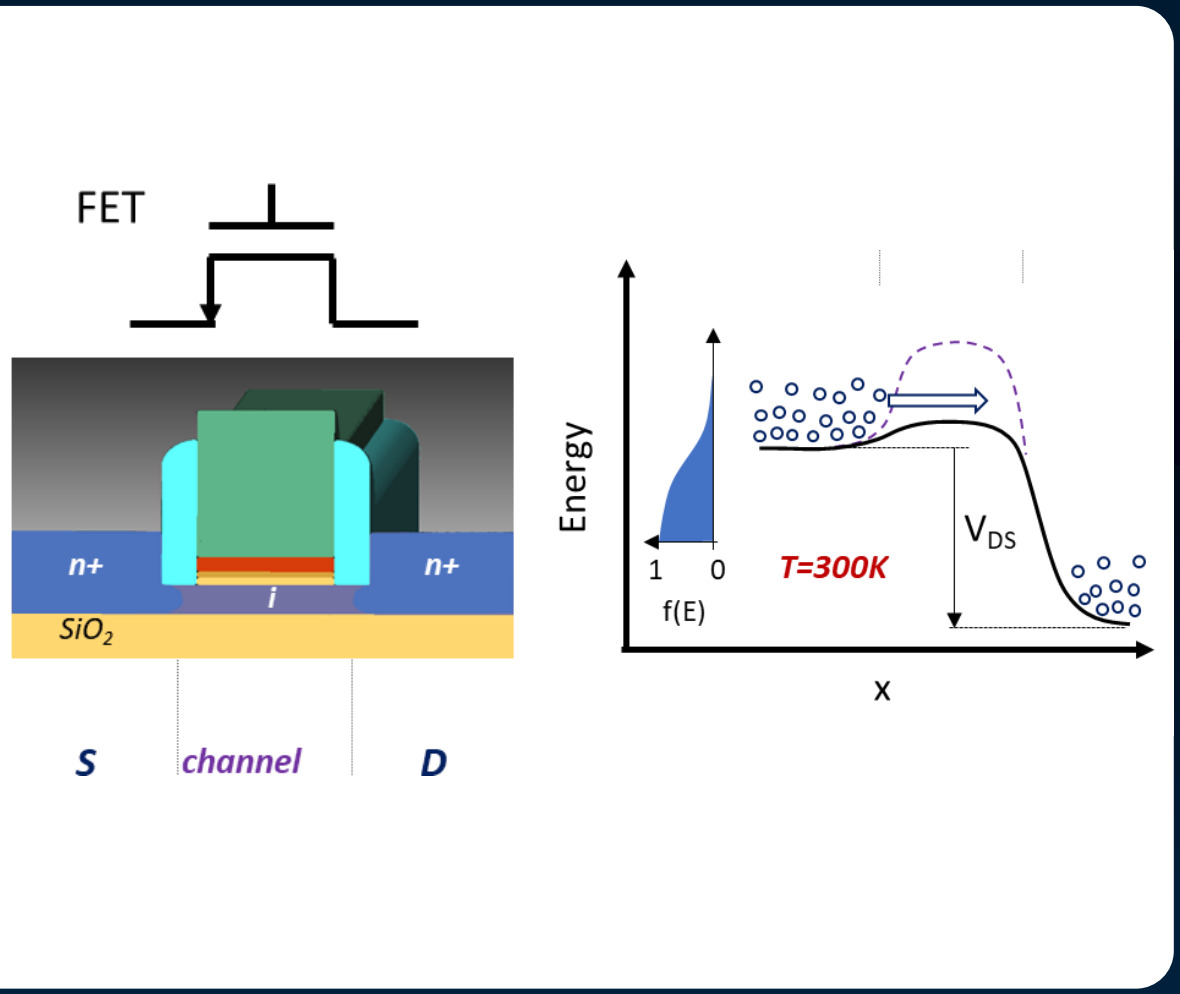
- **Transform a transistor into a good qubit**

Fastest path to leverage semiconductor industry potential

› **Transform a transistor into a good qubit**



Silicon spin qubits, from transistors…



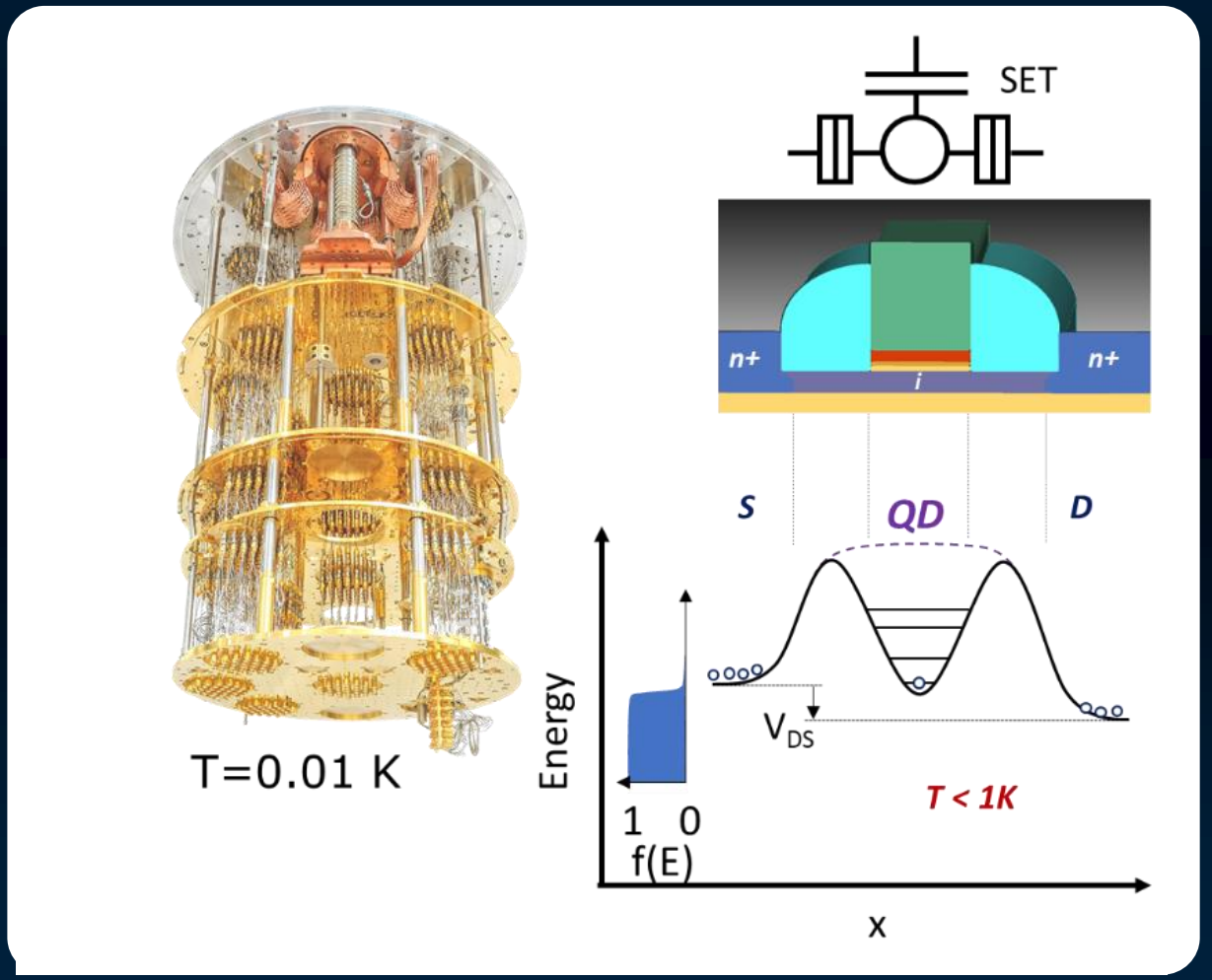
At room temperature:

- Carriers have significant thermal energy
- Diffusion over the S/channel barrier when VG is turned ON
- Continuous flow of carriers accelerated by large VDS

…To quantum dots

At low temperature:

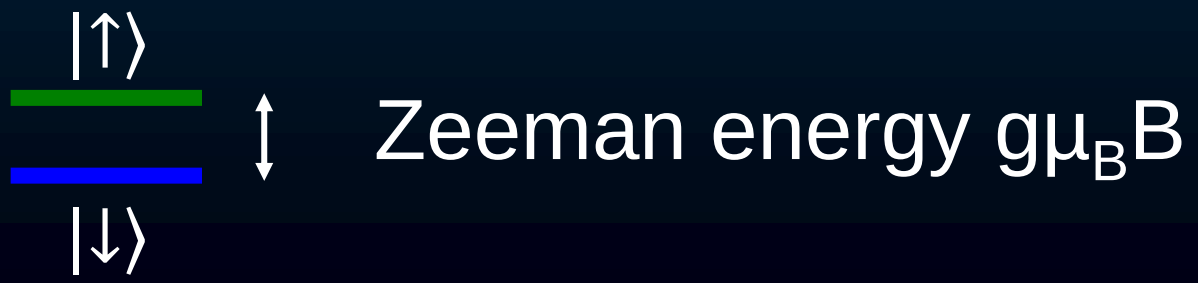
- Formation of a well between two barriers
- Carriers have no thermal energy and have to tunnel through
- Energy states are quantized in the well
- Small VDS to scan precisely the resolved quantum states



And to qubits

› **Utilize magnetic field to lift degeneracy between spin up and spin down**

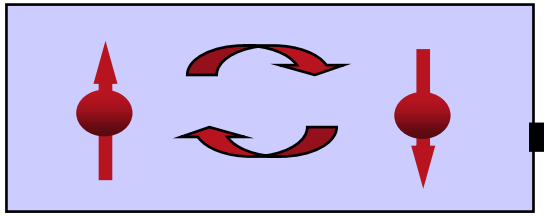
Static magnetic field B,
two-level spin qubit

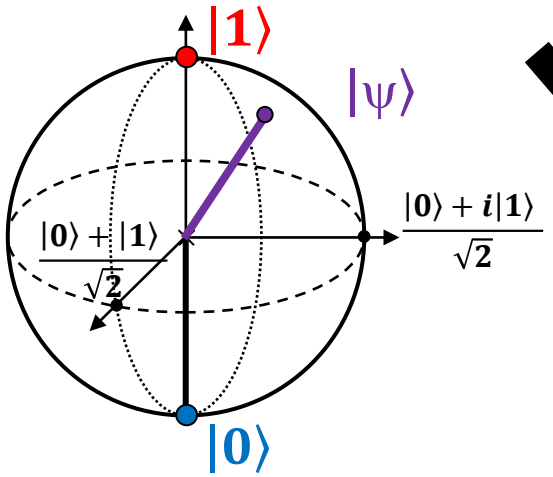


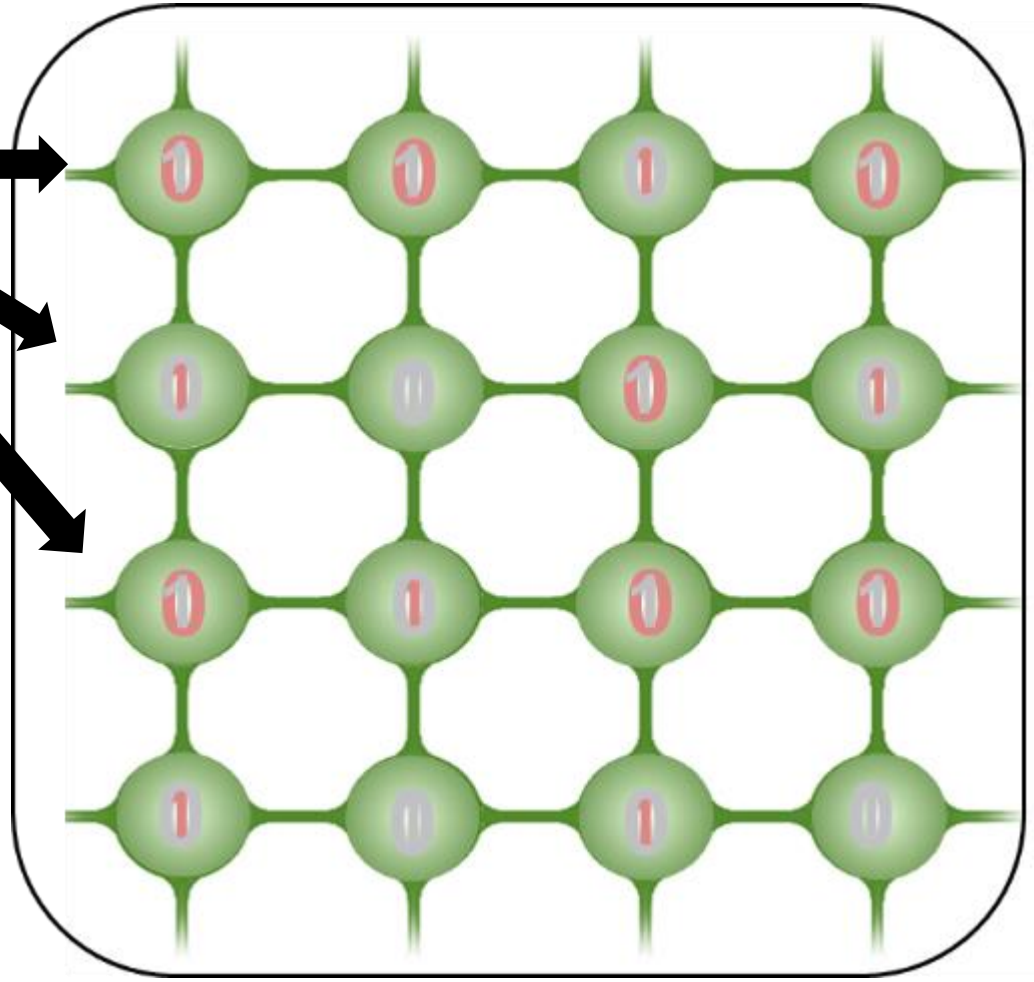
What is needed to implement algorithms now?

› Basic operations

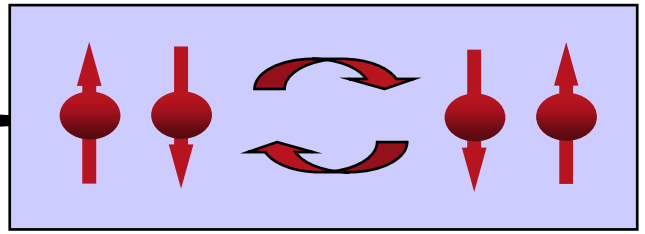
One-qubit gate



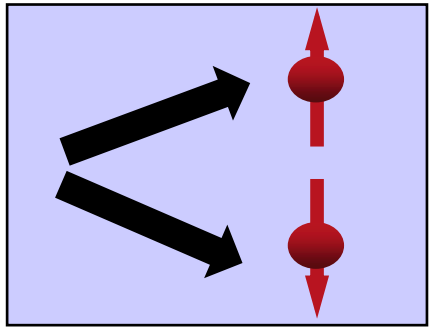




Two-qubit gate

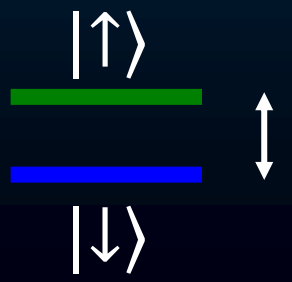


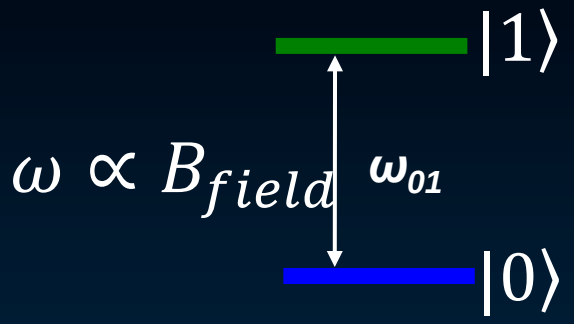
Read-out gate

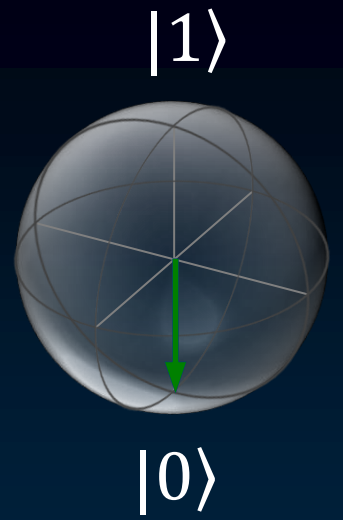


Single qubit gate, single qubit rotation

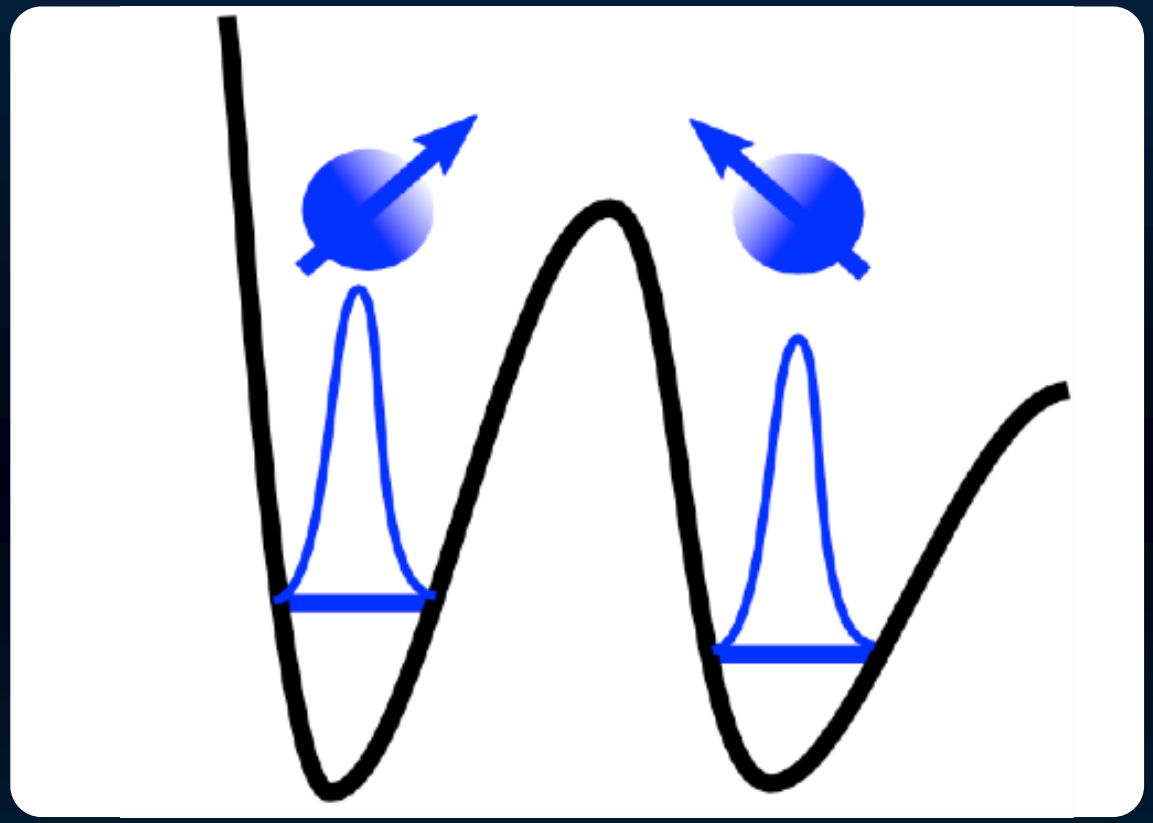
Static magnetic field B,
two-level spin qubit:

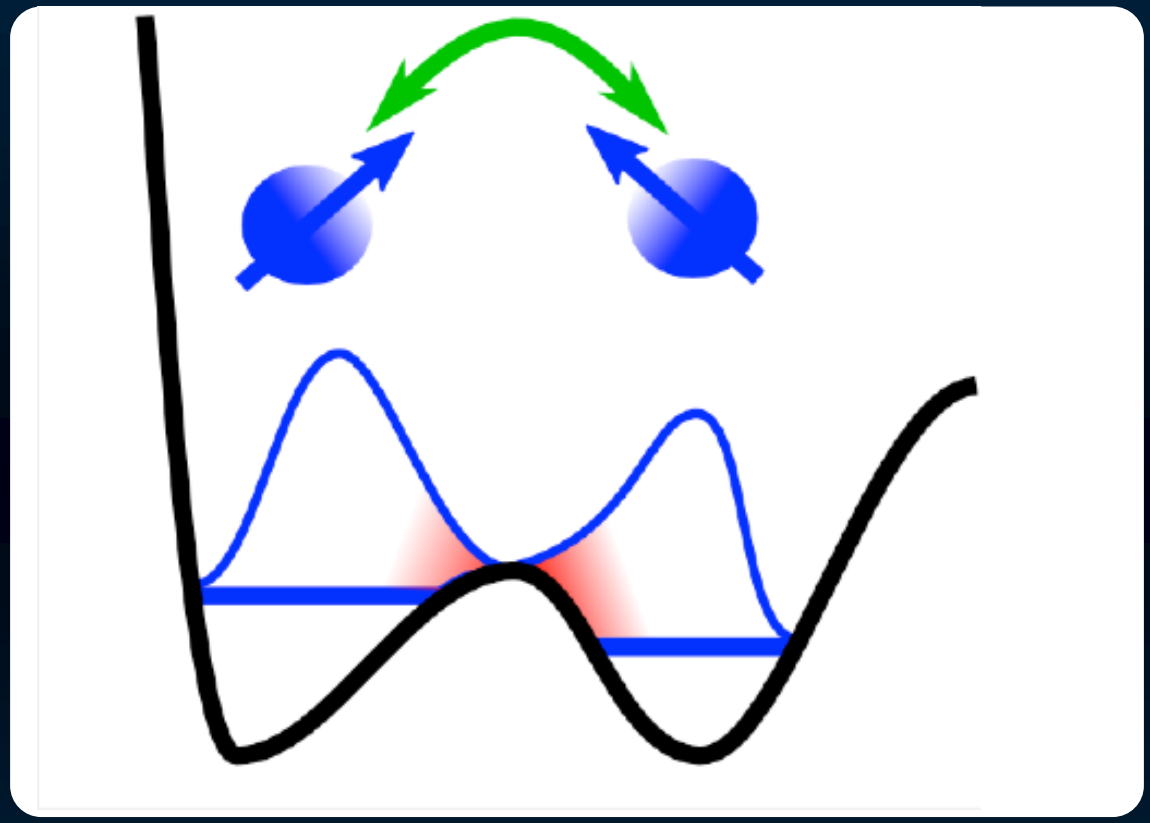






Two qubit gates by tunnel barrier lowering between adjacent dots

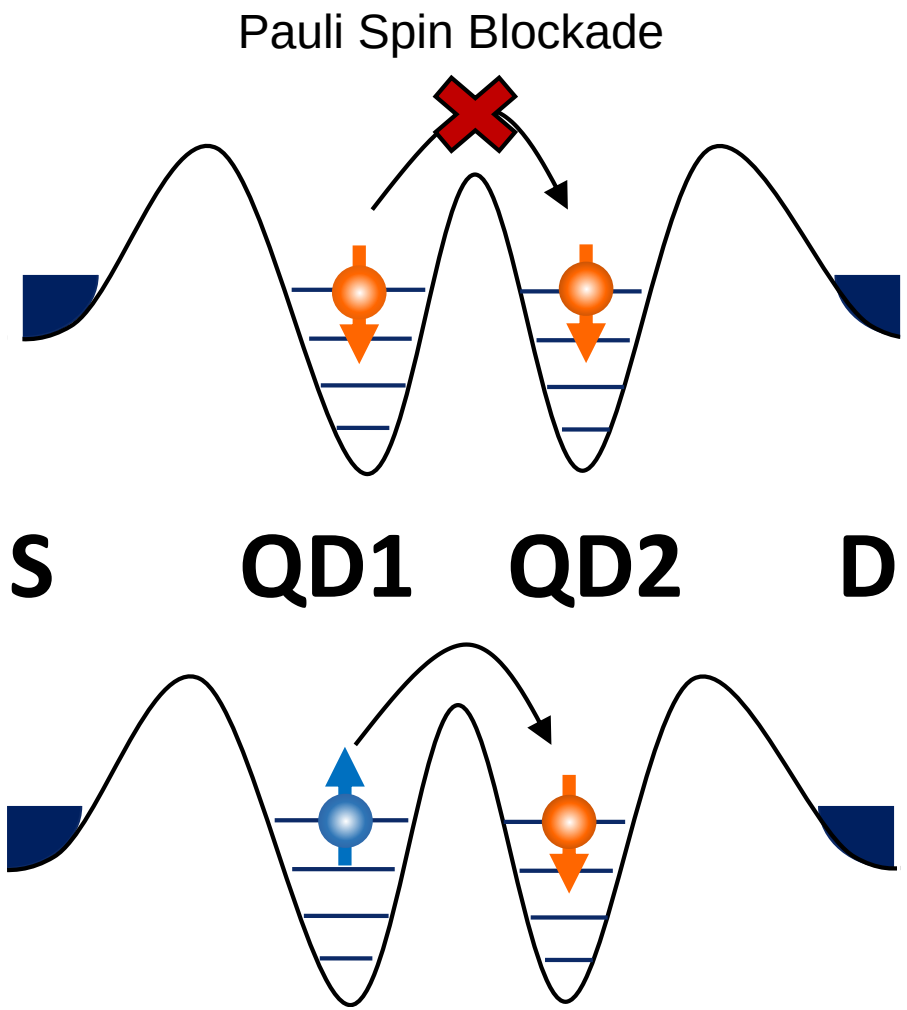


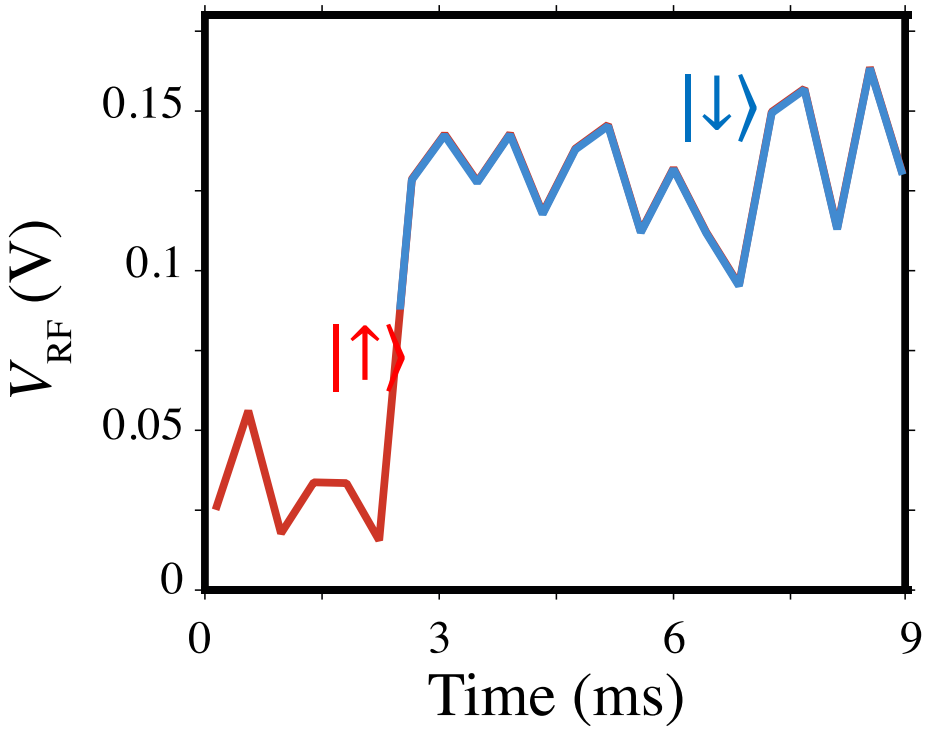


Spin exchange interaction

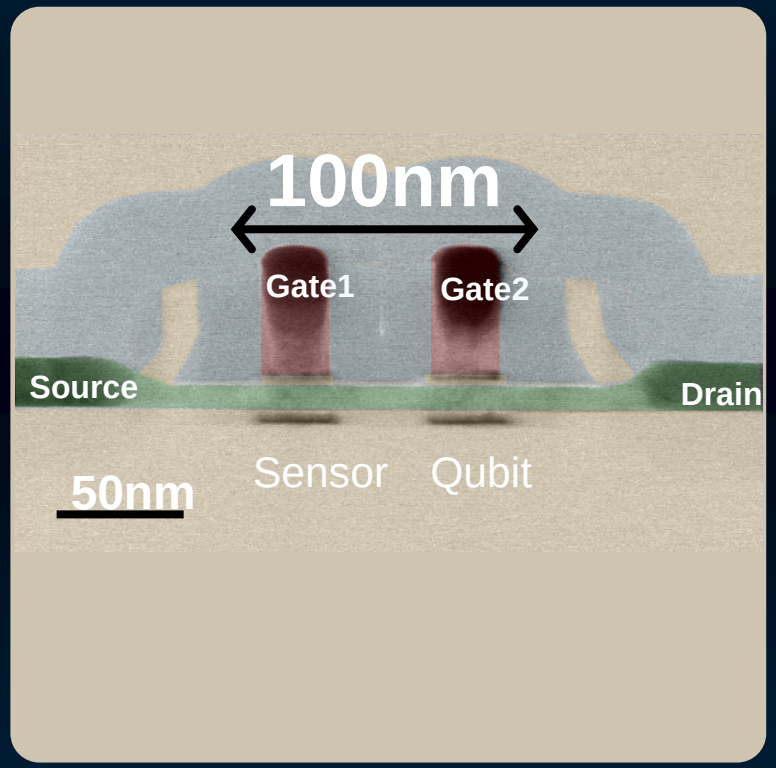
How to read out the value of the spin?

› Spin to charge conversion

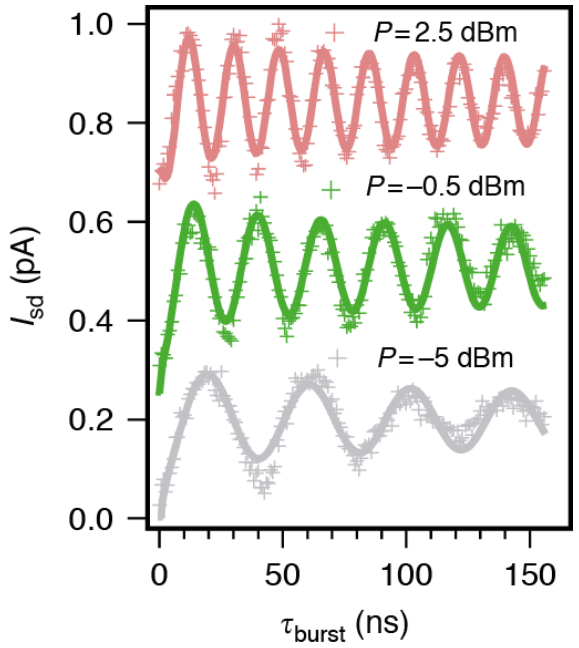




2016 first transistor derived into a qubit



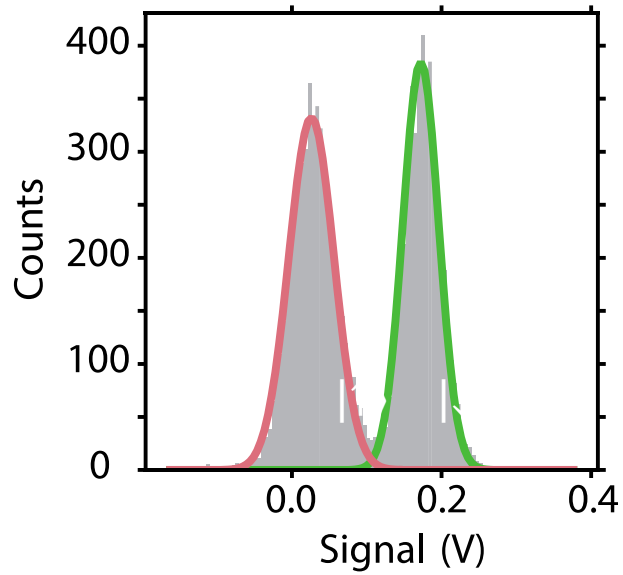
Single qubit gate



Manipulation time 20ns

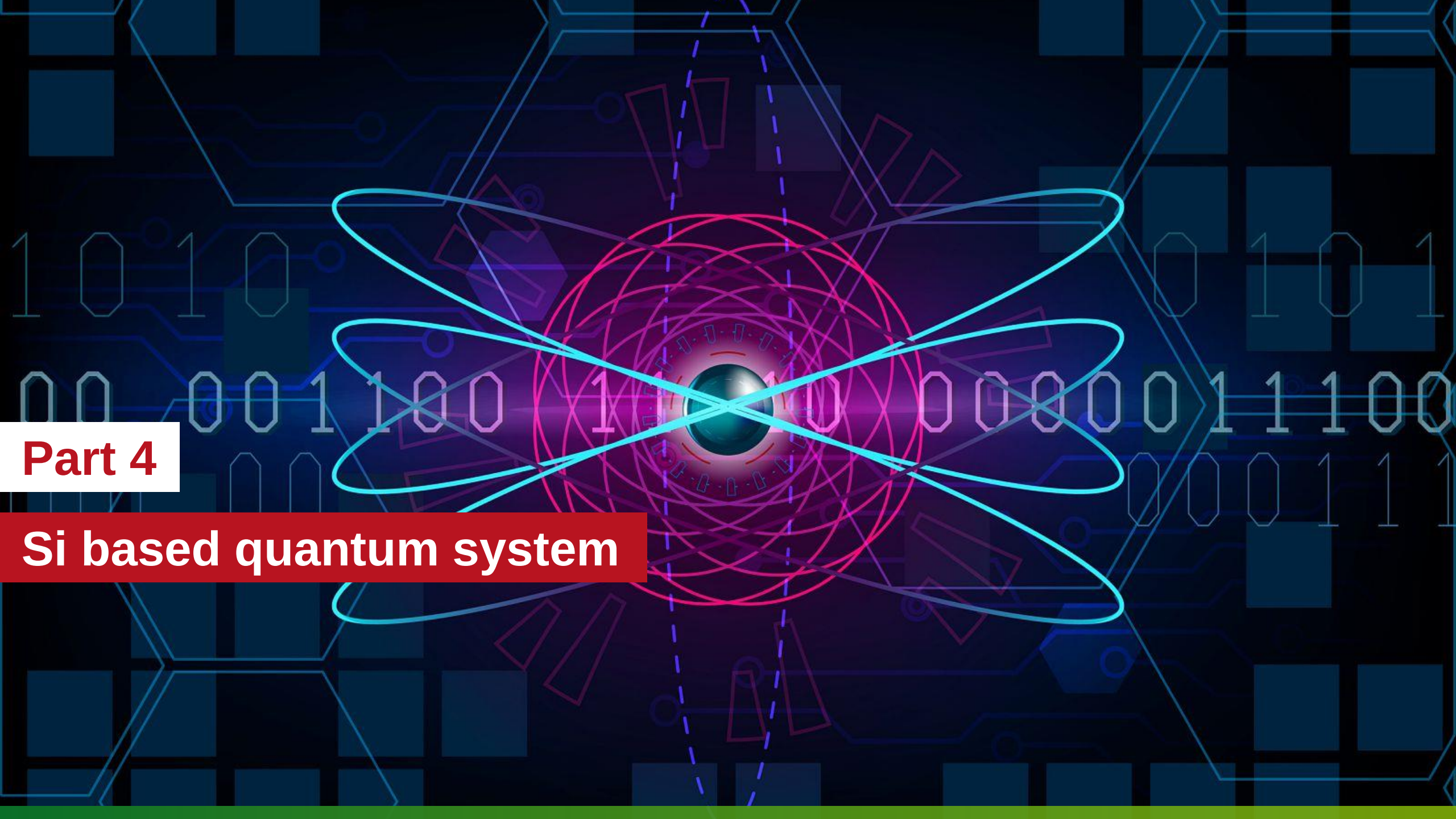
R. Maurand, Nat. Comm. (2016)

High fidelity RF scalable spin read-out



Fidelity > 99%

M. Urdampilleta, Nat .Nanotech (2019)



Part 4

Si based quantum system

Silicon based quantum computer

Cryo control electronics

- Low power fast electronics

Cryo wires and connectors

- Need customized solutions.

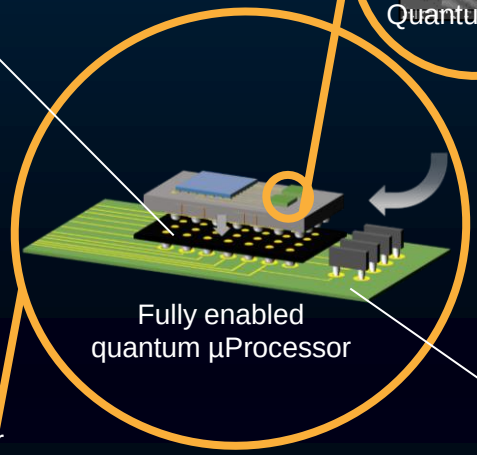
Cryostats

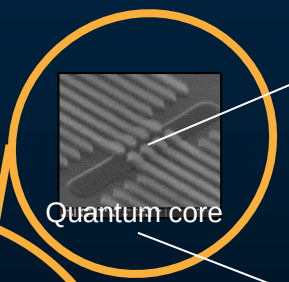
- High power ~1W @ 1K

Room T° electronics

- AWG

Firmware layer





Substrates

Device Technology

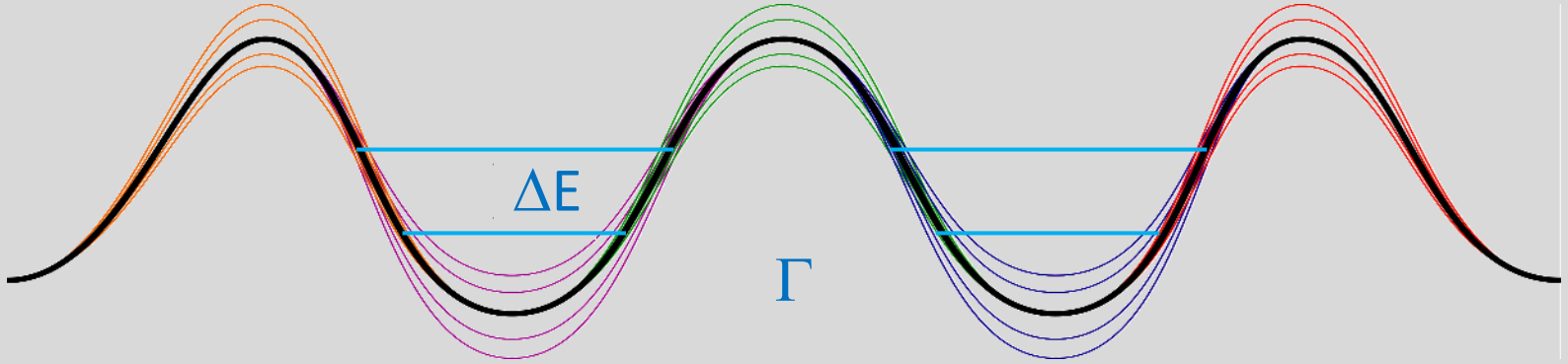
Core FDSOI technology

- Dedicated DRM
- Dedicated material expertise

Packaging

- 3D interposers
- Cryopackage

Application Layer or Work Load



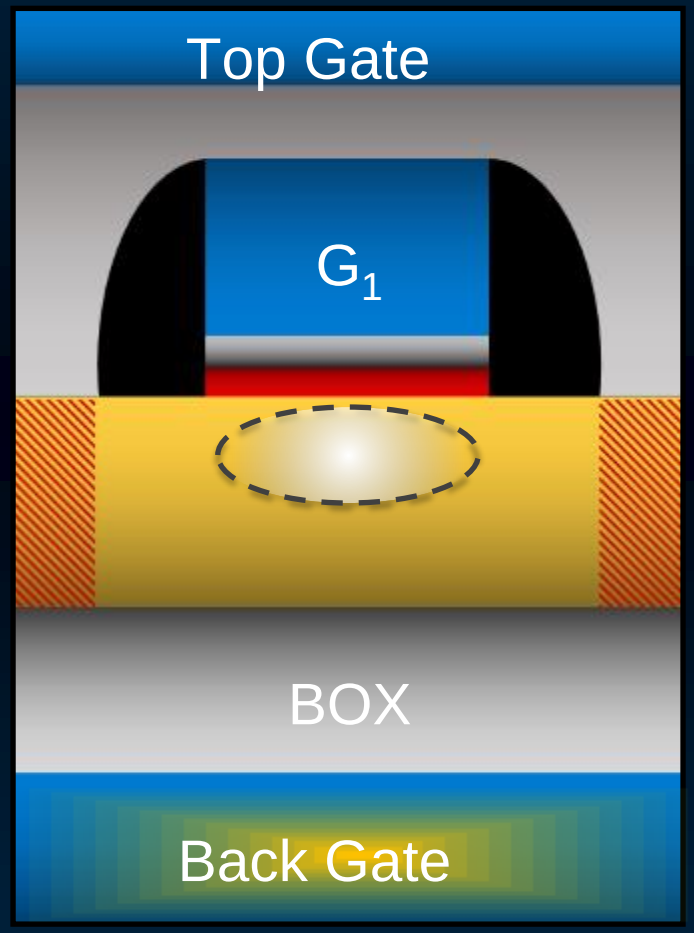
Well defined (electrostatically controlled) quantum wells separated by tunnel barriers

Quantum Interface

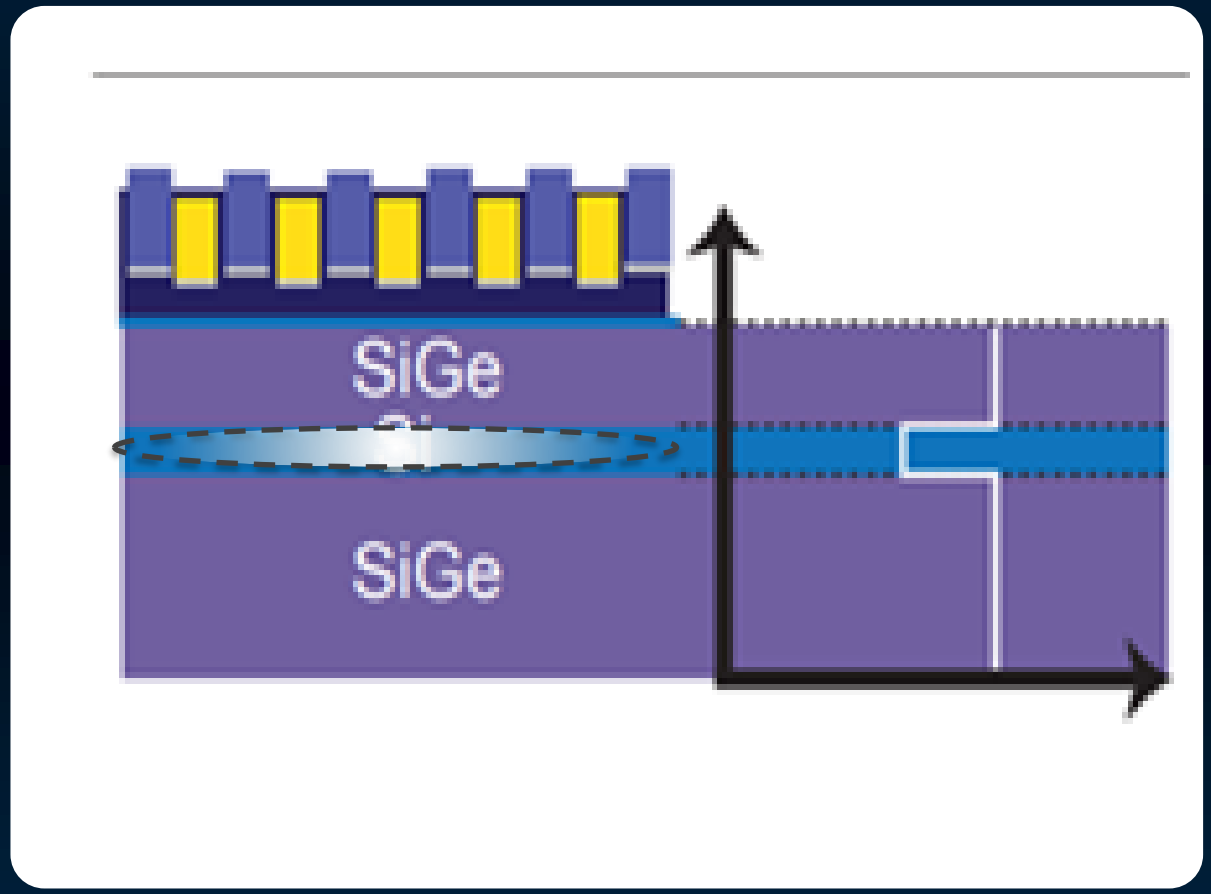
Quantum Chip

Moving away from interfaces

› **Two options**



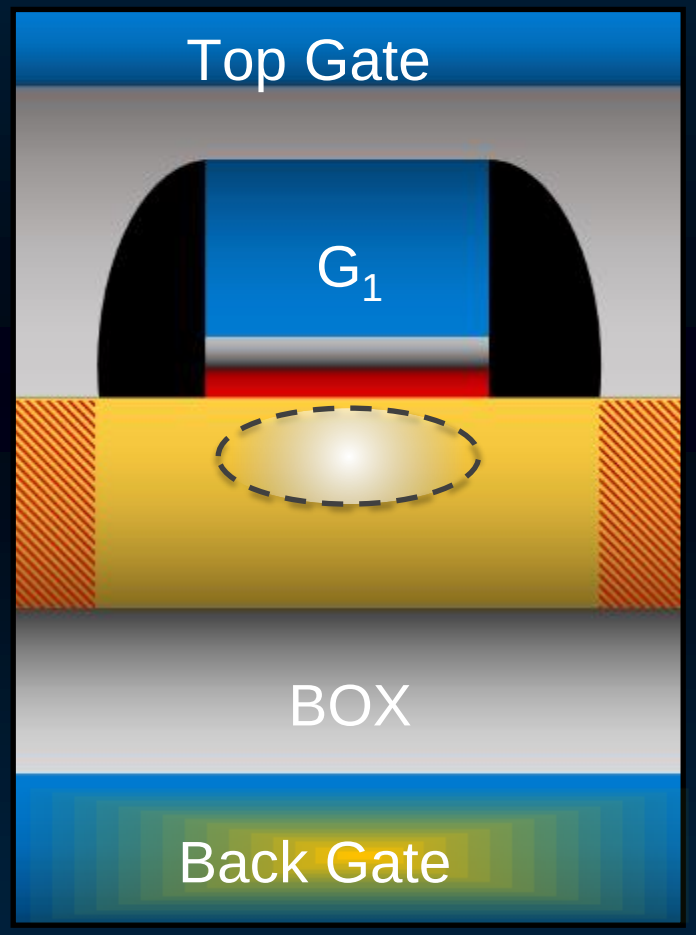
SOI

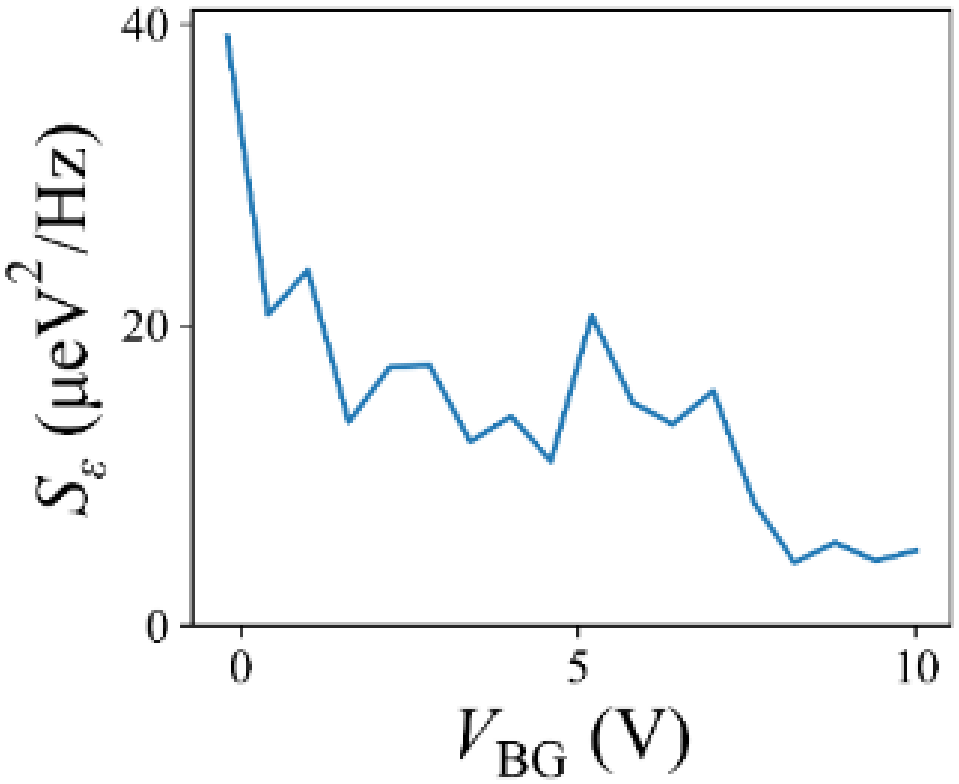


2DEG

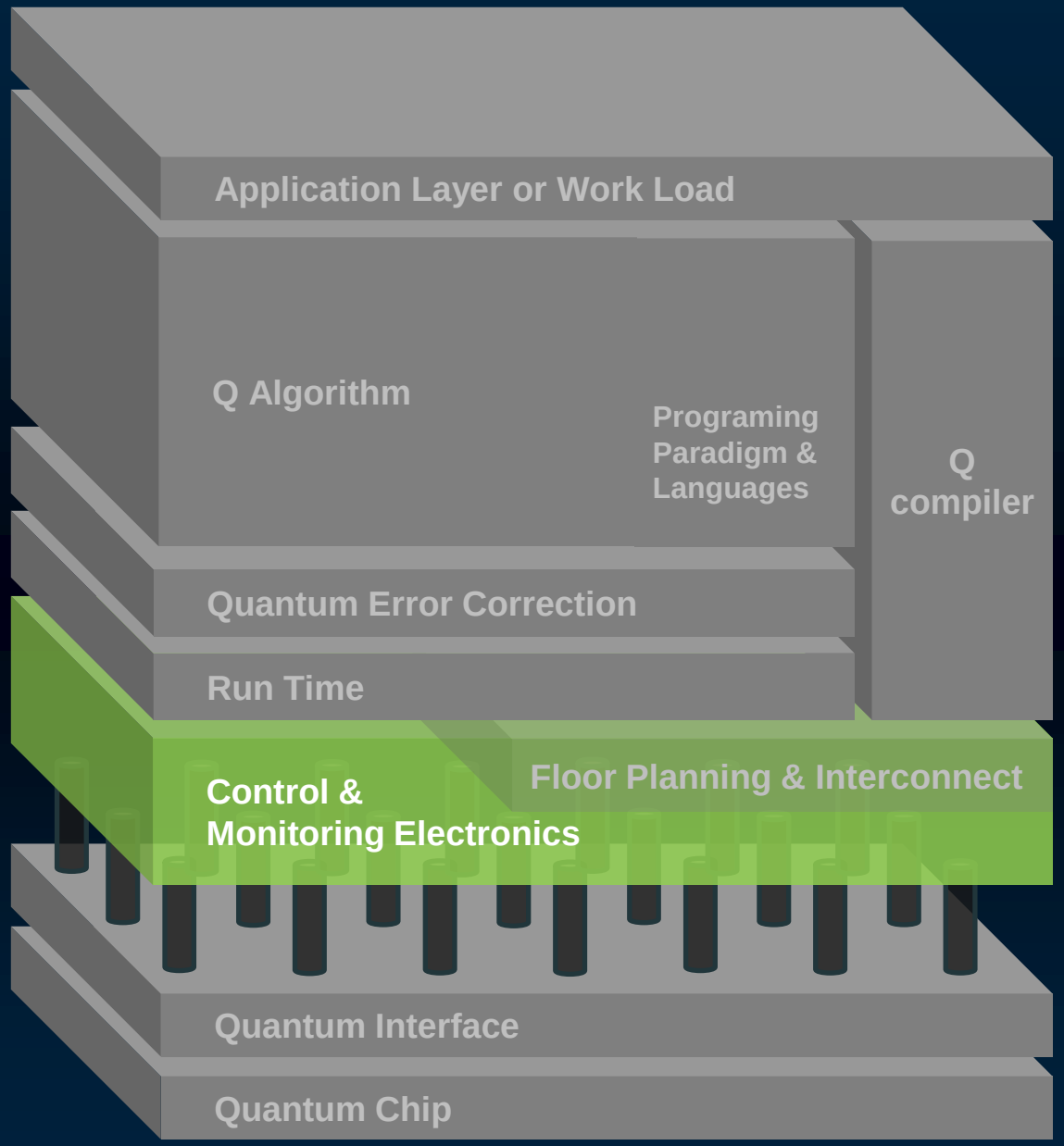
FD-SOI back gate moves away from the interfaces

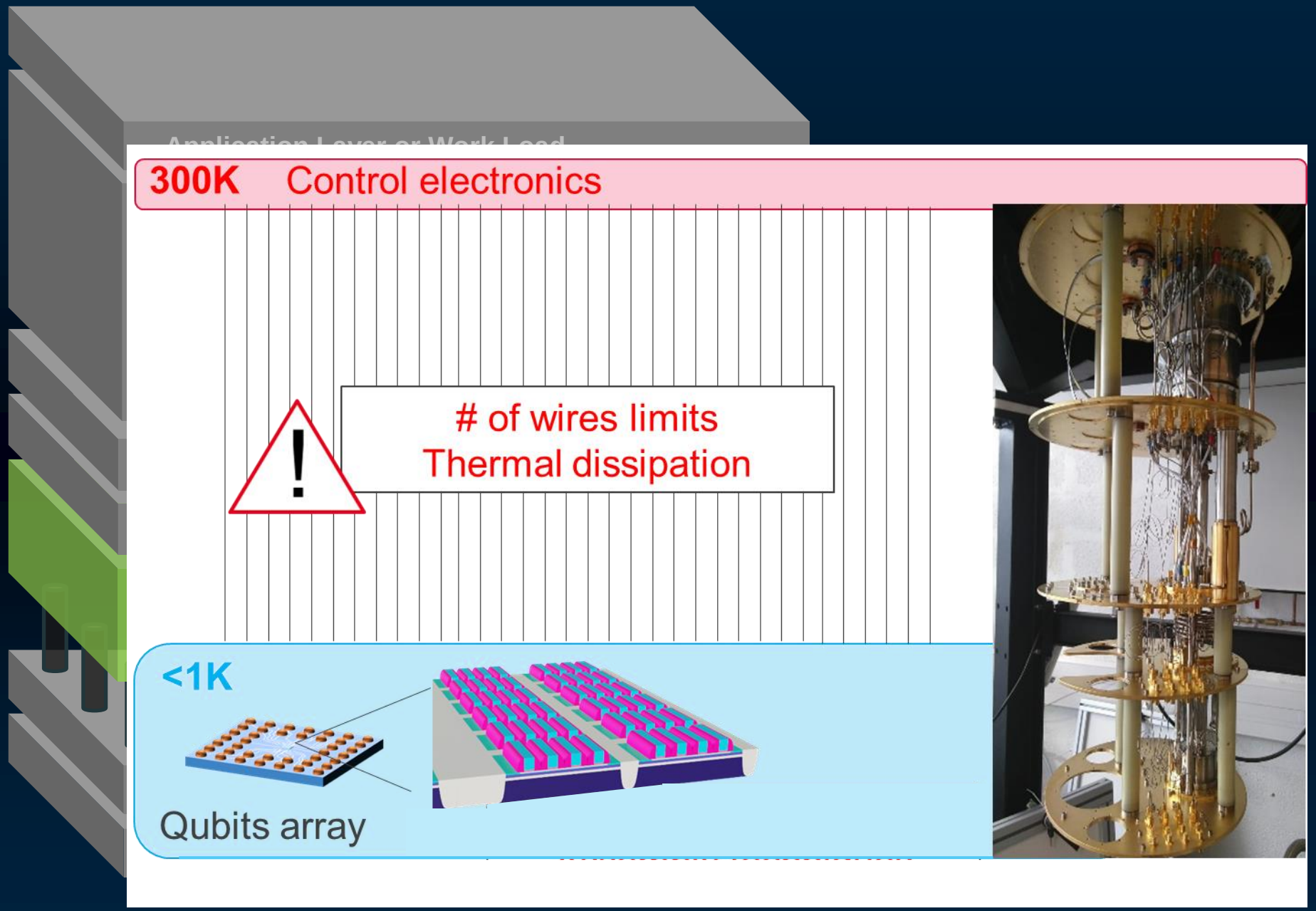
› **Charge noise decreases of one order of magnitude**



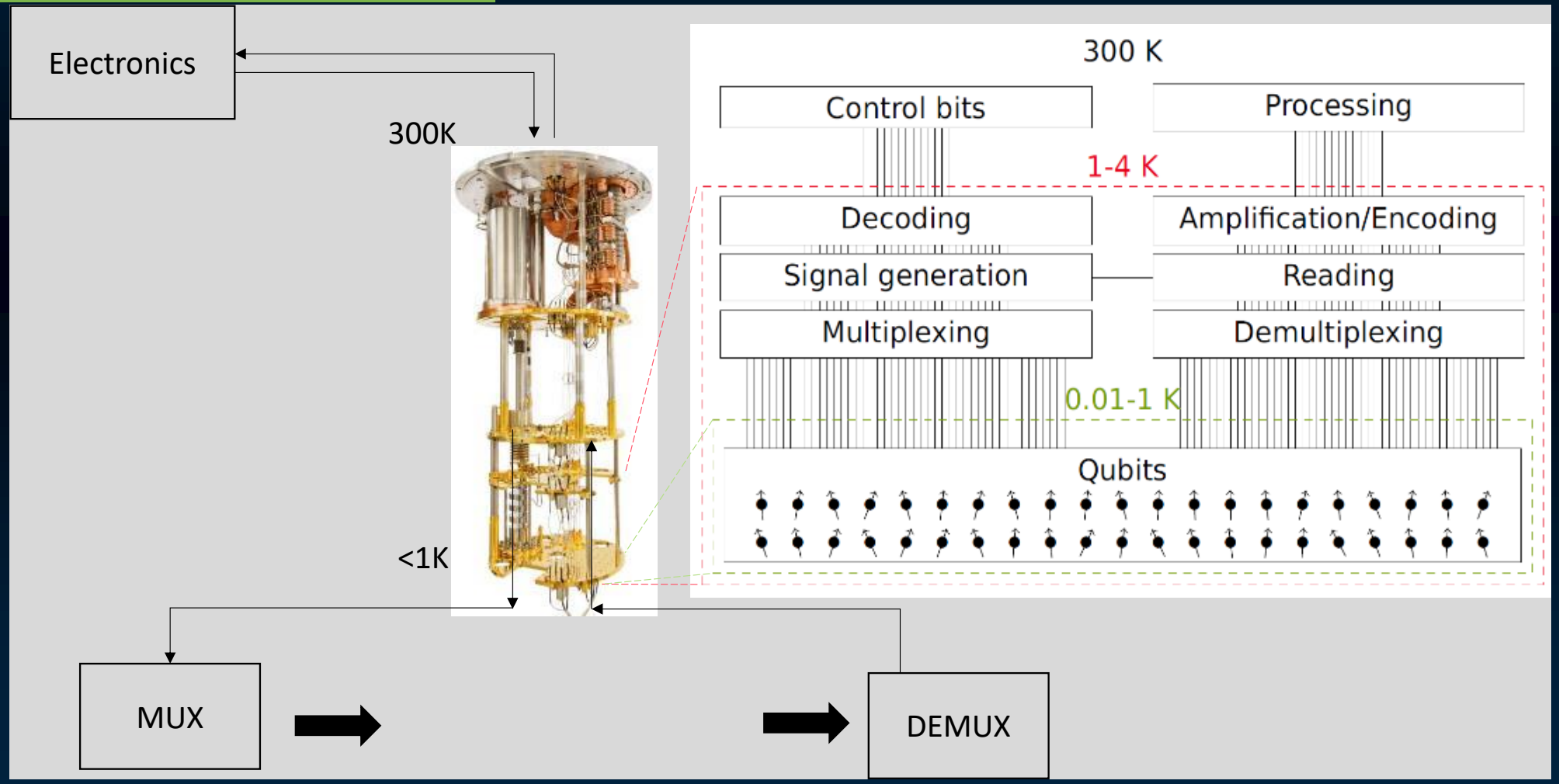


C. Spence and M. Urdampilleta, ArXiv


Application Layer or Work Load
Q Algorithm
Programing
Paradigm &
Languages
Q
compiler
Quantum Error Correction
Run Time
Floor Planning & Interconnect
Control &
Monitoring Electronics
Quantum Interface
Quantum Chip


Application Layer or Work Load
300K Control electronics
# of wires limits
Thermal dissipation
<1K
Qubits array

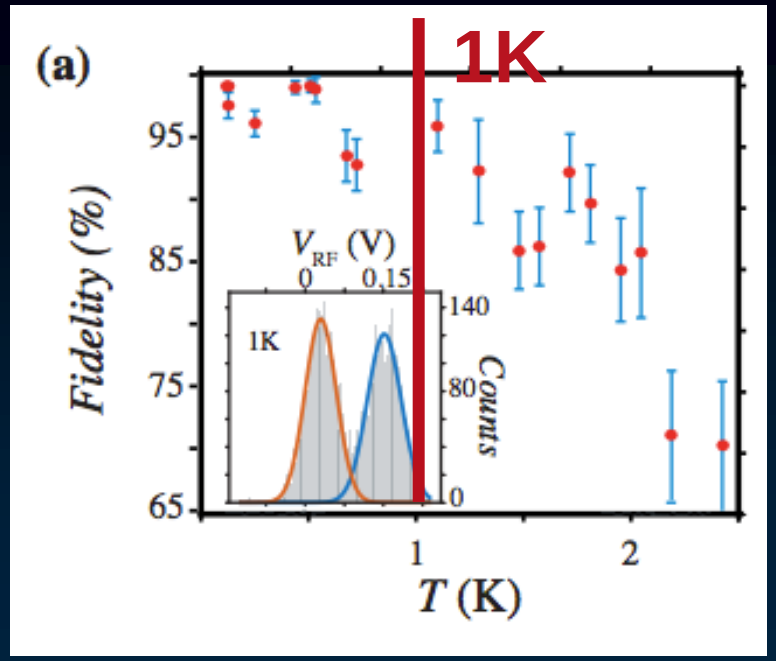
Control & Monitoring Electronics



Control &
Monitoring Electronics

T° of operation	Typical cooling power
20mK	30µW
100mK	1mW
1K	100mW-1W

Urdampilleta et al.,
arXiv:1809.04584



Dissipated power

=

activity x # of MOS x $f_{operation}$ x C_{load} x V^2

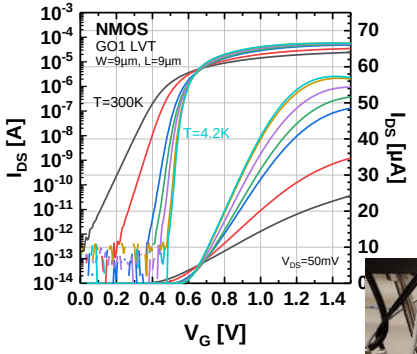
FD-SOI cryogenic control circuits development

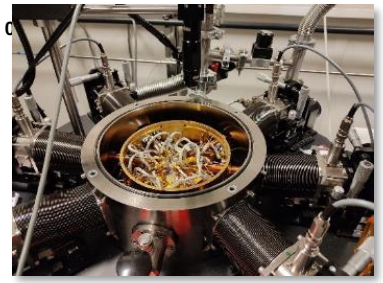
Lower power electronics

Paper 34.6 Wednesday @ 4.05pm
M. Cassé, IEDM 2022

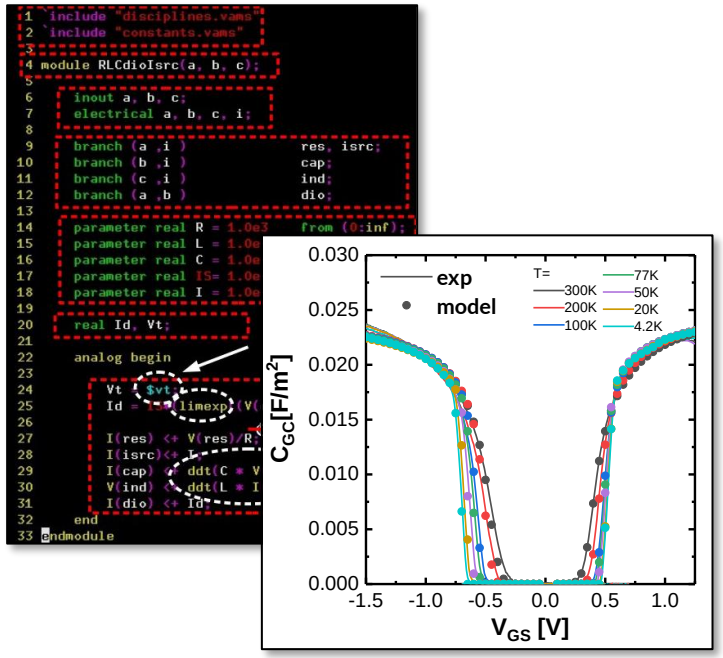
Characterization and modelling

T=300K -100mK

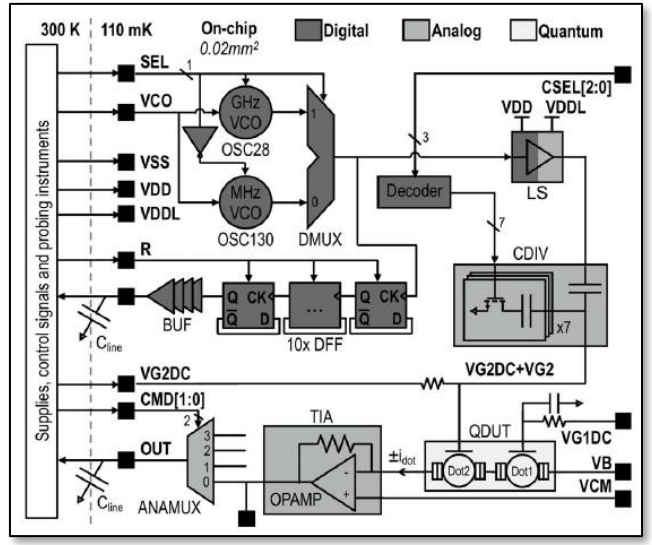




Simulation and CAD tools



IC design and test



B. Cardoso Paz et al., VLSI (2020)
M. Cassé et al. Appl. Phys. Lett. (2020)
M. Cassé et al.,, IntechOpen, (2022)

Back bias

In situ Vt centering

Allows ultra low power RF and digital IC design

FD-SOI as a SoC technology for qubits and control electronics

Successful integration at 1K and tested down to 50mK

1. Biasing the two quantum dots from on-chip bias tees,
2. Applying GHz mV-level modulation from on-chip frequency- and amplitude-controlled clock generators
3. Measuring the induced current through the device from a multiplexed on-chip transimpedance amplifier (TIA).

1µW @ 50mK

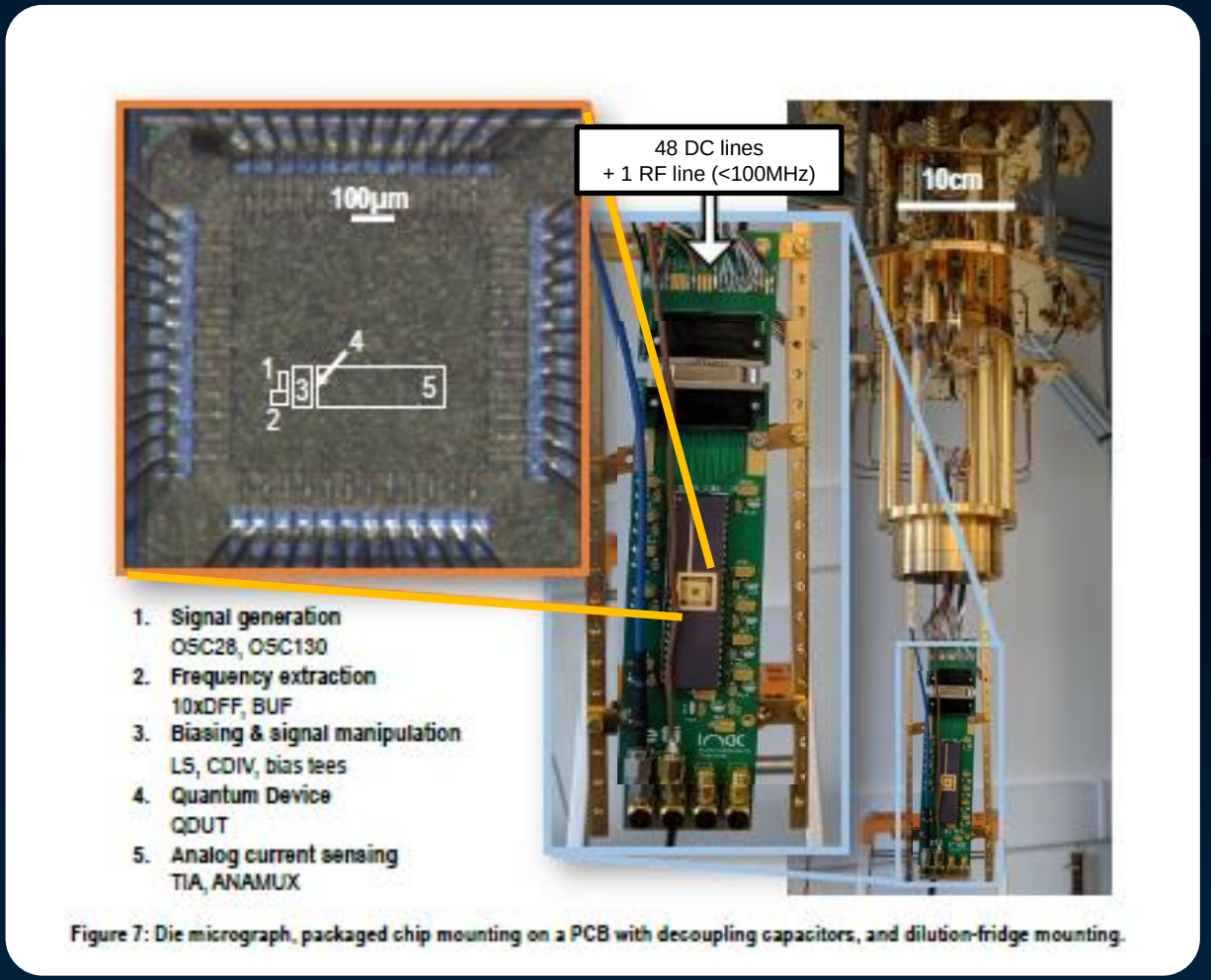


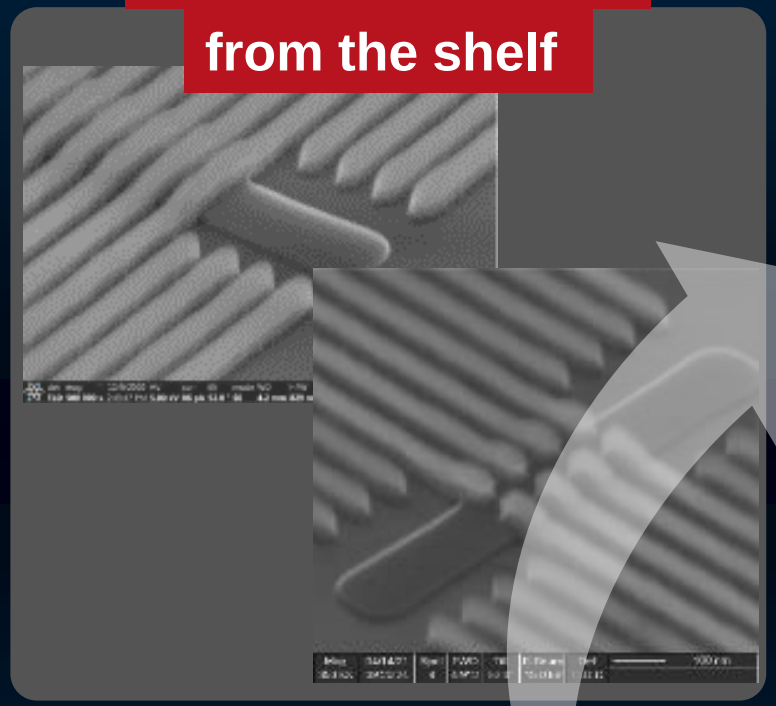
Figure 7: Die micrograph, packaged chip mounting on a PCB with decoupling capacitors, and dilution-fridge mounting.

ISSCC 2020' L. Le Guevel

Applied Phys Rev, L. Le Guevel, 2021

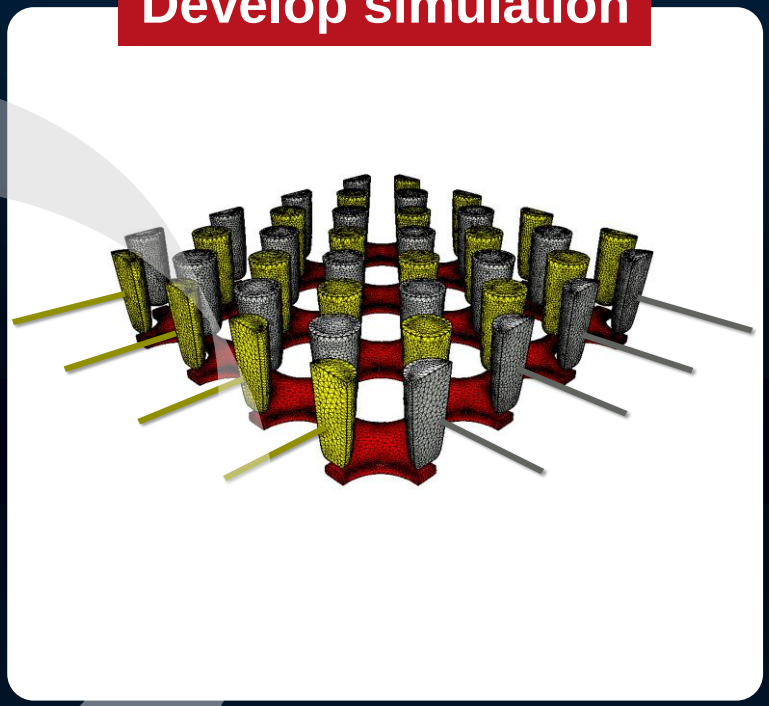
Leveraging VLSI methodology

Technology almost from the shelf

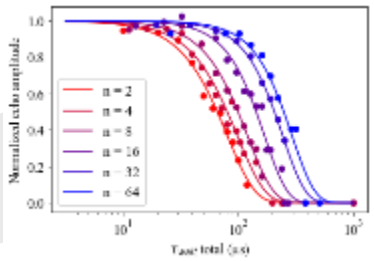


Set up statistical characterization

Develop simulation

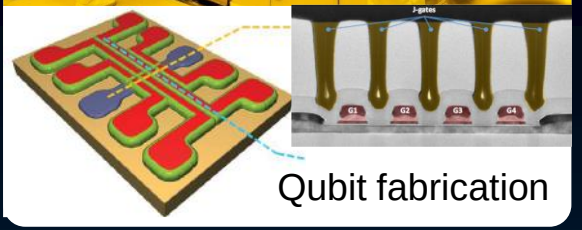


Physics experiments



From room to low temperature statistical data

Clean room
months / batch

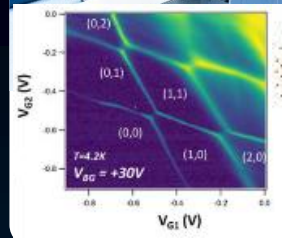


Qubit fabrication

Room T
12 hours / wafer

Basic functionalities testing

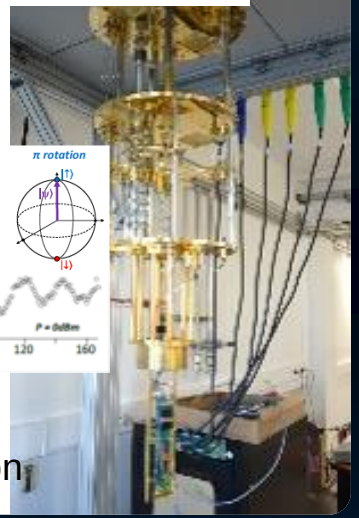
~1K
>2mn / device

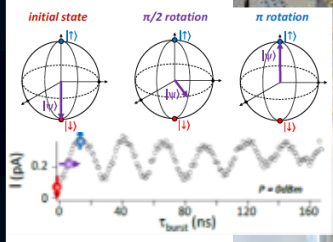


erc

Qudot testing

<100 mK
weeks /device





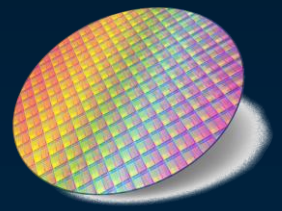
Qbit manipulation

300mm wafer process:
FDSOI CMOS platform

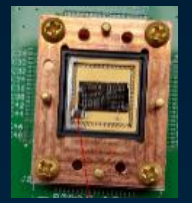
≳ 1000 devices
~ 100 dies

300mm full-wafer prober:
Parametric testers

300mm full-wafer prober:
Bluefors cryoprober

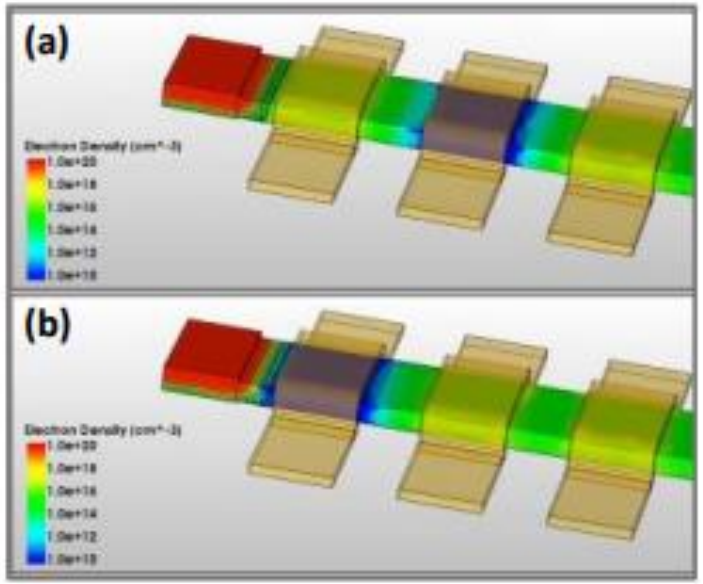


die (<1cm) mounted on a dilution fridge

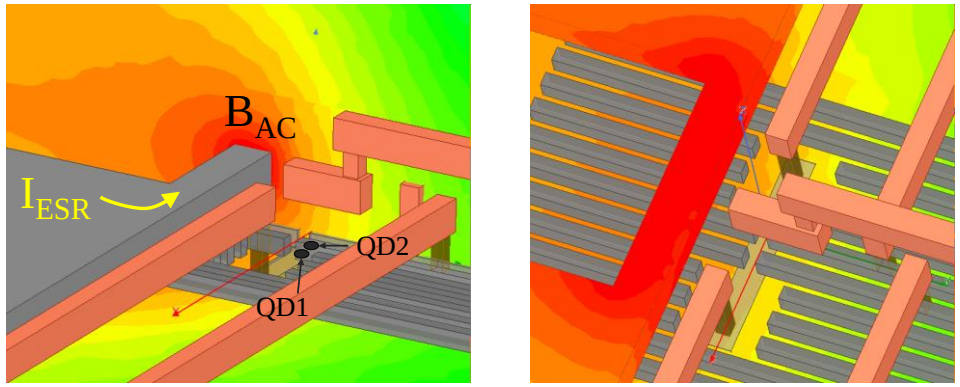


Multi-scale tools for Quantum Computer Aided Design

› Structure & electromagnetism, Classical TCAD



H. Niebojewski, VLSI (2022)

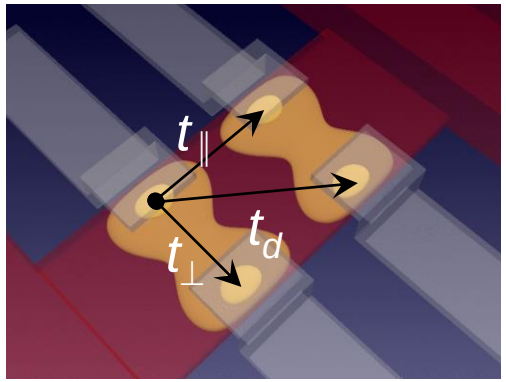


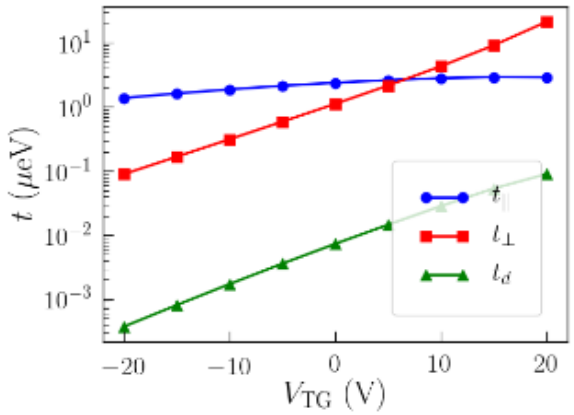
H. Jacquinot SISPAD (2022)

Magnetic field created
by the RF current through an ESR line, used to manipulate spins

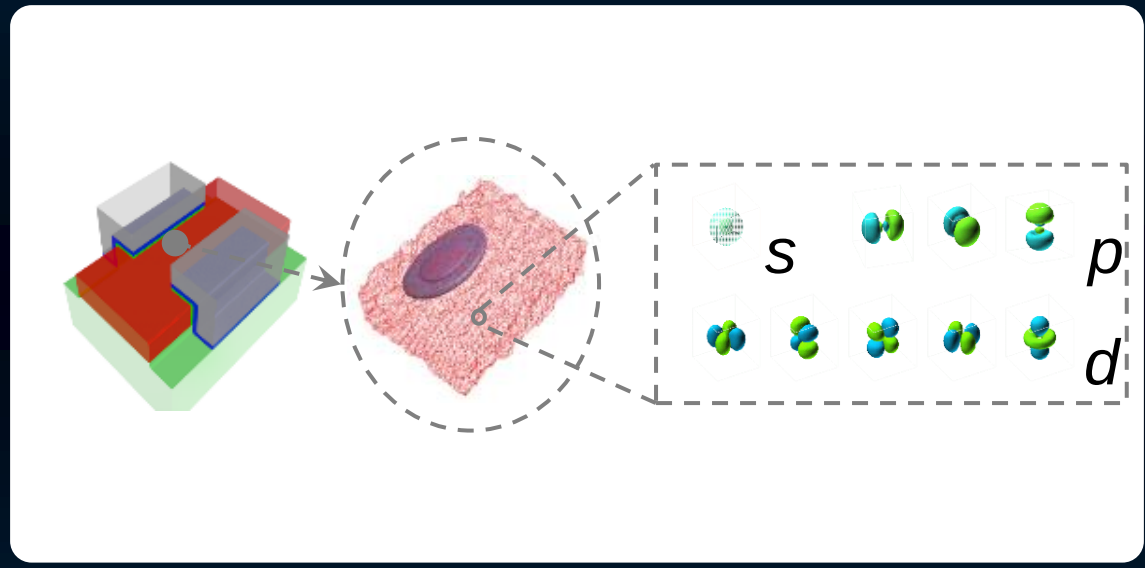
Electronic structure of the dots

- Finite differences/elements solutions effective mass of of k.p equations
- Wave functions as linear combination of atomic orbitals





Tunnel couplings between 4 dots wrt the bias on an extra top gate (not shown) at the M1 level



YM Niquet, IEDM 2020 J.Li, B. Venuticci, YM Niquet, unpublished

Atomistic modeling of a "corner dot" with surface roughness included

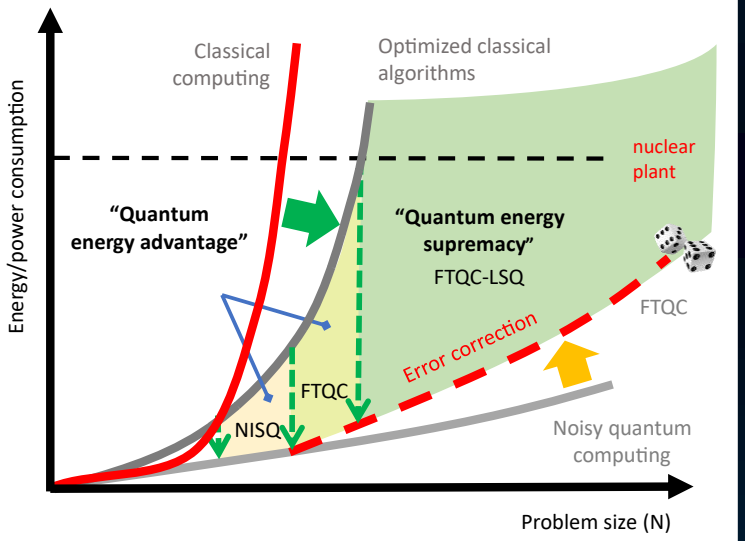
Key scientific questions

› is there a quantum energy advantage vs classical computing as quantum processors scale up?

› how different is it from the quantum computational advantage?

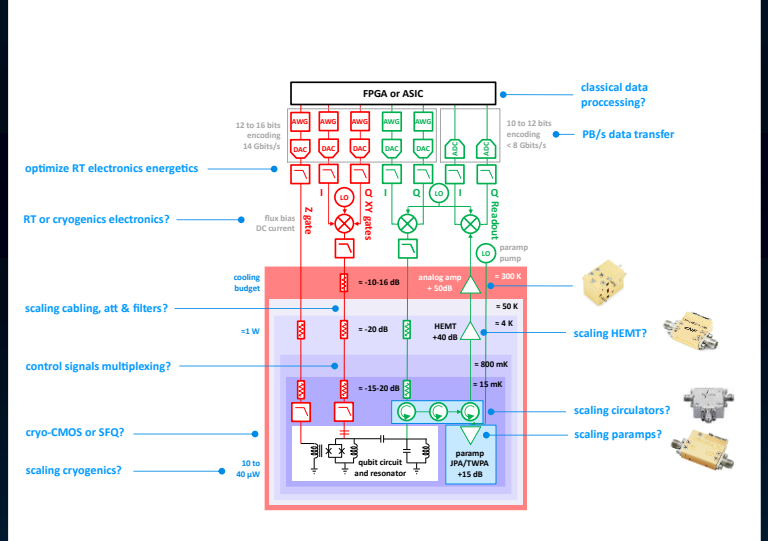
#QEI

the quantum energy initiative



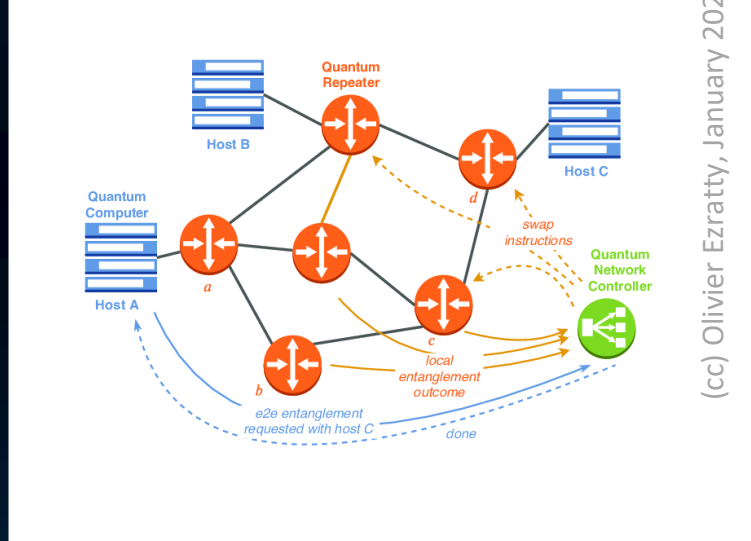
is there a **quantum energy advantage** vs classical computing as quantum processors scale up?

how different is it from the **quantum computational advantage**?



what is the fundamental **minimal energetic cost** of quantum computing?

how to **avoid energetic dead-ends** on the road to LSQ?

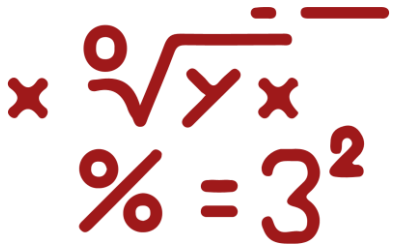


will **other quantum technologies** present energetic challenges?

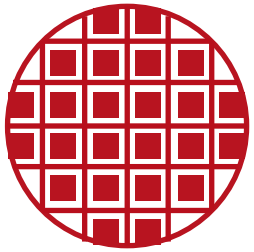
quantum communications and sensors

Key messages and perspectives

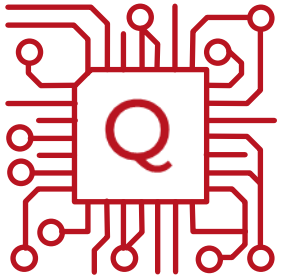
› Turn scientific firsts into reliable quantum processor units



Quantum computing has the potential to tackle untractable problems



Silicon provides good qubits and the semiconductor industry knows how to fabricate millions of them



Ecosystem and methods are in place to leverage the potential

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Silicon based quantum computer

- Spin off from CEA and CNRS, France
- www.siquance.com

Siquance technological roadmap

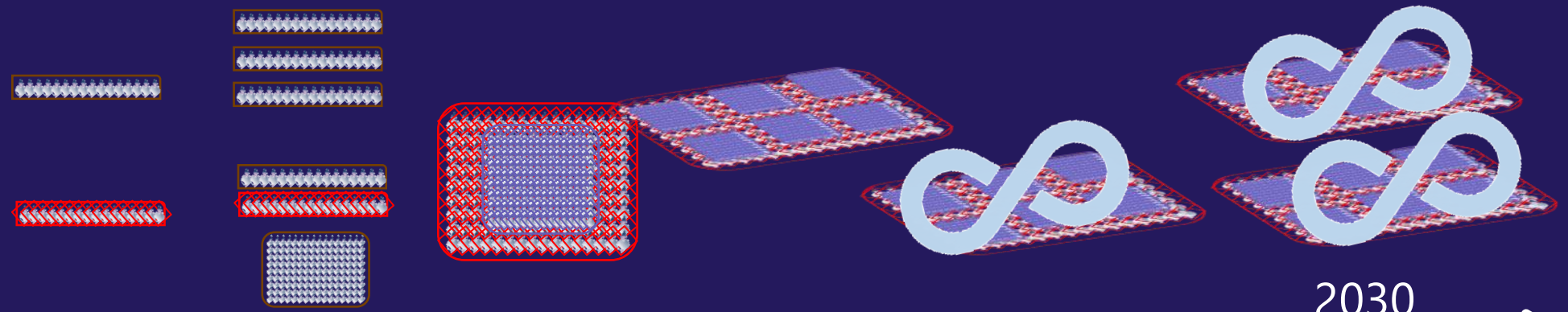
Noisy quantum systems

Quantum advantage PoV

Large scale quantum computing robust to errors

Multi-core 1D quantum processor

Multi-core 2D quantum processor



2022

2030

SoC qubit+cryocontrol
On line cloud access

SoC qubit
array+Cryocontrol

Quantum links

Large scale
quantum
processors

THANK YOU

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