ICOS Workshop – Sustainable Electronics & International Cooperation On Semiconductors

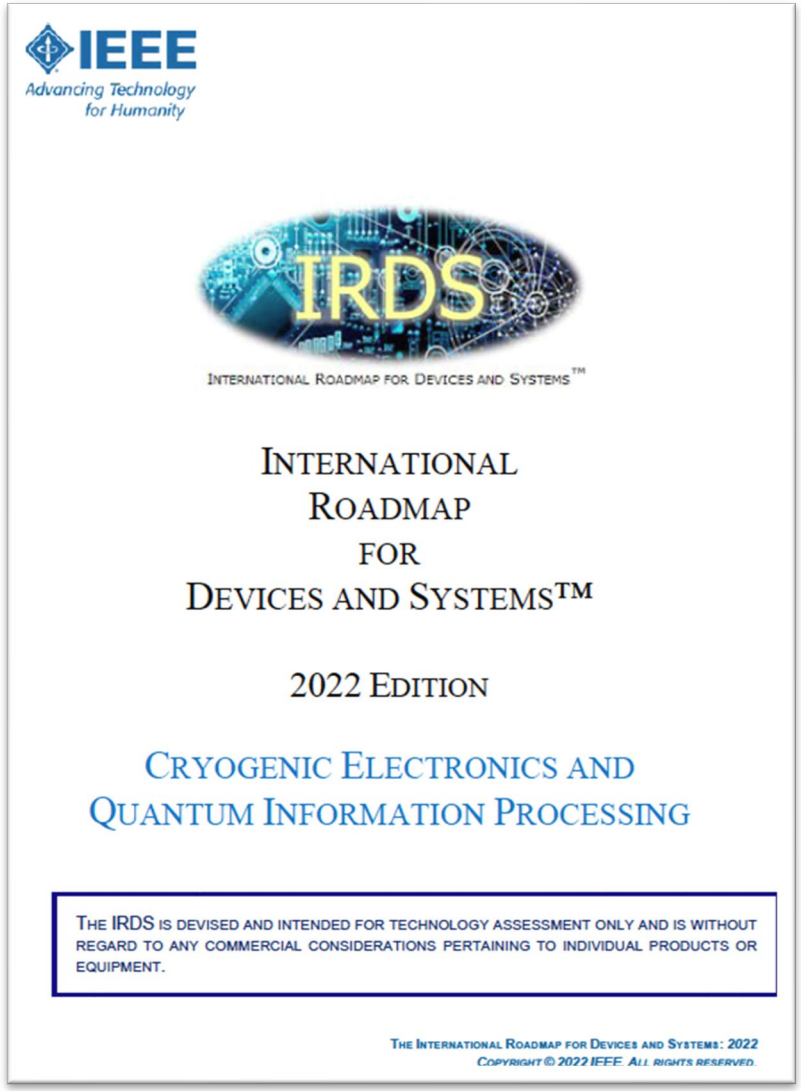
2023-04-27 Grenoble, France (virtual)

IRDS technology roadmaps for Cryogenic Electronics and Quantum Information Processing (CEQIP)

CEQIP Summary Presentation

2022 Edition and 2023 Update

- IRDS IFT Cross-team and Collaborative Alignments
- Coverage
  - Superconductor Electronics (SCE)
    - Roadmap (partial)
  - Cryogenic Semiconductor Electronics
  - Quantum Information Processing (QIP)
    - 2022: QC not yet ready for roadmaps
    - 2023: Roadmap started for superconducting QC
- Summary slides by area:
  - Difficult Challenges: Near- and Long-term
  - Technology Assessment Updates
  - New Technology Requirements
  - Breakthroughs in Technology, Research
- Recommendations and Plans
- Appendix: Team Members



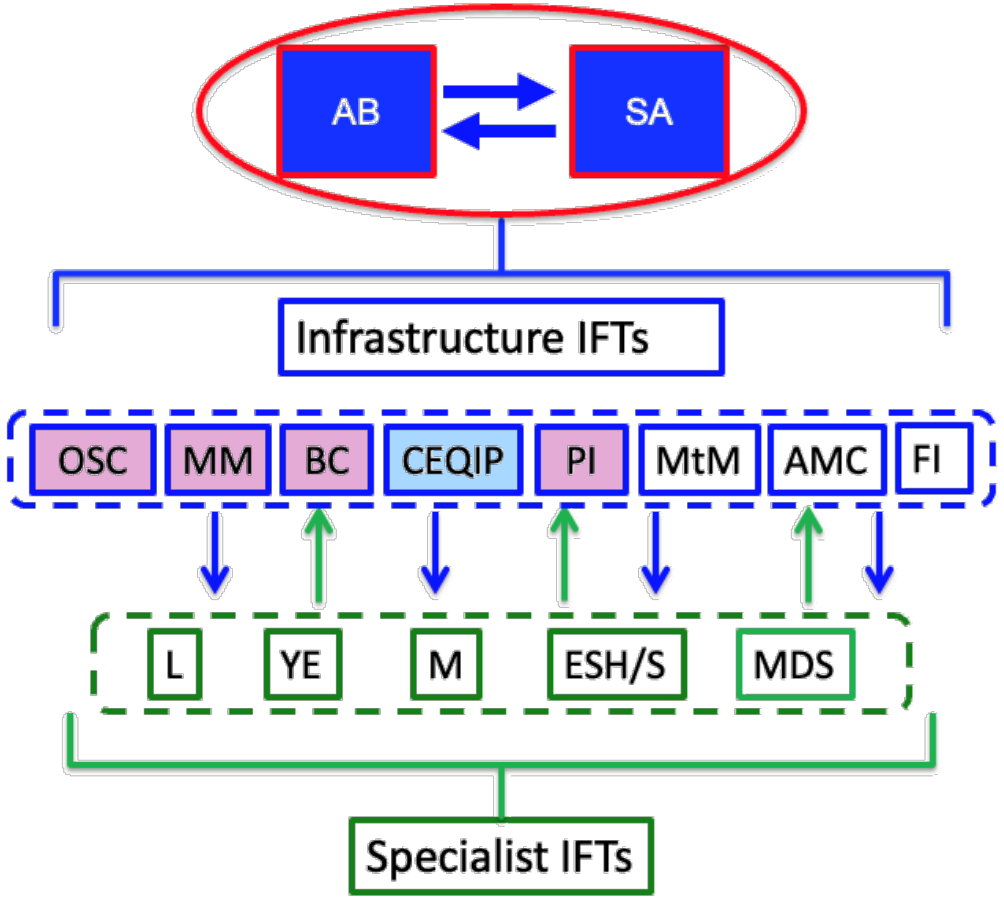
Available: https://irds.ieee.org/editions

IRDS IFT Cross-team and Collaborative Alignments

IFT: International Focus Team

- CEQIP primary interactions with IRDS teams
  - **AB**: Application Benchmarking
  - **SA**: Systems and Architectures
  - **BC**: Beyond CMOS
  - **MM**: More Moore
  - **OSC**: Outside System Connectivity
  - **PI**: Packaging and Integration

- External Organizations (contact person)
  - IEEE Quantum Initiative (Erik DeBenedictis)
  - QED-C: Quantum Economic Development Consortium (Erik DeBenedictis)
  - UK National Quantum Computing Centre Roadmap (Michael Cuthbert)



IFT structure of the IRDS

2022 IRDS Executive Summary, Fig. ES35

2023 Report: Superconductor Electronics (SCE)

2.1. **Introduction to SCE**
2.2. **Applications and Market Drivers for SCE**
- 2.2.1. Cloud (Digital Computing)
- 2.2.2. Measurement and Calibration Systems
- 2.2.3. Communications
- 2.2.4. Quantum Computing

2.3. **Present Status for SCE**
- 2.3.1. Logic
- 2.3.2. Memory
- 2.3.3. Switching Devices
- 2.3.4. Other Circuit Elements for SCE
- 2.3.5. Architectures and Applications
- 2.3.6. Fabrication for SCE
- 2.3.7. Electronic Design Automation (EDA) for SCE
- 2.3.8. Packaging and Testing for SCE
- 2.3.9. Interconnects for SCE
- 2.3.10. Refrigeration

2.4. **Benchmarking and Metrics for SCE**
- 2.4.1. Device and Circuit Benchmarking
- 2.4.2. Scaling of Devices and Circuits
- 2.4.2. System and Application Benchmarking

2.5. **Active Research Questions for SCE**
2.6. **Roadmaps for SCE**

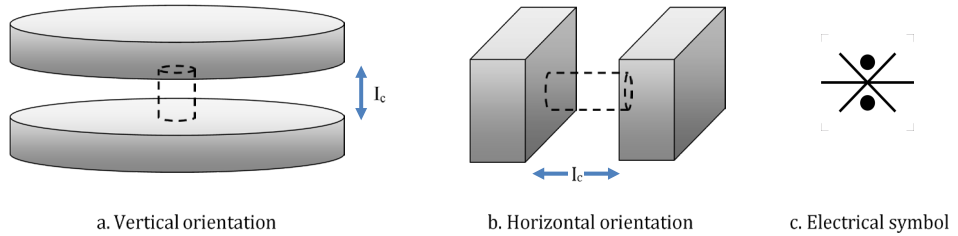


Figure CEQIP-1. Josephson Junction Device Structures

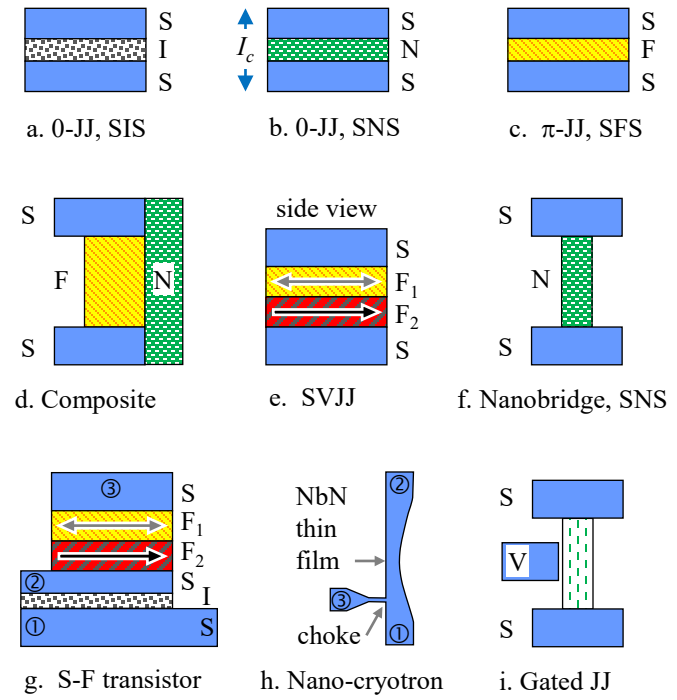


Figure CEQIP-3. Superconductor (S) switching devices

SCE Status

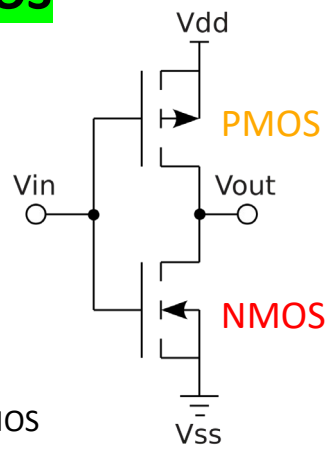
2023 Update

- Status summary
  - SCE is a developing technology with a small market and big promise
  - Quantum information processing (QIP) is an emerging driver
  - Logic: Many competing approaches
  - Memory: Little available; no clear solutions
  - Fabrication: Research + some commercial
- Key needs
  - Power supply
  - Sensitivity to external magnetic fields, currents, and trapped flux
  - Area reduction
  - Logic
  - Memory
  - Fabrication for scale
  - Testing

Logic: Searching for a Winning Combination

Semiconductor logic families

1960s	1980s
ECL	ECL
DTL	DTL
TTL	TTL
NMOS	NMOS
PMOS	PMOS
CMOS	**CMOS**



en.wikipedia.org/wiki/CMOS

Superconductor logic families

2010s+	2030s
– RSFQ	
– ERSFQ	
– eSFQ	
– DSFQ	
– HFQ	?
– nTron	
– xSFQ	
~ SFQ-AC	
~ RQL	
~ PML	
~ AQFP	
~ DQFP	
~ RQFP	
~ PCL	

Considerations:

- Performance
- Power
  - Static
  - Dynamic
  - Supply
- Cost
  - Ease of design
  - Area
  - Fabrication process
  - Yield
  - Shielding
- Compatibility
- …

Superconductor Digital Logic Families

Name	*SFQ*	*Power*	*Static Power*	*Dynamic power per switch*	*Trans-formers*	*Clocked Gates*	*JJ count $\log_{10}(n)$*
RSFQ: rapid single flux quantum	1	– DC	High	$\alpha I_c \Phi_0 f$	-	Yes	4.4
LR-RSFQ: inductor-resistor RSFQ	1	– DC	Low	$\alpha I_c \Phi_0 f$	-	Yes	1.6
LV-RSFQ: low-voltage RSFQ	1	– DC	Low	$\alpha I_c \Phi_0 f$	-	Yes	3.7
ERSFQ: energy-efficient RSFQ	1	– DC	0 *	$I_b \Phi_0 f$	-	Yes	3.8
eSFQ: efficient SFQ	1	– DC	0 *	$I_b \Phi_0 f$	-	Yes	3.4
Clockless SFQ	1	– DC					2.8
DSFQ: dynamic SFQ	1	– DC	‡	‡	-	Some	0.7
TSFQ: temporal SFQ	1	– DC			-	No	(2.8)
xSFQ: alternating SFQ	2	– DC	‡	‡	-	No	
nTron: nanowire cryotron	1	– DC	~0	varies	-	Yes	1.5
hTron: heater-cryotron nanowire	1	– DC	~0	varies	-	Yes	1.2
HFQ: half flux quantum	0.5	– DC	Low		-	Yes	1.2
SFQ-AC: AC-powered SFQ	1	~ AC	‡	‡	P	Yes	5.9
RQL: reciprocal quantum logic	2	~ AC	Low	$\alpha I_c \Phi_0 f\ 2/3$	P, G	Some	4.9
PML: phase mode logic	1	~ AC	Low	$\alpha I_c \Phi_0 f\ /3$	P, G	Some	
PCL: phase conserving logic	1	~ AC	Low		G	No	
AQFP: adiabatic quantum flux parametron	-	~ AC	~0	$\alpha I_c \Phi_0 2 f\ \tau_{sw}/\tau_x$	P, G	Yes	4.3
RQFP: reversible QFP	-	~ AC	~0	$\alpha I_c \Phi_0 2 f\ \tau_{sw}/\tau_x$	P, G	Yes	1.4

Other metrics?

- Area
- Current
- Logic depth
- JJ per gate
- Scalability

2023 Table CEQIP-4

SCE Memory

A critical need

- Several approaches
- Memory problems
  - Small memory capacity
  - Low area density
  - No commercial sources

2023 Table CEQIP-6 Superconductor Memory Status

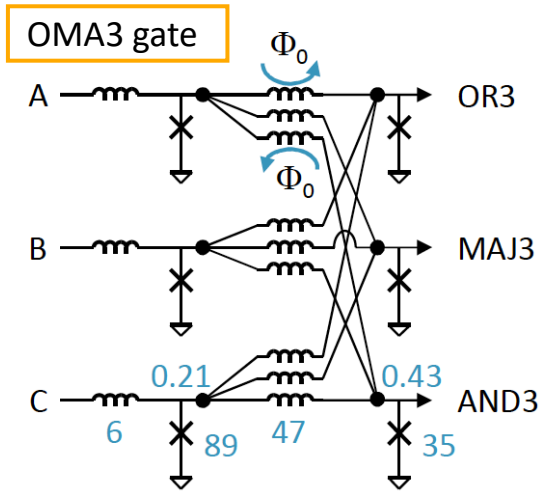
Name	*RAM*	*Bit Cell Area [μm^2]*	*Latency [ns]*		*Energy [fJ]*		*Static Power*	*Bits*
			Read	*Write*	*Read*	*Write*		
SR: shift register, ac-biased		300 (15×20)						202 280
SR: shift register			0.02	0.02	0.1	0.1	0.2 mW	64
VTM: vortex transition memory	✓	99 (9×11)	0.10	0.10	100	100		72
JJ-RAM: Josephson junction RAM	✓	484 (22×22)					4.5 mW	4096
RQL-RAM: reciprocal quantum logic	✓	1452 (33×44)						1024
PRAM: PTL-RAM	✓	1452 (33×44)						512
SHE-MTJ: Spin Hall effect magnetic tunnel junction	✓	2470 (38×65)	0.10	2	1000	8000		16
SNM: superconducting nanowire memory	✓	26.5 (5×5.3)	0.10	3	10	10		8
Hybrid: JJ-CMOS	✓		2 ~ 4	2 ~ 4	100	100		65 536

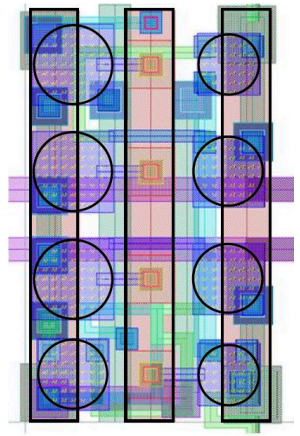
Recent progress: Superconductor Electronics (SCE)

New logic family: Pulse conserving logic (PCL)

- Logic
  - Dual rail signals (free inversion)
  - 12 levels of logic at 30 GHz
  - Density ~10 M gates/cm^2
  - Gates include: OA2, OMA3
- Memory: Josephson SRAM
  - 4 MB/cm^2 density
  - 30 GHz throughput
- Power supply
  - AC power and bias currents
  - Zeroth-order resonance (ZOR) of uniform amplitude and phase
  - Efficiency increases with *f* and activity factor

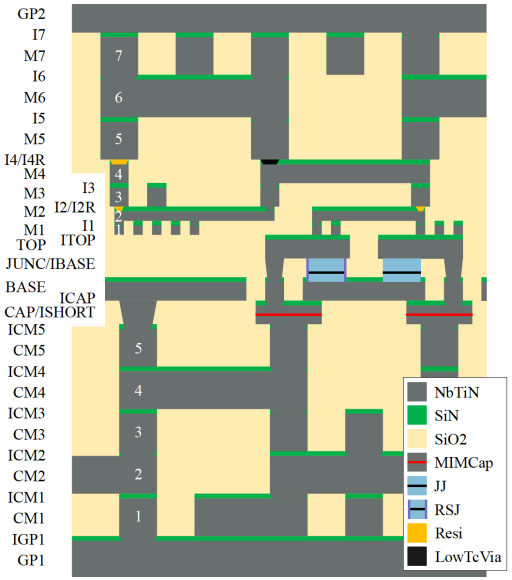
▸ Many questions, demonstration needed

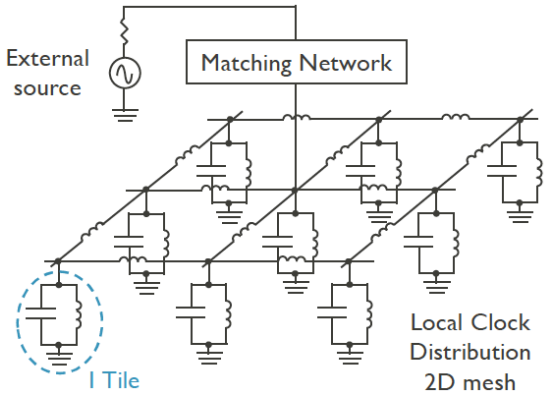




memory cell (1 μm × 2 μm)

Q. Herr +, 2023, doi: 10.48550/arXiv.2303.16792





A. Herr +, 2023, doi: 10.48550/arXiv.2303.16792

Roadmap: Fabrication for Superconductor Electronics (SCE)

Year	2022	2023	2024	2025	2026	2027	2028
Digital SCE Fabrication							
"Node Range" label (nm)	**"250"**	**"250"**	**"150"**	**"150"**	**"150"**	**"150"**	**"90"**
Substrate material, maximum size (mm)	Si, 200	Si, 200	Si, 200	Si, 200	Si, 200	Si, 200	Si, 300
Wiring							
Superconductor	Nb	Nb	Nb	Nb	Nb	Nb	Nb
Superconductor layers	**8**	**8**	**10**	**10**	**10**	**10**	**12**
Linewidth, minimum (nm)	**250**	**250**	**150**	**150**	**150**	**150**	**90**
Ic, minimum (μA/)	**200, 1200**	**200, 1200**	**100, 580**	**100, 580**	**100, 580**	**100, 580**	**50, 290**
Junctions, Switching							
Junction materials	Al/AlOx	Al/AlOx	Al/AlOx	Al/AlOx	Al/AlOx	Al/AlOx	Al/AlOx
Junction layers	**1**	**1**	**2**	**2**	**2**	**2**	**2**
Junction critical current densities, Jc (μA/μm^2)	**100, 600**	**100, 600**	**100, 600**	**100, 600**	**100, 600**	**100, 600**	**100, 600**
Minimum junction diameter (nm)	**500**	**500**	**350**	**350**	**350**	**350**	**250**
Minimum junction critical current, Ic (μA)	**20, 118**	**20, 118**	**10, 58**	**10, 58**	**10, 58**	**10, 58**	**5, 29**
Killer defect density per layer (1/cm^2)	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**	**< 0.1**
Jc wafer-to-wafer variation	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**
Maximum relative spread (σ/Ic) at minimum Ic	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**	**3%**
Junctions, Magnetic (Pi)							
Junction materials			Ni	Ni	Ni	Ni	Ni
Junction layers	0	0	1	1	1	1	1
Junction critical current densities (μA/μm^2)			**3000**	**3000**	**3000**	**3000**	**3000**
Junction diameter, minimum (nm)	**500**	**500**	**350**	**350**	**350**	**350**	**350**
Resistors							
Resistor material	Mo, MoNx	Mo, MoNx	Mo, MoNx	Mo, MoNx	Mo, MoNx	Mo, MoNx	Mo, MoNx
Resistor layers	1	1	1	1	1	1	1
Resistor sheet resistance (Ω/☐)	**2, 6, 10**	**2, 6, 10**	**2, 6, 10**	**2, 6, 10**	**2, 6, 10**	**2, 6, 10**	**2, 6, 10**
HKI (high kinetic inductance) Layers							
HKI material	MoNx	MoNx	NbNx	NbNx	NbNx	NbNx	NbNx
HKI layers	1	1	1	1	1	1	1

2023 Table CEQIP-17

Difficult Challenges (Near-term) for SCE

Technology roadblocks, gaps, and possible disconnects within the roadmap

Near-Term Challenges: 2022–2029	*Summary of Issues (why is it a challenge?)*
Logic (current implementations)	• Many competing approaches • Sensitivity to magnetic fields and fabrication variation • Supply current is mostly spent biasing junctions • Power and clock pulse distribution add complexity and jitter • Scalable to solve big problems (DSP, AI, QC, HPC)
Memory	• Density is too low for single-flux-quantum memory (like SRAM) • Multiplexing is difficult for single-flux-quantum logic • New materials and processes add cost
Phase shift elements	• Present approach (external supply current through inductors) does not scale. DC bias is ~ 0.7 *Ic* per junction, so chip supply current becomes too large for > 1 million junctions. Inductors require shielding. • Phase batteries such as pi junctions require new materials, device layer.
NbN or NbTiN fabrication process	• NbN and NbTiN now deposited by reactive sputtering, which is difficult to make uniform across a 200 mm or 300 mm diameter wafer • CVD or ALD processes will require development

2023 Table CEQIP-16

Difficult Challenges (Long-term) for SCE

Technology roadblocks, gaps, and possible disconnects within the roadmap

Long-Term Challenges: 2030–2037	*Summary of Issues (why is it a challenge?)*
Switching device scalable below 200 nm	• Nb/Al-AlOx/Nb Josephson junctions are almost good enough • Alternatives will require different materials and fabrication processes, possibly including magnetic materials
3-terminal switching device	• Small available flux ~ 2 mA·pH or voltage ~ 1 mV • Fabrication more difficult than the traditional tri-layer device
Integrated circuit fabrication processes	• Foundries for commercial production now process 200 mm or smaller wafers using equipment lacking state-of-the-art capability. • Temperatures are currently limited to < 200 °C, which requires different processes than CMOS technology, which has a limit of 400 °C. • Circuit approaches and fabrication processes are interdependent, requiring co-development. • Magnetic materials need to be added.
Optical input/output (I/O)	• Heat budget in the low-temperature environment is very low. • Optical data links require development of efficient SFQ-to-optical converters.

- But can these wait?

2023 Table CEQIP-16

Cryogenic Semiconductor Electronics

2023 Update

3.1. **Introduction**

3.2. **Applications and Market Drivers for Cryo-Semi**

3.3. **Present Status for Cryo-Semi**

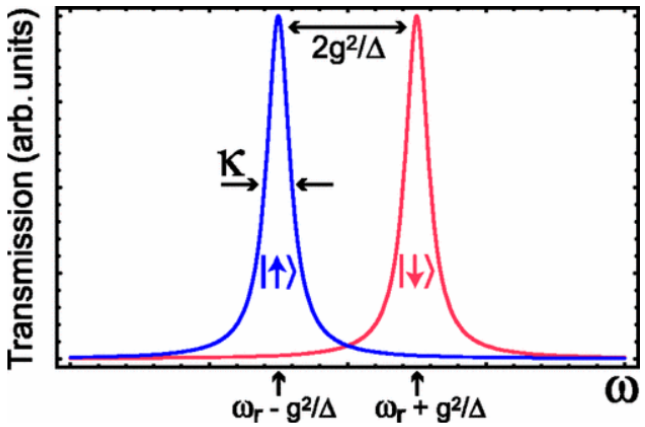
- 3.3.1. Transistor Characterization and Modeling
- 3.3.2. Applications ≥ 10 K
- 3.3.3. Applications < 10 K

3.4. **Active Research Questions for Cryo-Semi**

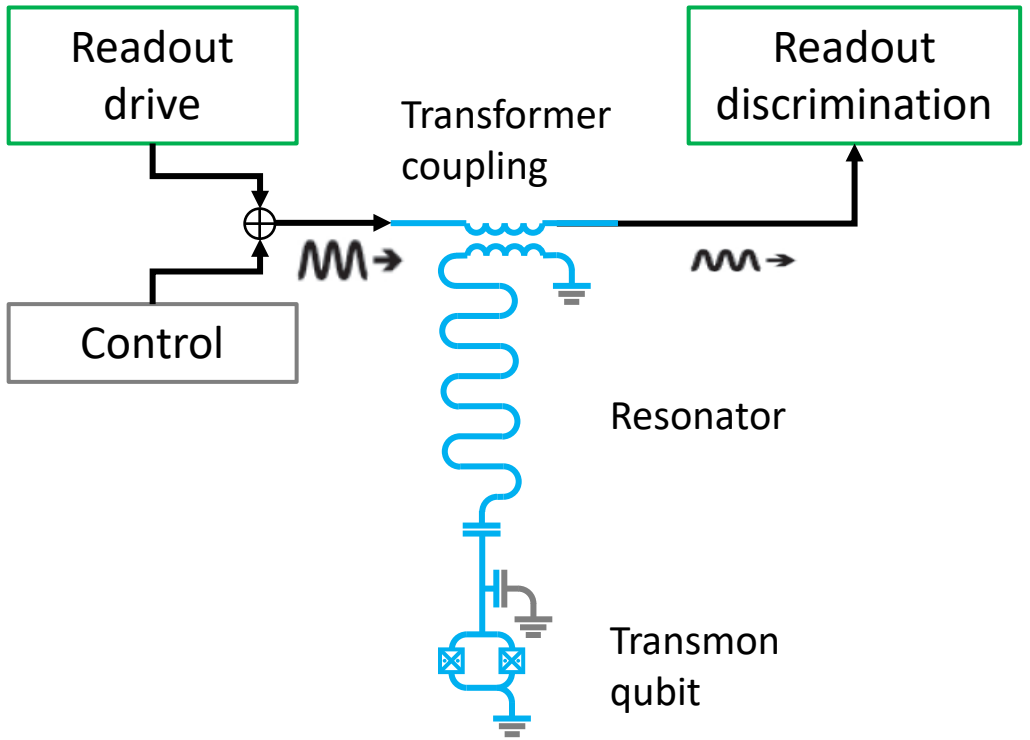
Qubit Control and Readout: Basics

Microwave engineering

- **Control**: Microwave signals change the qubit state
- **Readout**: Microwave transmission depends on qubit state



Blais +, 2004, doi: 10.1103/PhysRevA.69.062320

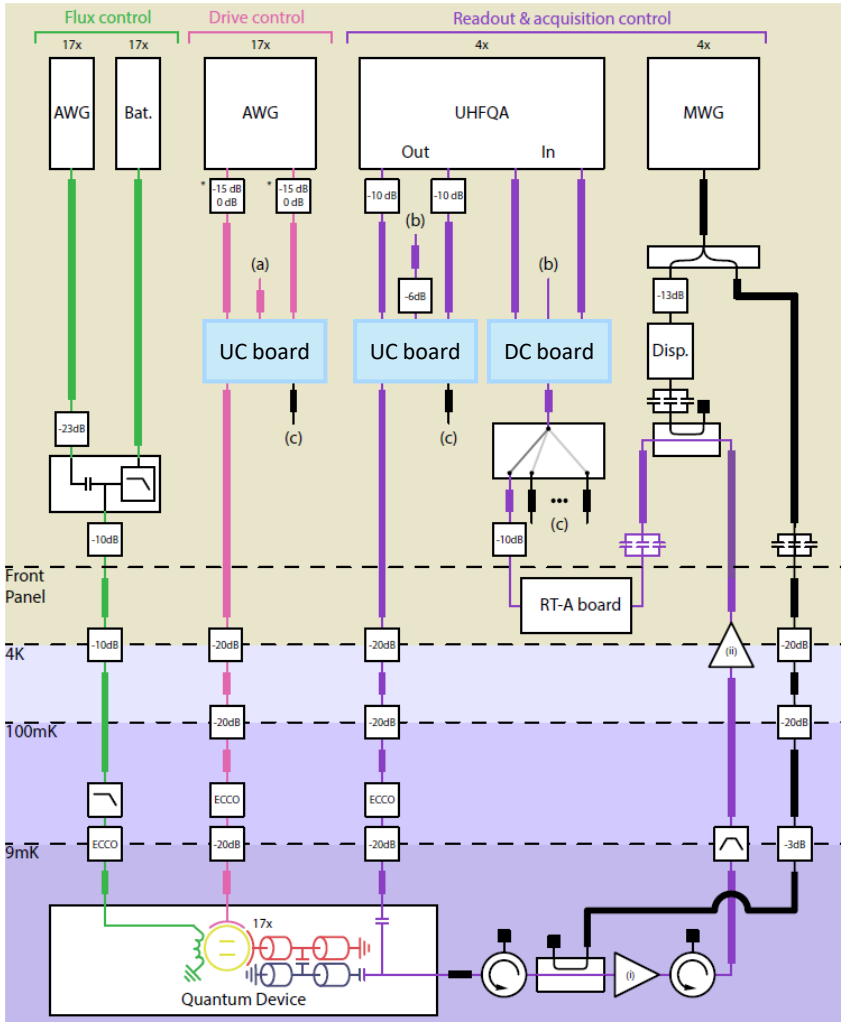


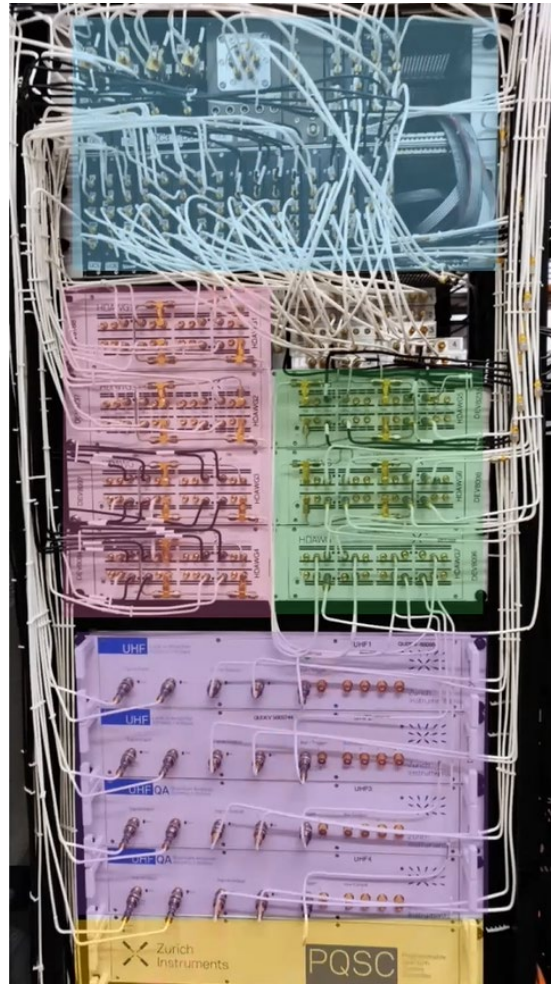
Qubit Control: Room-Temperature Electronics

The starting point

- Qubit Control (HDAWG)
  - Flux drives
  - Baseband RF drives
- Qubit Readout (UHFQA)
  - Baseband signal generation and analysis (FPGA)
- Frequency conversion electronics (up, down) for qubit drive and readout
- Synchronization using PQSC

- Next steps:
  - Commercial, modular equipment customized for qubit control and readout

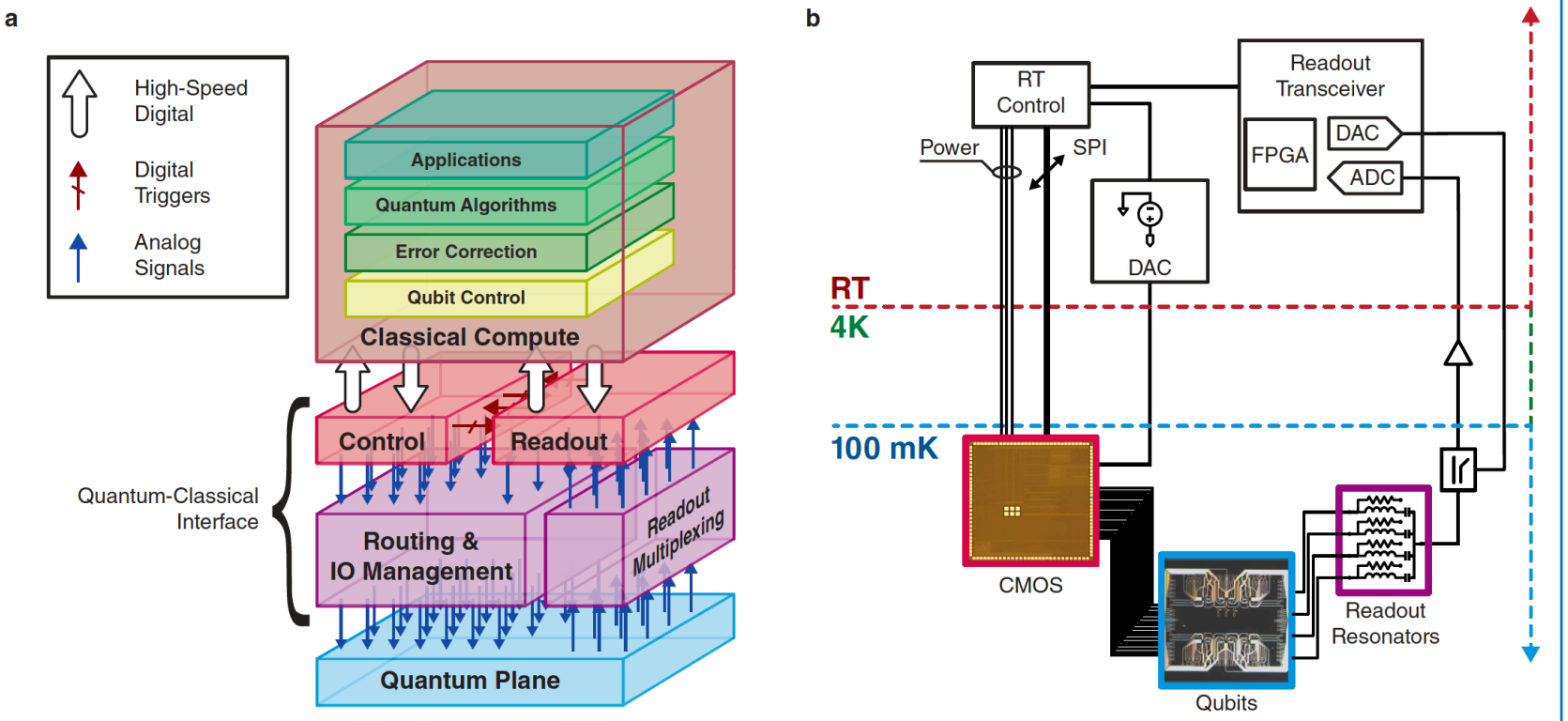




Krinner +, "Realizing repeated quantum error correction in a distance-three surface code", 2022, doi: 10.1038/s41586-022-04566-8

Quantum computing support applications

Qubit interface, control, and readout using cryogenic semiconductor electronics



Microsoft: System to control and read out up to 32 voltage-controlled Si-qubits (not yet interacting) [1]

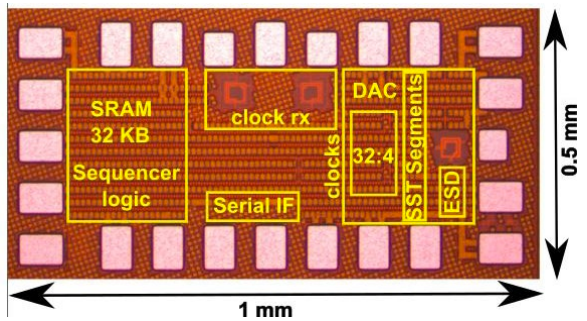
[1] S. J. Pauka *et al.*, "Characterizing quantum devices at scale with custom cryo-CMOS," *Phys. Rev. Appl.*, vol. 13, no. 5, p. 054072, May 2020, doi: 10.1103/PhysRevApplied.13.054072.

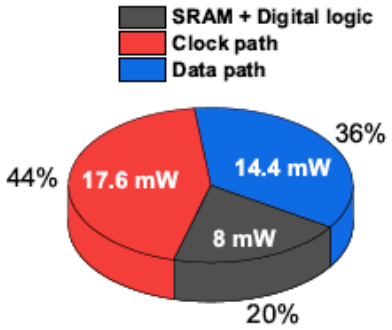
[2]. B. Patra, M. Mehrpoo, A. Ruffino, F. Sebastiano, E. Charbon, and M. Babaie, "Characterization and analysis of on-chip microwave passive components at cryogenic temperatures," *IEEE J. Electron Devices Soc.*, Apr. 2020, doi: 10.1109/JEDS.2020.2986722.

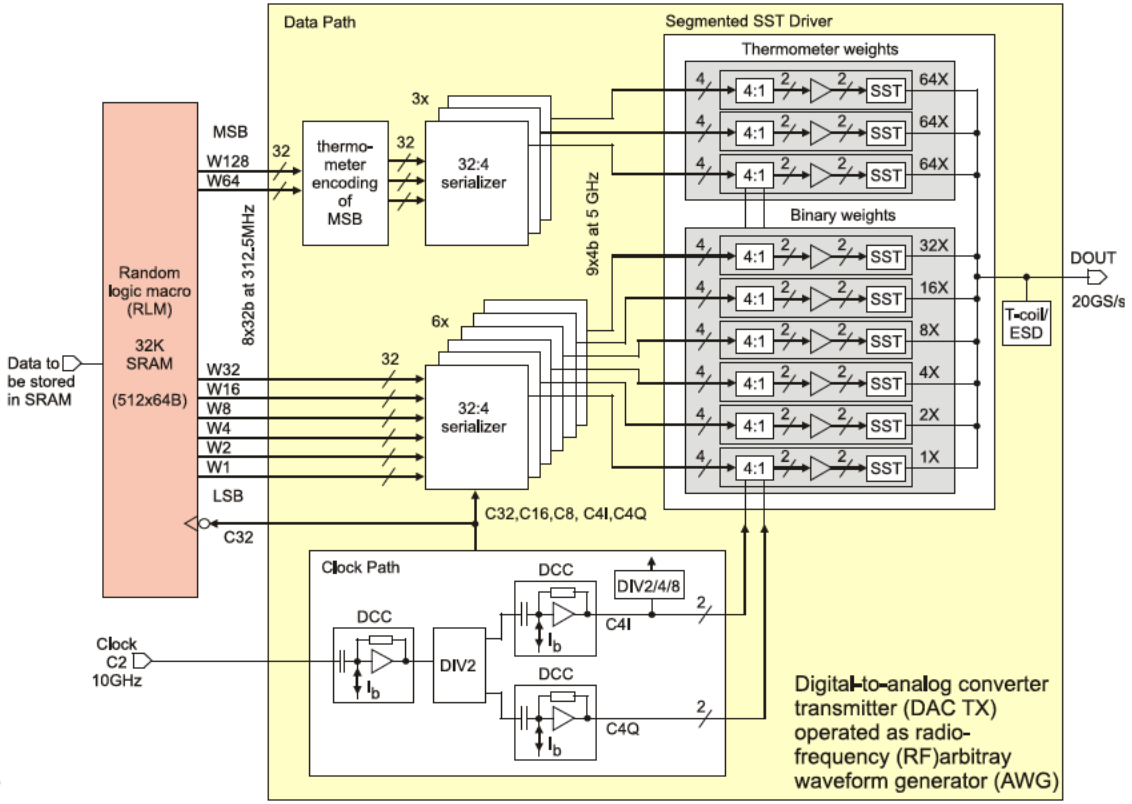
Quantum computing support applications

Development continues

- Digital to analog converter (DAC)
  - 32 KiB on-chip memory (SRAM)
  - 14 nm CMOS technology
  - Output at 4 K temperature:
    Qubit control waveforms in the
    1 GHz to 18 GHz frequency range
  - Sampling rate: 40 GSa/s max.
  - 40 mW power dissipation at 4 K







Prathapan +, “A cryogenic SRAM based arbitrary waveform generator in 14 nm for spin qubit control,” 2022, doi: 10.1109/ESSCIRC55480.2022.9911459.

Quantum Information Processing (QIP)

2022 Edition

4.1. **Introduction**

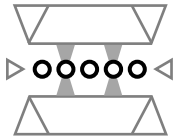
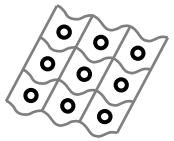
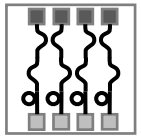
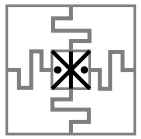
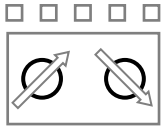
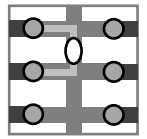
4.2. **Applications and Market Drivers for QIP**
- 4.2.1. Optimization
- 4.2.2. Cryptanalysis
- 4.2.3. Quantum Simulation
- 4.2.3. Quantum Machine Learning

4.3. **Present Status for QIP**
- 4.3.1. Regional Efforts in QIP
- 4.3.2. Analog Quantum Computing: Status
- 4.3.3. Gate-Based Quantum Computing: Status
- 4.3.4. Topological Quantum Computing: Status
- 4.3.5. Quantum Communication and Sensing: Status

4.4. **Benchmarking and Metrics for QIP**

4.5. **Active Research Questions for QIP**

Quantum computing: Still a race with several contenders

	Natural qubits			Synthetic qubits			
Qubit:	 **Trapped ion**	 **Neutral atom**	 **Photonic**	 **Superconducting**	 **Quantum dot**	 **Topological**	 **N-V diamond**
Basis	Electron spin of ionized atoms	Internal states of atoms trapped in an optical lattice	Optical photons in waveguides	Nonlinear oscillator circuits containing Josephson junctions	Impurity dopants in a semiconductor	Majorana particles in nanowires	Spin state of N atom + vacancy defect in diamond
$E_{transition}$ (= hf, k_BT)	1 – 700 THz 50 – 30,000 K	~ 4 MHz ~ 200 µK	100 – 200 THz 4,800+ K	2 – 10 GHz 0.1 – 0.5 K	10 – 50 GHz 0.5 – 2.5 K	?	300 – 800 THz 15,000+ K
T_{system}	1 – 300 K	4 – 300 K	1 – 300 K	0.01 – 0.05 K	0.1 – 1 K	?	1 – 300 K
Pros	Long lifetime, low gate error	Many qubits, 2D, maybe 3D	Linear optical gates, photonic IC	Fast gates, adjustable, easy fabrication size	High density, CMOS compatible	Lower errors	Room temperature operation?
Cons	Slow gates, vacuum, many lasers	Hard to control individual qubits, noise, high errors	Superconducting single photon detectors	T noise, variability, large size, mK temperatures	T noise, low temperatures, high errors	Device? Magnetic field?	Variability, detector?

System temperatures vary by approach

Gate-Based Quantum Computing Status Summary

Early attempt at comparisons

- The overall picture is that no approach has emerged as most likely to scale to the millions of qubits needed.

Qubit type	*Quantum volume*	*Qubit count*	*Qubit connectivity*	*2-qubit gate depth*	*Quantum teleportation*	*Qubit function*	*System scalability*
Superconducting	512	127	3.25	667	0.42 m	fair	fair
Trapped ion	4096	32	10	> 100,000	yes	fair	fair
Quantum dot	—	4	1	104	-	poor–fair	fair–good
Photonic	—	4			1400 km	poor	fair

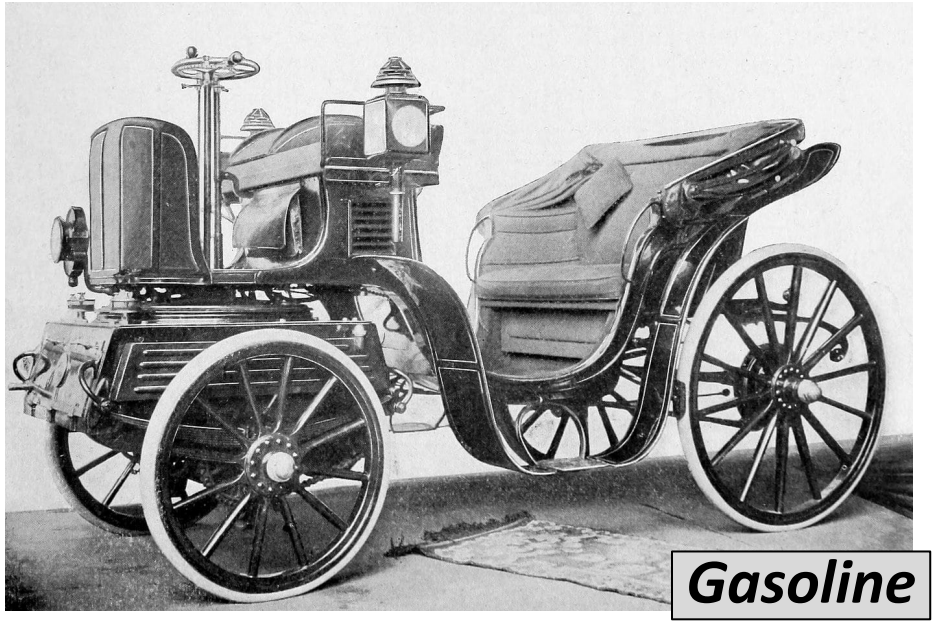
2022 Table CEQIP-23

Quantum volume metric: https://en.wikipedia.org/wiki/Quantum_volume
2-qubit gate depth: ratio of coherence time divided by 2-qubit gate time (T_2^*/t_{2q})

- Better method needed!

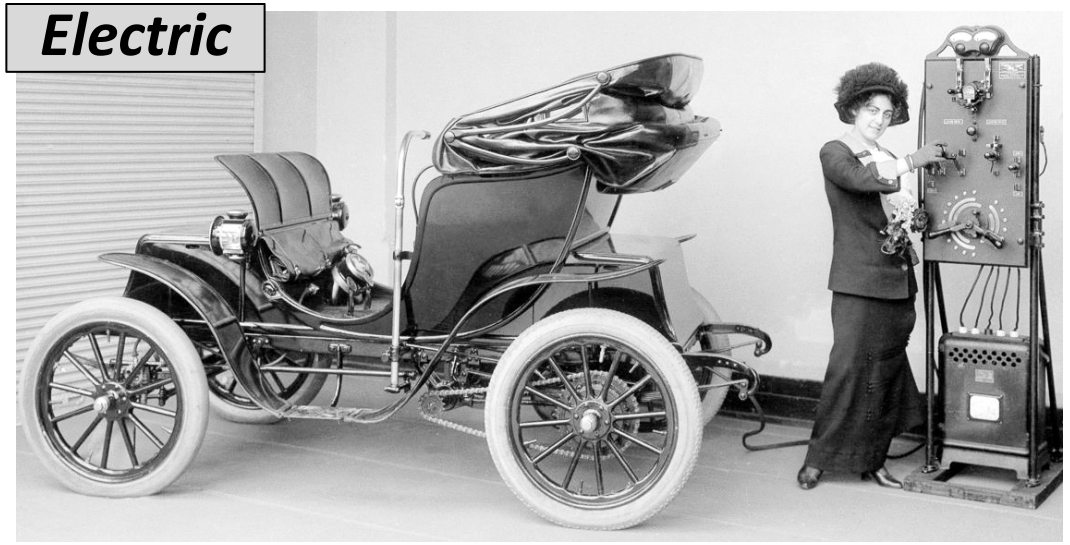
Searching for a winning combination (QC edition)

Automobile analogy, circa 1900



Gasoline

Electric



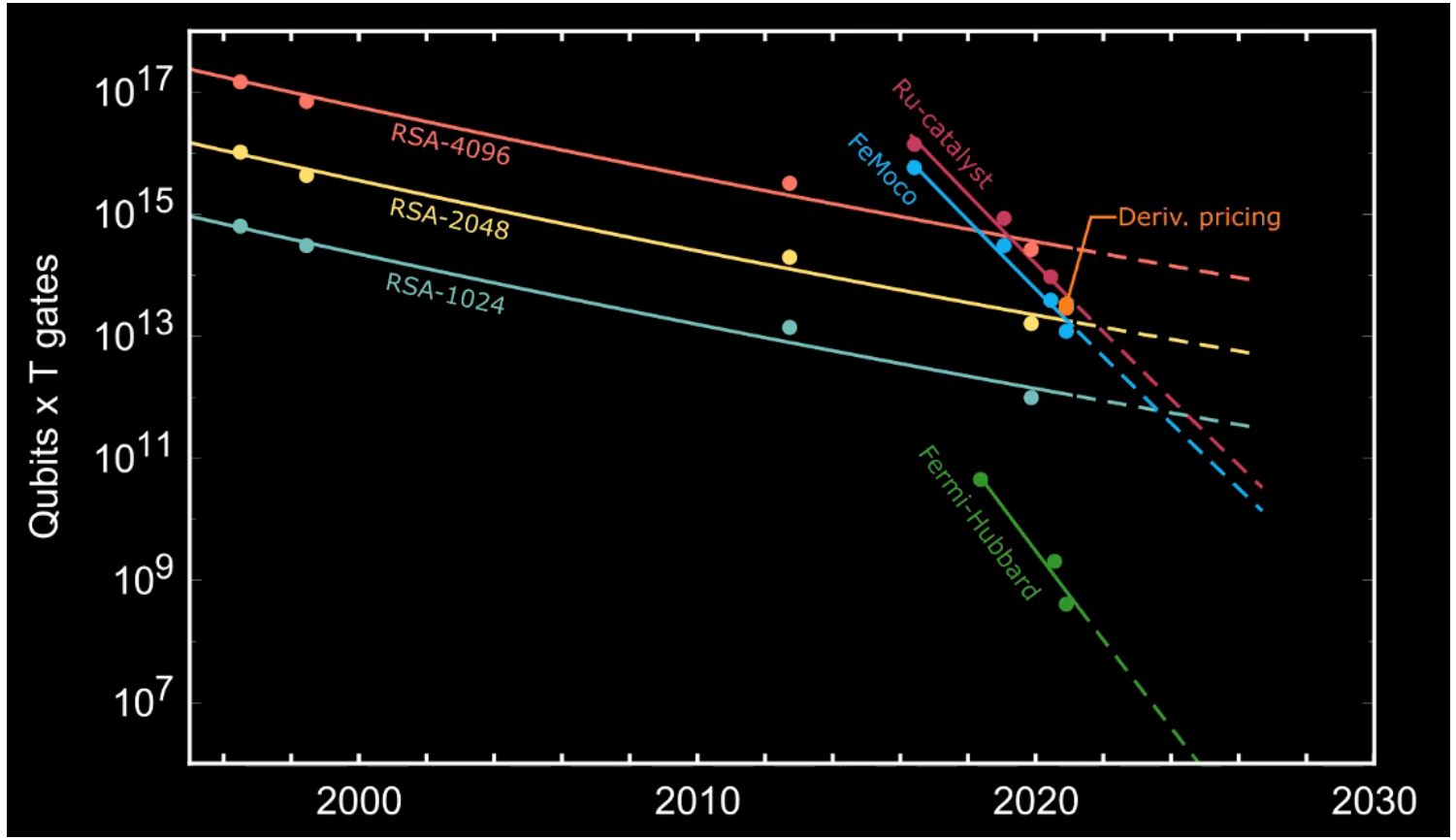
Steam

- The eventual winner was not obvious at the time.

Application Requirements

Key applications require millions of qubits and billions of quantum gate operations

- **Derivative pricing**: Financial market pricing of options
- **FeMoco**: Find the complex chemical process behind nitrogen fixation
- **Fermi-Hubbard**: model for strongly-correlated electronic systems
- **RSA**: Breaking RSA encryption (Rivest–Shamir–Adleman) with the indicated number of bits
- **Ru-catalyst**: Understand and possibly replace the Ru catalyst used in the Haber-Bosch process to produce ammonia



T gate: $\pi/4$ rotation around Z axis on the Bloch sphere

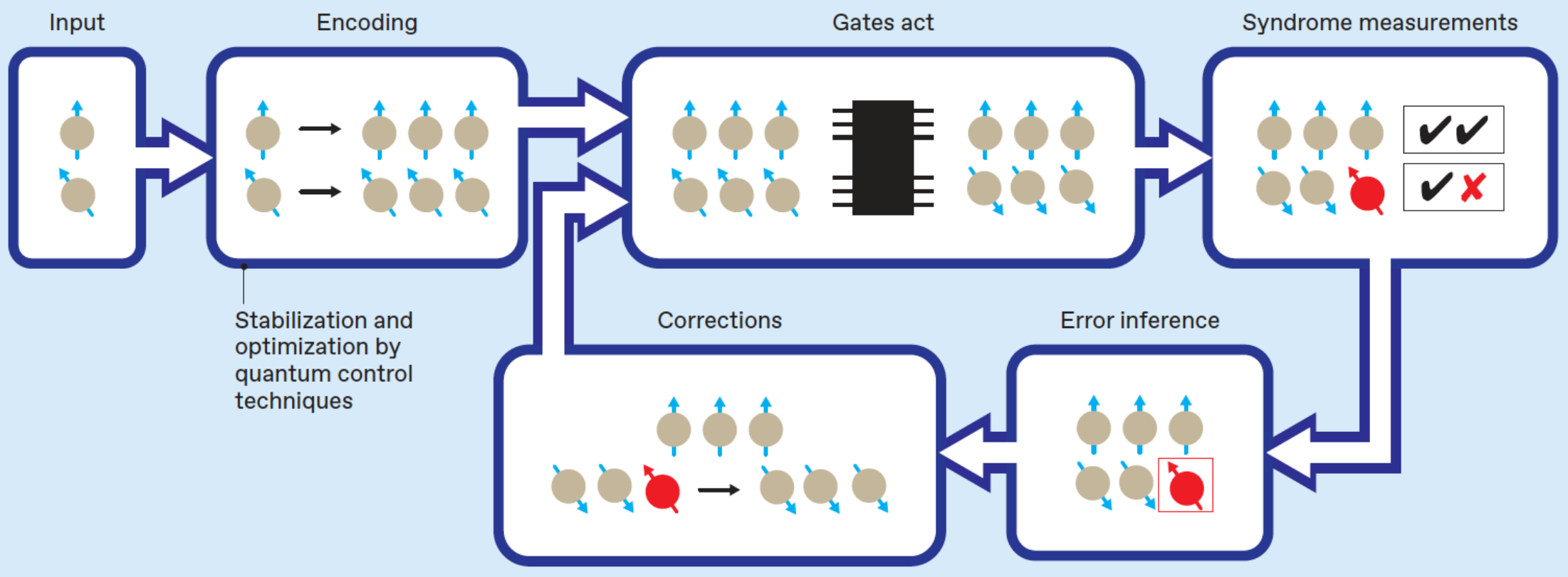
Credit: Mercedes Gimeno-Segovia (PsiQuantum) QCE22, 2022-09-20

Quantum Computing Process Overview

Gill +, "Quantum computing: A taxonomy, systematic review and future directions", 2022, doi: [10.1002/spe.3039](https://doi.org/10.1002/spe.3039)

- Optimize the complete system!

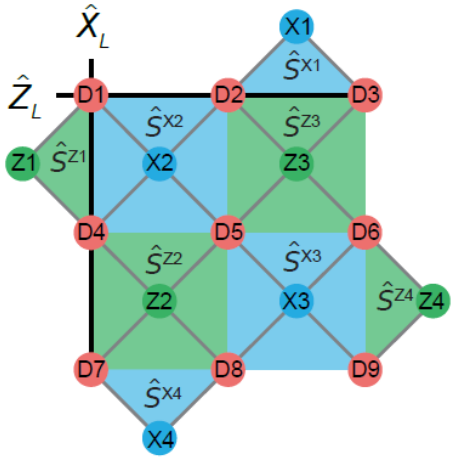
Gate Operation Cycle in Quantum Computing

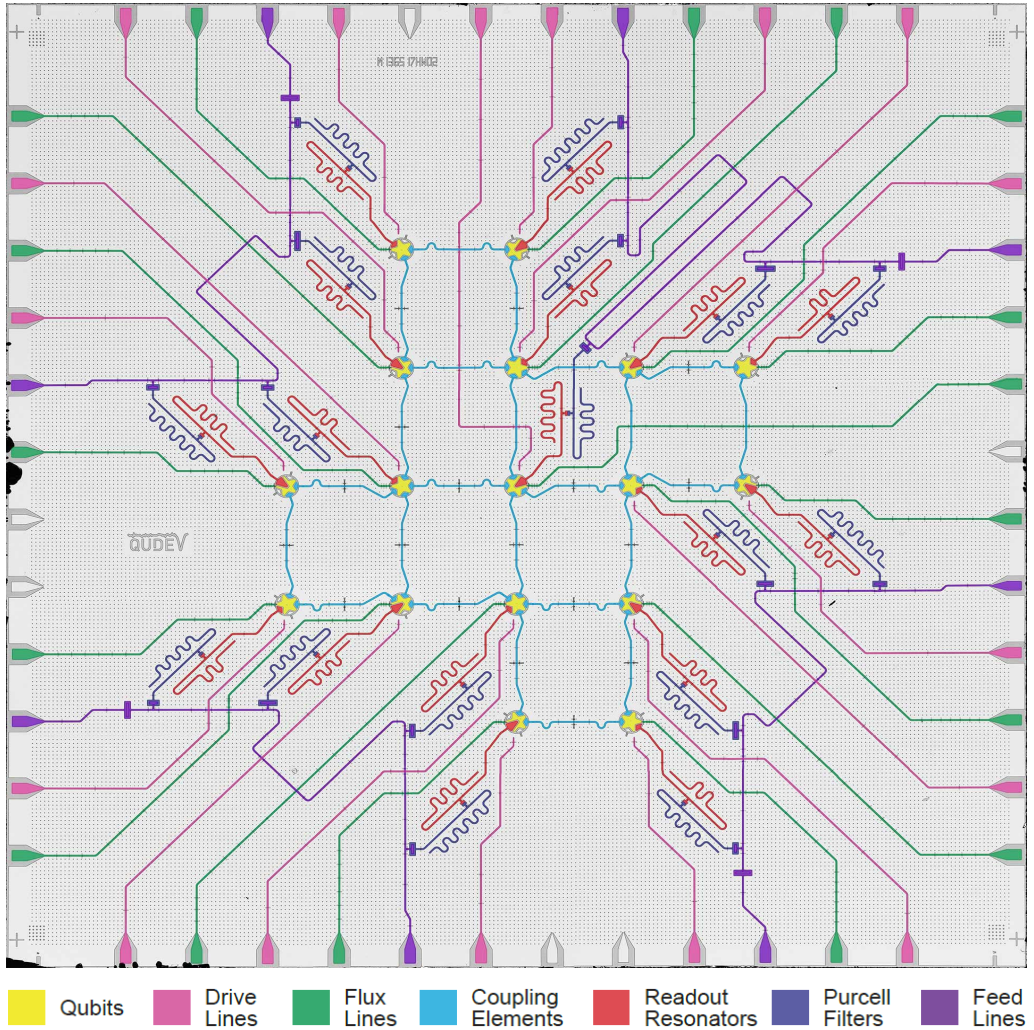


Biercuk and Stace, "Quantum error correction at the threshold," *IEEE Spectrum*, 2022, doi: 10.1109/MSPEC.2022.9819881

Distance-3 Surface Code Qubit Chip

- Chip size ~ 15 mm × 15 mm
- Qubits are too small to see!
  - D 9 Data qubits (3×3 grid)
  - X 4 X-type auxiliary qubits (phase flip errors)
  - Z 4 Z-type auxiliary qubit (bit flip errors)
    - 9+4+4 = **17** qubits total
- Plenty of space for control line connections (low overall circuit density)
- Logical qubit error probability was only slightly worse than the physical qubit error probability, indicating progress towards error reduction



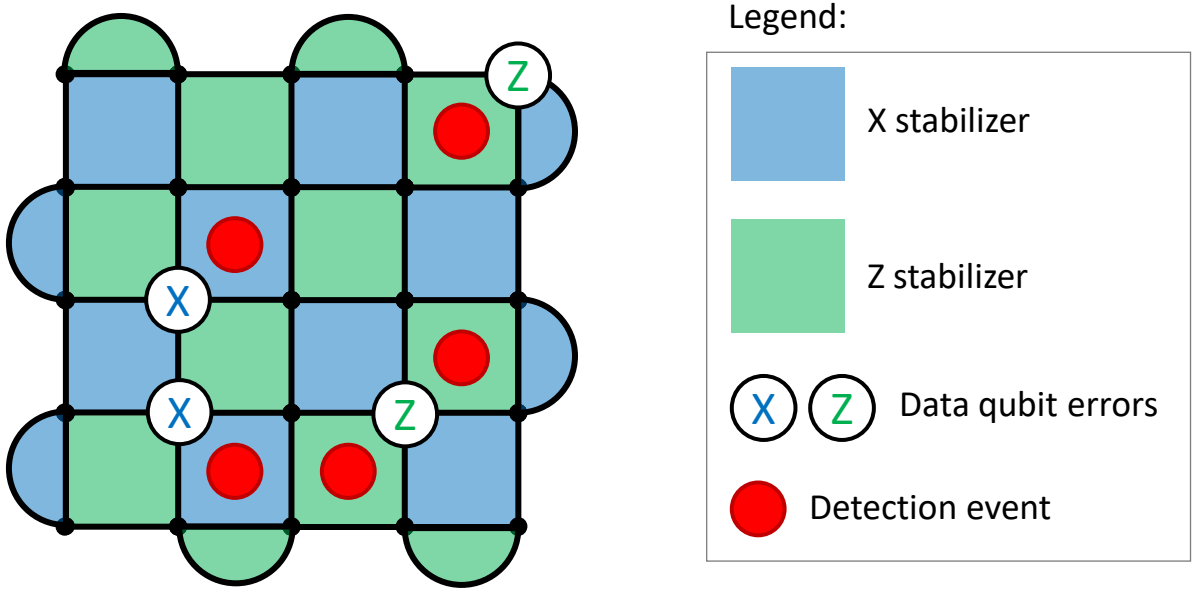


Krinner +, "Realizing repeated quantum error correction in a distance-three surface code", 2022, doi: 10.1038/s41586-022-04566-8

Error Inference by ‘Decoding’

Use syndrome pattern to determine error location, type

- Error types
  - Bit flip (Z) errors detected by Z stabilizers
  - Phase flip (X) errors detected by X stabilizers
  - Bit + phase flip (Y) errors
  - Measurement errors
- Limited number of correctable errors
  - Surface code = $(d - 1)/2$
  - Depends on the EC code

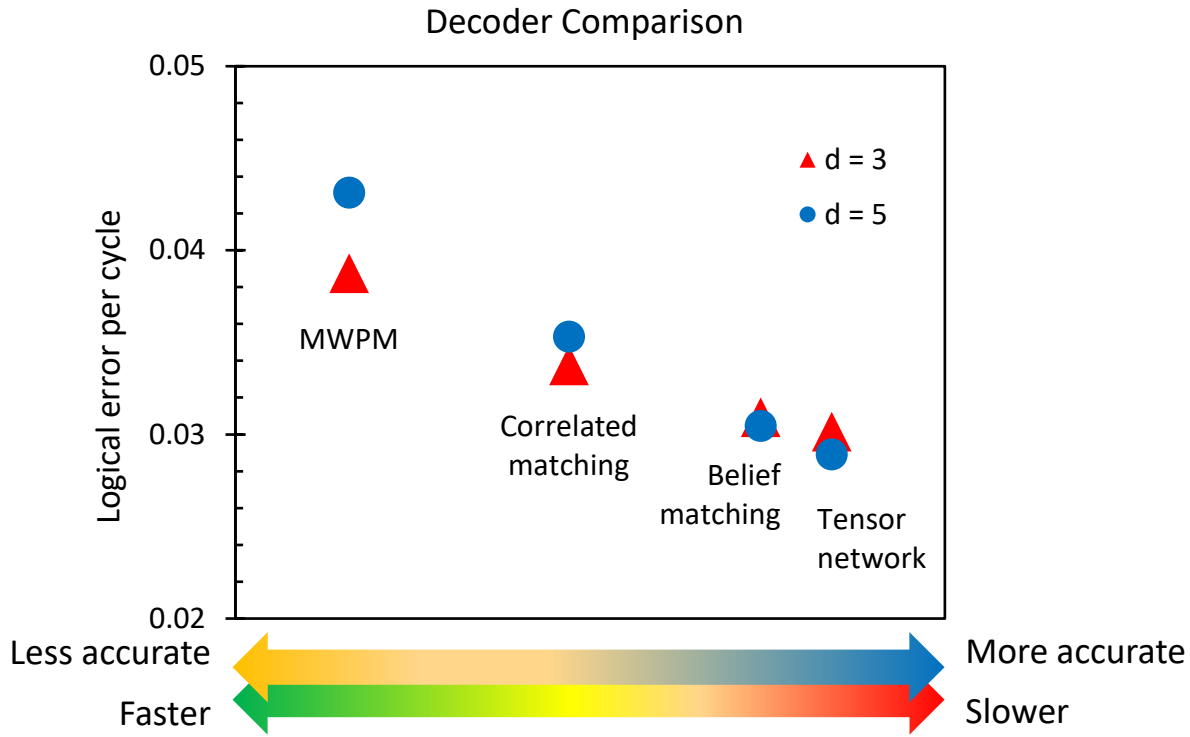


Error Correction: Decoder Considerations

Why decoders for superconducting quantum computing must be fast

- Difficulty grows with
  - Code size
  - Error number and characteristics
  - Measurement rate
- Example:
  - d = 30 surface code (1799 physical qubits)
  - 1 µs per error correction cycle (<< T1, T2)
  - = ~ 1 Gbit/s per logical qubit
  - = ~ 1 Pbit/s per million logical qubits
- Lookup tables can't handle the complexity!
- Latency determines error correction cycle time and thus overall computation speed

▸ More system-level tradeoffs

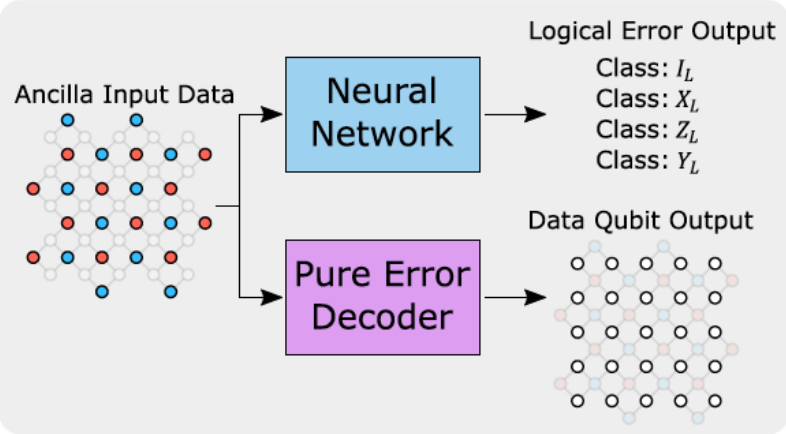


Newman, "Decoding experimental surface code data," Google Quantum Summer Symposium, July, 2022. https://www.youtube.com/watch?v=UP0AoXCT9xU

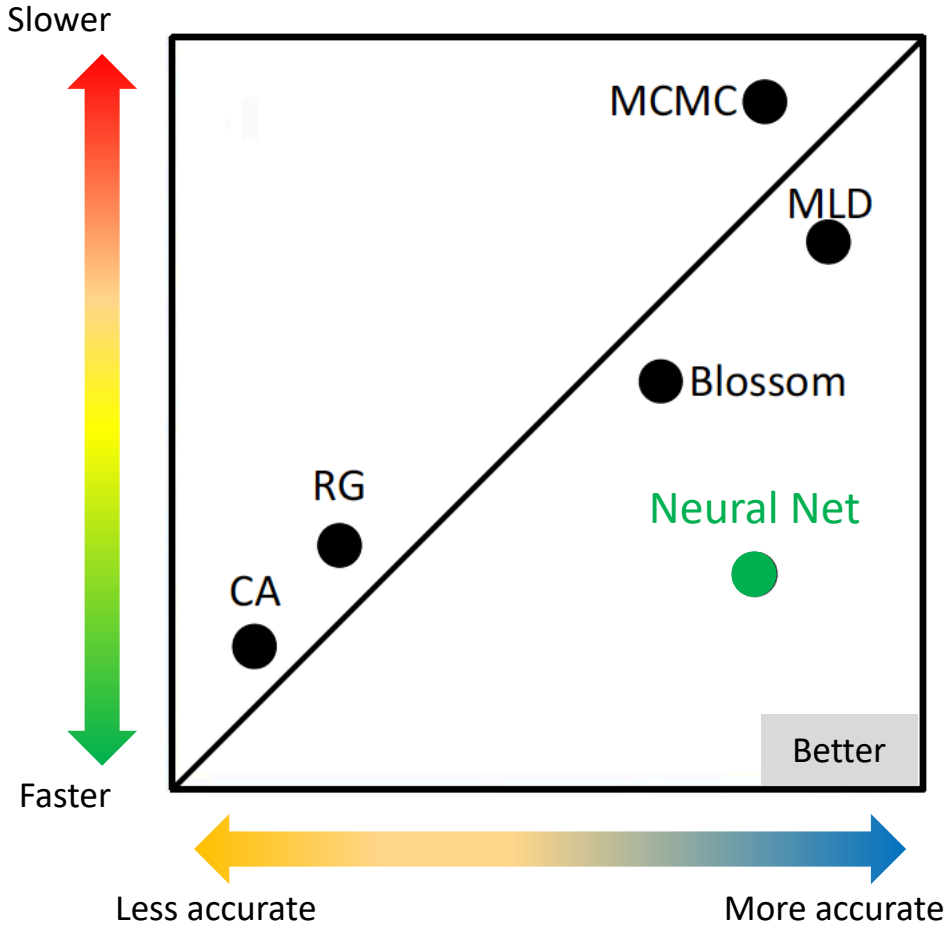
Decoder Options

Need fast and accurate pattern recognition

- Computation by
  - Classical, digital processing (supercomputer?)
  - Neural network
  - Quantum processing (?)



Overwater +, "Neural-network decoders for quantum error correction using surface codes," 2022, doi: 10.1109/TQE.2022.3174017

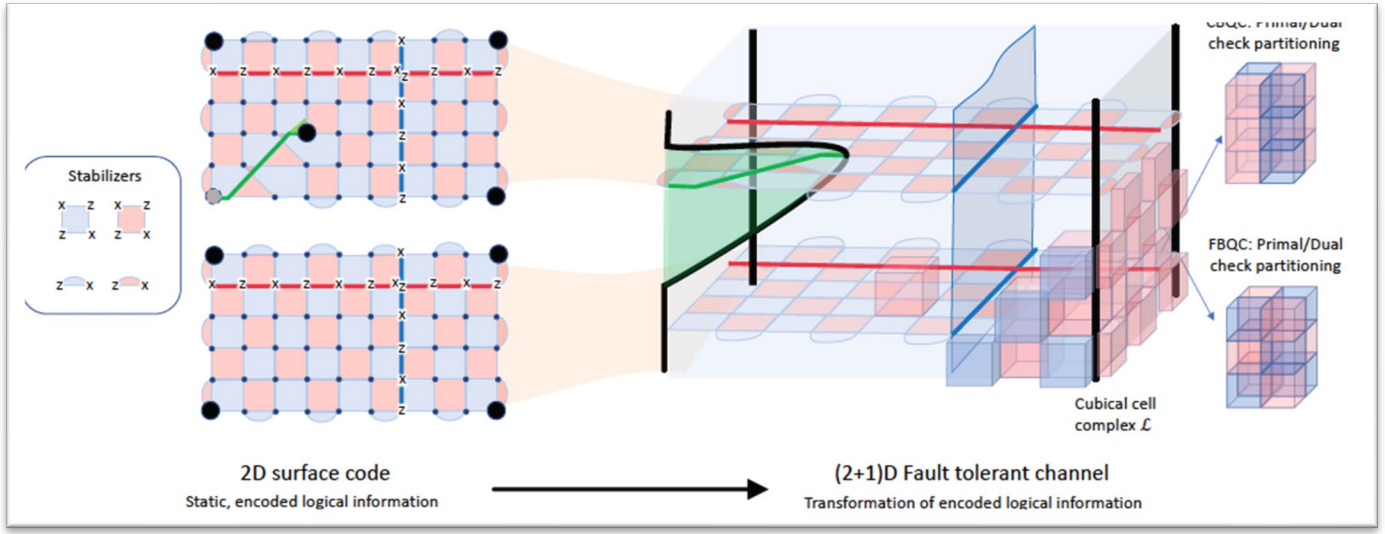


Varsamopoulos +, "Decoding surface code with a distributed neural network–based decoder," 2020, doi: 10.1007/s42484-020-00015-9

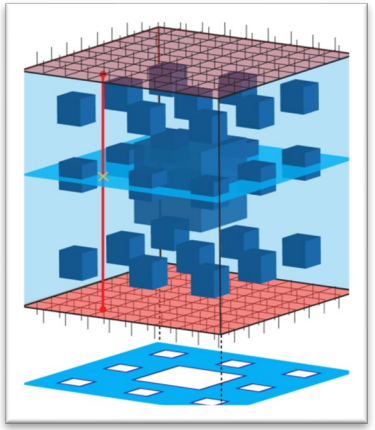
Error Correction: Alternatives to the Surface Code

There is more than one way to skin a qubit!

- Low-density parity check (LDPC) codes [1]
  - 2D, 4D hyperbolic codes
  - Freedman-Meyer-Luo codes
  - Tensor products
  - Fibre bundle codes
  - Lifted product codes
  - Balanced product codes
- Logical blocks [2]
- Fractal and topological codes [3, 4]



Logical block formation [2]



3D fractal surface code [3]

[1] Breuckmann +, "Quantum low-density parity-check codes," 2021, doi: 10.1103/PRXQuantum.2.040101

[2] Bombin +, "Logical blocks for fault-tolerant topological quantum computation," 2021, arXiv:2112.12160

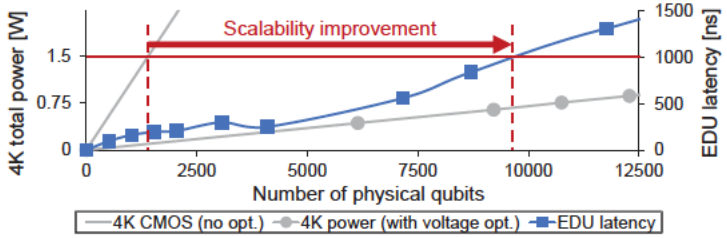
[3] Zhu +, "Topological order, quantum codes, ... fractal geometries," 2022, doi: 10.1103/PRXQuantum.3.030338

[4] Kubica +, "Single-shot quantum error correction ... toric code", 2022, doi: 10.1038/s41467-022-33923-4

Limits for superconducting qubit control

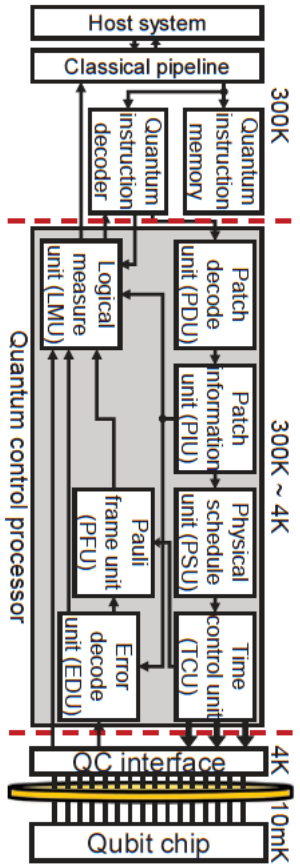
Where are the breakpoints?

- **XQsim**: quantum control processor simulator (open-source, cross-technology)
- Scalability analysis
  - Maximum number of qubits subject to constraints (delay, power, area)
  - Did not include QC interface



CMOS @ 4 K scalability analysis [1, Fig. 17b]

[1] Byun +, "XQsim: modeling cross-technology control processors for 10+K qubit quantum computers," Jun. 2022, doi: 10.1145/3470496.3527417.



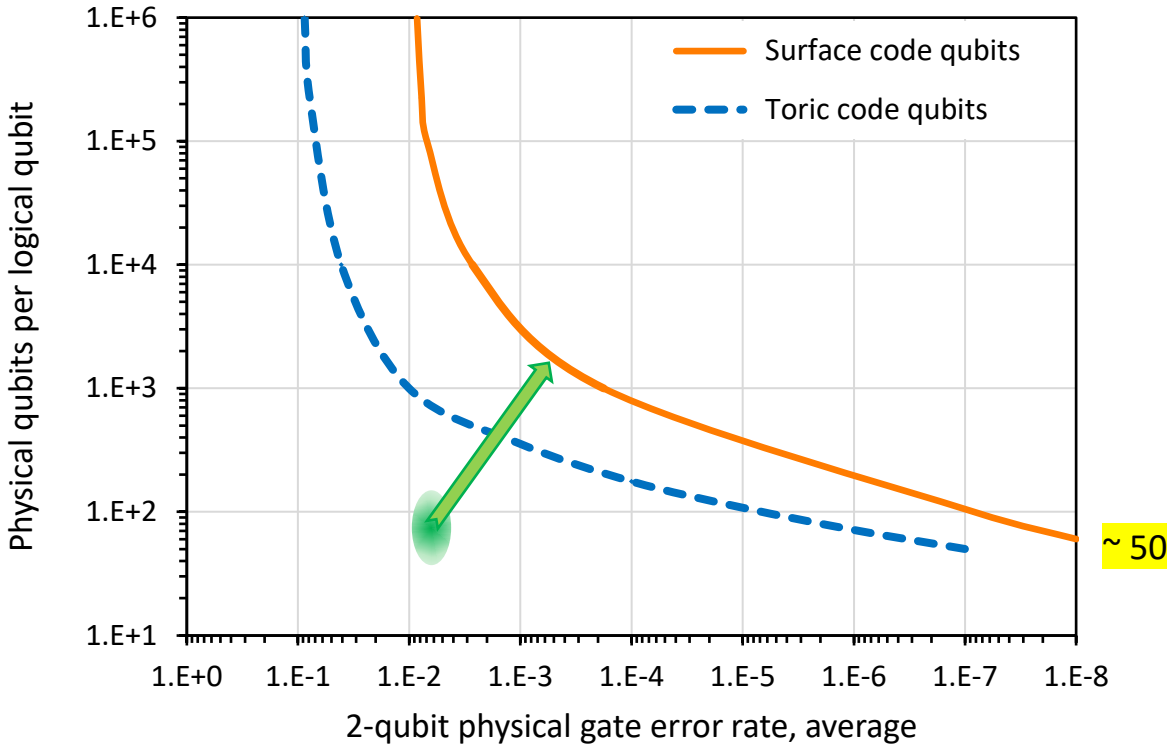
Fault-tolerant quantum computer system overview [1, Fig. 1]

Error decoder	
1e-3	Phys. error rate
15	Code distance
QECOOL:	Baseline error decoder
Physical quantum gate latency	
14 ns	1-qubit gate
26 ns	2-qubit gate
600 ns	Measurement
Refrigeration and wiring	
1.5 W	4 K power budget
620 cm^2	4 K area budget
31 mW, 10 Gb/s coaxial cable 300-4 K	
Clock frequency	
1.5 GHz	CMOS @ 4 K or 300 K
21 GHz	RSFQ or ERSFQ @ 4 K
Qubits controllable (limiting factor)	
1,700	CMOS @ 300 K (heat leak)
9,800	CMOS @ 4 K (delay)
4,600	RSFQ @ 4 K (power)
59,000	ERSFQ @ 4 K (power)
?	AQFP @ 4 K (?)

Error Correction Resources

Number of physical qubits per logical qubit depends on several factors

- Examples:
  - Surface code [1] with $p_{th} \approx$ 1.E−2,
    Perfect decoder,
    Logical error: p_L = 1.E−18
  - Toric code [2] with $p_{th} \approx$ 1.E−1,
    Perfect decoder,
    Logical error: p_L = 1.E−15
- Needed:
  - Better EC codes (high threshold)
  - Hardware to implement the EC code
  - Lower gate error rates
    (~ 100× below threshold)



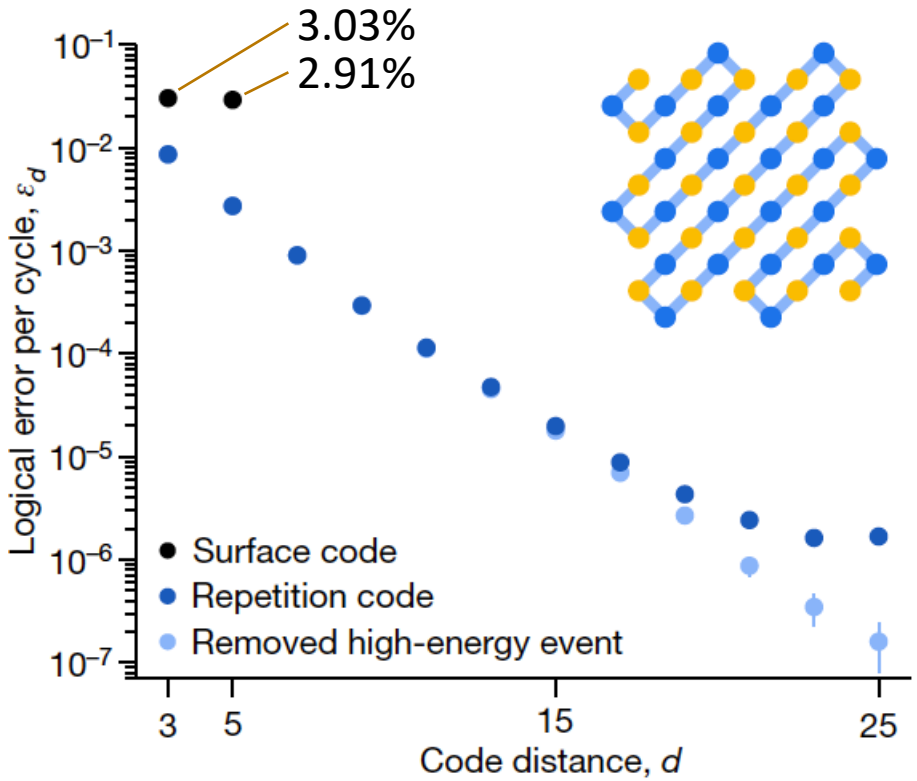
[1] Sevilla and Riedel, "Forecasting timelines of quantum computing," Dec. 2020. arXiv:2009.05045
[2] Biercuk, QCE, 2022-09-20; extrapolation based on: Watson +, New J. Phys. 16, 093045 (2014)

QEC Status Update

First demonstration of improvement in the logical error with increasing code size

- Google Quantum hardware
  - 72-qubit superconducting device
  - 17-qubit distance-3 (d = 3) surface code
  - 49-qubit distance-5 (d = 5) surface code
  - 49-qubit d = 3 to 25 repetition codes
- Surface code logical error improvement was slight but larger than the experimental error
- Next steps:
  - Bigger codes
  - Lower physical qubit error rates
  - Cosmic ray mitigation

▸ Milestone 2 of 6 to get to a 1000 qubit QC

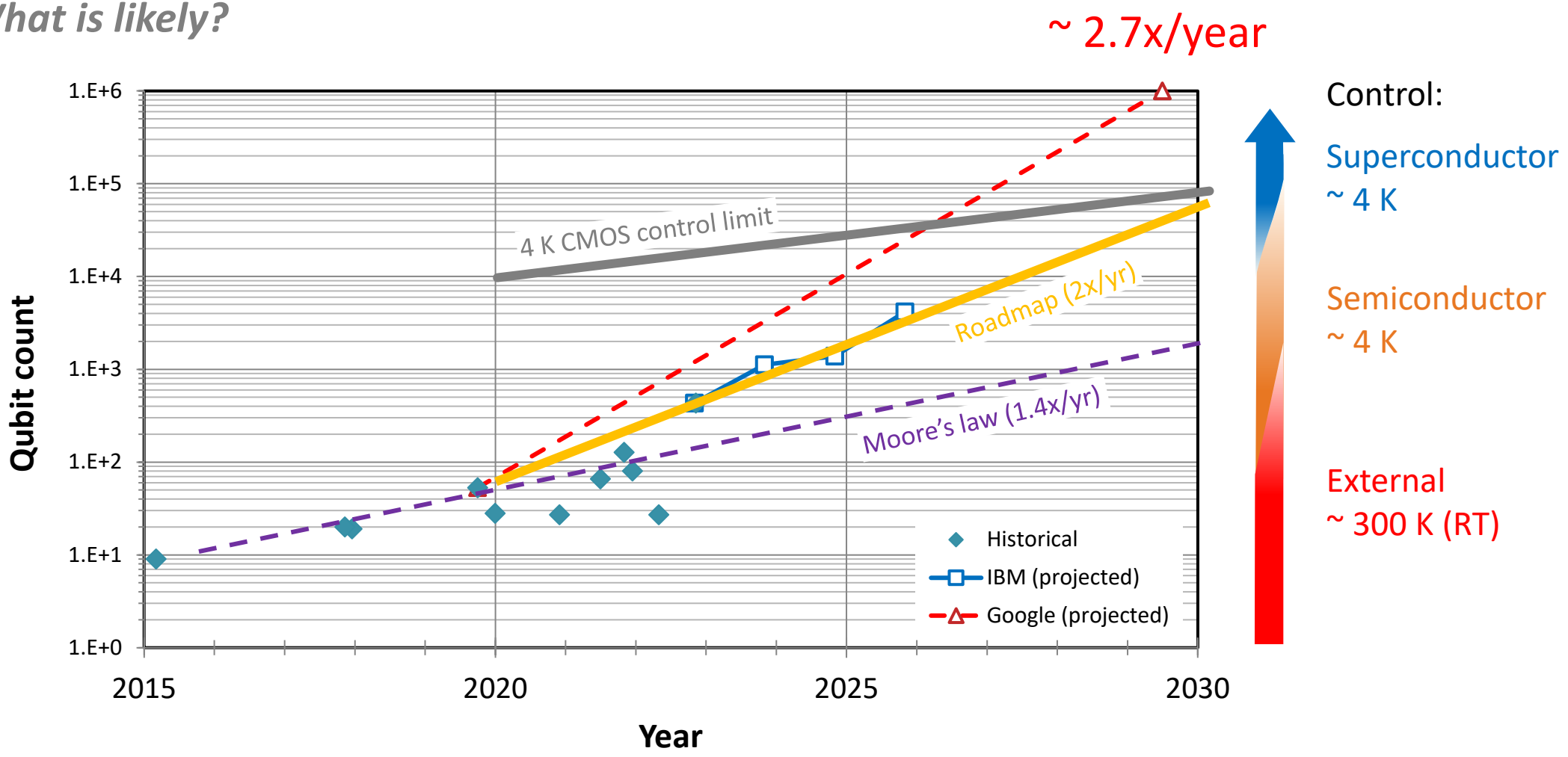


Acharya +, "Suppressing quantum errors by scaling a surface code logical qubit," *Nature*, Feb. 2023, doi: 10.1038/s41586-022-05434-1

(158 authors!)

Superconducting Qubit Roadmap

What is likely?



Google: https://www.cnet.com/tech/computing/quantum-computer-makers-like-their-odds-for-big-progress-soon/

IBM: https://research.ibm.com/blog/ibm-quantum-roadmap-2025

Historical: 2023 Figure CEQIP-8

Superconducting QC Roadmap

Metric	2020	2022	2024	2026	2028	2030	2032
Qubit growth per year	2×	2×	2×	2×	2×	2×	2×
Qubit count	5.5e+1	2.2e+2	8.8e+2	3.5e+3	1.4e+4	5.6e+4	2.2e+5
Qubit type	Transmon	Transmon	Transmon	Transmon	?	?	?
Qubit lifetime T1, med. [ms]	0.5					10	
2 qubit gate error rate, median (p_2Q)	1.0e-2					1.0e-4	
Gate depth (1/p_2Q)	1.0e+2					1.0e+4	
Error correction code	Surface	Surface	Surface	Surface	Surface	Surface	?
Phys. qubits per logical qubit				1800	1800	1568	1568
Logical qubit count				1	7	35	140
Logical qubit error rate						1.0e-15	
Control type, temp. [K]	CMOS, 300	CMOS, 300	CMOS, 300	CMOS, 4	CMOS, 4	CMOS, 4	SCE, 4
SCE control complexity [JJ]	1.1e+5	4.5e+5	1.8e+6	7.2e+6	2.9e+7	1.2e+8	4.6e+8

In Progress

2022 Difficult Challenges (Near-term) for QC

Technology roadblocks, gaps, and possible disconnects within the roadmap

Near-Term Challenges: 2022–2029	*Summary of Issues (why is it a challenge?)*
Physical qubits	• Design and fabrication of qubit devices with enhanced qubit coherence times and gate fidelities
Logical qubits	• Implementation of fully error-corrected logical qubits and protected gate operations
Readout of qubits	• Development of scalable, cryogenic qubit readout hardware
Interconnects, cryogenic to room temperature	• Development of low thermal conductance and high bandwidth interconnects between different temperature stages of cryogenic- and room-temperature electronics
Control electronics	• Location close to the qubits has the lowest latency but too close can disturb the qubits. Operating environments close to the qubits can be challenging (e.g., cryogenic, high vacuum).

- We still don't know how to build a full-scale quantum computer.

Recommendations

For the 2024 Edition

1. Superconductor Electronics (SCE)
   - Roadmap based on driver applications (QC, others?)
   - Difficult challenges need timelines to solution

2. Cryogenic Semiconductor Electronics (Cryo-Semi)
   - Continue to monitor status

3. Quantum Information Processing (QIP)
   - Roadmap superconducting quantum computing, start roadmap for ion trap QC (others?)
   - Members needed to improve coverage!

Backup

2023 CEQIP Members

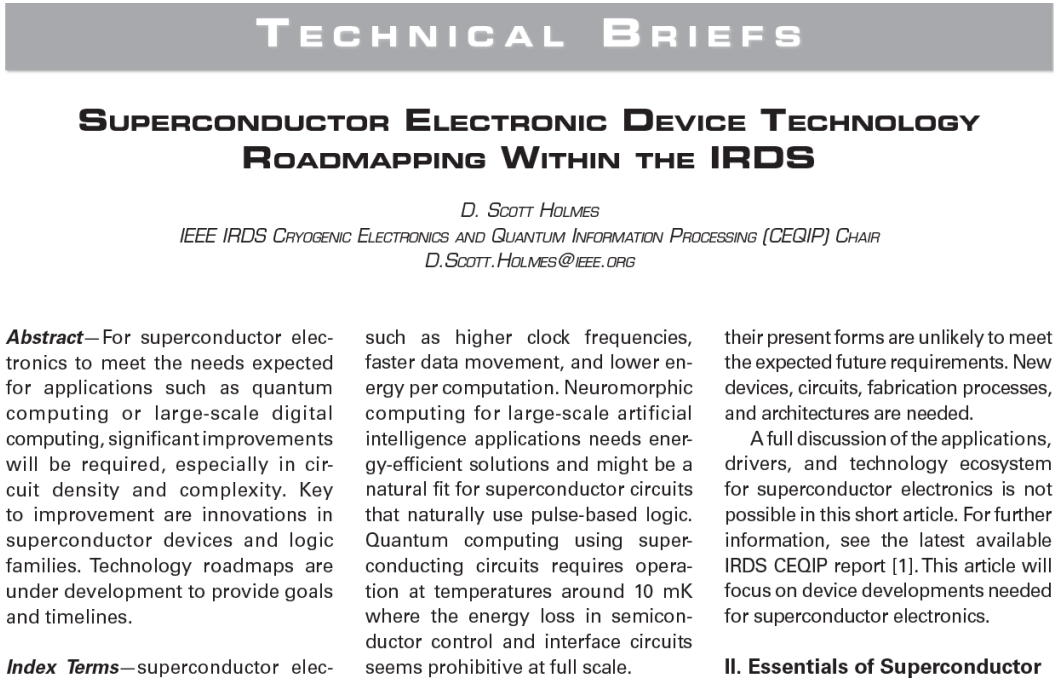
Name	Area	Organization	Region
Byun, Ilkwon	Cryo-Semi, QIP-QC	Seoul National University, Korea	Asia
Cuthbert, Michael	Cryo, QIP	National Quantum Computing Centre, UK	Europe
DeBenedictis, Erik	QIP-QC	Zettaflops, USA	Americas
Delfanazari, Kaveh	QIP-QC	University of Glasgow, UK	Europe
Fagaly, Bob	SCE-App	Honeywell (retired), USA	Americas
Fagas, Giorgios	QIP	Tyndall National Institute, Ireland	Europe
Febvre, Pascal	SCE-Fab	Université Savoie Mont Blanc, France	Europe
Filippov, Timur	SCE-Log	Hypres, USA	Americas
Fourie, Coenrad	SCE-EDA	Stellenbosch University, South Africa	Africa
Frank, Mike	SCE-Log, -Rmap	Sandia National Laboratories, USA	Americas
Gupta, Deep	SCE, Cryo-Semi	SEACORP, USA	Americas
Herr, Anna	SCE	IMEC, Belgium	Europe
Herr, Quentin	SCE	IMEC, USA	Americas
Holmes, D Scott [Chair]	SCE, Cryo-Semi, QIP	Booz Allen Hamilton, USA	Americas
Humble, Travis	QIP-QC	Oak Ridge National Laboratory, USA	Americas
Leese de Escobar, Anna	SCE-App, -Bench	Laconic, USA	Americas
Min, Dongmoon	Cryo-Semi, QIP-QC	Seoul National University, Korea	Asia
Mueller, Peter	QIP-QC-SC	IBM Zürich, Switzerland	Europe
Mukhanov, Oleg	QIP-QC, SCE-Log	Seeqc, USA	Americas
Nemoto, Kae	QIP	The National Institute of Informatics (NII), Japan	Asia
Papa Rao, Satyavolu	SCE-Fab, QIP	SUNY Polytechnic, USA	Americas
Pelucchi, Emanuele	QIP-QC	Tyndall National Institute, Ireland	Europe
Plourde, Britton	QIP	Syracuse University, USA	Americas
Soloviev, Igor	SCE	Lomonosov Moscow State University, Russia	Europe
Tzimpragos, George	SCE-Logic, -Metrics, -Rmap	University of Michigan, USA	Americas
Weides, Martin	SCE, QIP	University of Glasgow, UK	Europe
Yoshikawa, Noboyuki	SCE-Log, -Bench	Yokohama National University, Japan	Asia
You, Lixing	SCE	SIMIT, CAS, China	Asia

Additions for 2023

13: Americas
10: Europe + Africa
5: Asia
==========
28 total

References

1. "IRDS 2022: Cryogenic Electronics and Quantum Information Processing," IEEE International Roadmap for Devices and Systems, 2022. https://irds.ieee.org/editions/2022
2. D. S. Holmes, "Superconductor electronic device technology roadmapping within the IRDS," *IEEE Electron Devices Society Newsletter*, pp. 6–11, Apr. 2022. https://eds.ieee.org/images/files/newsletters/Newsletter_Apr22.pdf



TECHNICAL BRIEFS

SUPERCONDUCTOR ELECTRONIC DEVICE TECHNOLOGY ROADMAPPING WITHIN THE IRDS

D. SCOTT HOLMES
IEEE IRDS CRYOGENIC ELECTRONICS AND QUANTUM INFORMATION PROCESSING (CEQIP) CHAIR
D.SCOTT.HOLMES@IEEE.ORG

Abstract—For superconductor electronics to meet the needs expected for applications such as quantum computing or large-scale digital computing, significant improvements will be required, especially in circuit density and complexity. Key to improvement are innovations in superconductor devices and logic families. Technology roadmaps are under development to provide goals and timelines.

Index Terms—superconductor electronics, roadmapping, IRDS

such as higher clock frequencies, faster data movement, and lower energy per computation. Neuromorphic computing for large-scale artificial intelligence applications needs energy-efficient solutions and might be a natural fit for superconductor circuits that naturally use pulse-based logic. Quantum computing using superconducting circuits requires operation at temperatures around 10 mK where the energy loss in semiconductor control and interface circuits seems prohibitive at full scale.

their present forms are unlikely to meet the expected future requirements. New devices, circuits, fabrication processes, and architectures are needed.

A full discussion of the applications, drivers, and technology ecosystem for superconductor electronics is not possible in this short article. For further information, see the latest available IRDS CEQIP report [1]. This article will focus on device developments needed for superconductor electronics.

II. Essentials of Superconductor