Ferroelectric memories – Enabler for novel computing architectures

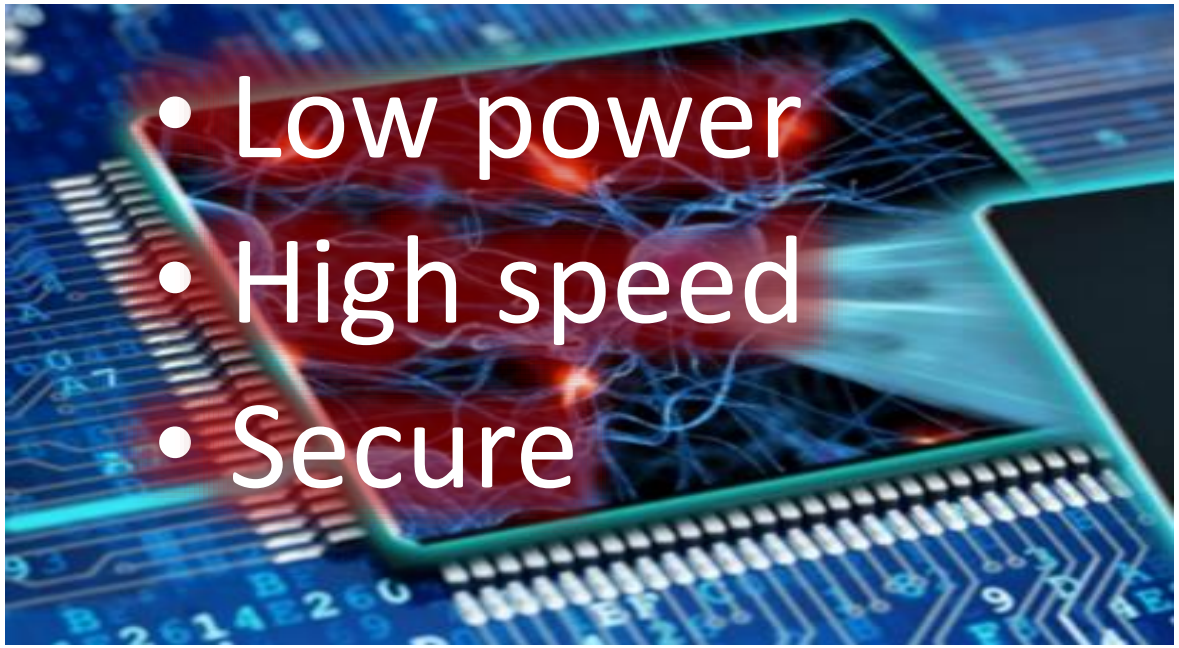
Konrad Seidel

Fraunhofer IPMS

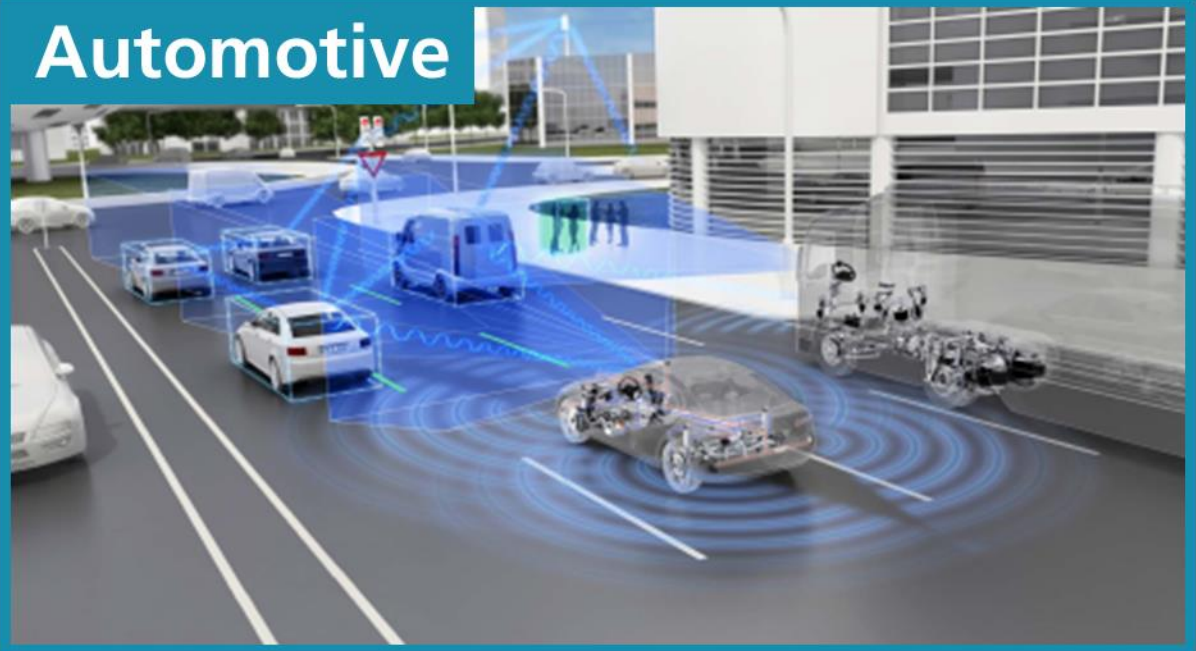
Automotive

Industry

Consumer / Medical



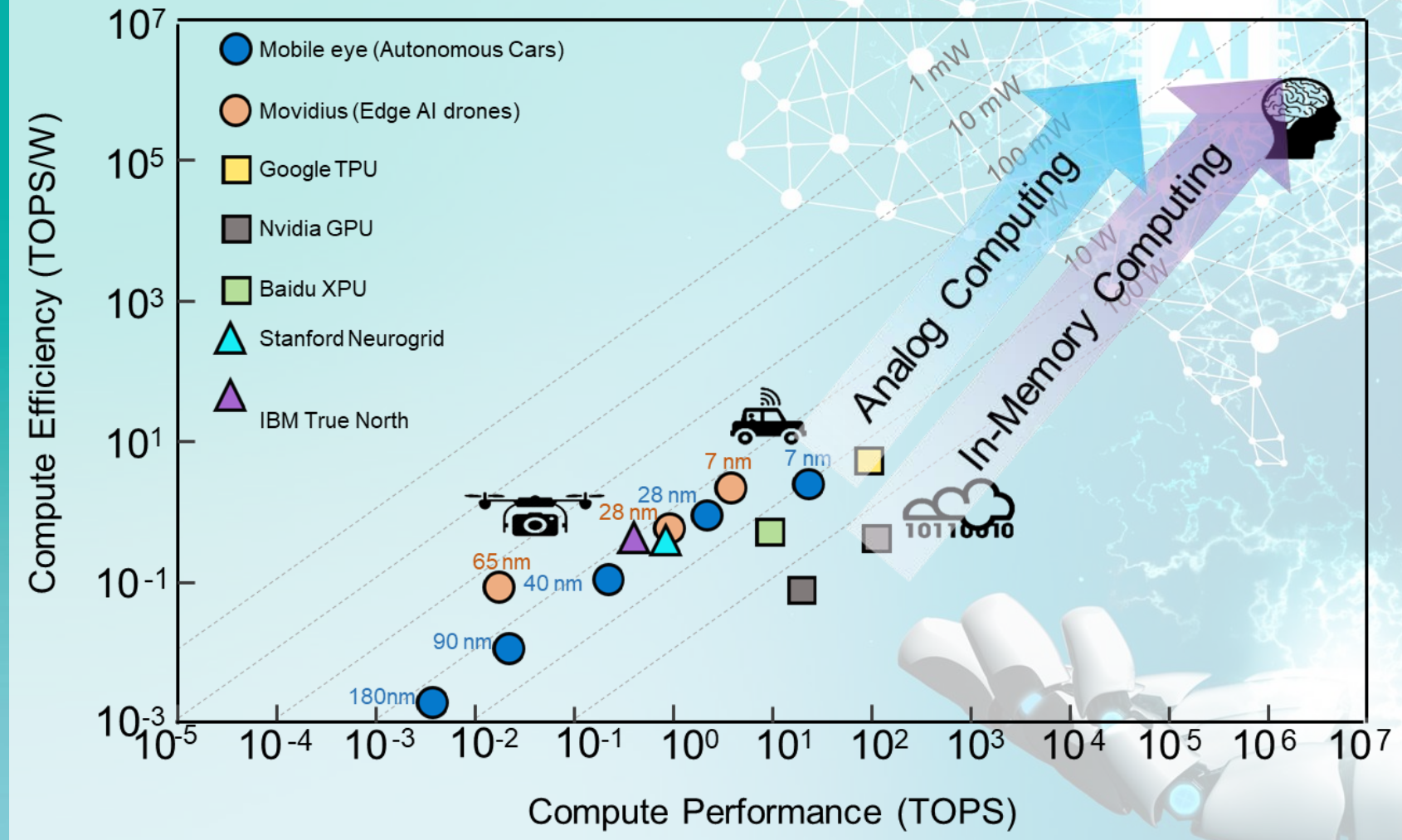
Automotive



Industry

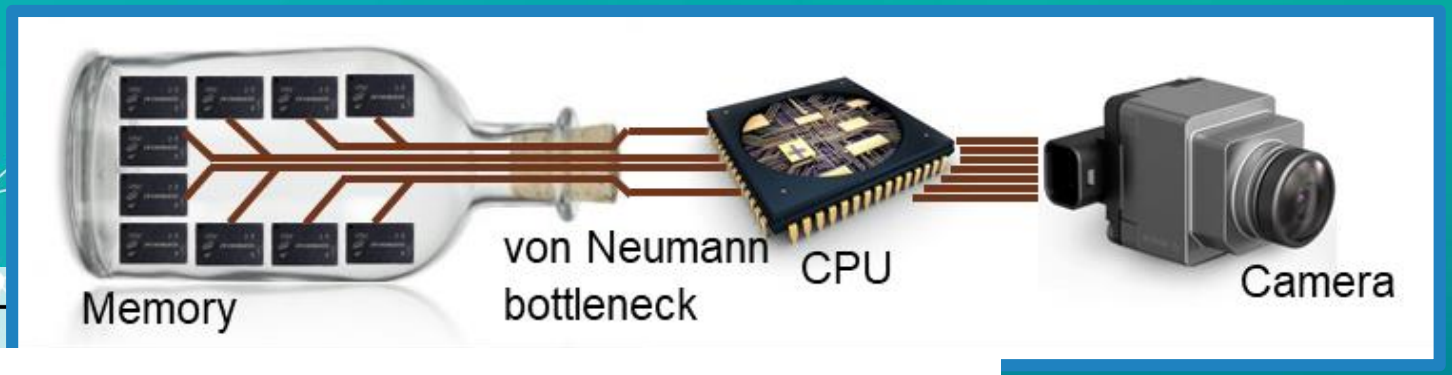
Consumer / Medical

- Low power
- High speed
- Secure

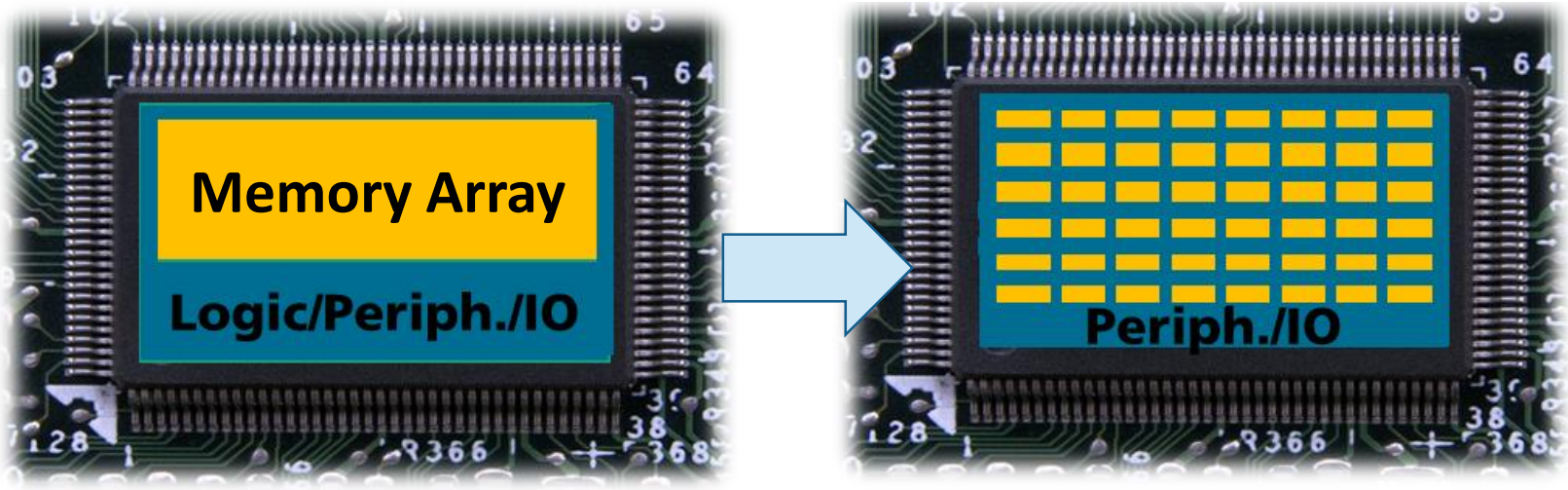


- **Low power**
- **Low latency**
- **Analog**

A. Keshavarzi et al., “Ferroelectronics for edge intelligence,” IEEE Micro 2020



Combine memory with computing

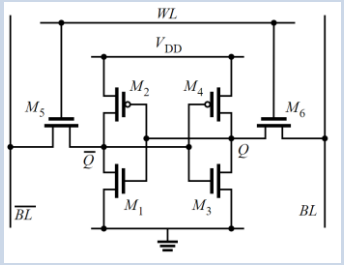
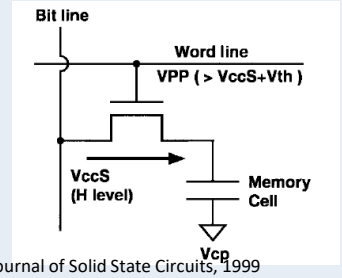
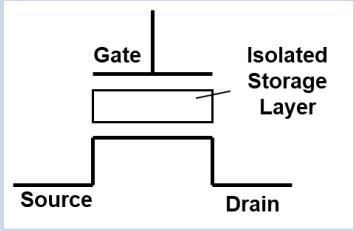


- power
- Low latency
- Analog

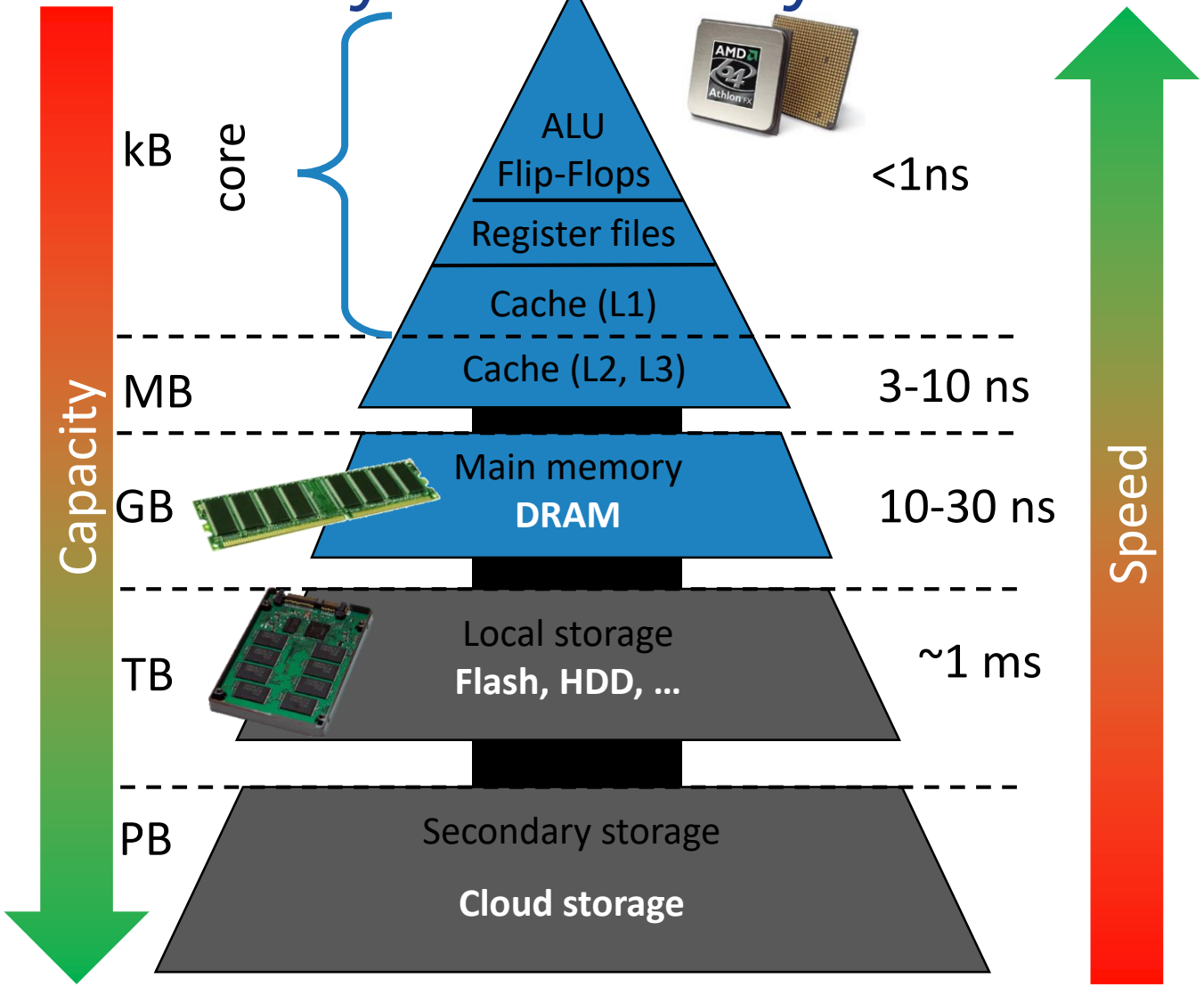
A. Keshavarzi et al., “Ferroelectronics for edge intelligence,” IEEE Micro 2020

Conventional Memory hierarchy

volatile | Non-volatile

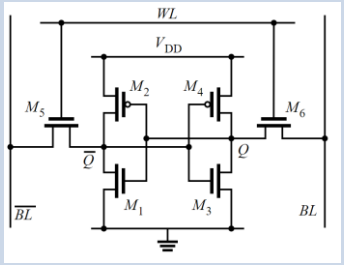
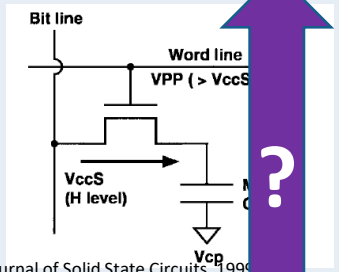
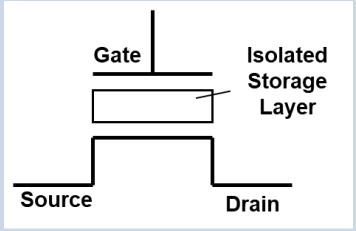
Technology	Volt	Speed	Size	NV
SRAM – 6T 	0.5V ☺	~1ns ☺	6T ☹	☹
DRAM – 1T1C 	0.8V ☺	10ns 😐	1T1C 😐	☹
Flash – 1T 	~12V ☹	10µs ☹	1T ☺	☺

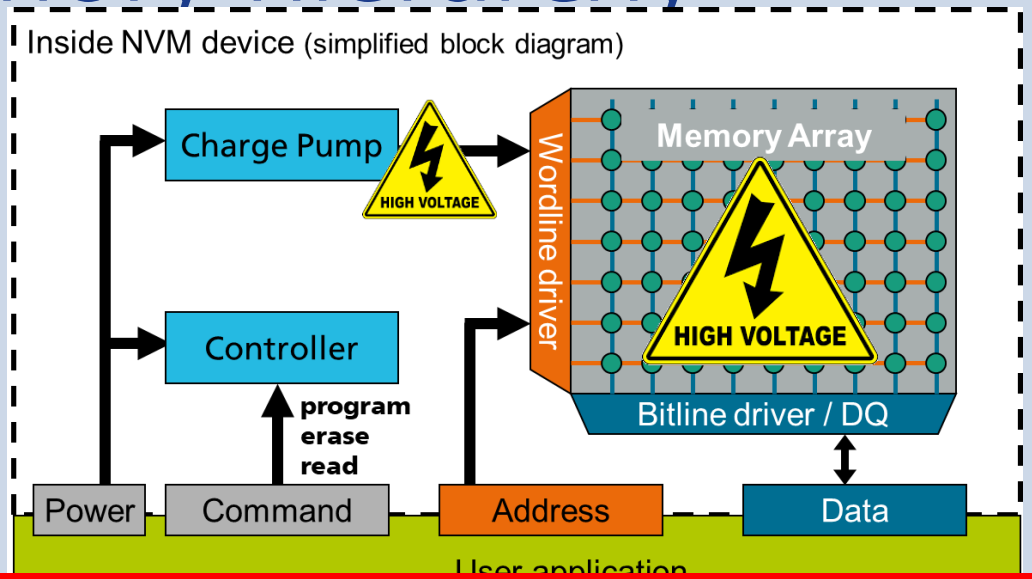
Yamazaki, Journal of Solid State Circuits, 1999



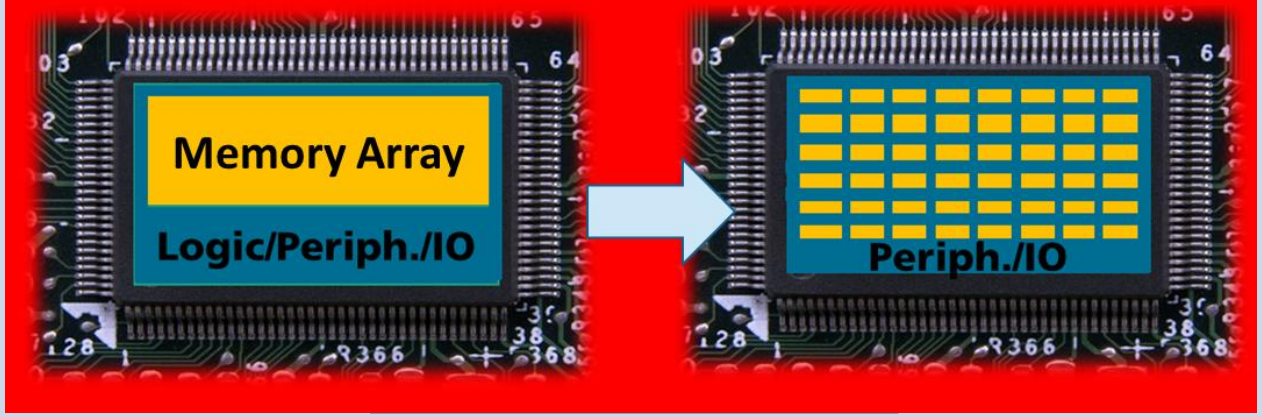
Adopted from: Bojan Jovanovic

Conventional Memory hierarchy

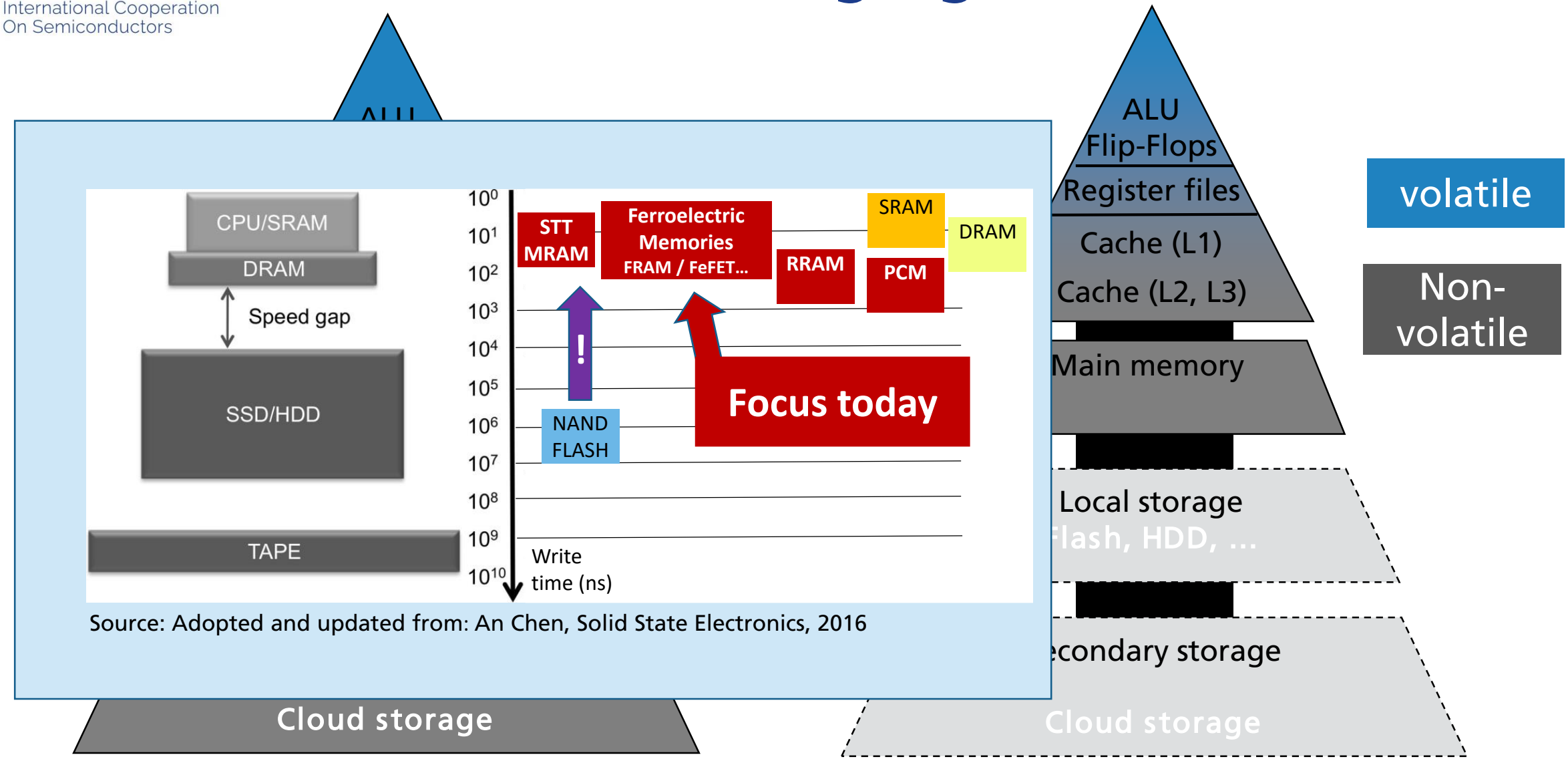
Technology	Volt	Speed	Size	NV
SRAM – 6T 	0.5V ☺	~1ns ☺	6T ☹	☹
DRAM – 1T1C  Yamazaki, Journal of Solid State Circuits, 1999	0.8V ☺	10ns 😐	1 C ?	?
Flash – 1T 	~12V ☹	10µs ☹	1T ☺	☺



Combine memory with computing



The role of Emerging NVM



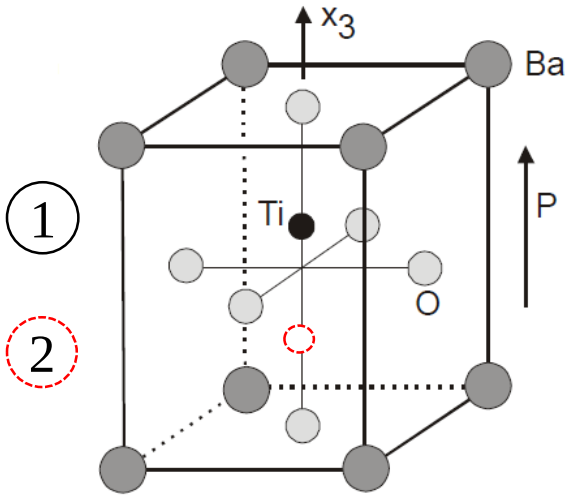
Source: Adopted and updated from: An Chen, Solid State Electronics, 2016

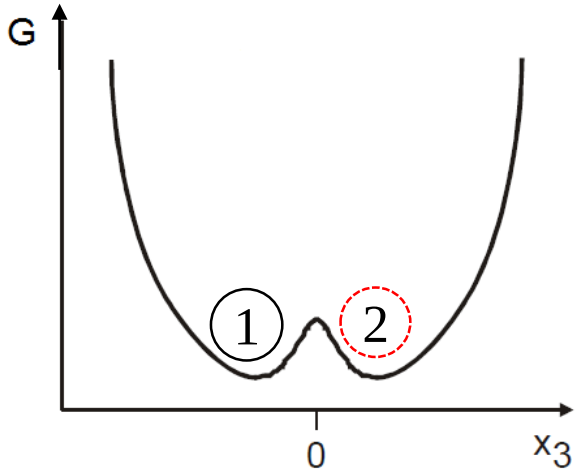
Ferroelectrics in general

No iron involved!

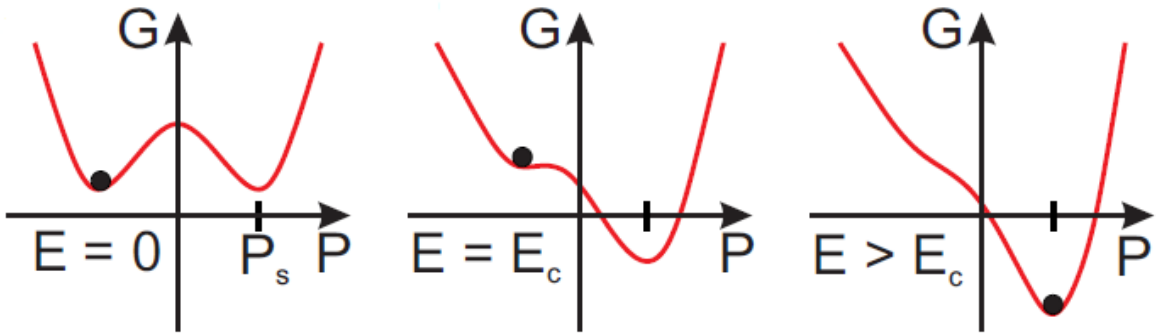
Just similar behavior like Ferromagnetic

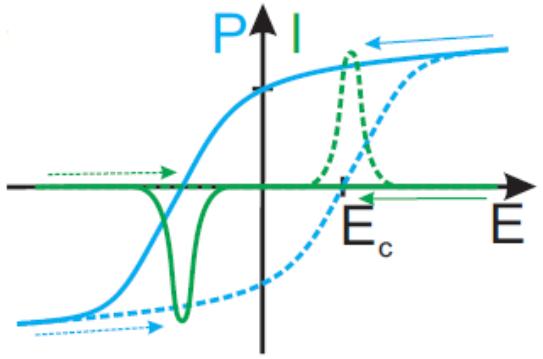
- Crystal structure with polar axis contain two stable states



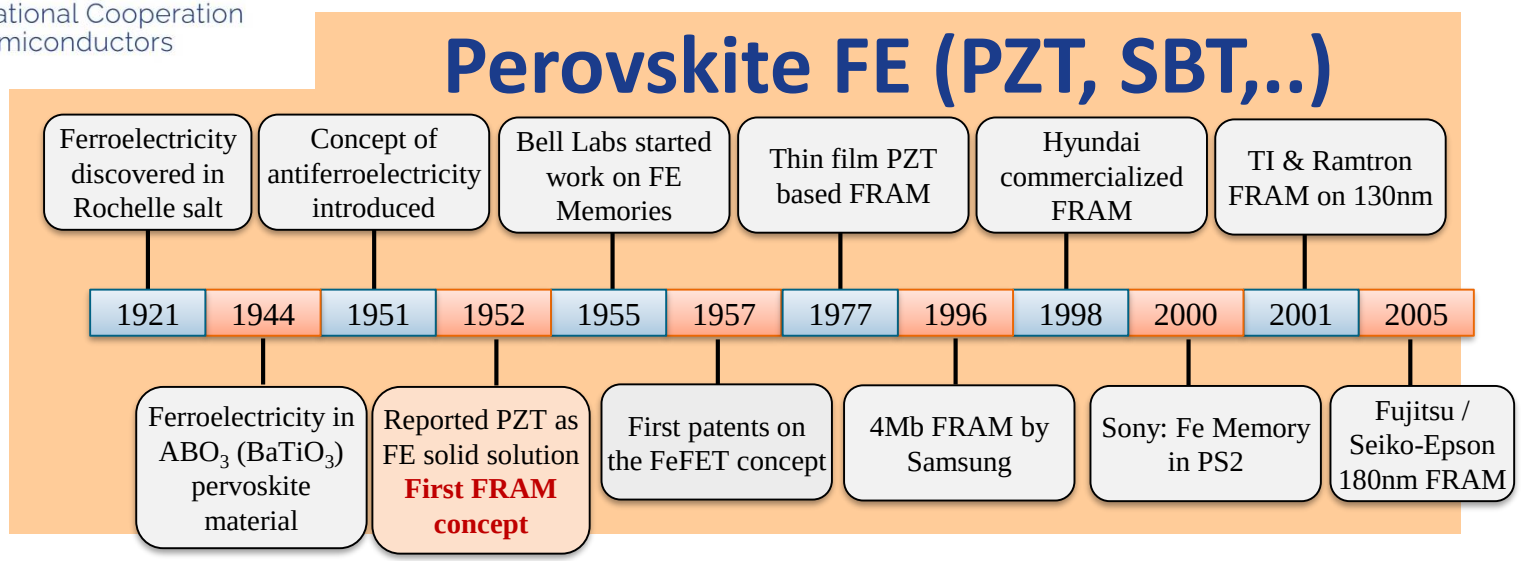


- Reversible switching between these two states over external E-Field possible





FE - Memories

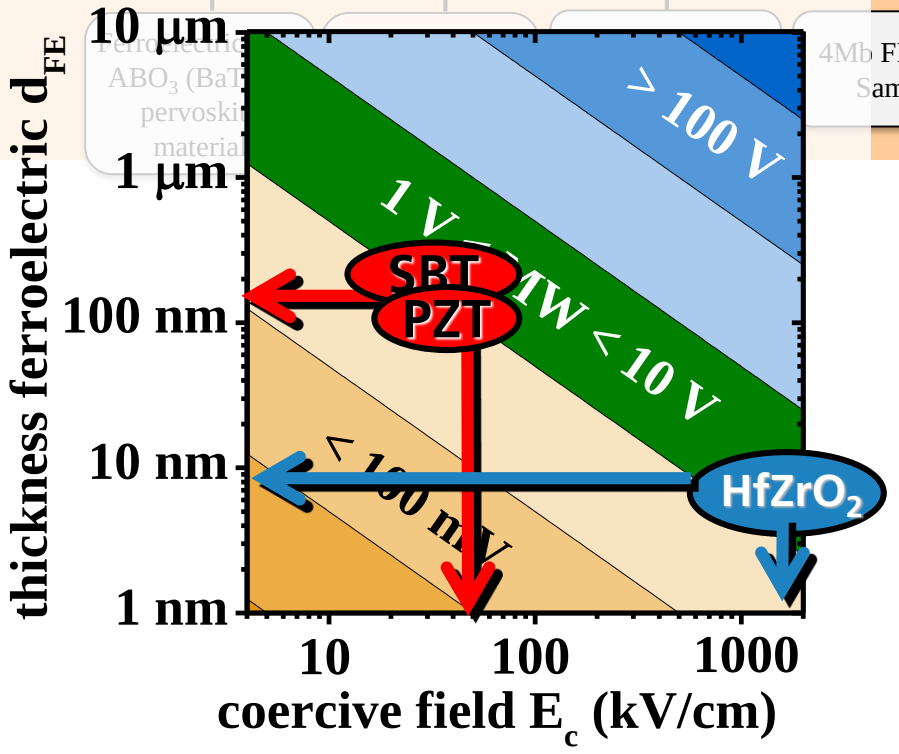

Perovskite FE (PZT, SBT,..)
Ferroelectricity discovered in Rochelle salt
Concept of antiferroelectricity introduced
Bell Labs started work on FE Memories
Thin film PZT based FRAM
Hyundai commercialized FRAM
TI & Ramtron FRAM on 130nm
1921
1944
1951
1952
1955
1957
1977
1996
1998
2000
2001
2005
Ferroelectricity in ABO_3 ($BaTiO_3$) pervoskite material
Reported PZT as FE solid solution
First FRAM concept
First patents on the FeFET concept
4Mb FRAM by Samsung
Sony: Fe Memory in PS2
Fujitsu / Seiko-Epson 180nm FRAM

FE - Memories

Perovskite FE (PZT, SBT,..)

Hafnium oxide Era (Fluorite-structured)

- 1921 — Ferroelectricity discovered in Rochelle salt
- 1944 — Concept of antiferroelectricity introduced
- 1951 — Bell Labs started work on FE Memories
- 1952 — Thin film PZT based FRAM
- 1955 — Hyundai commercialized FRAM
- 1957 — TI & Ramtron FRAM on 130nm
- 1977 — 4Mb FRAM by Samsung
- 1996 — Sony: Fe Memory in PS2
- 1998 — Fujitsu / Seiko-Epson 180nm FRAM
- 2000 — Ferroelectricity discovered in Si doped Hafnium oxide material
- 2001 — Ferroelectricity in binary oxides revealed
- 2005 — 28 nm HKMG FeFET integration with FE binary oxide
- 2007 — First report of 22 nm FDX based FeFET
- 2011 — Leti reported BEOL FeRAM
- 2012 — Sony Semicond. reported BEOL FeRAM
- 2017
- 2019
- 2020



~10nm

Potential

#1 Scalability

#2 CMOS compatibility

FE - Memories

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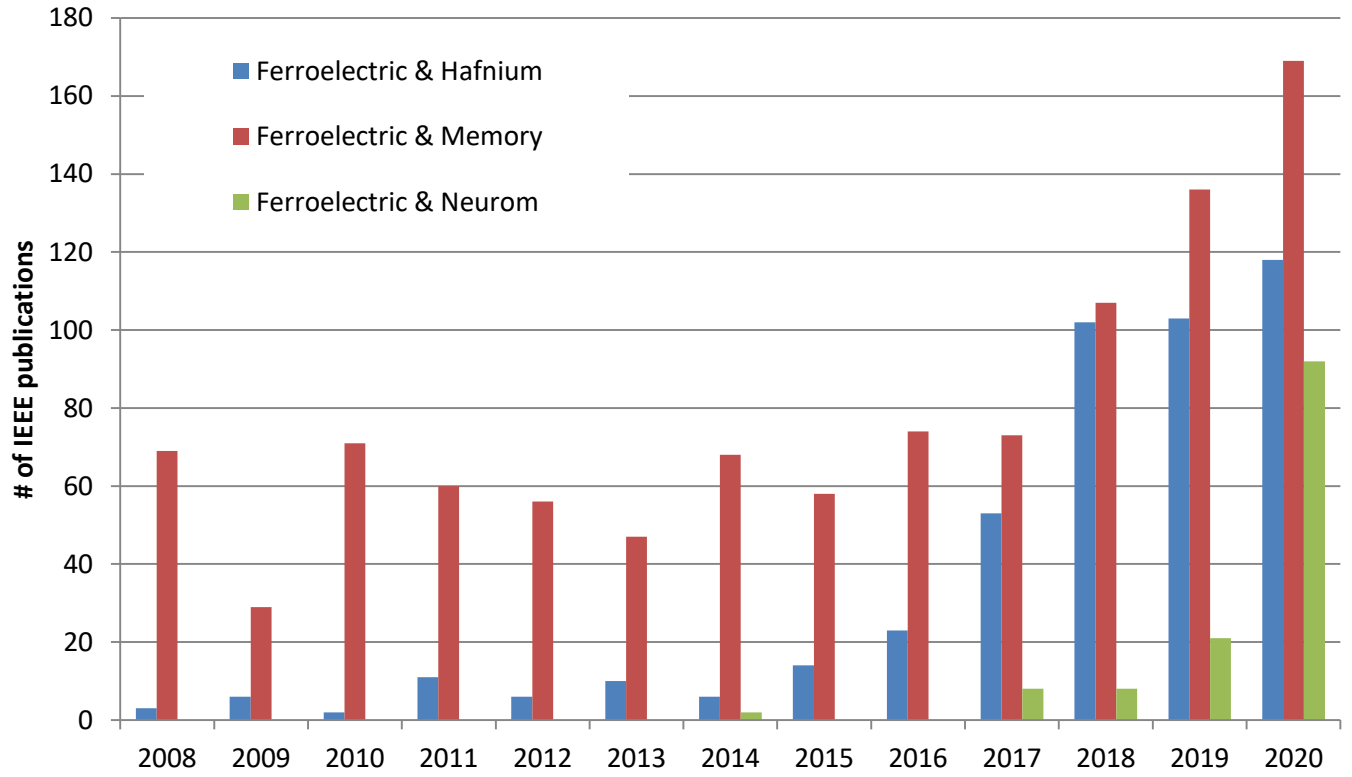

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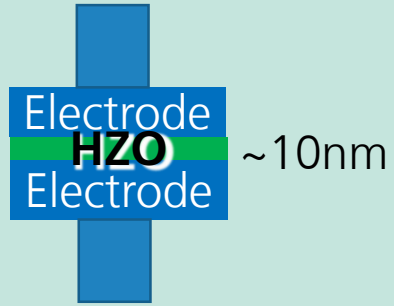
Advantages

#1 Scalability

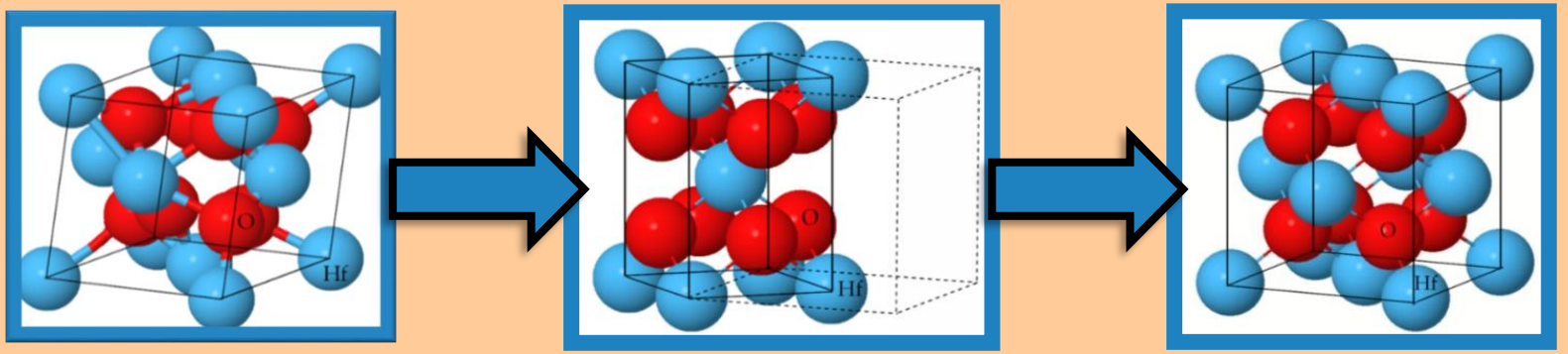
#2 CMOS compatibility



~10nm

Ferroelectric HfO_2

Dielectric only



monoclinic
($P2_1/c$) $\varepsilon_r \sim 20$

tetragonal
($P4_2/nmc$) $\varepsilon_r \sim 35$

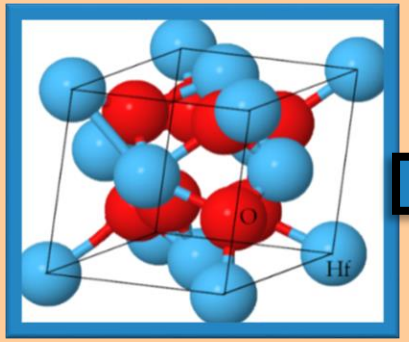
cubic
($Fm\underline{3}m$) $\varepsilon_r \sim 28$

temperature / stress / doping / confinement

→ **ferroelectricity requires non-centrosymmetry**

Ferroelectric HfO_2

Dielectric only



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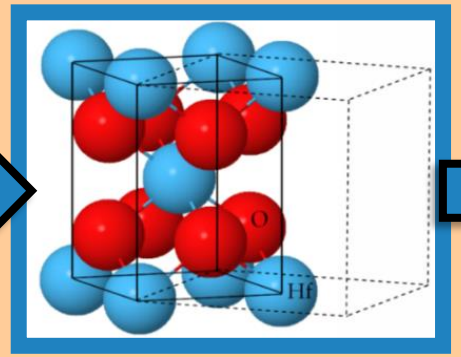

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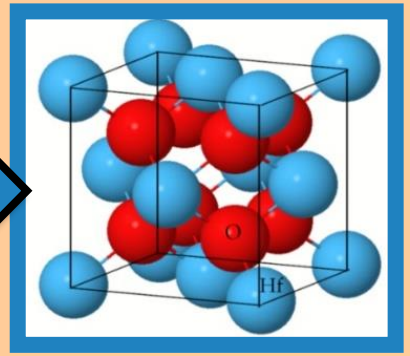

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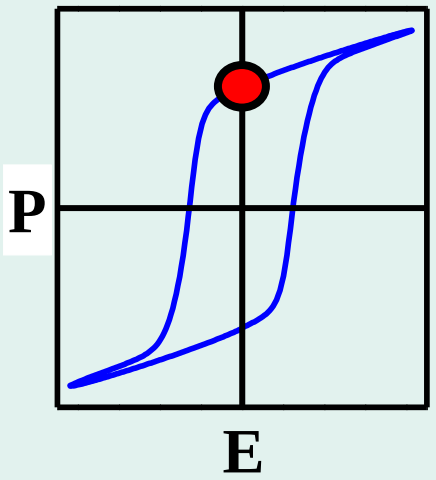
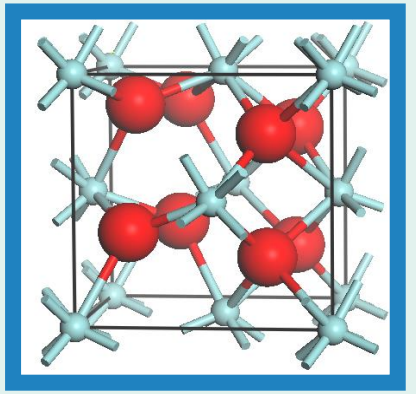
Ferroelectric



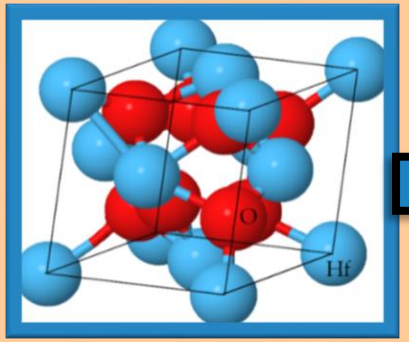
confinement
stress
doping
Zr, Si, La,...



orthorhombic
($Pbc2_1$) $\varepsilon_r \sim 25$

Ferroelectric HfO_2

Dielectric only



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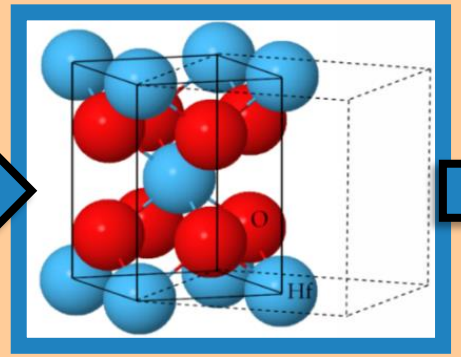

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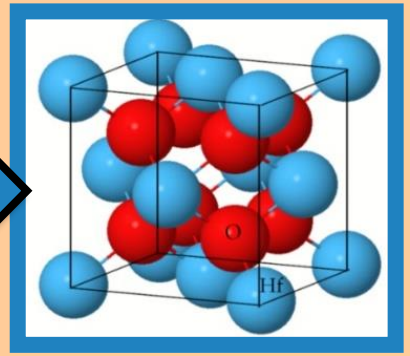

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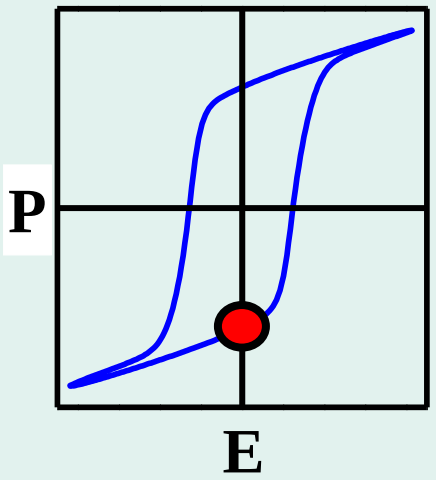
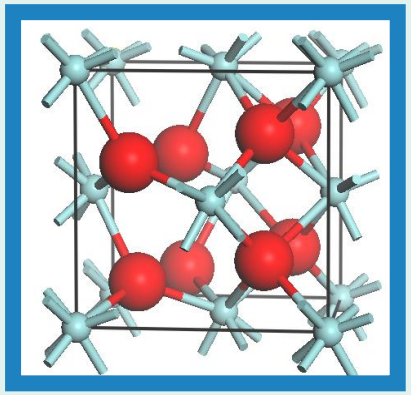
Ferroelectric



confinement
stress
doping



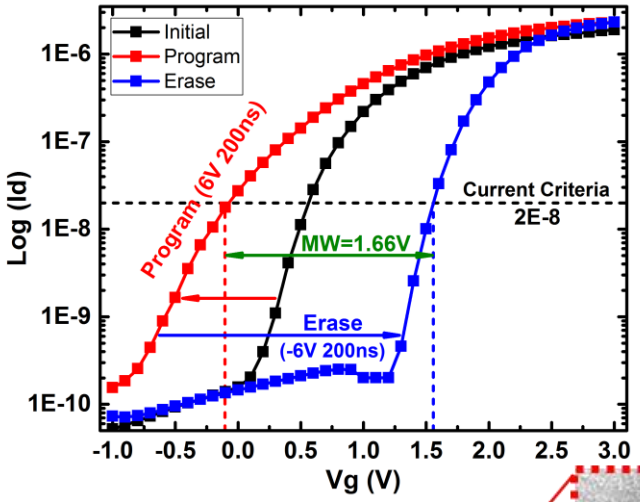
orthorhombic
($Pbc2_1$) $\varepsilon_r \sim 25$

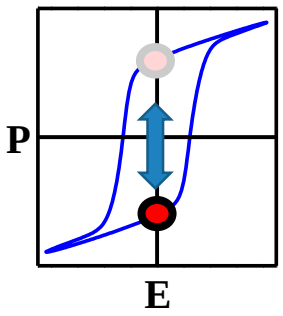
The material looks nice…

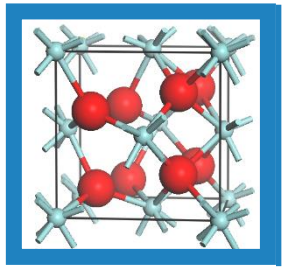
How to build Storage elements out of it?

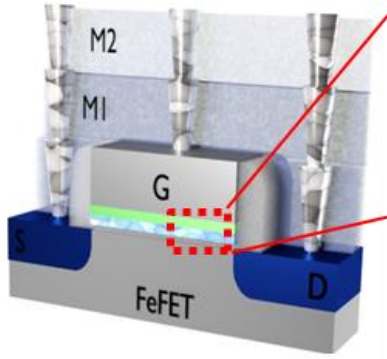
FE Memory device concepts

1T FEOL FeFET

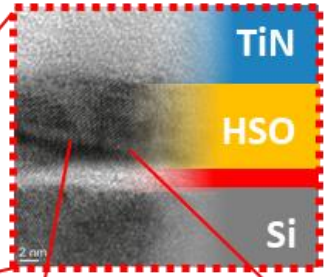




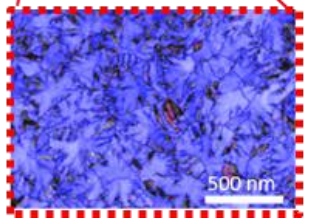




MFIS



SiO_2

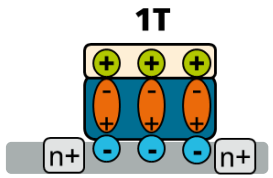


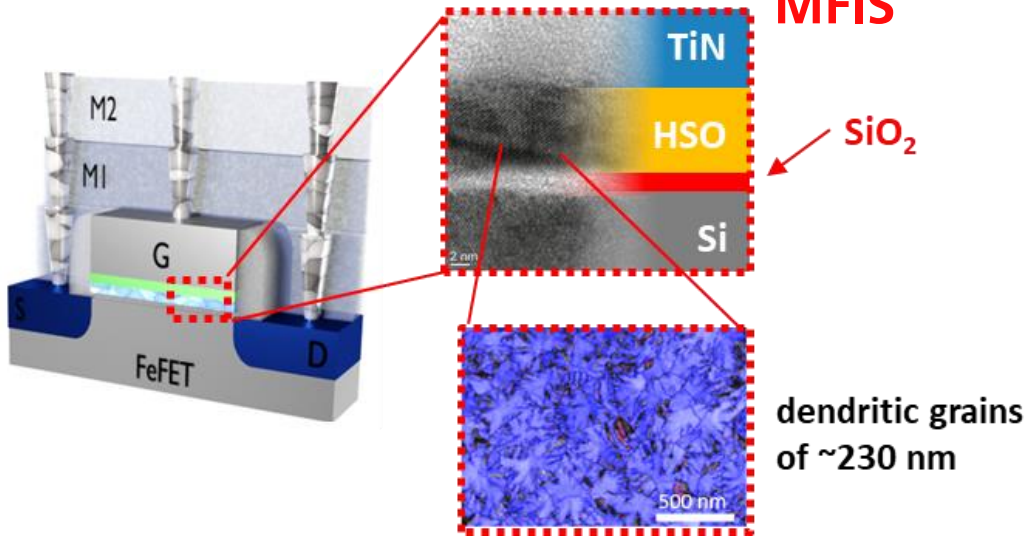
dendritic grains of ~230 nm

FE Memory device concepts

1T FEOL FeFET

- ☺ Non-destructive readout
- 😐 Asymmetric MFIS electrodes → limited reliability
- 😐 Alignment with CMOS FEOL device process





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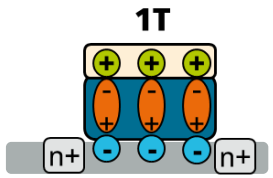
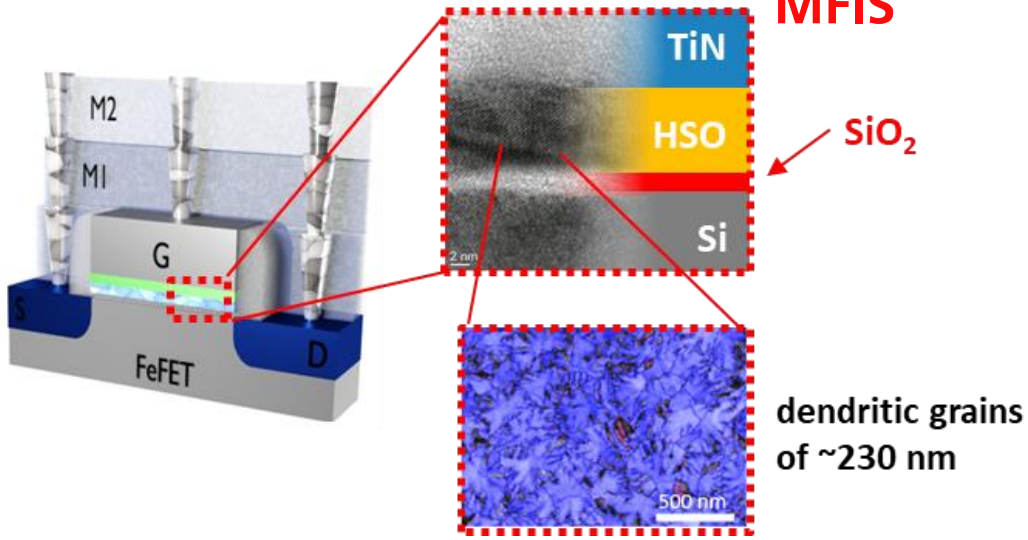
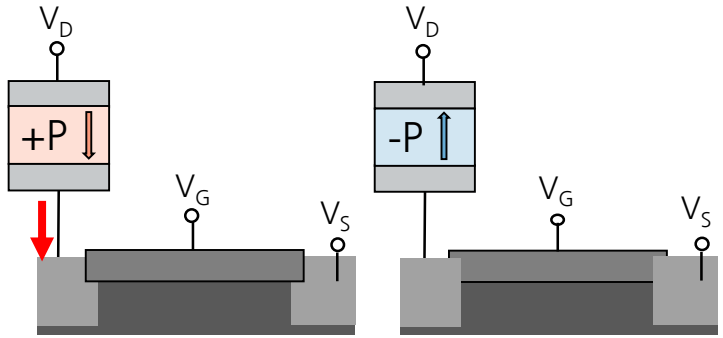


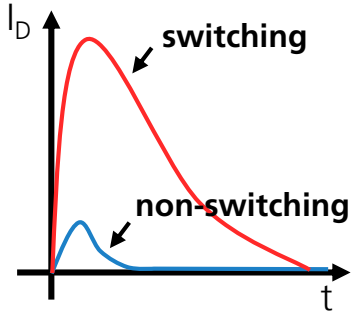
MFIS



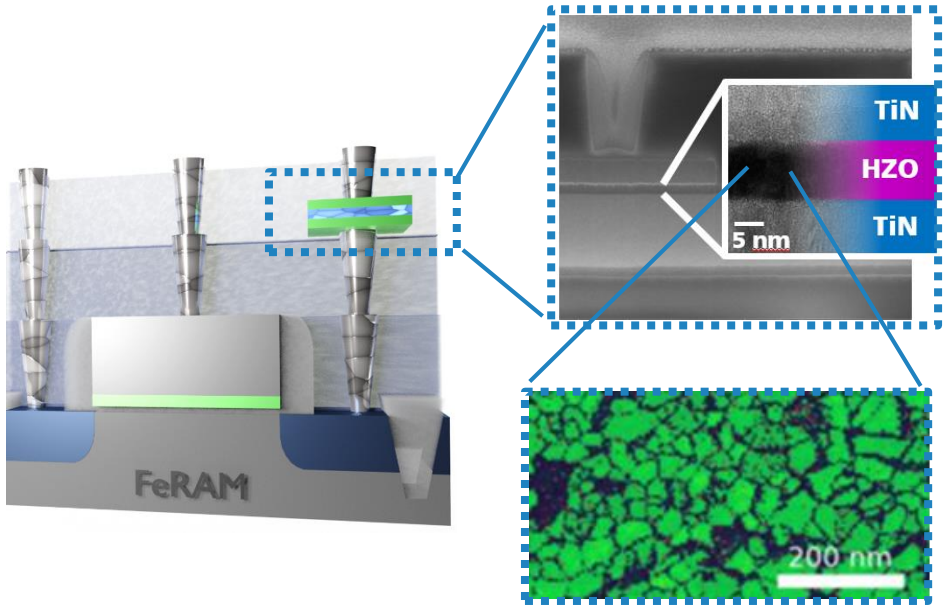
dendritic grains of ~230 nm

1T1C FRAM





MFM



columnar grains of ~23 nm

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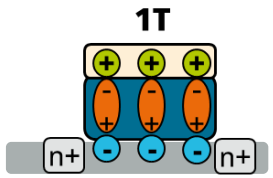
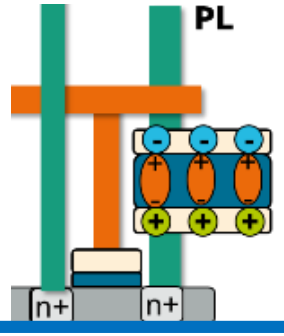
- 😐 Alignment with device process

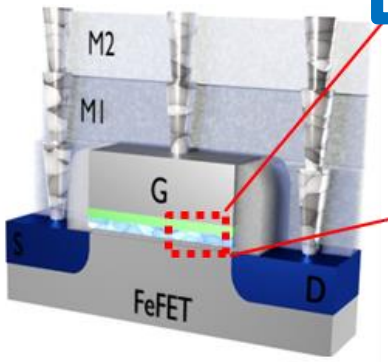


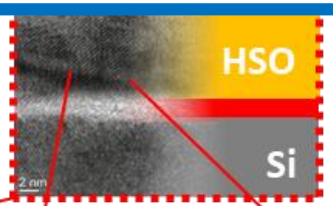
1T1C FRAM

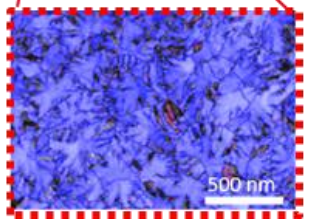


- ☹ Destructive readout
- ☺ Symmetric MFM electrodes → good reliability
- ☺ Standard CMOS FEOL device

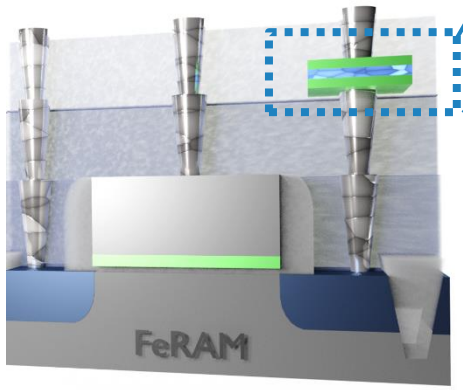
Can we combine the good properties?



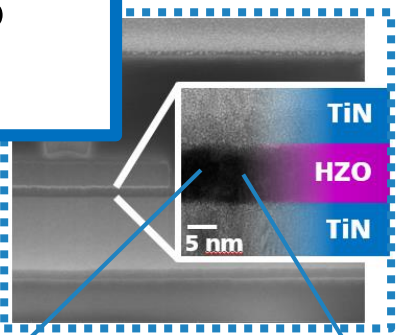


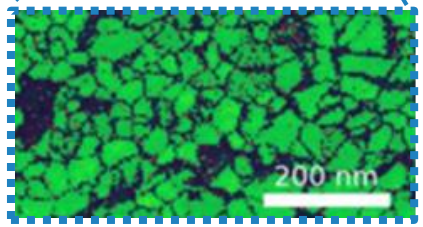


dendritic grains of ~230 nm



MFM

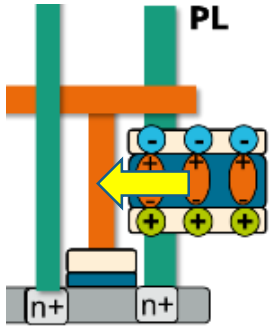




columnar grains of ~23 nm

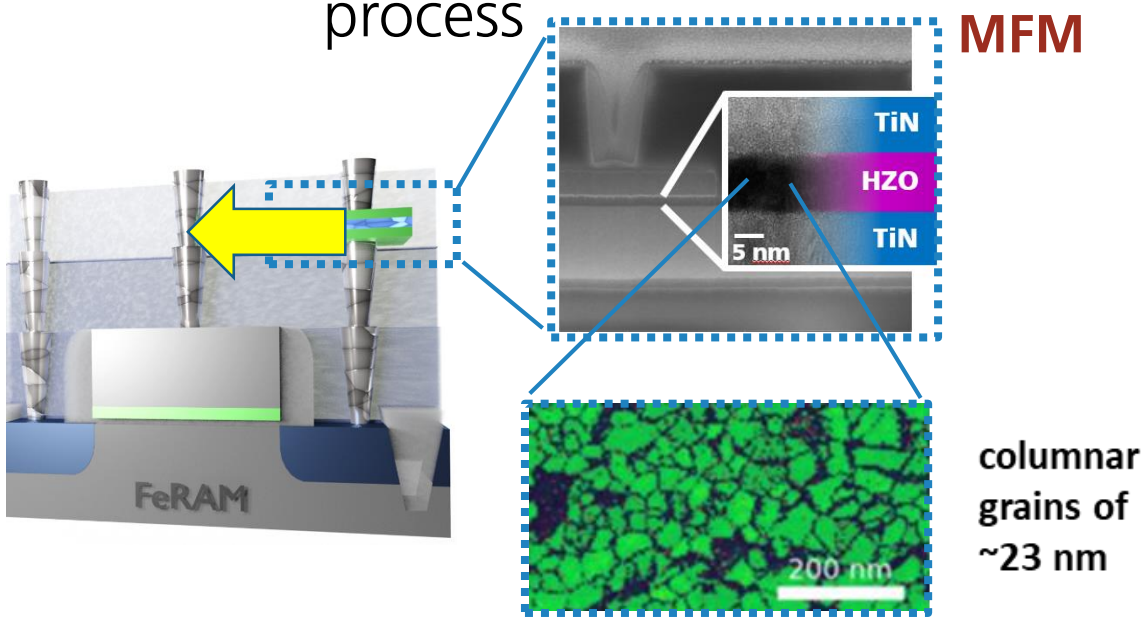
FE Memory device concepts

☺ Non-destructive readout



☺ Symmetric MFM electrodes
→ good reliability

☺ Standard CMOS FEOL device process

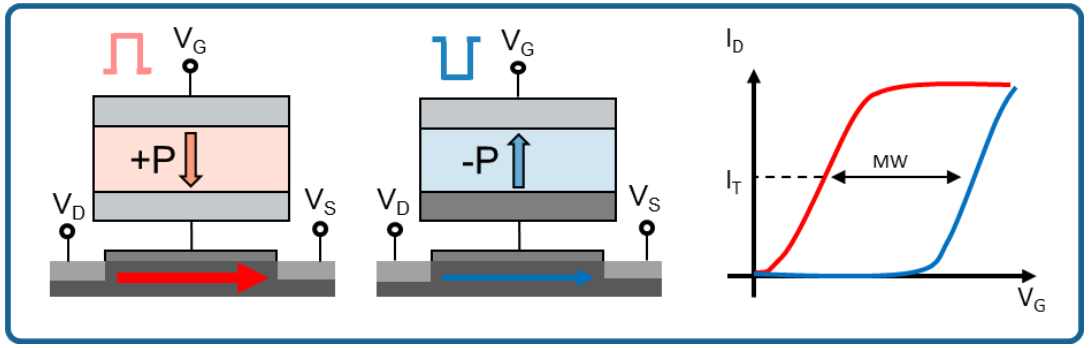


→ Make a BEOL capacitor FeFET

FE Memory device concepts

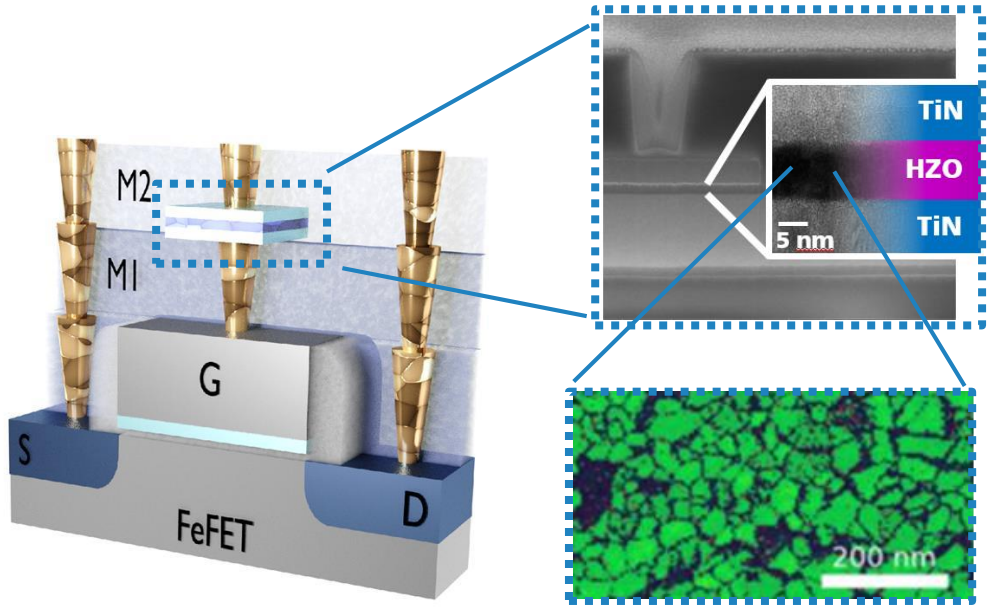
1T1C BEOL FeFET (MFMIS)

- ☺ Non-destructive readout
- ☺ Symmetric MFM electrodes → good reliability
- ☺ Standard CMOS FEOL device process



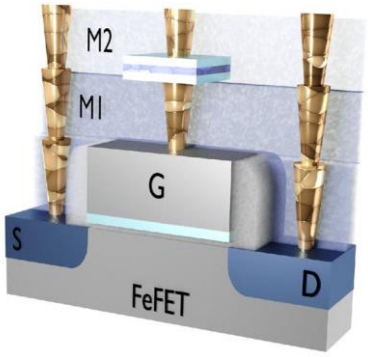
Challenges

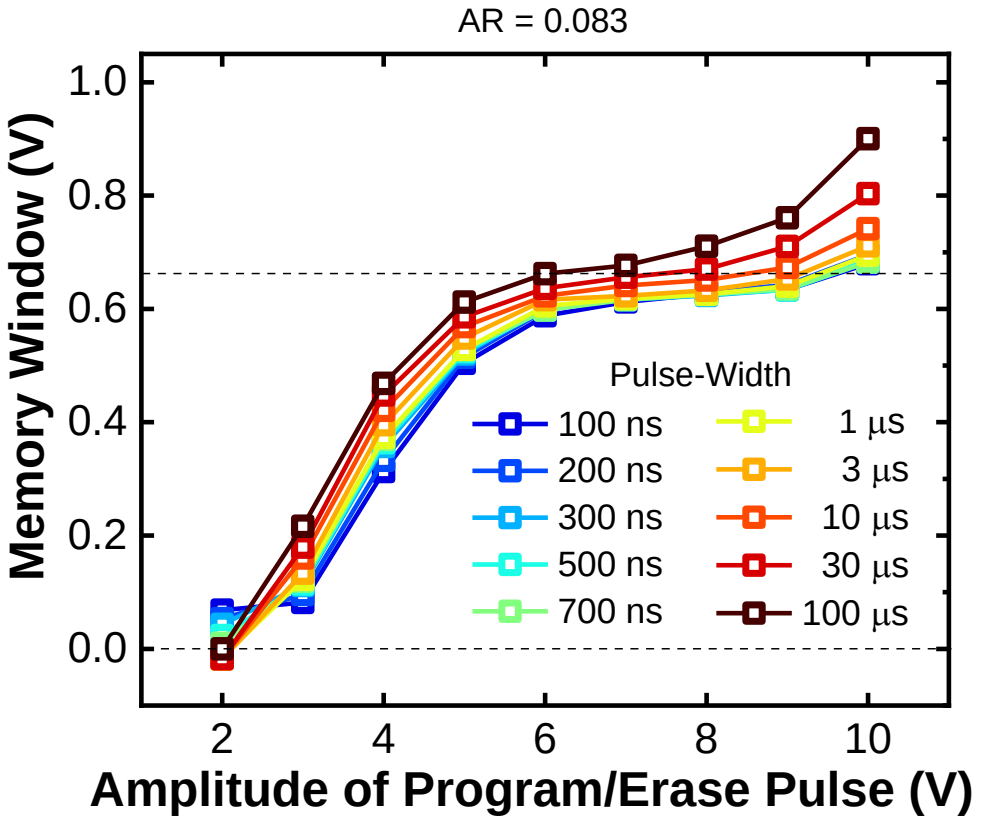
- 😐 BEOL ferroelectric device integration (thermal budget)
- 😐 Understanding and handling of Floating Node
- 😐 Scalability

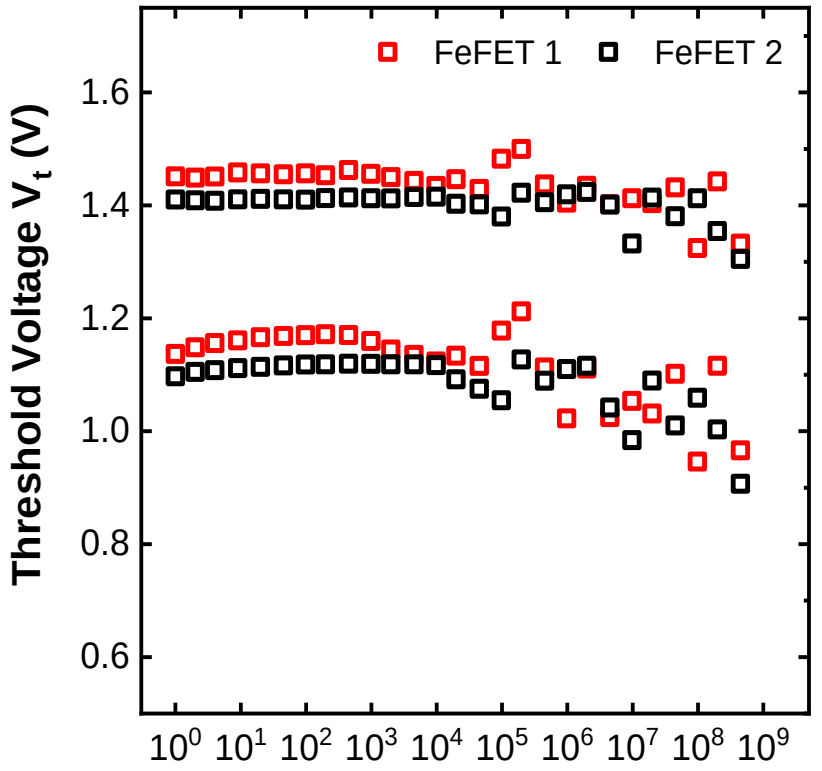


FE Memory device concepts

1T1C BEOL FeFET (MFMIS)



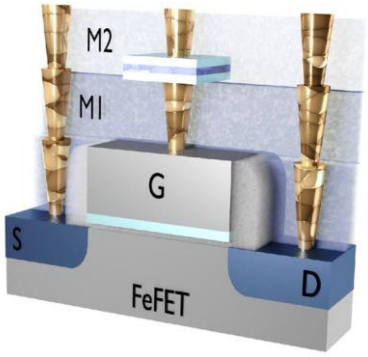


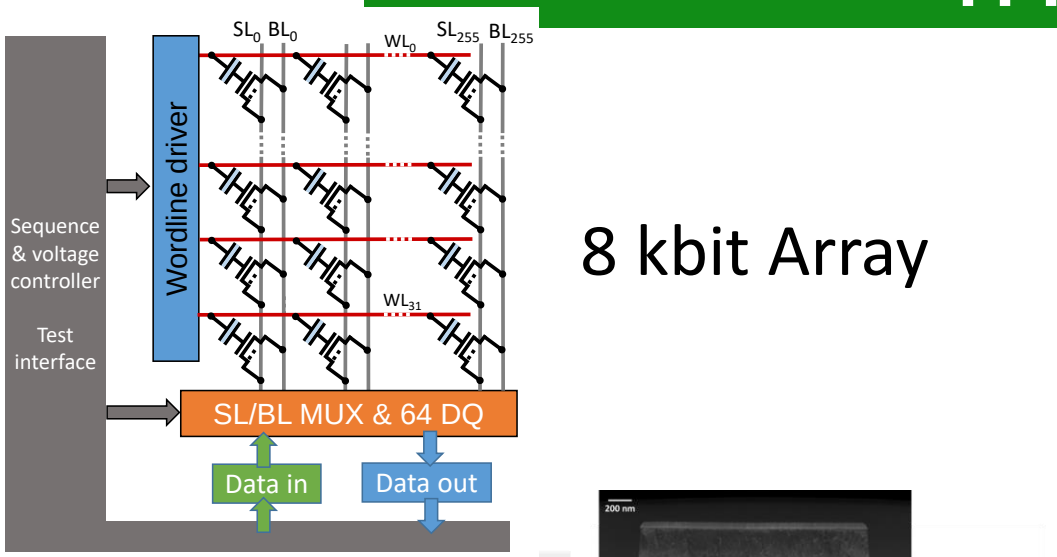


D. Lehninger *et al.*, EDL 2022

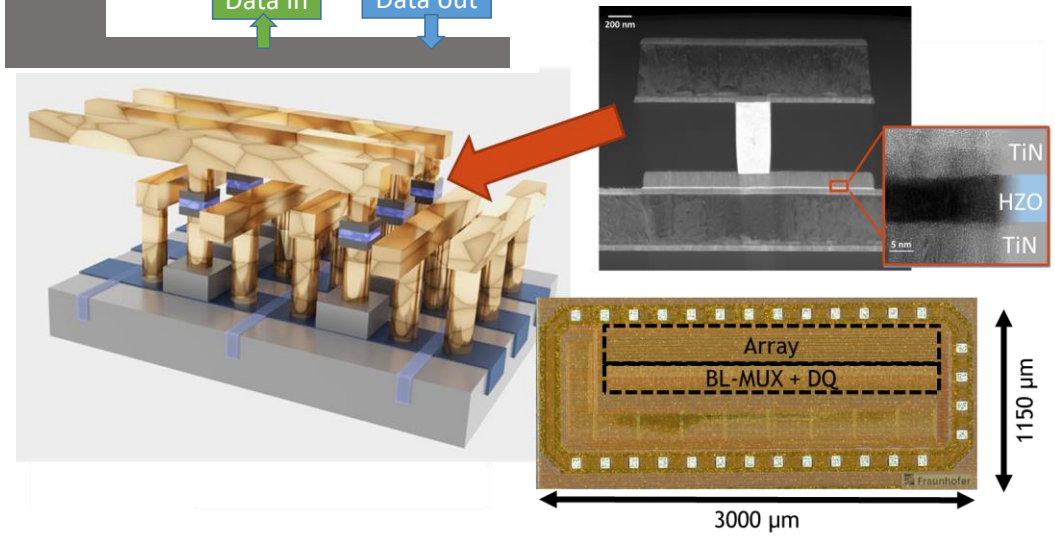
FE Memory device concepts

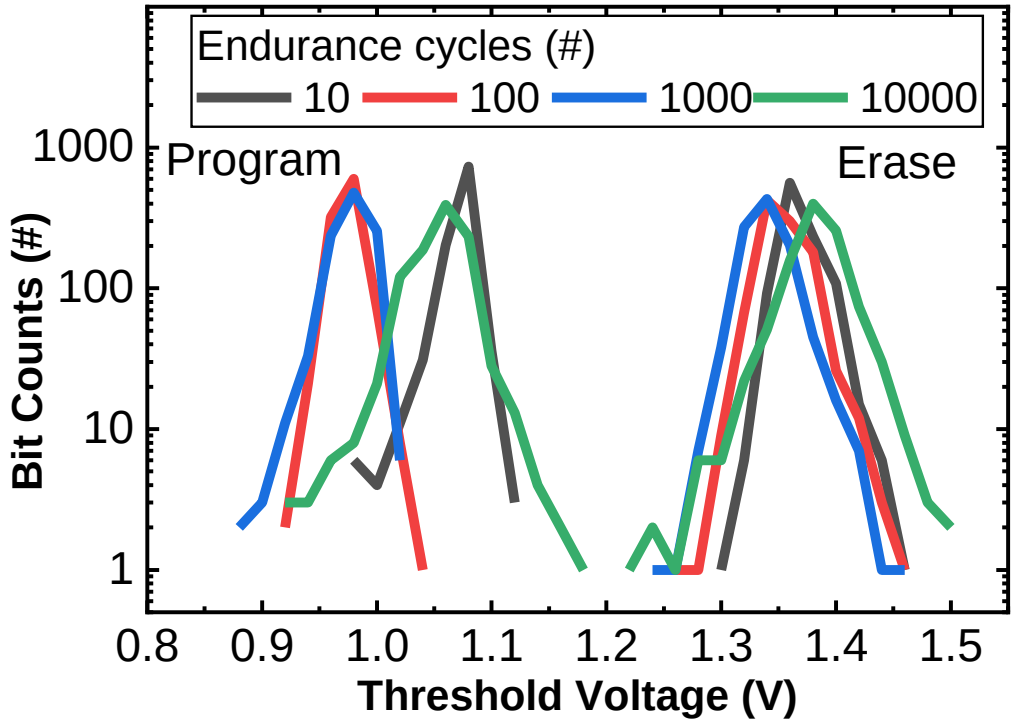
1T1C BEOL FeFET (MFMIS)





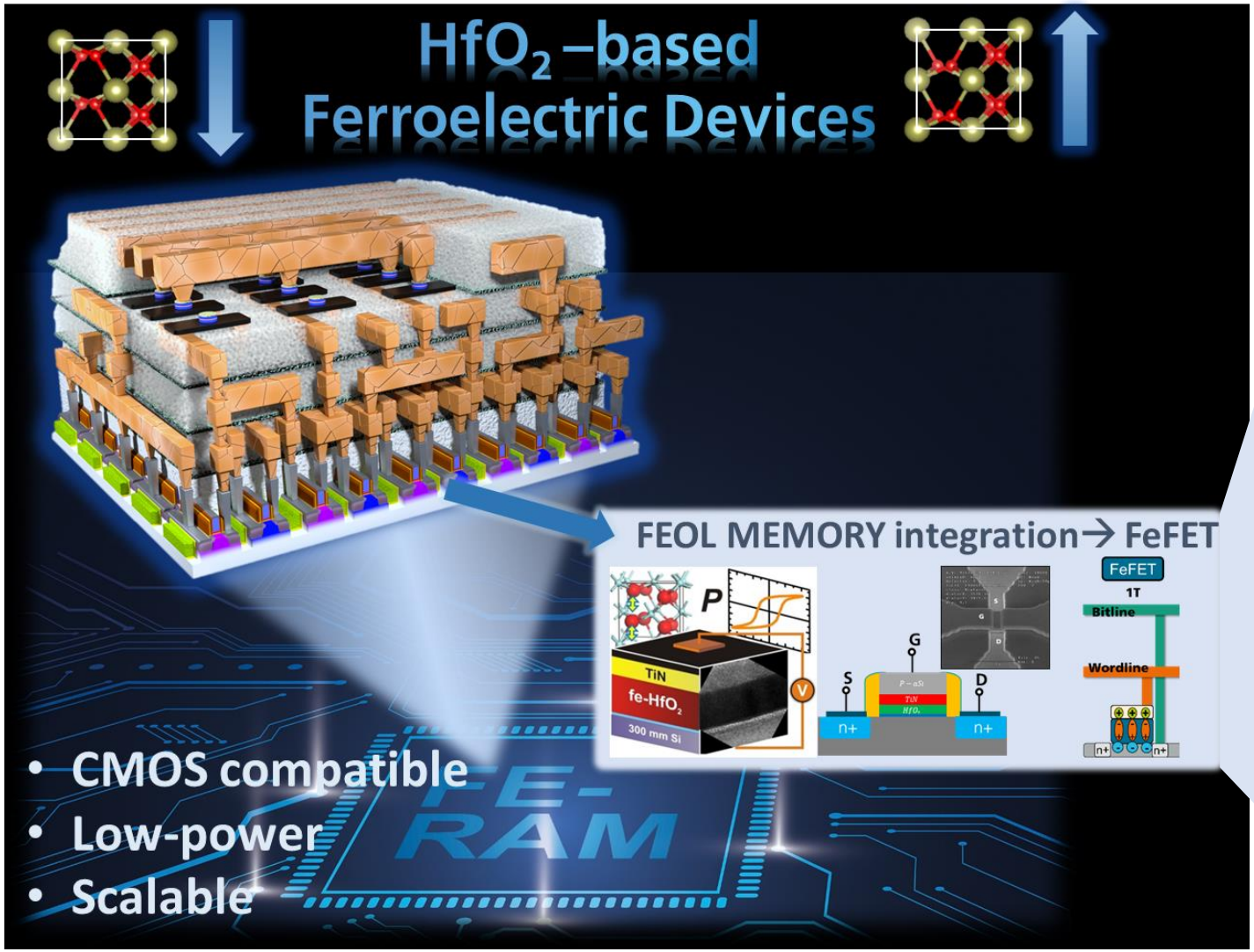
8 kbit Array



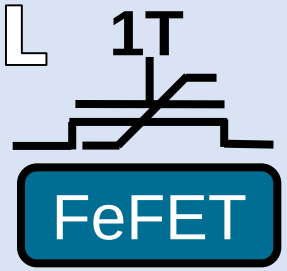


K. Seidel *et al.*, VLSI 2022

Integration in Chip Technologies



FEOL 1T

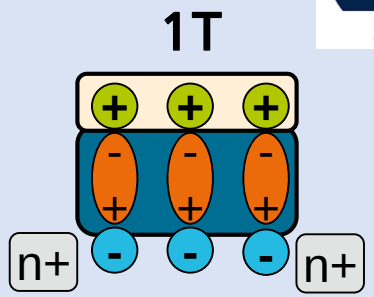


→1T cell size

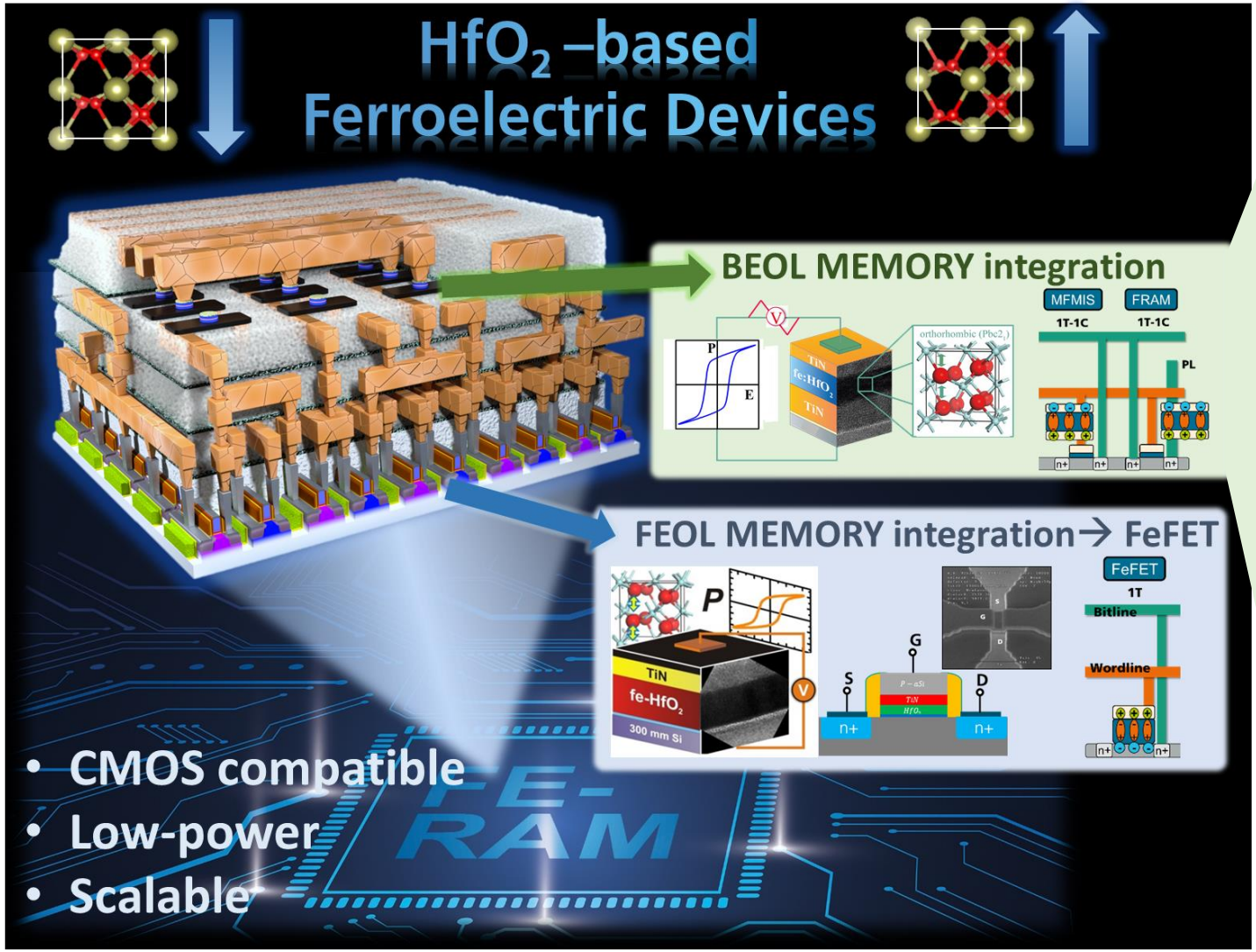
→Non destructive read memory

→FEOL Integration

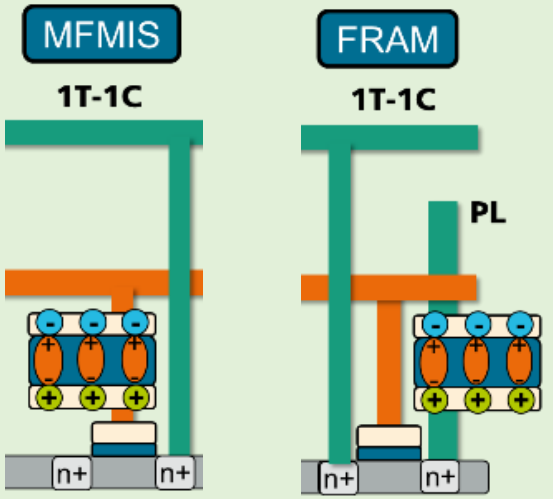
→Depolarization



Integration in Chip Technologies



BEOL



StorAIge

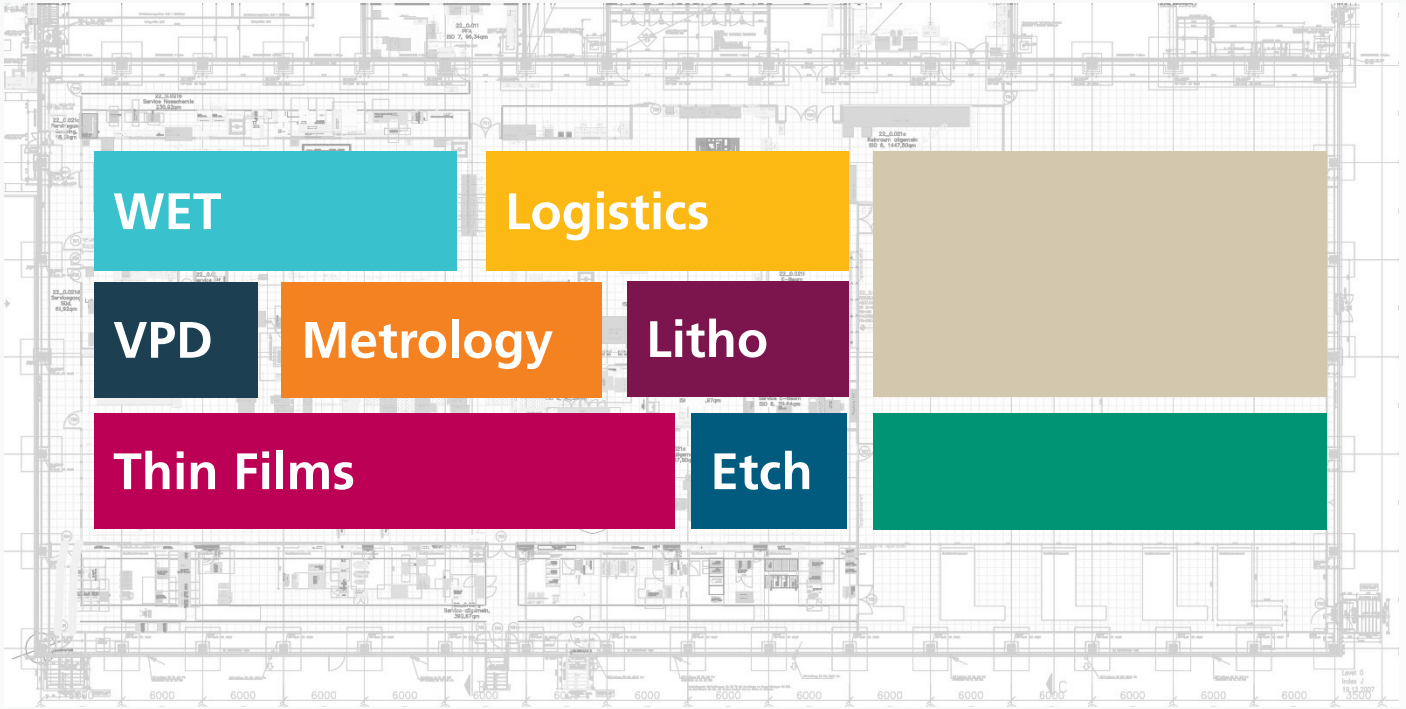
ECSEL Joint Undertaking

Project StorAIge

→BEOL storage integration for Edge-AI application

Fraunhofer IPMS – Center Nanoelectronic Technologies (CNT)

- Fully industry standard CMOS cleanroom
- ~2700 m² used CR and lab area
- More than 80 tools for 300mm processing and metrology installed
- ISO9001:2015 certification



Fraunhofer IPMS – Center Nanoelectronic Technologies (CNT)

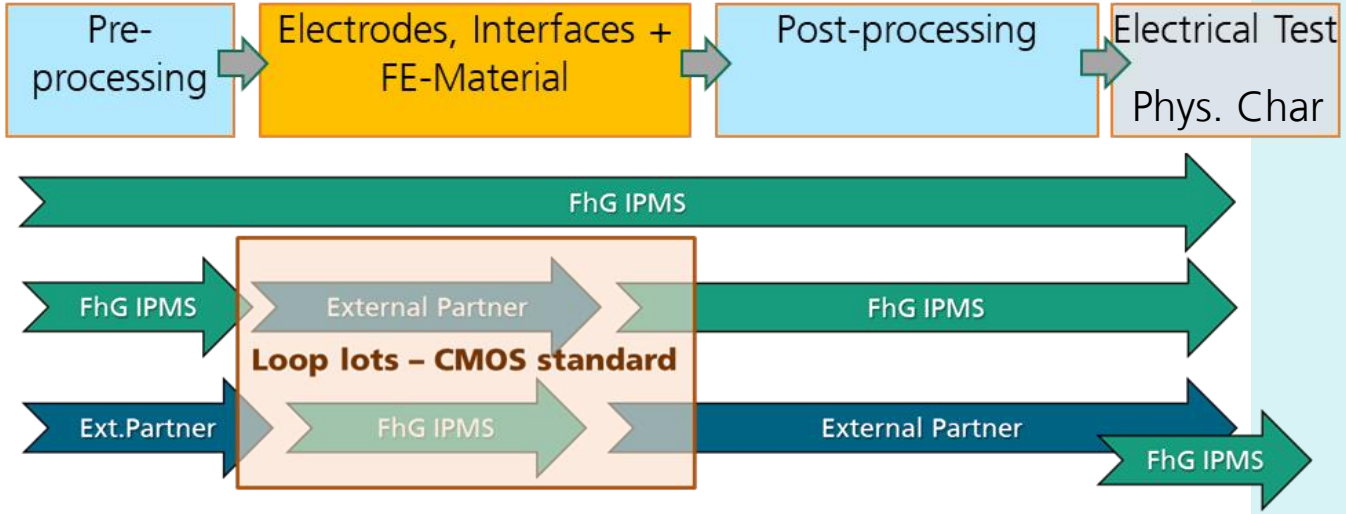
Spintronic

Ferroelectric / RRAM

+ many more tools (electrodes, patterning, cleaning,…)

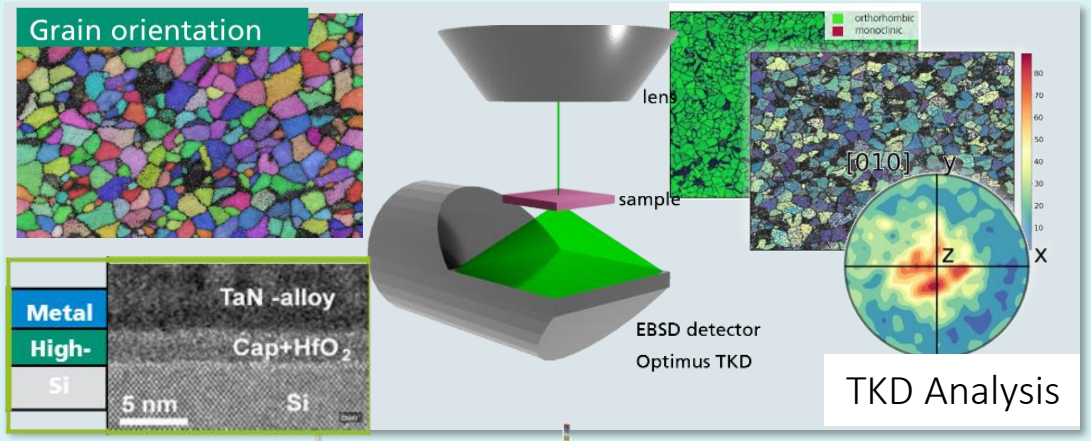
Acceleration!

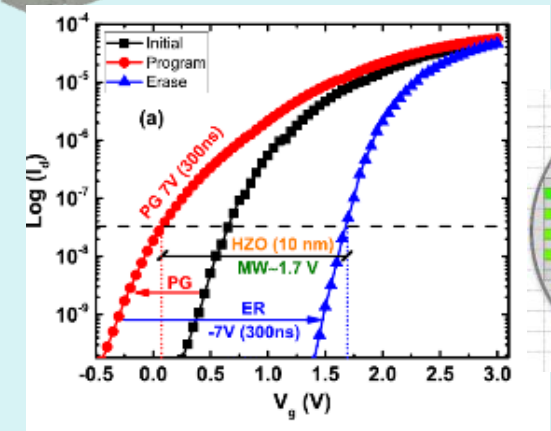
Various material exchange options

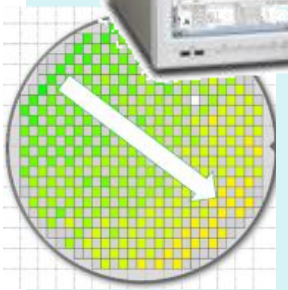


Offer for partners: looplots & characterization support

Ferroelectric characterization portfolio

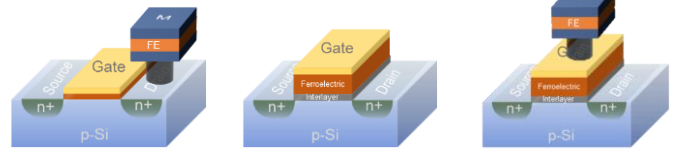






Performance indicators

FRAM FeFET FeMFET

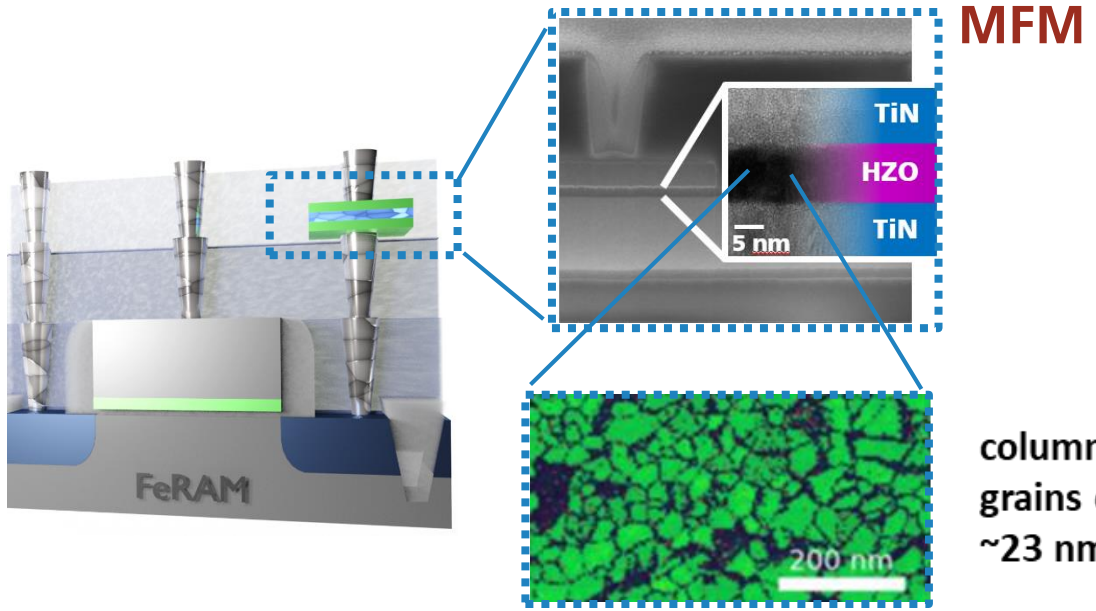


	eSRAM	eDRAM	FG Flash	SONOS	ReRAM	PCM	STT-MRAM	FeRAM	FeFET	FeMFET
Mechanism	Cross-coupled inverter+charge	Charge on capacitor	Charge on FG	Charge in Nitride	Filament formation	Phase change	Spin transfer torque, magnetic	Polarization switching	Polarization switching	Polarization switching
Cell Structure	6T	1T1C	1.5T	2T	1T-1R	1T-1R	1T-1R	1T-1C	1T	1T-1C
Cell Size	120-150 F^2	40 F^2	50 F^2	60 F^2	60 F^2	60 F^2	50 F^2	50 F^2	20-30 F^2	30-40 F^2
MLC	No	No	Yes	Yes	Yes	Yes	No	Potential	Yes	Yes
R_{on}/R_{off} ratio	N/A	N/A	$>10^4$	$>10^4$	10-100	10-100	<10	N/A	$>10^4$	$>10^4$
Integration Node	7nm FinFET	22nm FinFET	40nm	28nm HKMG	22nm FinFET	40nm	22nm FinFET	130nm	22nm FDSOI	180nm[1]
Additional Masks	0	5+	13+	5+	3+	3+	3+	2-3	1	2-3
Energy/bit	~1 fJ	~1 pJ	100 pJ	~10 pJ	>10 pJ	100 pJ	>10 pJ	~1 pJ	~1 fJ	~10 fJ
Latency	<1 ns	>10 ns	0.1-1 ms	10-100 ns	>100 ns	>100 ns	>10 ns	>10 ns	~1 ns	10 ns
Endurance	10^{16}	10^{16}	10^4-10^5	10^4-10^6	10^5-10^7	10^5-10^7	10^6-10^7	$>10^{14}$	10^5-10^9	10^{10}
Retention	volatile	Refresh	10 yrs	10 yrs	10 yrs	10 yrs	10 yrs	10 yrs	10 yrs	10 yrs

adopted from A. Keshavarzi et al, IEEE Micro, 2020

Performance indicators

Integration & Scaling



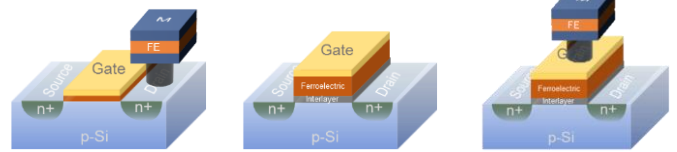
MFM

columnar grains of ~23 nm

Potential

#1 Scalability

#2 CMOS compatibility



FeRAM	FeFET	FeMFET
Polarization switching	Polarization switching	Polarization switching
1T-1C	1T	1T-1C
50 F^2	20-30 F^2	30-40 F^2
Potential	Yes	Yes
N/A	$>10^4$	$>10^4$
130nm	22nm FDSOI	180nm[1]
2-3	1	2-3
~1 pJ	~1 fJ	~10 fJ
>10 ns	~1 ns	10 ns
$>10^{14}$	10^5-10^9	10^{10}
10 yrs	10 yrs	10 yrs

Performance indicators

Low Write Voltage and Energy

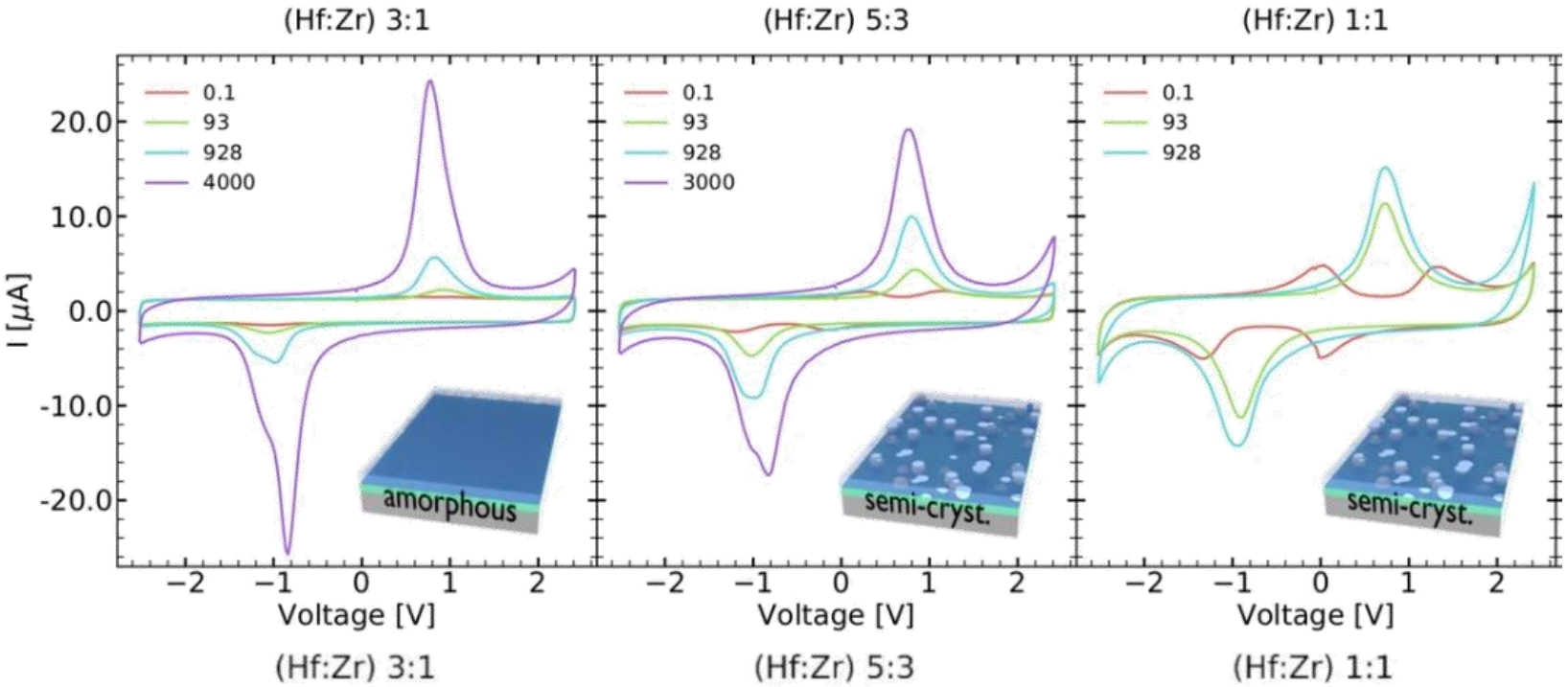
Potential

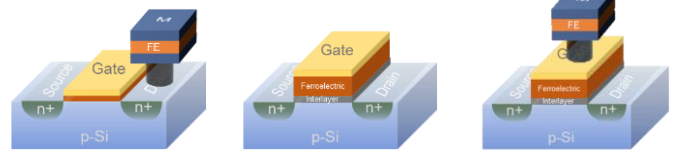
#1 Scalability

#2 CMOS compatibility

#3 Low Power

M.Lederer *et al*., Sci Rep 11, 22266 (2021). https://doi.org/10.1038/s41598-021-01724-2





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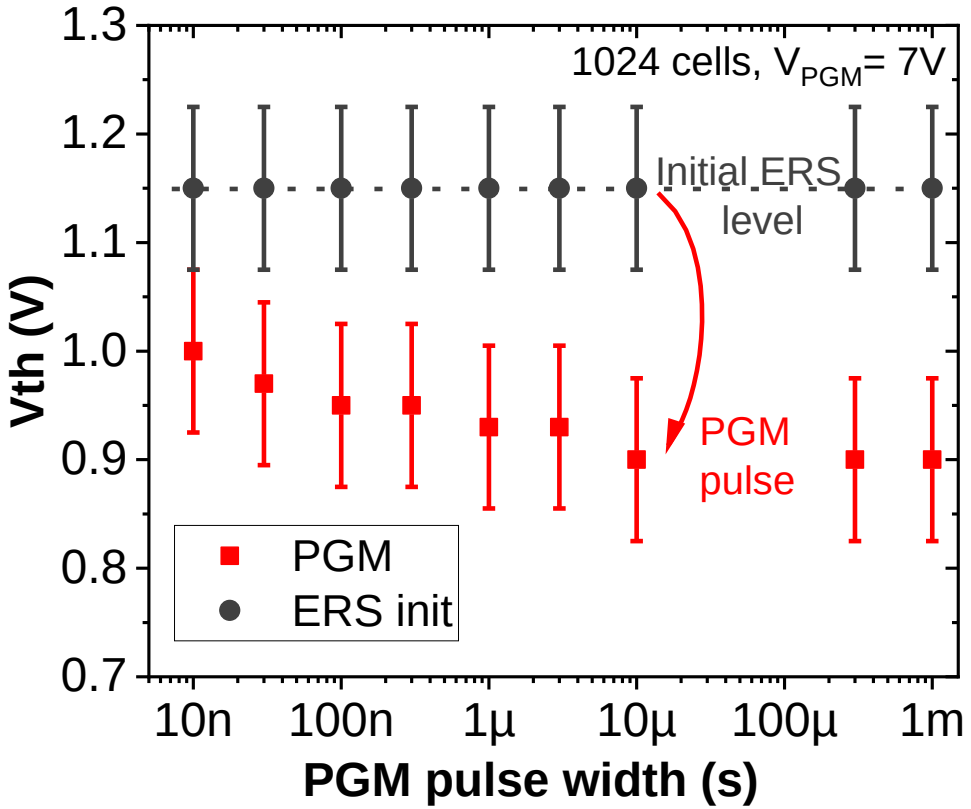
10 yrs	10 yrs	10 yrs

Performance indicators

Write speed test on FeMFET Array



K. Seidel *et al.*, VLSI 2022

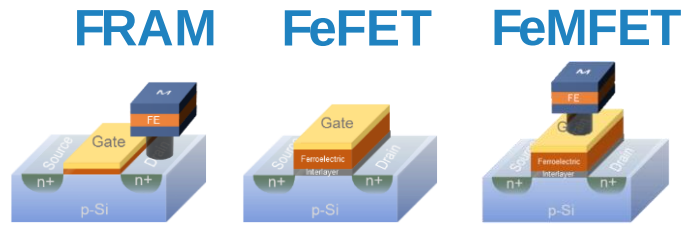
Potential

#1 Scalability

#2 CMOS compatibility

#3 Low Power

#4 High Speed



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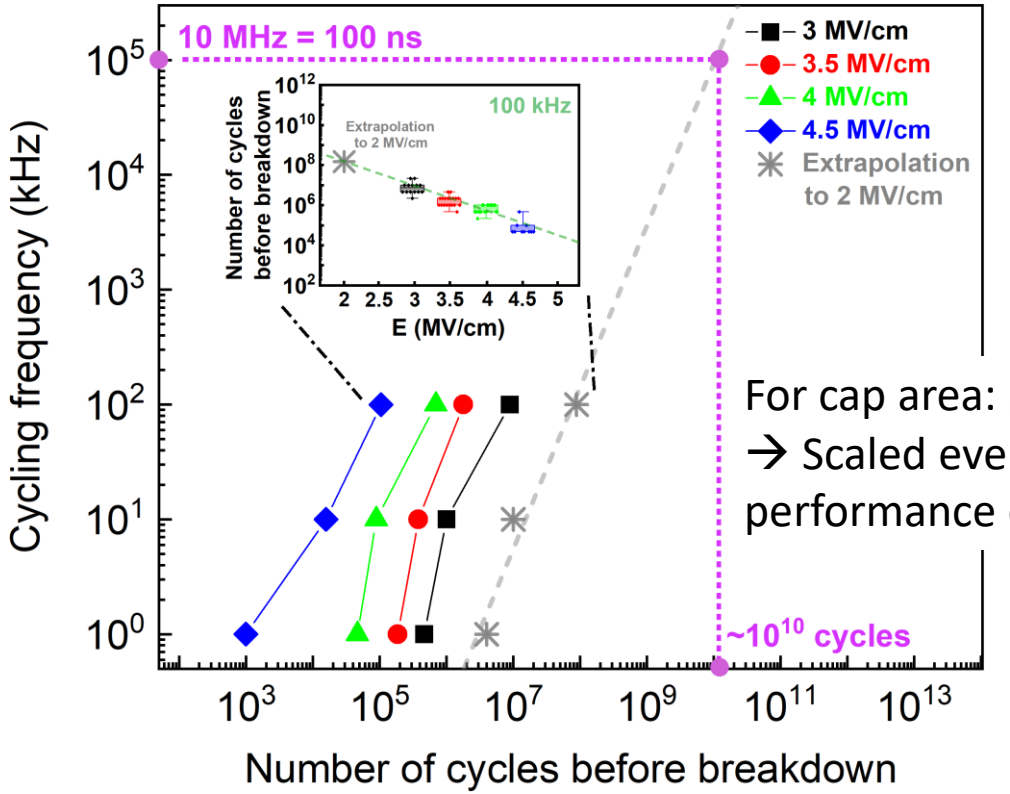
Performance indicators

Endurance on large MFM caps



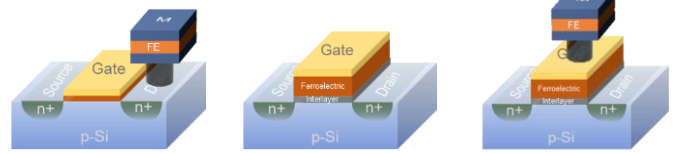
For cap area: 25k µm²!
→ Scaled even better performance expected

A. Sunbul, Adv. Eng. Mater., 25: 2201124. https://doi.org/10.1002/adem.202201124

Potential

#1 Scalability
#2 CMOS compatibility
#3 Low Power
#4 High Speed
#5 High Endurance (MFM)

FRAM **FeFET** **FeMFET**



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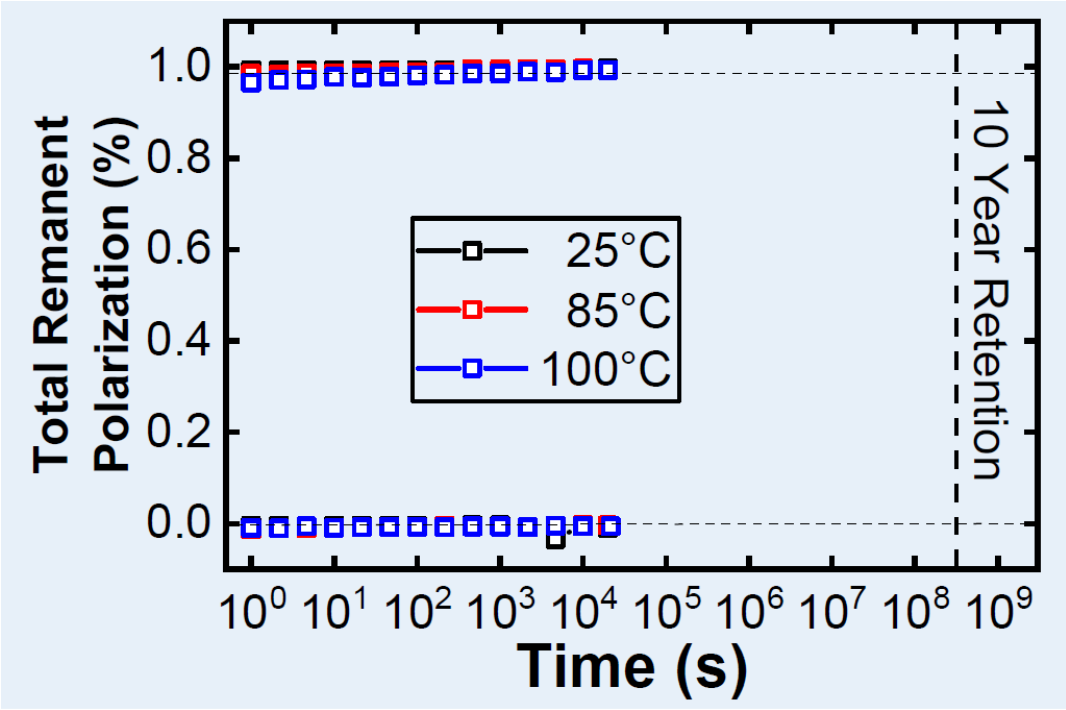
10 yrs	10 yrs	10 yrs

Performance indicators

Retention on large MFM caps

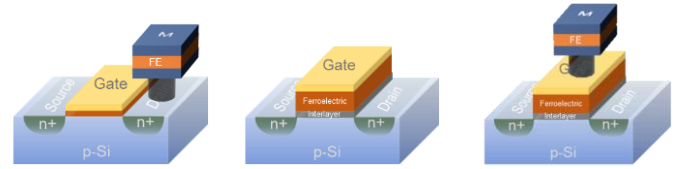


K. Seidel *et al.*, VLSI 2022

Potential

#1 Scalability
#2 CMOS compatibility
#3 Low Power
#4 High Speed
#5 High Endurance (MFM)
#6 Low Retention

FRAM **FeFET** **FeMFET**



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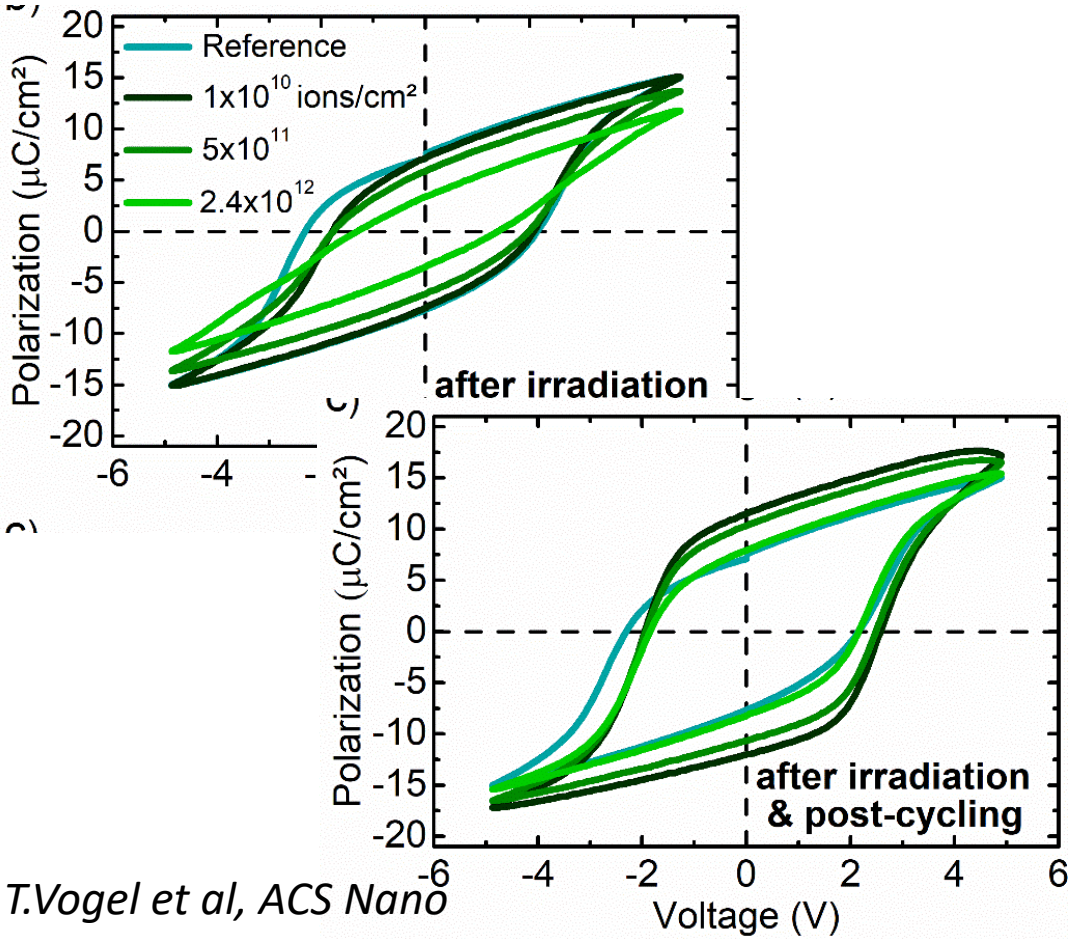
10 yrs	10 yrs	10 yrs

Performance indicators

Radiation tests

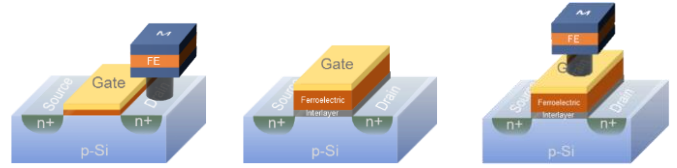


T.Vogel et al, ACS Nano

Potential

#1 Scalability
#2 CMOS compatibility
#3 Low Power
#4 High Speed
#5 High Endurance (MFM)
#6 Low Retention
#7 Radiation hardened

FRAM **FeFET** **FeMFET**



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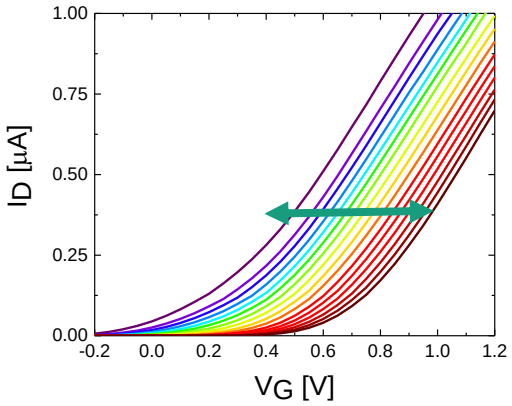
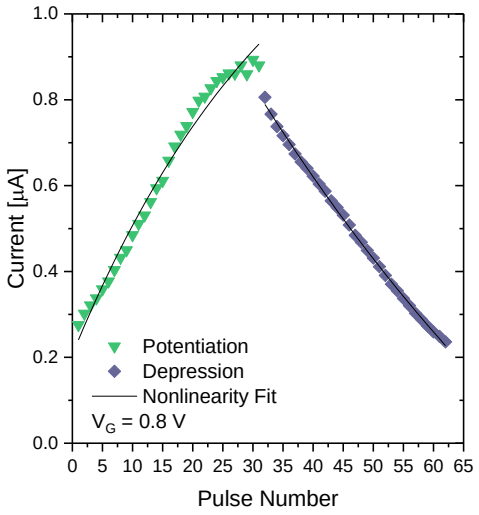
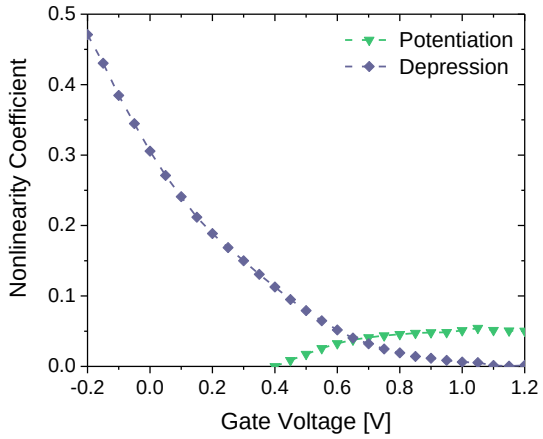
>10 ns	~1 ns	10 ns
$>10^{14}$	10^5-10^9	10^{10}
10 yrs	10 yrs	10 yrs

Performance indicators

Switching tests







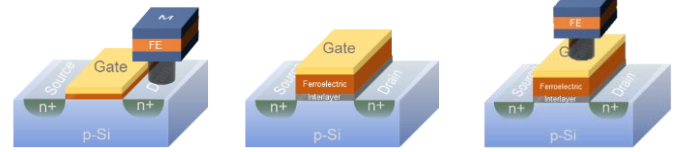
M. Lederer, ISIF 2019

Potential

#1 Scalability
#2 CMOS compatibility
#3 Low Power
#4 High Speed
#5 High Endurance (MFM)
#6 Low Retention
#7 Radiation hardened
#8 Analog MLC switch

Ideal for analog in Memory computing

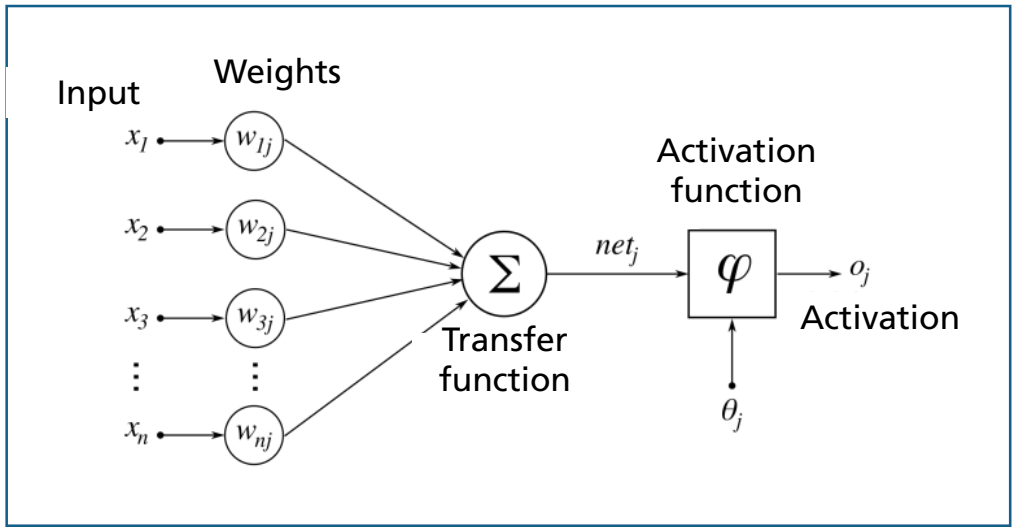
FRAM **FeFET** **FeMFET**



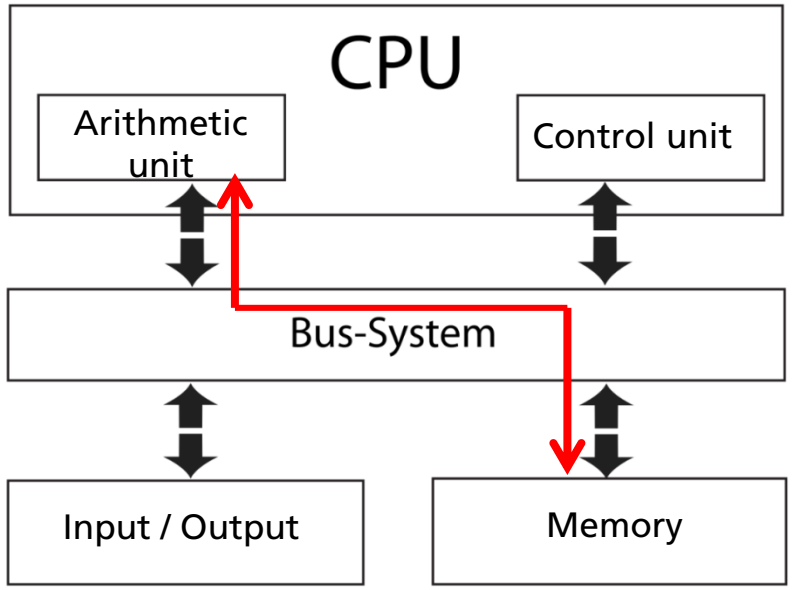
FeRAM	FeFET	FeMFET
Polarization switching	Polarization switching	Polarization switching
1T-1C	1T	1T-1C
50 F^2	20-30 F^2	30-40 F^2
Potential	Yes	Yes
N/A	>10^4	>10^4
130nm	22nm FDSOI	180nm[1]
2-3	1	2-3
~1 pJ	~1 fJ	~10 fJ
>10 ns	~1 ns	10 ns
>10^{14}	10^5-10^9	10^{10}
10 yrs	10 yrs	10 yrs

How to do computing with such memories?

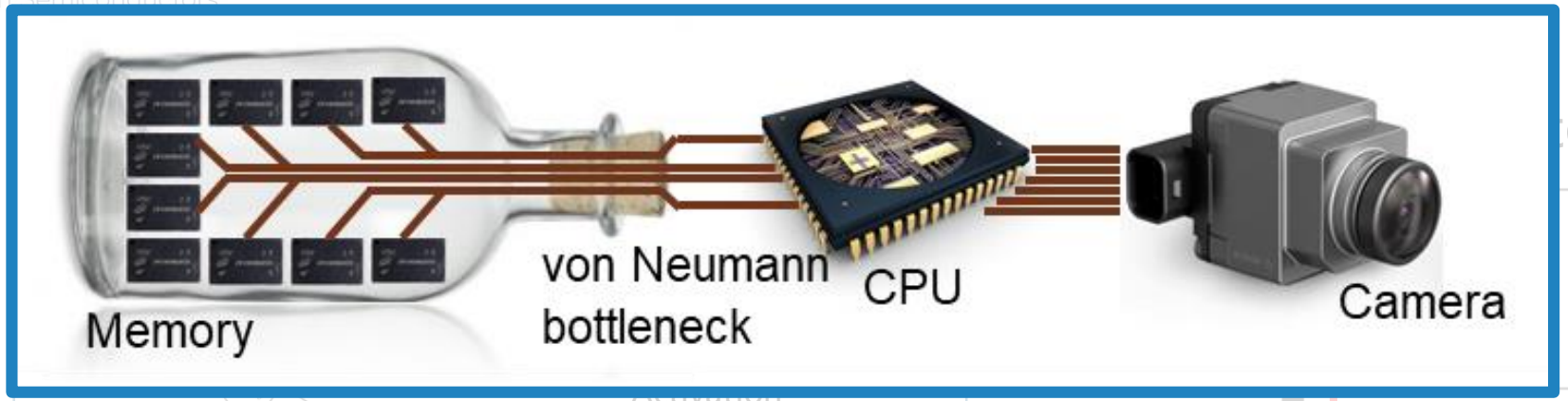
Computing for Artificial Intelligence



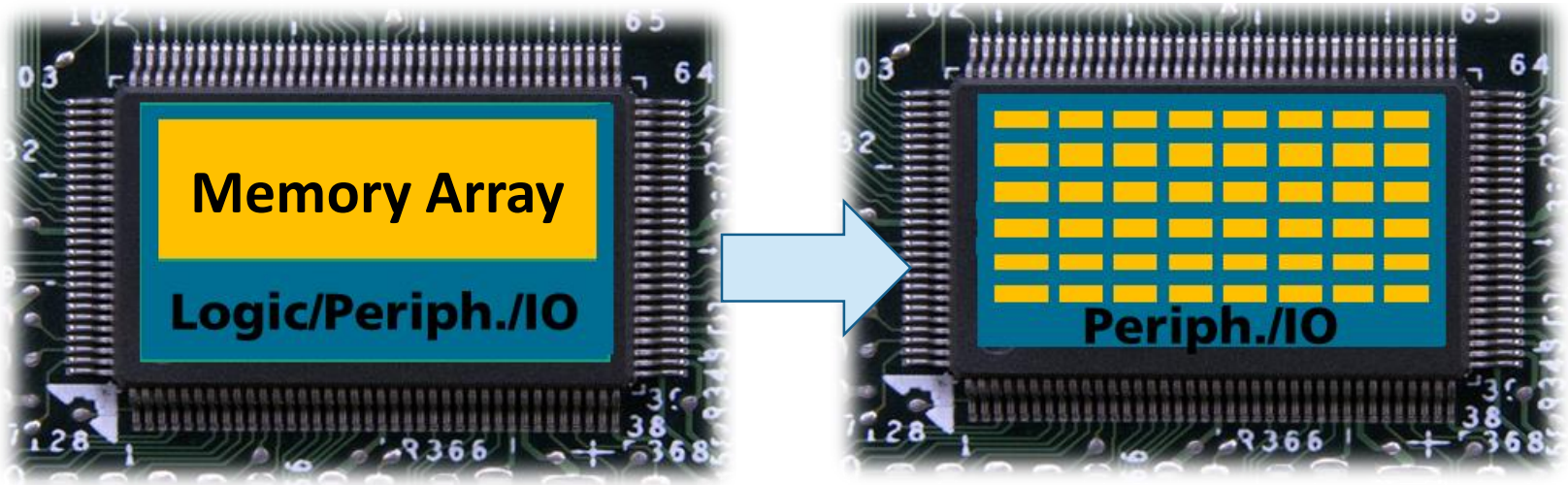
Conventional architecture



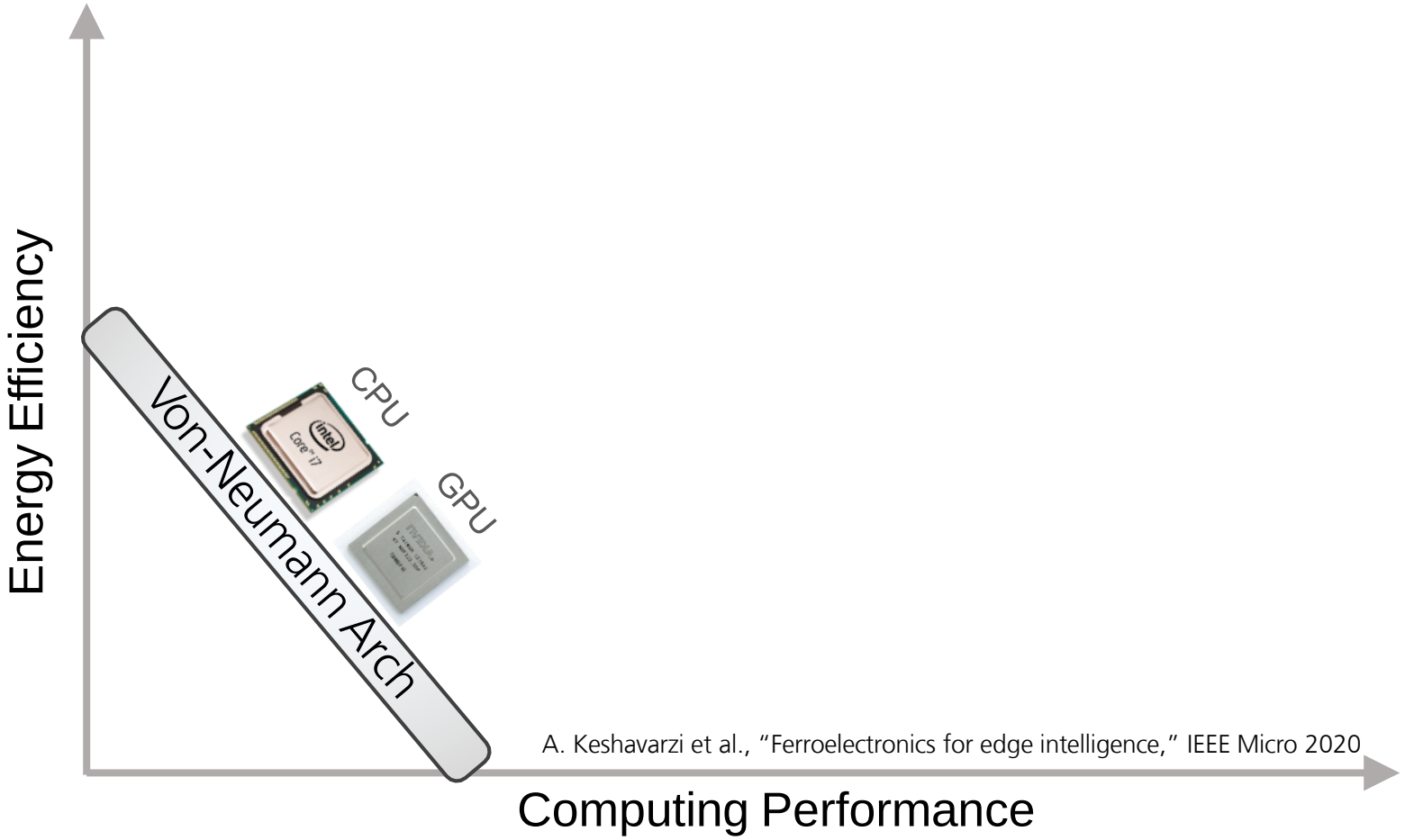
Computing for Artificial Intelligence



Combine memory with computing



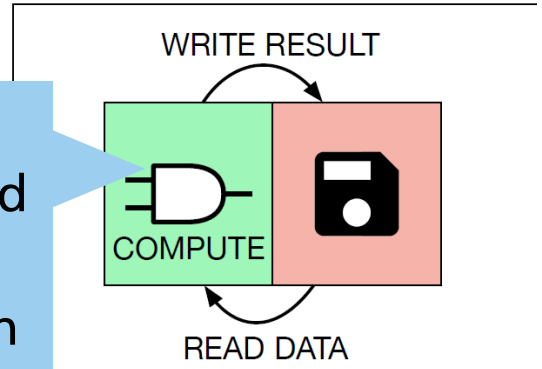
Hardware Approaches

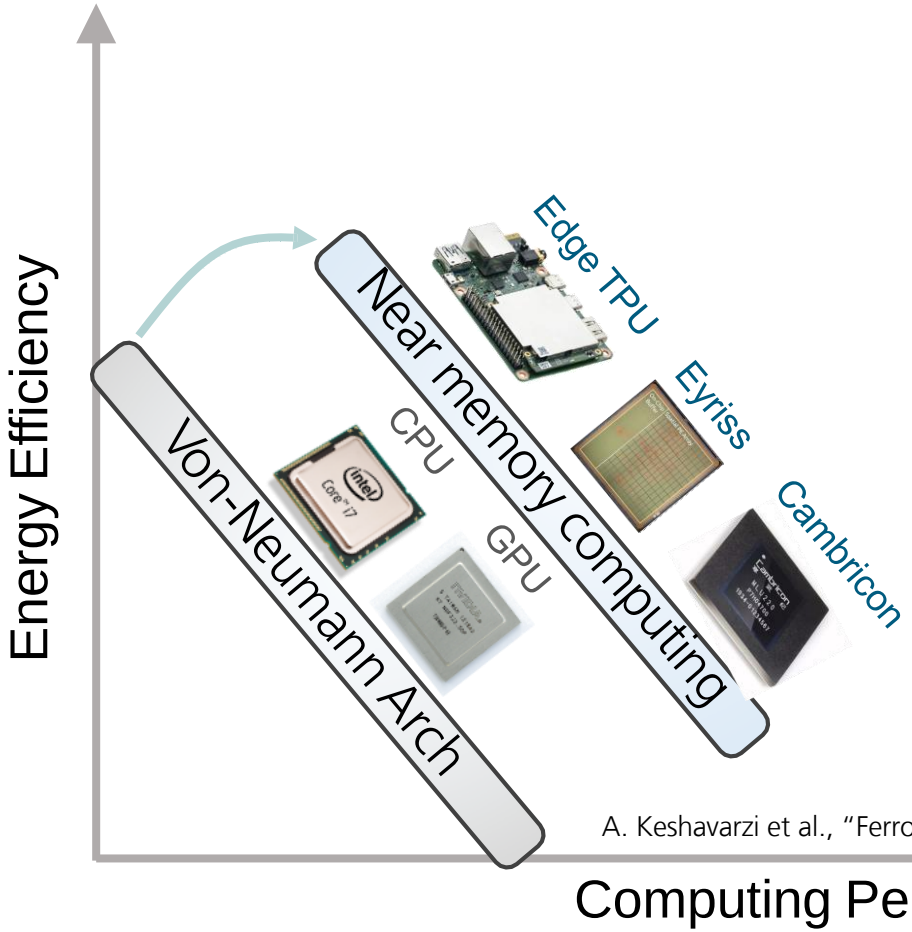


A. Keshavarzi et al., "Ferroelectronics for edge intelligence," IEEE Micro 2020

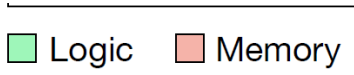
Hardware Approaches

- Computing and storage separated
- Closer proximity by 3D integration





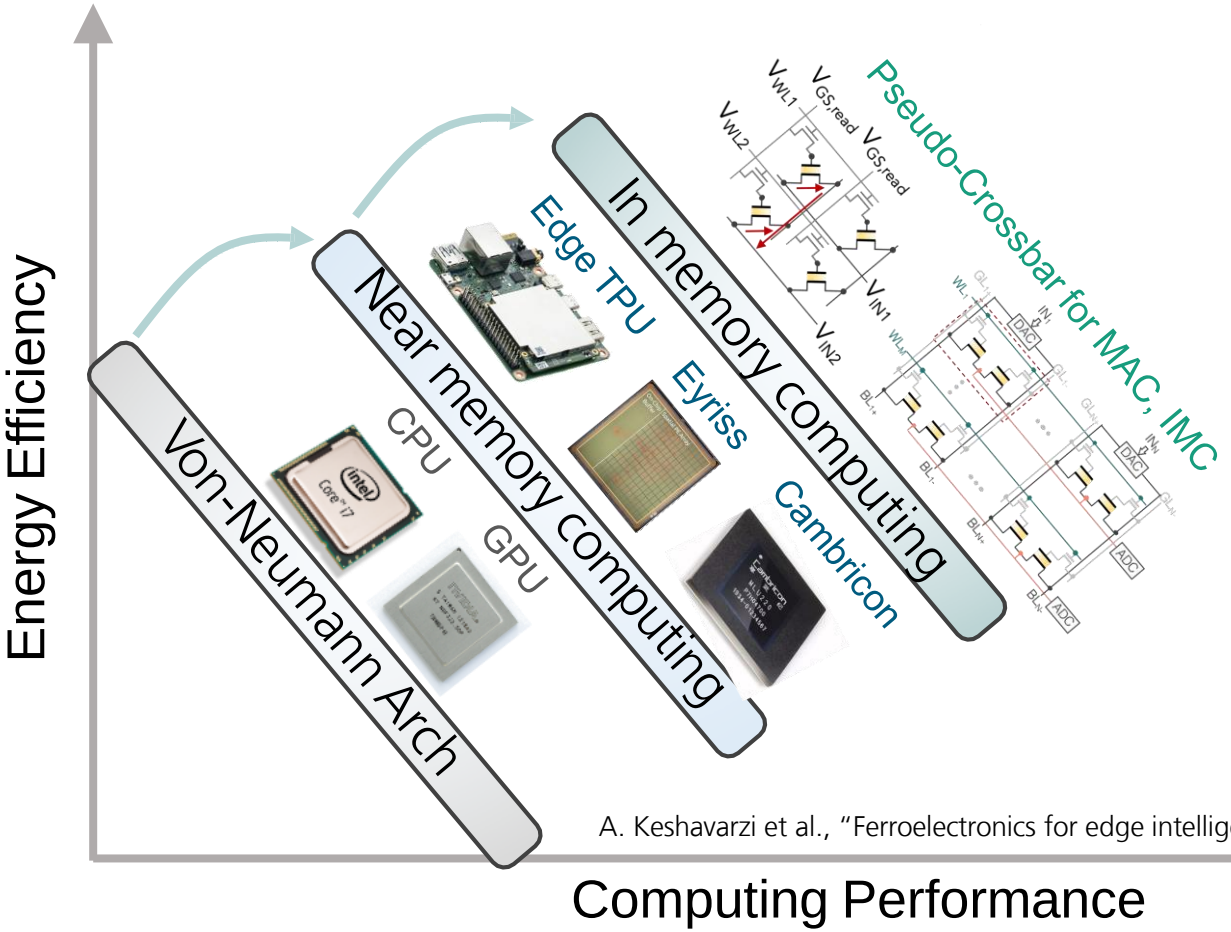
A. Keshavarzi et al., "Ferroelectronics for edge intelligence," IEEE Micro 2020



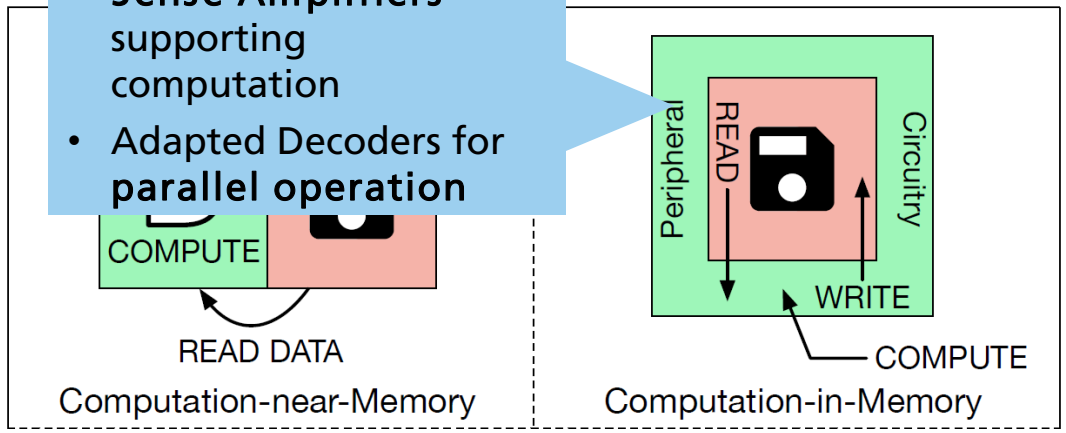
G.Santoro, G. Turvani, M. Graziano, Micromachines 2019

Hardware Approaches

- Segmented Memory arrays utilizing **analog** features
- **Sense Amplifiers** supporting computation
- Adapted Decoders for **parallel operation**



A. Keshavarzi et al., "Ferroelectronics for edge intelligence," IEEE Micro 2020

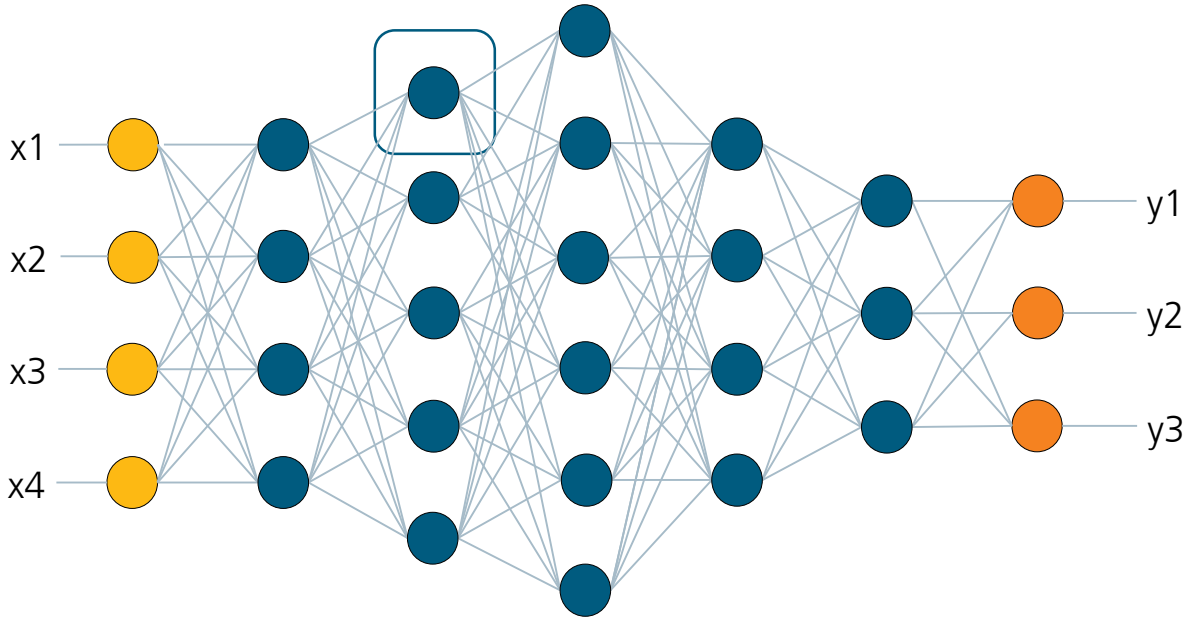


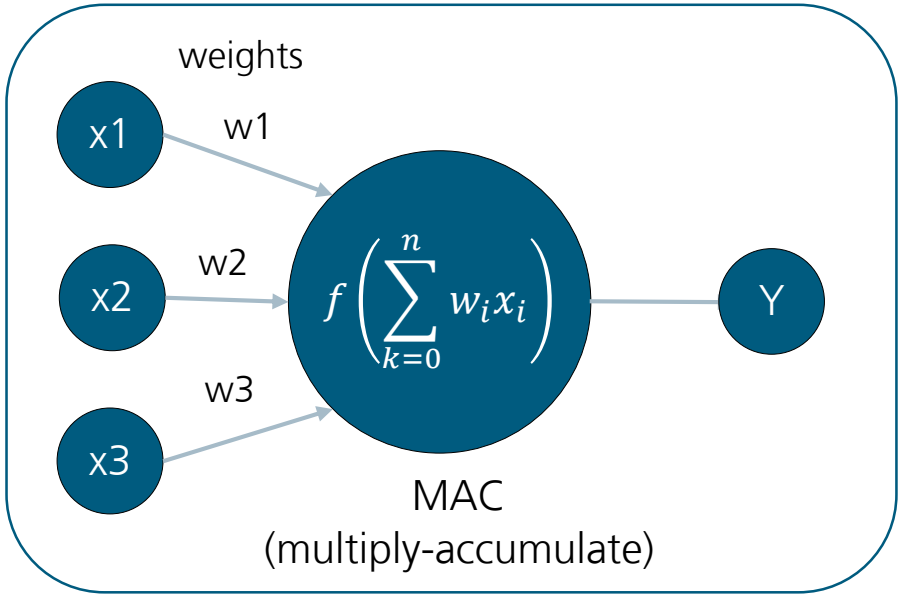
Logic Memory

G.Santoro, G. Turvani, M. Graziano, Micromachines 2019

Computation in Memory

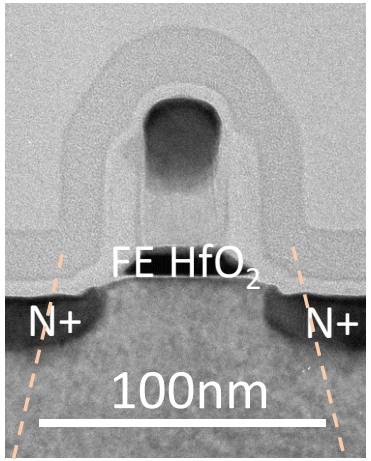
Performance determined by MAC operations

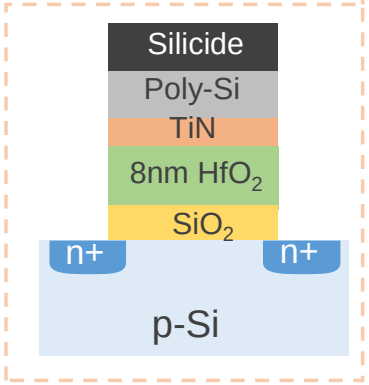


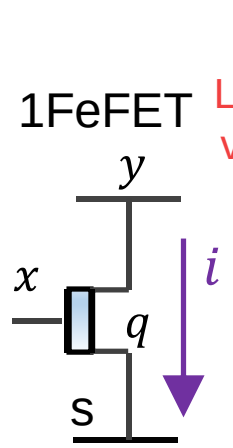


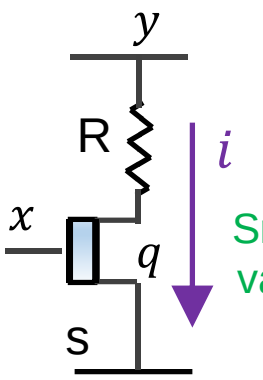
Computation in Memory

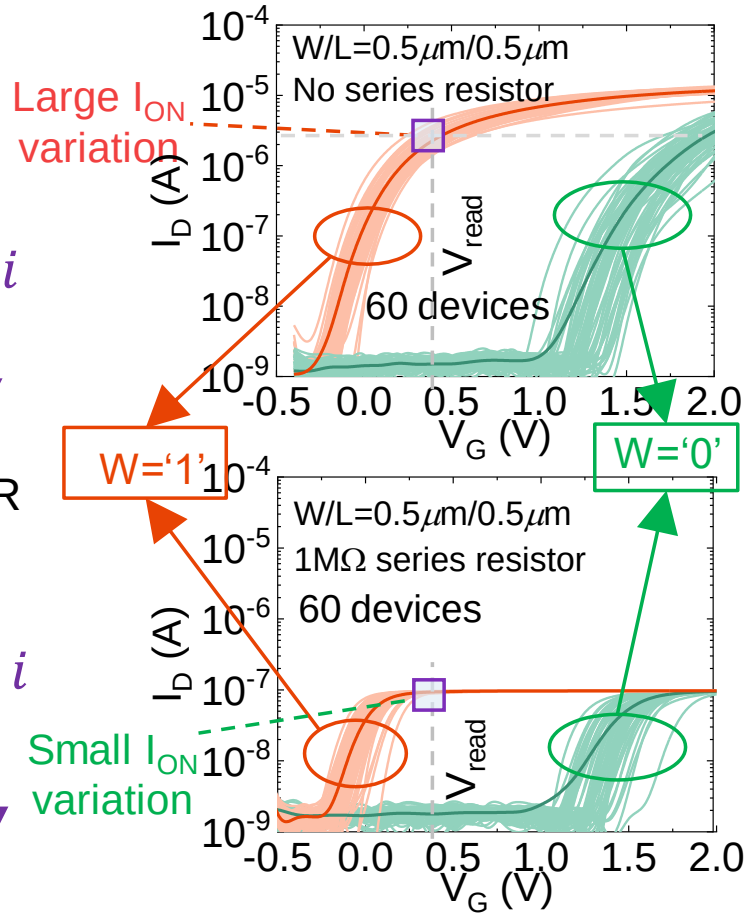
1F1R bitcell concept for accurate accumulation

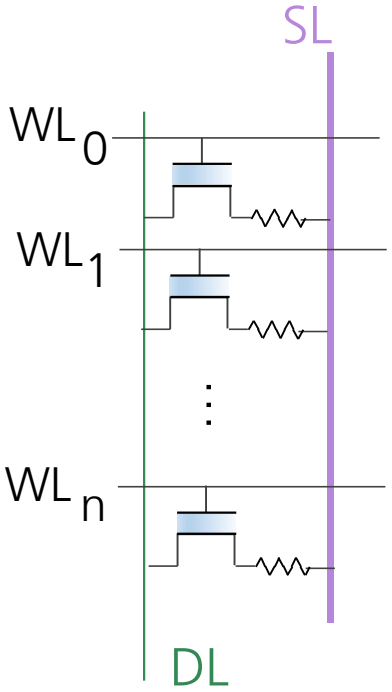


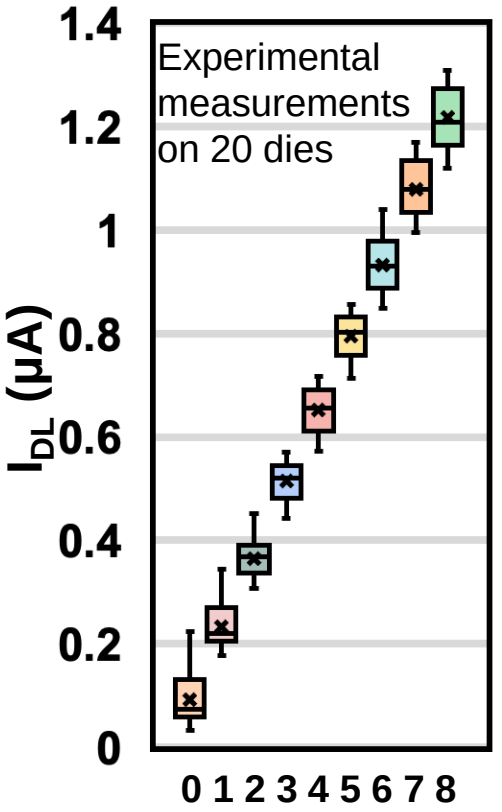










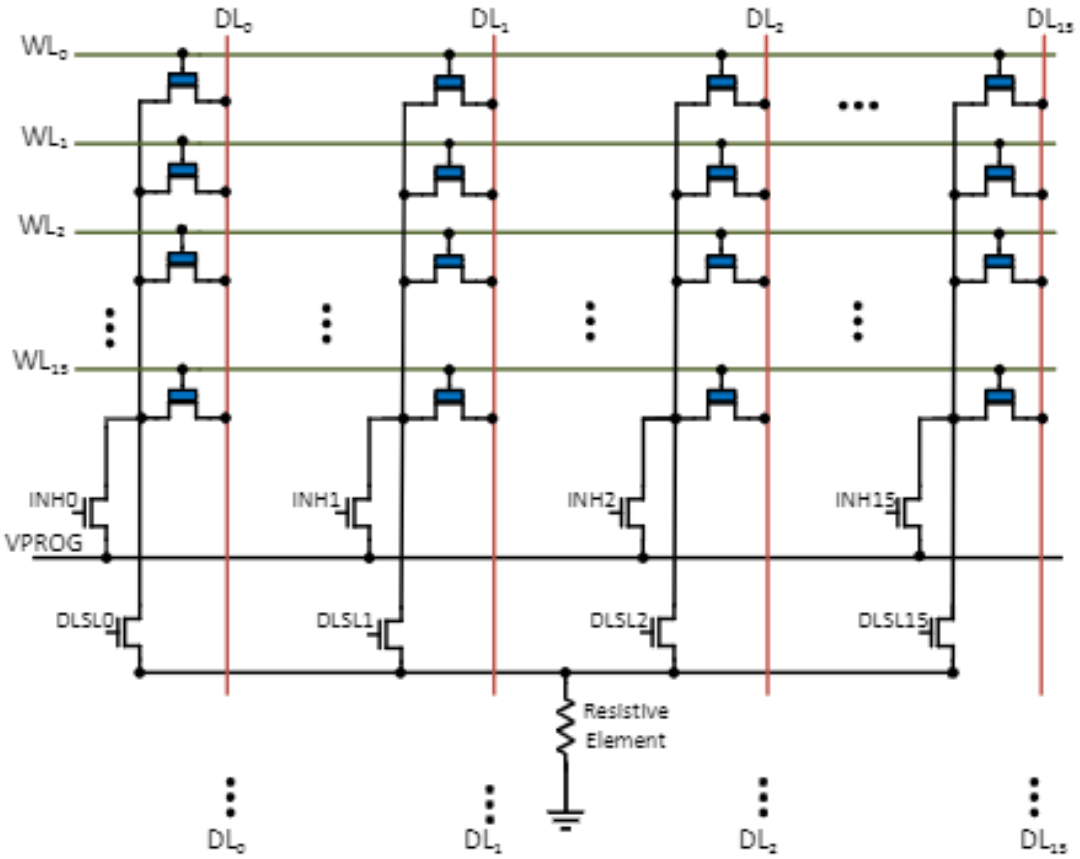


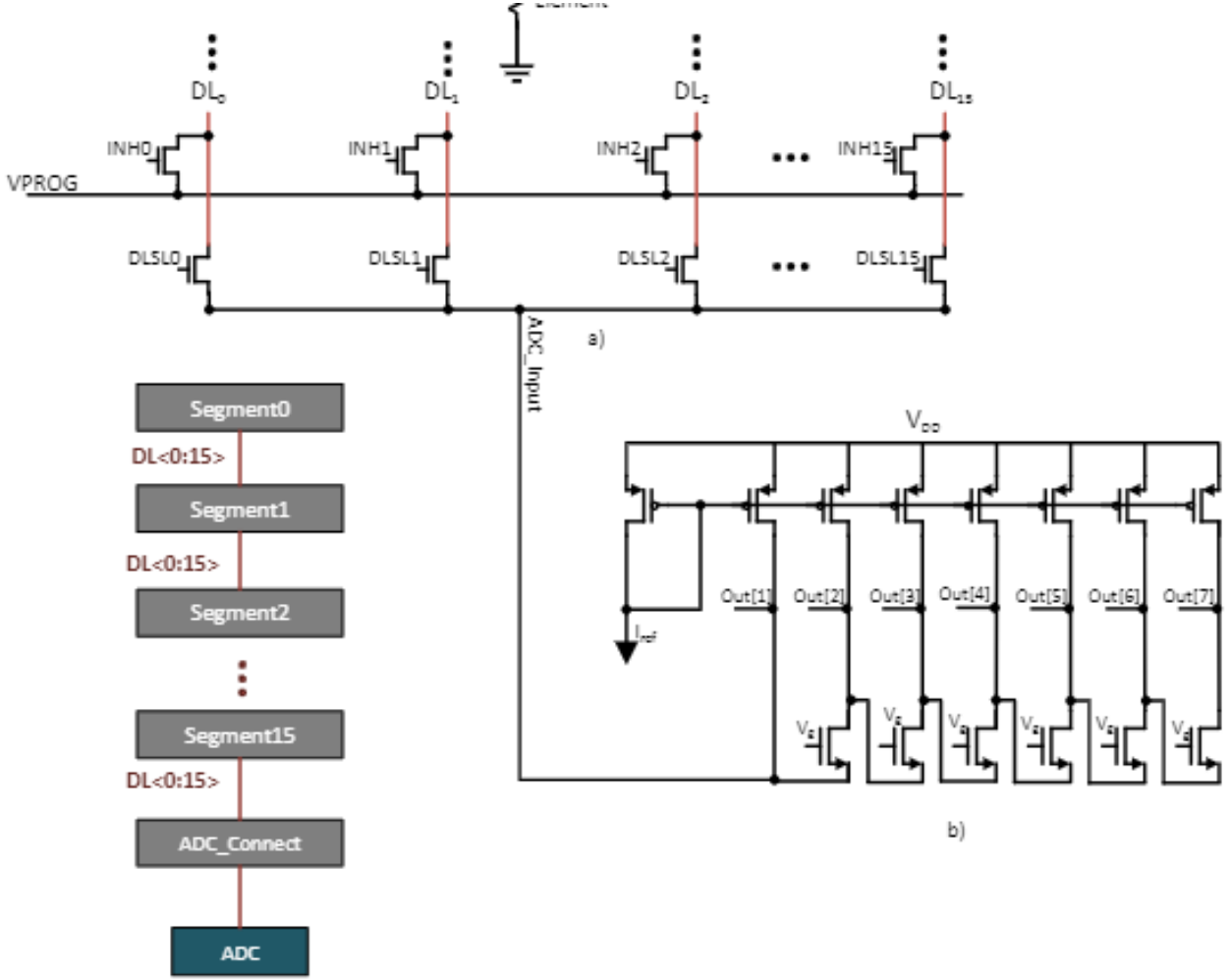
T. Soliman et al. Ultra Low Power Flexible Precision FeFET based Analog In-memory Computing, IEDM 2020

S. De et al. First Demonstration of Ultra-High Precision 4Kb 28nm HKMG 1FeFET-1T Based Memory Array Macro for Highly Scaled Deep Learning Applications, in prep

Computation in Memory

Segment Concept for high Utilization

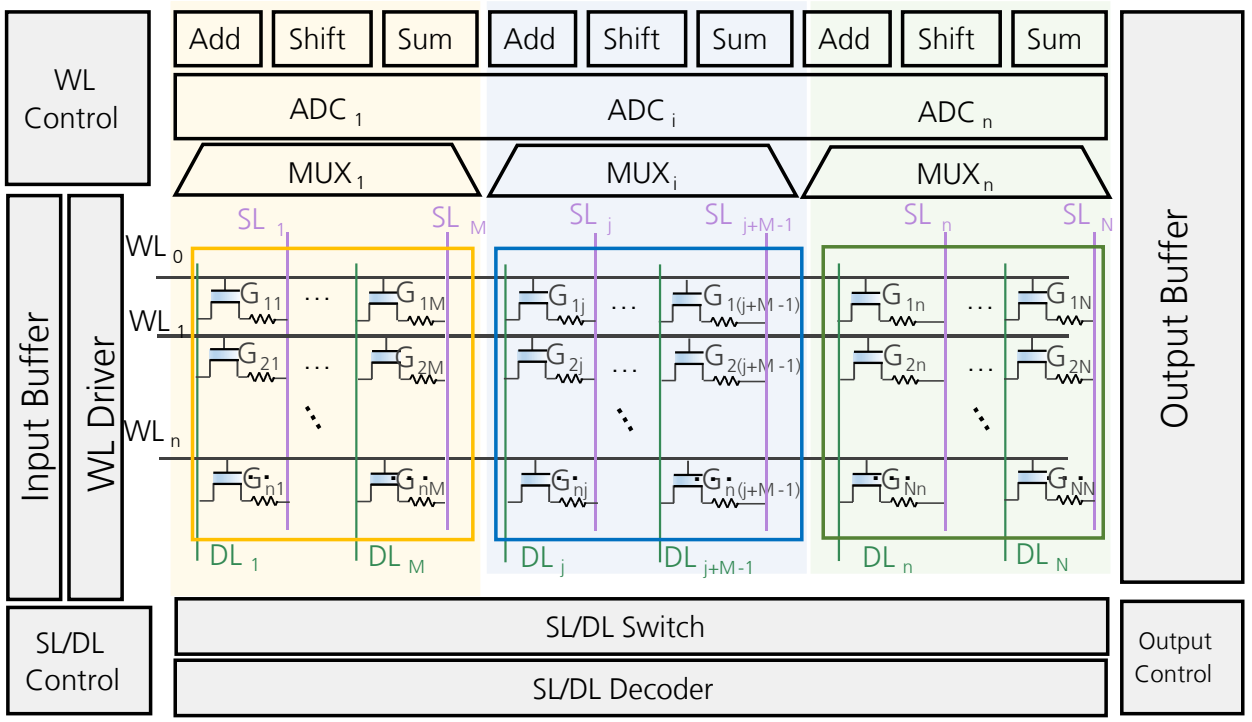




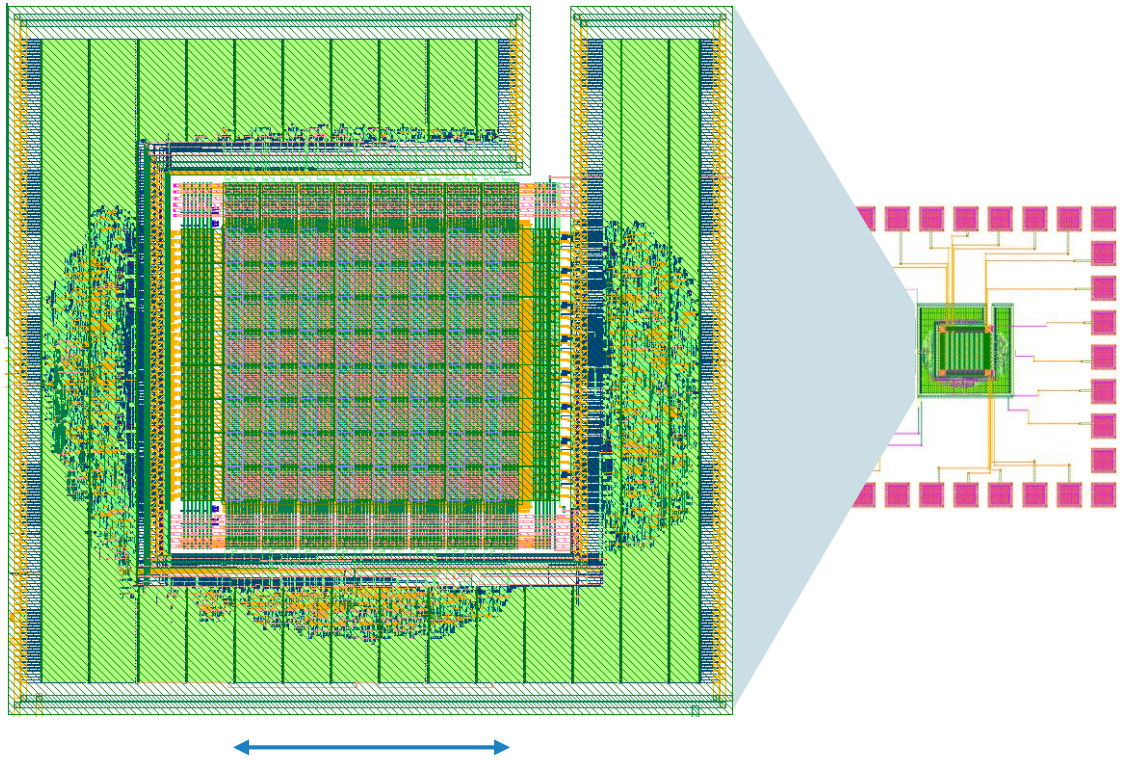
T. Soliman et al. Ultra Low Power Flexible Precision FeFET based Analog In-memory Computing, IEDM 2020

Computation in Memory

Process Element (PE)



4kb crossbar with SPI interface in 28SLPe



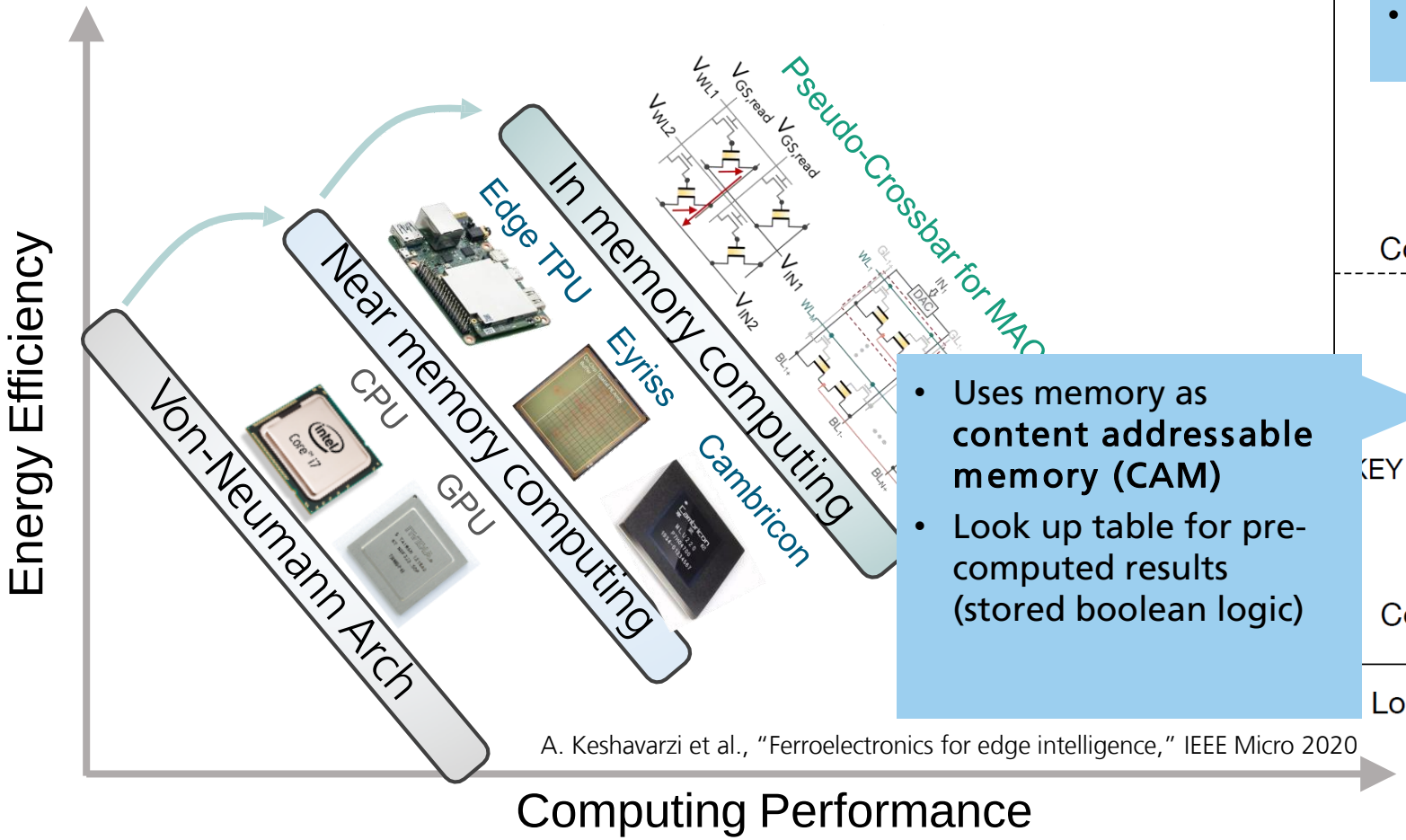
S. De et al. First Demonstration of Ultra-High Precision 4Kb 28nm HKMG 1FeFET-1T Based Memory Array Macro for Highly Scaled Deep Learning Applications, in prep

Y. Qian et al. Acceleration of Quadratic Unconstrained Binary Optimization Problems with FeFET Computing-in-Memory Arrays: Prime Factorization as a Case Study, VLSI 2022

T. Soliman et al. A Ferroelectric FET Based In-memory Architecture for Multi-Precision Neural Networks, SOCC 2021

Power-Performance D ce

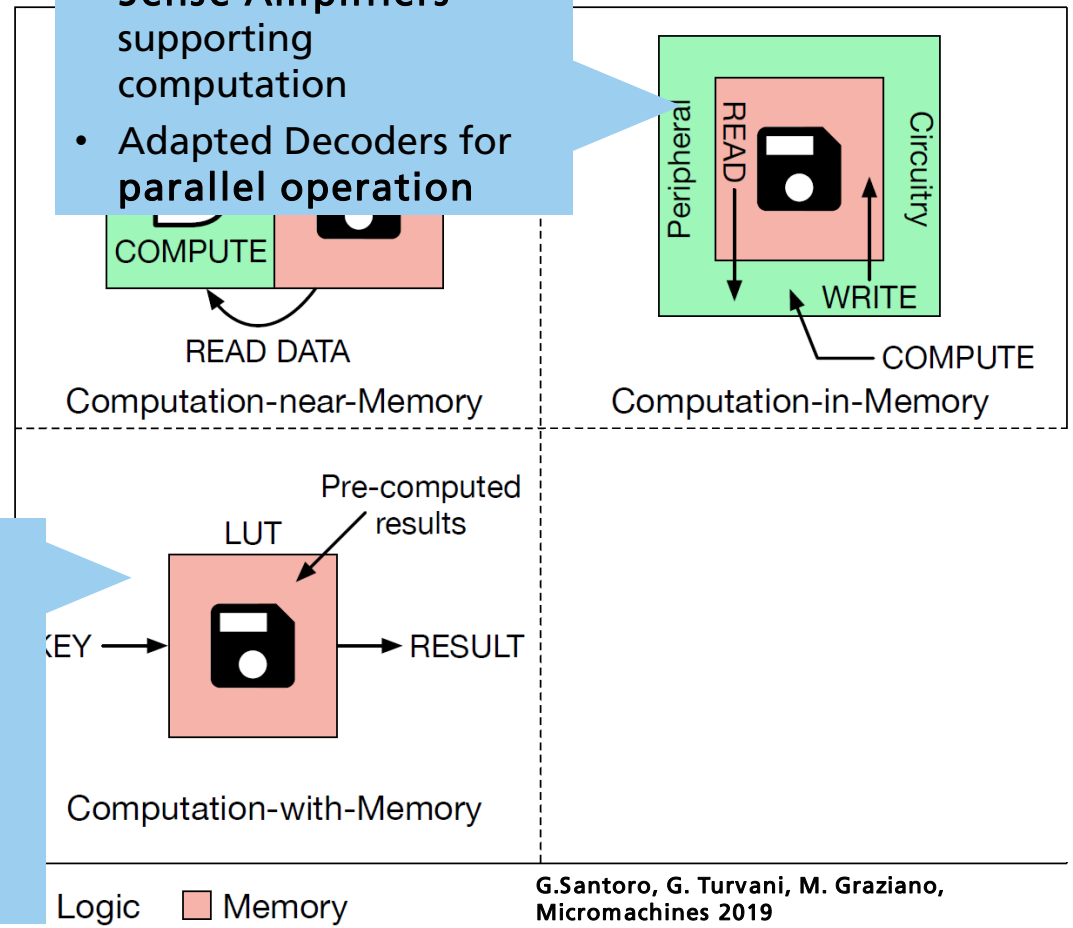
Technology Roadmap for Energy Eff



- Uses memory as **content addressable memory (CAM)**
- Look up table for pre-computed results (stored boolean logic)

A. Keshavarzi et al., "Ferroelectronics for edge intelligence," IEEE Micro 2020

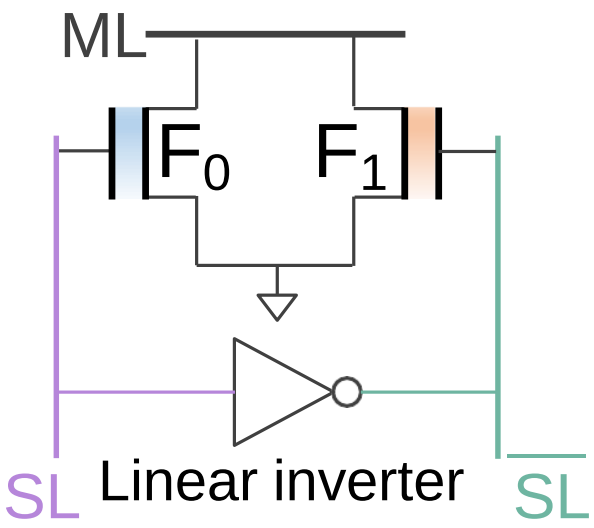
- Segmented Memory arrays utilizing **analog** features
- **Sense Amplifiers** supporting computation
- Adapted Decoders for **parallel operation**

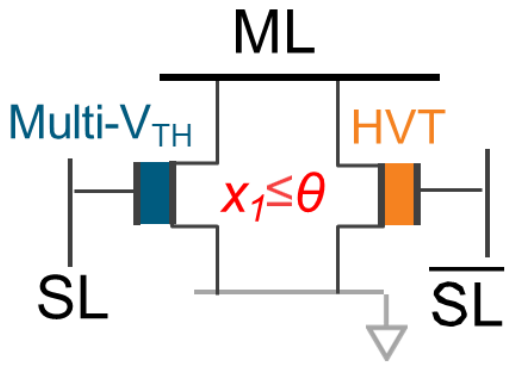


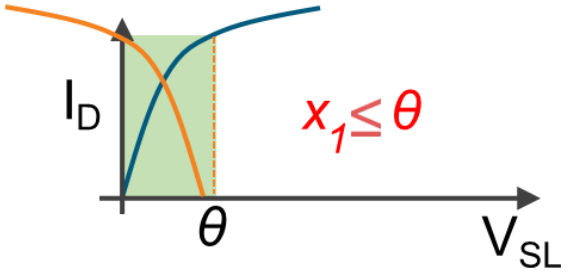
G.Santoro, G. Turvani, M. Graziano, Micromachines 2019

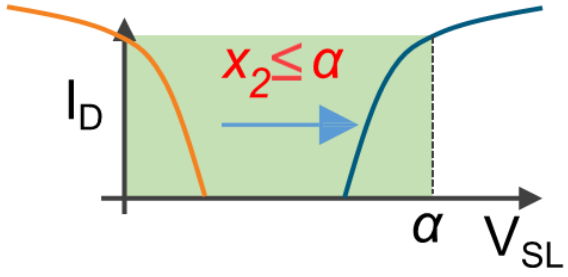
Analog Ferroelectric CAM

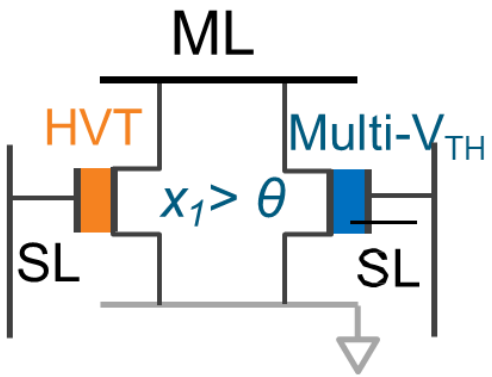
2FeFET cell

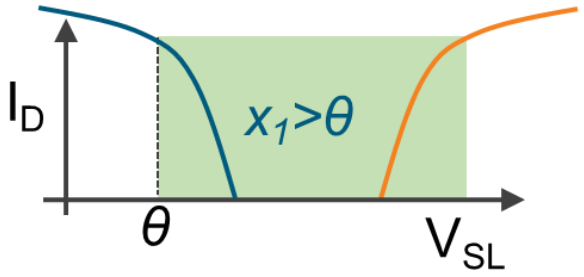


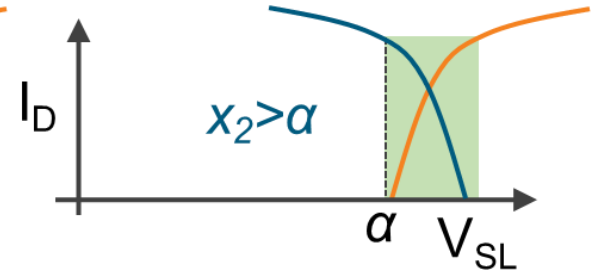










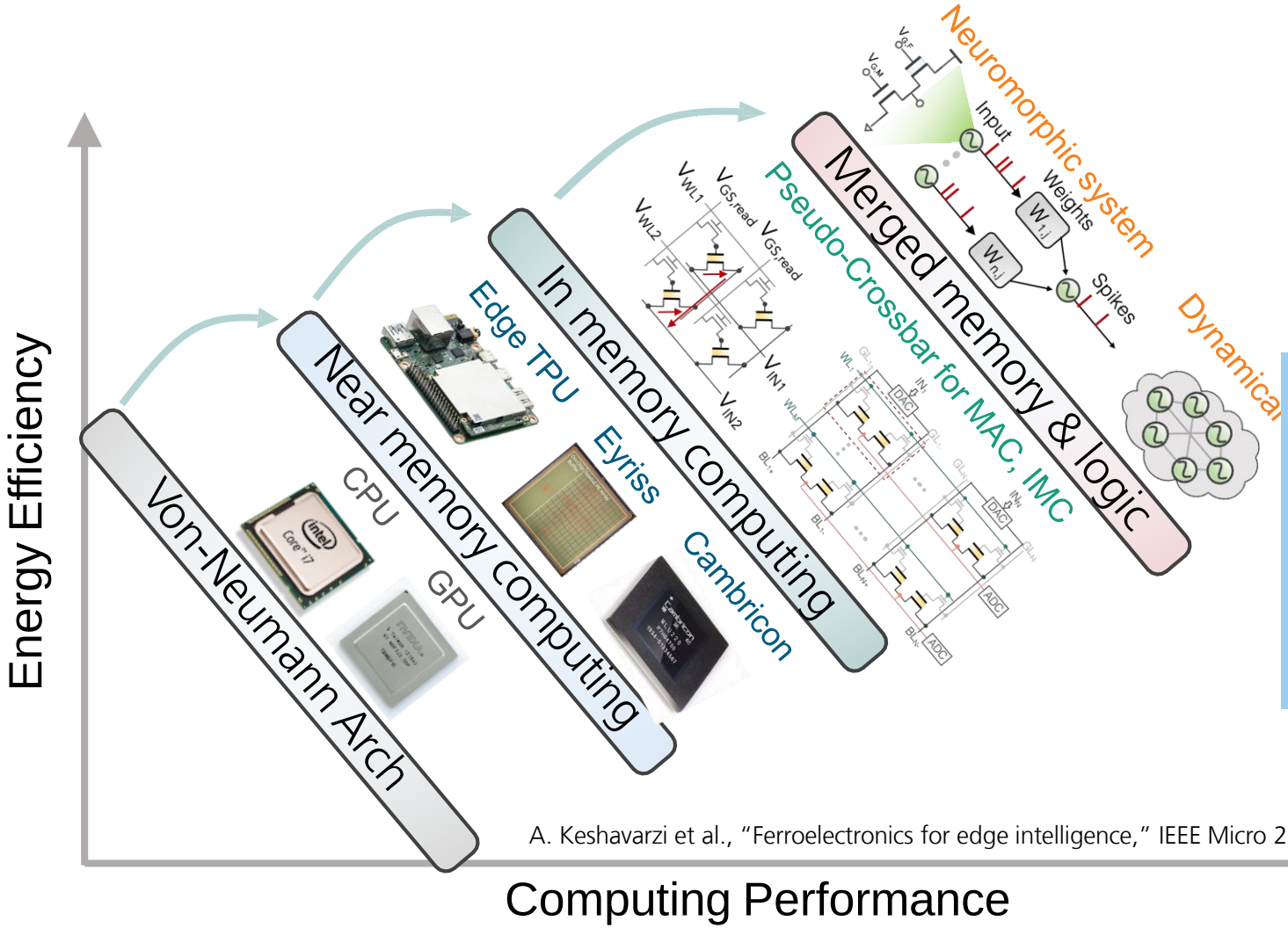


Fixing one FeFET to HVT state, the 2FeFET CAM becomes an analog CAM, capable of doing a threshold detection.

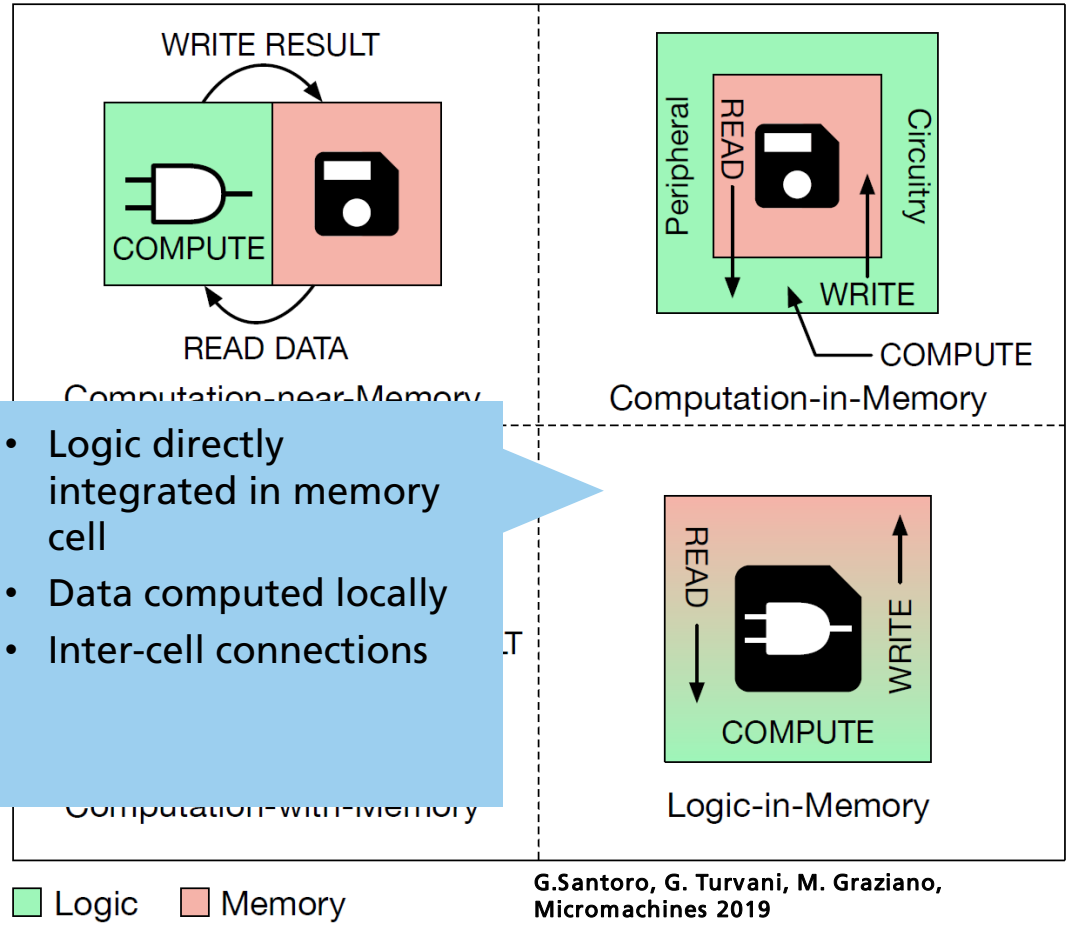
X. Yin, et al., Deep random forest with ferroelectric analog content addressable memory, Nature Electronics (under review)

Power-Performance Design Space

Technology Roadmap for Energy Efficient Computing



A. Keshavarzi et al., "Ferroelectronics for edge intelligence," IEEE Micro 2020

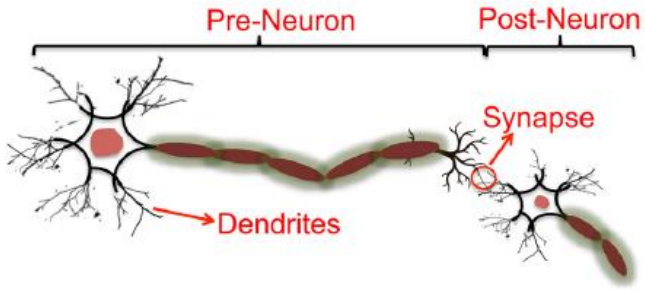


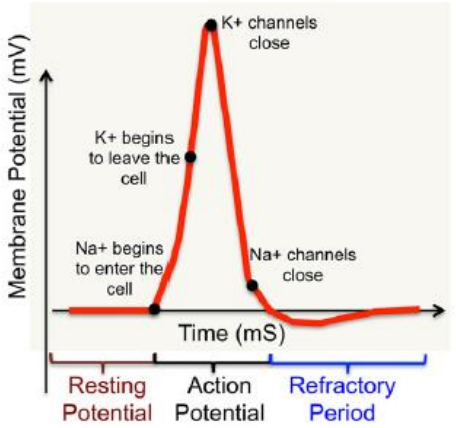
- Logic directly integrated in memory cell
- Data computed locally
- Inter-cell connections

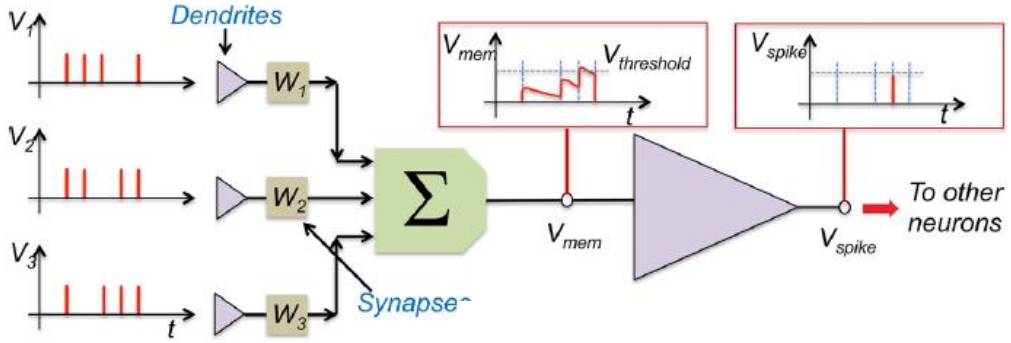
G.Santoro, G. Turvani, M. Graziano, Micromachines 2019

Logic in Memory

Memory as Neuron & Synapse







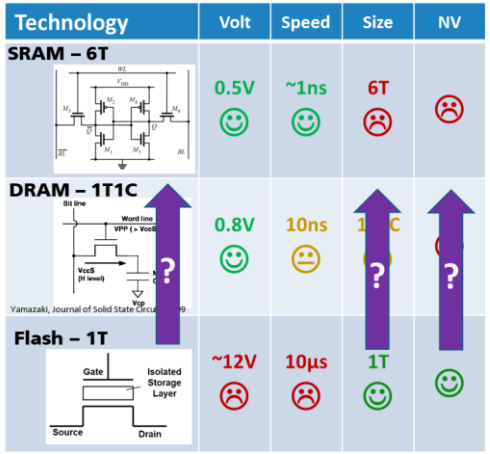
The Leaky-Integrate-Fire Model:

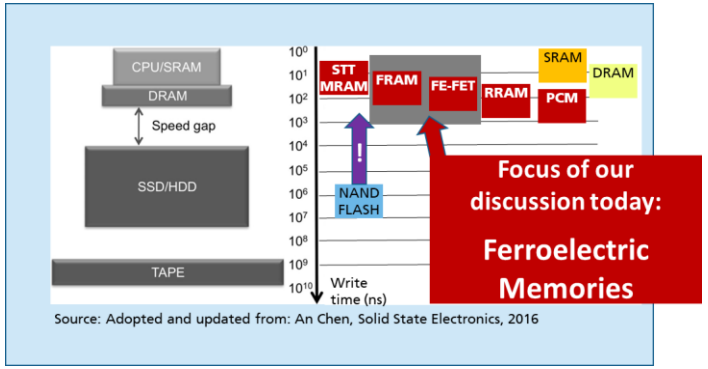
$$\frac{du}{dt} = -\frac{u(t)}{\tau} + \frac{I_{ext}(t) + I_{syn}(t)}{C}$$

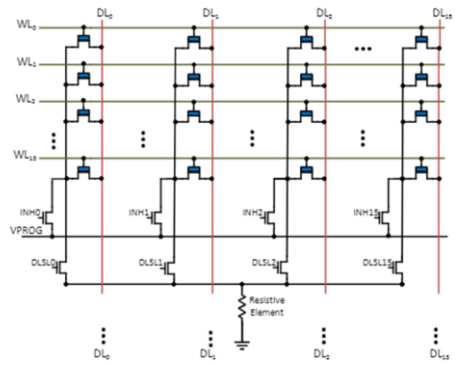
I. Chakraborty et.al Appl. Phys. Rev. 7, 021308 (2020);

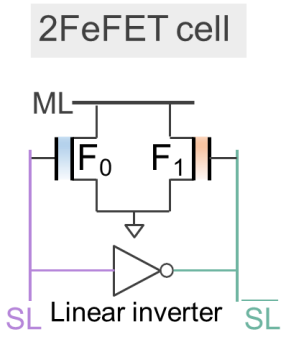
Summary

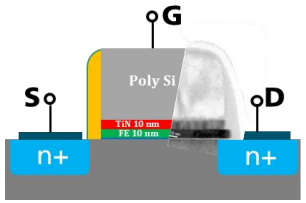
- Limitations of current computing hardware
- Emerging memories as potential game-changer
- Ferroelectric memories as potential solution
- Practical implementation options

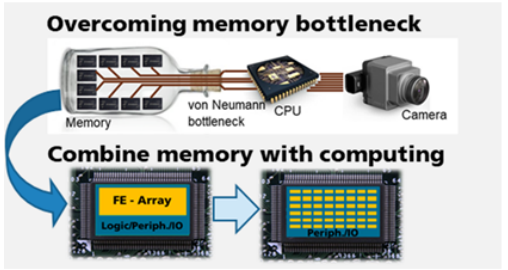


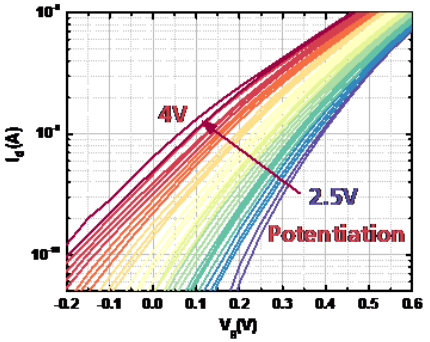












Fraunhofer IPMS

ECSEL Joint Undertaking
Electronic Components and Systems for European Leadership

Bundesministerium für Bildung und Forschung

Many thanks

- to the entire Team of Fraunhofer IPMS supporting this work
- To our funding & project partners
- To the CNT team at Fraunhofer IPMS for the always high motivation and great scientific work

Forschungsfabrik Mikroelektronik Deutschland

THANK YOU FOR YOUR ATTENTION

ICOS International Cooperation On Semiconductors

Funded by the European Union

SiNANO Institute

IRDS International Roadmap for Devices and Systems

This project has received funding from the European Union's Horizon Europe research and innovation programme under GA Nº 101092562